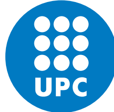

Universitat Politècnica de Catalunya

Departament d'Enginyeria Electrònica

# Mixed-Signal Alternate Test and Binning Using Digitally Encoded Signatures

Thesis submitted in partial fulfillment of the requirements for the
PhD Degree issued by the Universitat Politècnica de Catalunya
in its Electronic Engineering Program

Álvaro Gómez Pau

Advisors:

Joan Figueras Pàmies
Luz Balado Suárez

July 2017

# Acknowledgments

After all these years of research, it comes the time of wrapping things up and writing the thesis. It has not been an easy journey although I have enjoyed every step. On the other hand, I would have not overcome all the difficulties alone, that is why I am grateful to so many people.

First of all, I would like to thank my advisors, Professor Joan Figueras and Professor Luz Balado, for their dedication, advice, trust, support and guidance during my thesis. They have dedicated an endless number of hours discussing, reviewing and guiding me through the amazing world of research. They have been a model to follow, not only in research, but also in facing my professional life.

My gratefulness also goes to all the members and staff of the Departament d'Enginyeria Electrònica at ETSEIB, and specially to those of the QINE research group. Since the beginning of this journey, they all have made me feel like being at home.

I am also grateful to Professor Abhijit Chatterjee from Georgia Institute of Technology and Professor José Pineda de Gyvez from Eindhoven University of Technology for hosting my two short-term research stays in 2013 and 2014, respectively. They introduced me to amazing research topics.

I do not want to forget anyone, but my mind is not capable of remembering all the names of those who, in one way or another, have contributed to my research or have helped me during the course of these years. To all of them, thank you very much.

This thesis has been possible thanks to PhD scholarship BES-2011-044129 under the project TEC2010-18384, funded by the Spanish Ministry of Economy and Competitiveness. Also, the two short-term research stays, EEBB-I-13-07342 and EEBB-I-14-09005, have been funded by the Spanish Ministry of Economy and Competitiveness.

Last but not least, I would like to express my huge gratitude to my family and Neus. They have been my greatest support during all these years. Their help, warmth, understanding and affection have been a fundamental pillar. I would like also to say sorry because all the time that would have had to be ours and it was this thesis. It will be certainly rewarded.

Thank you all!

Álvaro Gómez Pau
Barcelona, May 2017

# Contents

**1 Introduction** **1**

1.1 Motivation . . . . . . . . . . 2

1.2 Objectives . . . . . . . . . . 3

1.3 Thesis Organization and Contributions . . . . . . . . . . 3

**2 State of the Art** **11**

2.1 Alternate Test of Mixed-Signal Circuits . . . . . . . . . . 12

2.2 State of The Art Methods in Alternate Test . . . . . . . . . . 13

2.2.1 Regression Techniques . . . . . . . . . . 13

2.2.2 Classification Techniques . . . . . . . . . . 16

2.3 Alternate Test of MEMS Systems . . . . . . . . . . 19

2.4 Binning of Mixed-Signal Circuits . . . . . . . . . . 20

2.5 Selection of Alternate Measurements . . . . . . . . . . 22

**3 Alternate Test and Binning Based on Octree Encoded Signatures** **23**

3.1 Test of Mixed-Signal Circuits Using Digitally Encoded Signatures . . . 23

3.1.1 Octree Encoding Fundamentals . . . . . . . . . . 24

3.1.2 Test Using Octree Data Structures . . . . . . . . . . 28

3.1.3 Efficiency Metrics . . . . . . . . . . 28

3.2 Test Application: Band-Pass Biquad Filter . . . . . . . . . . 31

3.2.1 Filter Design and Test Specifications . . . . . . . . . . 31

3.2.2 Alternate Measurements Space . . . . . . . . . . . . . . . . . . 32
3.2.3 Statistical Training Phase . . . . . . . . . . . . . . . . . . . . . 34
3.2.4 Simulation Results . . . . . . . . . . . . . . . . . . . . . . . . 36
3.3 Test Application: Low-Pass Biquad Filter with Boundary Densification 40
3.3.1 Statistical Training Phase with Boundary Densification . . . . 40
3.3.2 Simulation Results . . . . . . . . . . . . . . . . . . . . . . . . 48
3.4 Binning of Mixed-Signal Circuits Using Digitally Encoded Signatures . 51
3.4.1 Octree Encoding for Quality Binning . . . . . . . . . . . . . . . 54
3.4.2 Binning Using Octree Data Structures . . . . . . . . . . . . . . 56
3.4.3 Efficiency Metrics: Bin Escapes . . . . . . . . . . . . . . . . . . 57
3.5 Binning Application: 4th Order Band-Pass Butterworth Filter . . . . 57
3.5.1 Filter Design and Bin Specifications . . . . . . . . . . . . . . . 57
3.5.2 Alternate Measurements Space . . . . . . . . . . . . . . . . . . 59
3.5.3 Statistical Training Phase . . . . . . . . . . . . . . . . . . . . . 60
3.5.4 Simulation Results . . . . . . . . . . . . . . . . . . . . . . . . 61
3.5.5 Comparison with Support Vector Machines Classifier . . . . . . 64
3.6 Summary and Comments . . . . . . . . . . . . . . . . . . . . . . . . 66

**4 Alternate Test of Heterogeneous Systems 71**
4.1 Integrated MEMS Capacitive Accelerometers . . . . . . . . . . . . . 71
4.1.1 Mechanical Subsystem . . . . . . . . . . . . . . . . . . . . . . . 72
4.1.2 Capacitive Transducer Subsystem . . . . . . . . . . . . . . . . 73
4.1.3 Electronic Conditioning Subsystem . . . . . . . . . . . . . . . . 74
4.2 Analog Characterization and Excitation of Dual Axis Capacitive Accelerometers . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 74
4.2.1 Vertical Spinning Proposal . . . . . . . . . . . . . . . . . . . . 75
4.2.2 Lissajous Compositions Under Parametric Defects . . . . . . . 76
4.2.3 Metric Definition . . . . . . . . . . . . . . . . . . . . . . . . . . 82
4.2.4 Diagnosis Efficiency Evaluation . . . . . . . . . . . . . . . . . . 82
4.3 Application to Accelerometer Sensitivity Test Using Octrees . . . . . . 83
4.3.1 Statistical Training Phase . . . . . . . . . . . . . . . . . . . . . 83
4.3.2 Simulation Results . . . . . . . . . . . . . . . . . . . . . . . . 88

4.4 Application to Accelerometer Axis Misalignment Diagnosis . . . . . . 90
4.4.1 Misalignment Metric Evaluation . . . . . . . . . . . . . . . . . 92
4.4.2 Misalignment Diagnosis Efficiency Evaluation . . . . . . . . . . 92
4.4.3 Experimental Setup . . . . . . . . . . . . . . . . . . . . . . . . 95
4.4.4 Experimental Results . . . . . . . . . . . . . . . . . . . . . . . 97
4.5 Summary and Comments . . . . . . . . . . . . . . . . . . . . . . . . 99

**5 Improving Octree Tessellation Efficiency 103**
5.1 Octree Ensemble . . . . . . . . . . . . . . . . . . . . . . . . . . . . 103
5.1.1 Multi-Directional Tessellations in the Measurements Space . . 104
5.1.2 Test Application: Band-Pass Biquad Filter . . . . . . . . . . . 105
5.1.3 Simulation Results . . . . . . . . . . . . . . . . . . . . . . . . . 109
5.2 Multiple Specification Band Guarding . . . . . . . . . . . . . . . . . 116
5.2.1 Multiple Specification Band Guarding in the Indirect Measurements Space . . . . . . . . . . . . . . . . . . . . . . . . . . . . 117
5.2.2 Test Application: Band-Pass Butterworth Filter . . . . . . . . 118
5.2.3 Simulation Results . . . . . . . . . . . . . . . . . . . . . . . . . 122
5.3 Summary and Comments . . . . . . . . . . . . . . . . . . . . . . . . 130

**6 Selection and Acquisition of Analog Signatures 133**
6.1 Selection of Analog Signatures for Mixed-Signal Testing . . . . . . . . 134
6.1.1 Criterion for Selecting a Subset of Alternate Measurements for Mixed-Signal Testing . . . . . . . . . . . . . . . . . . . . . . . . 134
6.1.2 Test Application: Band-Pass Biquad Filter . . . . . . . . . . . 137
6.1.3 Simulation Results . . . . . . . . . . . . . . . . . . . . . . . . . 140
6.2 Acquisition of Analog Signatures for Mixed-Signal Testing . . . . . . . 143
6.2.1 Adaptive Signature Generator System . . . . . . . . . . . . . . 143
6.2.2 Adaptive Signature Generator System Setup . . . . . . . . . . 146
6.2.3 Experimental Results Testing a Biquad Filter . . . . . . . . . . 152
6.3 Summary and Comments . . . . . . . . . . . . . . . . . . . . . . . . 155

**7 Conclusions and Future Work 159**
7.1 Contributions and Conclusions . . . . . . . . . . . . . . . . . . . . . 159

7.2 Future Work . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 161

**A List of Publications** **165**

# List of Figures


1.1 Thesis roadmap and published results for chapters 3 and 4 . . . . . . . 5

1.2 Thesis roadmap and published results for chapters 5 and 6 . . . . . . . 6

2.1 Example of MARS basis function . . . . . . . . . . . . . . . . . . . . . . 15

2.2 Basic perceptron structure . . . . . . . . . . . . . . . . . . . . . . . . . 17

2.3 Example of linear SVM machine separator and the generated boundary with maximum margin separation. The support vectors are also highlighted. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 18

2.4 Example of a non linear SVM machine separator after the transformation of the input space using a non linear kernel function. . . . . . . . 19

2.5 Example of performance bins for alternate analog and mixed-signal quality binning. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 21

3.1 Components, specifications, and measurements spaces . . . . . . . . . 24

3.2 Example of alternate measurement space . . . . . . . . . . . . . . . . . 25

3.3 Example of a quadtree generated with random data . . . . . . . . . . 26

3.4 Two dimensional octree encoding two clusters . . . . . . . . . . . . . . 27

3.5 Graph representation of the octree shown in Figure 3.4 . . . . . . . . . 27

3.6 Algorithm implementing the testing procedure using octrees . . . . . . 28

3.7 Example of octree node data structure defined in ANSI C . . . . . . . 31

3.8 Band pass filter schematic . . . . . . . . . . . . . . . . . . . . . . . . . 31

3.9 Analog signature generation and compaction . . . . . . . . . . . . . . . 33

3.10 Analog signature generation using orthogonal signal composition . . . 34
3.11 Example of Lissajous compositions as analog signatures . . . . . . . . 34
3.12 Band-pass Biquad filter samples in the measure space . . . . . . . . . 35
3.13 Filter's functional specifications distributions . . . . . . . . . . . . . . 35
3.14 Resulting octree after the training phase for the circuit shown in Figure 3.12 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 36
3.15 Octree levels distribution of the octree shown in Figure 3.14 . . . . . . 37
3.16 Testing phase results using $50 \times 10^3$ Monte Carlo samples . . . . . . . 38
3.17 Cumulative required comparisons distribution for the testing phase using octrees . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 39
3.18 Analog test metrics as a function of noise levels . . . . . . . . . . . . . 40
3.19 Densification algorithm to increase the number of circuits near the test decision boundary . . . . . . . . . . . . . . . . . . . . . . . . . . . 41
3.20 Monte Carlo simulations of the Biquad filter depicted in Figure 3.23 . 42
3.21 Monte Carlo samples of the Biquad filter after the application of the densification procedure . . . . . . . . . . . . . . . . . . . . . . . . . 43
3.22 Lissajous compositions of the nominal and deviated responses when a multitone signal is applied to a low-pass filter . . . . . . . . . . . . . 44
3.23 Schematic of the low-pass state variable filter used as case study . . . 45
3.24 Quadtree encoding the test acceptance and rejection regions . . . . . . 46
3.25 Resulting octree including the circuit samples generated with the boundary densification algorithm . . . . . . . . . . . . . . . . . . . . . . . 47
3.26 Octree levels distribution as a function of the Monte Carlo samples used with $N_1/N_0 = 100$ . . . . . . . . . . . . . . . . . . . . . . . . . 49
3.27 Octree levels distribution as a function of the Monte Carlo samples used with $N_1/N_0 = 500$ . . . . . . . . . . . . . . . . . . . . . . . . . 50
3.28 Analog test metrics for the two densification scenarios of $N_1/N_0 = 100$ and $N_1/N_0 = 500$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . 52
3.29 Sketch of the components, specifications, and alternate measurements spaces . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 53
3.30 Graph representation of the quadtree depicted in Figure 3.31 . . . . . 54
3.31 Example of a quadtree generated using 100 bivariate Gaussian samples and three bins . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 55
3.32 Monte Carlo samples of a 4th order band-pass Butterworth filter . . . 56

3.33 Schematic of the 4th order band-pass Butterworth filter used as case study . . . 58

3.34 Input-output composition when a 3 tone signal is applied to the band-pass Butterworth filter . . . 60

3.35 Kendall's Tau rank correlation coefficients between all the possible pairs of candidate alternate measurements . . . 61

3.36 Magnitude Bode plots of the band-pass Butterworth filter . . . 62

3.37 Octree encoding of the alternate measurements space shown in Figure 3.32 . . . 63

3.38 Octree levels distribution for the encoding shown in Figure 3.37 . . . 64

3.39 Binning phase results using a set of $50 \times 10^3$ Monte Carlo circuit samples 65

3.40 Cumulative percentage of binned circuits as a function of the achieved octree level . . . 66

3.41 Global bin escapes as a function of the number of circuit samples used in the training phase and the noise present in the alternate measurements 67

3.42 Grid search results for the comparison with support vector machines . 68

3.43 Best SVM classifiers using the training set shown in Figure 3.32 . . . 69

4.1 Stages of the acceleration to voltage transduction chain for integrated capacitive MEMS accelerometers . . . 72

4.2 Sketch of capacitive accelerometer inertial mass and comb fingers . . . 73

4.3 Sketch of a dual axis accelerometer mounted in a vertical spinning wheel and the accelerations involved . . . 75

4.4 Simulated Lissajous compositions of a dual axis IC accelerometer for different defect levels in the inertial mass . . . 77

4.5 Simulated Lissajous compositions of a dual axis IC accelerometer for different defect levels in the spring constant . . . 78

4.6 Simulated Lissajous compositions of a dual axis IC accelerometer for different defect levels in axes misalignment . . . 79

4.7 Simulated Lissajous compositions of a dual axis IC accelerometer for different defect levels in the medium permittivity or plate area . . . 80

4.8 Simulated Lissajous compositions of a dual axis IC accelerometer for different defect levels in the rest distance between plates . . . 81

4.9 Flow diagram showing an overview of the steps that characterize the training and testing phases . . . 84

4.10 Set of 50 Lissajous compositions generated with devices which sensitivities have been drawn from non correlated uniform distributions . . 85

4.11 Resulting specifications compliance and violation regions after digitizing the analog information of the Lissajous compositions shown in Figure 4.10 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 86

4.12 Octree encoding of the specifications compliance/violation regions for the case study presented in Figure 4.11 . . . . . . . . . . . . . . . . . . 87

4.13 Octree encoding of the specifications compliance/violation regions for the case study presented in Figure 4.12 . . . . . . . . . . . . . . . . . . 88

4.14 Lissajous trace information is replaced by its points of tangency with vertical and horizontal tangent lines . . . . . . . . . . . . . . . . . . . 89

4.15 Test escapes as a function of the number of bits used to encode the octree data structure . . . . . . . . . . . . . . . . . . . . . . . . . . . 90

4.16 Test yield loss as a function of the number of bits used to encode the octree data structure . . . . . . . . . . . . . . . . . . . . . . . . . . . 91

4.17 Test application time as a function of the number of bits used to encode the octree data structure . . . . . . . . . . . . . . . . . . . . . . . . 91

4.18 Lissajous trace compaction using the points of tangency with vertical and horizontal tangent lines . . . . . . . . . . . . . . . . . . . . . . . . 93

4.19 Calibration curves for $\beta$ angle ranging from $-20°$ to $+20°$ . . . . . . . 94

4.20 Diagnosis efficiency for each of the tangent points as a function of misalignment level . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 94

4.21 Diagnosis efficiency FOMs for each of the tangent points identified in the Lissajous curve . . . . . . . . . . . . . . . . . . . . . . . . . . . . 95

4.22 Photography of the experimental setup where the device is mounted . 96

4.23 Simulated and measured angular velocity profiles at the motor shaft . 96

4.24 Experimental Lissajous compositions of a dual axis IC accelerometer for $\{0, 5, 10, 15, 20\}°$ misalignment angles . . . . . . . . . . . . . . . . 97

4.25 Detail on how the experimental diagnosis procedure is carried out for tangency point 1 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 98

4.26 Diagnosed misalignments for each of the Lissajous tangency points and the weighted averaged diagnosis result . . . . . . . . . . . . . . . . . . 100

5.1 Example of a synthetic training set of indirect measurements and the corresponding octree encodings when $N_{\text{octrees}} = 3$ . . . . . . . . . . . . 105

5.2 Detail of the three rotated octrees depicted in Figure 5.1 . . . . . . . . 106

5.3 Example of multi-directional tessellation with $N_{\text{octrees}} = 1$ (left) and $N_{\text{octrees}} = 5$ (right) using the synthetic data set shown in Figure 5.1 . 106

5.4 Schematic of the Tow-Thomas Biquad filter used as case study . . . . 107

5.5 Magnitude Bode diagrams of the band-pass Biquad filter used as case study . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 108

5.6 Response of the band-pass Biquad filter when is excited with a multi-tone signal . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 109

5.7 Indirect measure space showing $10^4$ Monte Carlo circuit samples before applying the proposed multi-directional octree encoding technique . . 110

5.8 Indirect measure space encoded using a single octree . . . . . . . . . . 111

5.9 Indirect measure space encoded using 4 octrees . . . . . . . . . . . . . 112

5.10 Incurred test escapes metric resulting from the application of the proposed multi-directional tessellation technique . . . . . . . . . . . . . . 113

5.11 Incurred test yield loss metric resulting from the application of the proposed multi-directional tessellation technique . . . . . . . . . . . . 114

5.12 Average reduction and growth factors for the incurred false positive and false negatives test outcomes with respect to a single octree encoding 115

5.13 Incurred test yield loss metric as a function of a given test escape target 117

5.14 Example of multiple specification band guarding in the specifications space . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 118

5.15 Schematic of the 6th order band-pass Butterworth filter used as a case study . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 119

5.16 Magnitude Bode diagrams obtained by Monte Carlo simulations using technology statistical corner . . . . . . . . . . . . . . . . . . . . . . . . 120

5.17 Response of the Butterworth filter when it is excited with a multitone signal . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 121

5.18 Resulting octree after the application of the training phase to the set of $10^4$ Butterworth circuit samples shown in Figure **??** . . . . . . . . . 123

5.19 Levels distribution for the octree shown in Figure 5.18 . . . . . . . . . 124

5.20 Testing phase results using the octree shown in Figure 5.18 with band guarding factors of $r_1 = r_2 = 1$ . . . . . . . . . . . . . . . . . . . . . . 125

5.21 Cumulative percentage of tested circuits as a function of the achieved octree level for the testing phase . . . . . . . . . . . . . . . . . . . . . 126

5.22 Test escapes (left) and test yield loss (right) metrics as a function of the band guarding factors $r_1$ and $r_2$ . . . . . . . . . . . . . . . . . . . 127

5.23 Test escapes contour levels in the $r_1 - r_2$ plane . . . . . . . . . . . . . 127

5.24 Test yield loss contour levels in the $r_1 - r_2$ plane together with the resulting 1000 ppm test escape level from Figure 5.23 . . . . . . . . . . 128

6.1 Algorithm to select a subset of indirect measurements for mixed-signal testing . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 136

6.2 Schematic of the KHN Biquad filter used in the case study . . . . . . 138

6.3 Steady state transient response of the Biquad filter when it is excited with a multitone signal . . . . . . . . . . . . . . . . . . . . . . . . . . 139

6.4 Filter's frequency response obtained by Monte Carlo simulation . . . . 141

6.5 Pairwise scatter plots and distributions of filter performances obtained by Monte Carlo simulation . . . . . . . . . . . . . . . . . . . . . . . 142

6.6 Octree generated in the training phase encoding pass/fail circuits . . . 144

6.7 Scatter plot of test misclassifications as a function of the selection statistic . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 145

6.8 Scatter plot of test misclassifications as a function of the selection statistic for several Biquad topologies and filter outputs . . . . . . . . 146

6.9 Nominal and deviated analog signatures resulting from an XY signal composition . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 147

6.10 Integrated analog signal monitoring and digital signature generation . 148

6.11 Composition of two analog signals and four possible observation windows 148

6.12 Basic architecture of the signature generator system . . . . . . . . . . 149

6.13 Schematic of the integrated signature generator subsystem . . . . . . . 150

6.14 Layout of the integrated signature generator subsystem . . . . . . . . 150

6.15 Photograph of the integrated signature generator subsystem fabricated in an industrial 65 nm CMOS technology . . . . . . . . . . . . . . . . 151

6.16 Architecture of the 6-bit DAC based on an IWOC digital pattern generator . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 152

6.17 Photograph of the experimental setup . . . . . . . . . . . . . . . . . . 153

6.18 Oscilloscope chronograms of the signals involved in the serial transmission of the signature information . . . . . . . . . . . . . . . . . . . 154

6.19 Measured Lissajous composition of the input/output signals when a multitone is applied to a low-pass Biquad filter . . . . . . . . . . . . . 155

6.20 Simulated XY composition and the digitized experimental trace within the two observation windows considered in this case study . . . . . . . 156

6.21 Simulated and experimental data of the $\Delta y$ displacements of the two tangency points . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 157

# List of Tables

3.1 Band-pass Biquad filter test limits. . . . . . . . . . . . . . . . . . . . . . 32
3.2 Analog test metrics as a function of the number of Monte Carlo samples 37
3.3 Biquad filter functional specifications. . . . . . . . . . . . . . . . . . . . 45
3.4 Biquad filter testing simulation results. . . . . . . . . . . . . . . . . . . . 48
3.5 Butterworth filter design specifications. . . . . . . . . . . . . . . . . . . 58
3.6 Butterworth filter bin limits. . . . . . . . . . . . . . . . . . . . . . . . . 59
3.7 Bin escapes matrix for octrees based binning (%). . . . . . . . . . . . . 62
3.8 SVM classifiers training information. . . . . . . . . . . . . . . . . . . . . 68
3.9 Comparison between octrees and support vector machines. . . . . . . . 70
3.10 Bin escapes matrix for SVM classifier (%). . . . . . . . . . . . . . . . . 70

4.1 Metrics for 10° misalignment. . . . . . . . . . . . . . . . . . . . . . . . . 92
4.2 FOMs for diagnosis efficiency functions considering different misalignment levels. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 93
4.3 Experimental diagnosis results and discrepancies. . . . . . . . . . . . . 99

5.1 Band-pass Biquad filter specifications and test limits. . . . . . . . . . . 107
5.2 Performance and overhead evaluation. . . . . . . . . . . . . . . . . . . . 116
5.3 Butterworth filter components values. . . . . . . . . . . . . . . . . . . . 119
5.4 Band-pass Butterworth filter specifications. . . . . . . . . . . . . . . . . 119
5.5 Butterworth filter test limits. . . . . . . . . . . . . . . . . . . . . . . . . 120

5.6 Kendall's Tau rank correlation coefficient between candidate indirect measurement pairs. . . . . . 122
5.7 Multiple specification band guarding results. . . . . . 129
5.8 Multiple specification band guarding results when Gaussian noise is added to the indirect measurements. . . . . . 129

6.1 Band-pass Biquad filter specifications. . . . . . 138
6.2 Kendall's Tau rank correlation coefficients between candidate indirect measurements for the band-pass KHN Biquad filter. . . . . . 143
6.3 Measured observation windows limits. . . . . . 153
6.4 Measured $\Delta y$ displacements for several $\Delta f_0$ deviation levels and diagnosis and test results. . . . . . 156

# Chapter 1

# Introduction

Society is continuously experiencing the advancements in electrical engineering as well as in computer technology. We all use electronics in a daily basis, consciously or unconsciously. Desktop computers, embedded systems, sensors, and actuators have become common elements in our everyday lifestyle. We all use them and we all expect these devices to function properly in developing the task they are supposed to. Hence, the following question arises: *Who is taking care all these elements function under the required specifications?* Well, test technology comes to the rescue. Every single device or subsystem within an electronic system has been tested, at least, at production stage and probably, if its functionality is critical within the system, it will be periodically tested until the end of its service life. In other words, none of us want the airbag in our car not to deploy in a collision because the embedded accelerometer did not function as expected. This probably gives us an idea of the important and crucial role of testing in the electronic industry.

This thesis is about electronic mixed-signal testing. As mentioned earlier, computers rule the XXI century world, but real world is still analog. Computers are constantly interacting with analog sensors, so there must be some piece of electronics linking these two worlds. This is the mixed-signal domain. For instance, the analog signals provided by sensors need to be filtered, boosted, clipped, or conditioned in any other form. Also, these signals will be digitized in order to allow the interaction with a computer, so an analog to digital conversion will be probably required too. These analog processing steps, amongst others, exemplify the kind of tasks carried out within the mixed-signal realm. At this point, it seems quite reasonable to highlight the importance and crucial role of testing the analog and mixed-signal circuitry within any electronic system. This field, as opposed to the digital domain, entails a considerable number of challenges and open problems with no systematic solutions and therefore, an amazing scenario to dive into.

This chapter serves as a motivation and introduction to the existing challenges in

analog and mixed-signal testing and more specifically, in *alternate* analog and mixed-signal testing. Some of these challenges are briefly exposed and discussed in order to motivate the pursued research of this thesis. The succinct motivation presented in this chapter will be later extended by the state of the art in Chapter 2. The general and specific objectives pursued in this thesis are listed and commented. The thesis organization is then described by providing a summary of each of the chapters and by framing them within the thesis roadmap as well as with the published results in referred journals and conferences.

## 1.1 Motivation

The extreme scalability in current VLSI circuits represents a remarkable challenge in nowadays microelectronics, both in the fields of design and test. New circuits are able to integrate in the same chip a growing number of devices which perform many different functions (digital processing, analog and mixed-signal processing, signal conditioning, data storage, sensing,. . . ). Because of this miniaturization, process variability, temperature, voltage and aging can make the circuit not to fulfill the set of functional specifications. These facts cause new failures to appear and therefore classic test and diagnosis methods based on specifications are becoming even more challenging.

Process variability is responsible of a large percentage of failures in VLSI circuits. Technological difficulties in the fabrication processes together with the hard to predict variability become the main concern in analog and mixed-signal circuits. As circuits scale down, the use of statistical methods in design, testing and diagnosis has grown considerably, what make classical approaches not that effieicnt. This calls for the need of new strategies to be used in robust designs, test and diagnosis of mixed-signal and heterogeneous circuits.

Classical CMOS processes represent a mature technology which requires advanced methods for testing, diagnosis and robustness as the reduction in size continues according to Moore's Law predictions, but there also exist emerging technologies which require novel paradigms to cope with the arising problems they present. Nevertheless, as it occurs in classical CMOS processes, variability plays a crucial role which has to be taken in special consideration.

Semiconductor industry is heavily demanding close to zero defect levels, specially for those safety critical applications seen in a wide variety of industries, such as automobile or aeronautics. The ever increasing device verification costs, together with the challenges encountered in analog and mixed-signal testing makes it an important focus of research. The cost impact of classic analog test techniques is not acceptable in high volume mixed-signal productions. The aforementioned scenario brings a set of challenges in the field of alternate test of analog and mixed-signal circuits and justifies the need of doing research in order to cope with all these demands and challenges.

## 1.2 Objectives

The objective of this dissertation is to propose methodologies to improve the alternate test and binning of analog and mixed-signal circuits as well as heterogeneous systems under the challenging scenario previously introduced. The forthcoming paragraphs focus on the specific objectives targeted in this thesis.

The efficiency in testing VLSI circuits is usually evaluated in terms of test escapes and test yield loss metrics. Such metrics are considered critical because of the high amount of incurred costs if faulty chips reach the market (test escapes) or non faulty chips are tagged as faulty (test yield loss). The key point to overcome these problems is to develop effective testing and quality binning techniques for analog and mixed-signal circuits to allow the reduction of these analog metrics. The capability of controlling and leveraging these two metrics becomes also a critical step in any production test program therefore allowing a proper adaption to the specified test target.

Heterogeneous systems testing comprise an extra dose of challenge. They include all the difficulties encountered in classical analog and mixed-signal testing plus the ones found due to their inherently non electrical nature depending on the transduction principle they exploit. This dissertation targets the proposal of novel alternate test strategies for testing MEMS accelerometers capable to overcome the existing challenges in dealing with such kind of devices.

Test application time plays a crucial role in analog and mixed-signal test technology and is one of the main objectives pursued in this dissertation. Test application time, together with test efficiency and the required resources conform a set of key aspects to decide whether or not adopting an alternate test technique over a classical specification based test approach. For that reason, the proposal of time efficient alternate testing methodologies for analog and mixed-signal circuits becomes an imperative goal in this thesis.

In an alternate testing scenario, there exist multiple susceptible measurements to perform and use within the testing procedure, albeit not all the measurements serve with the same efficiency to such endeavor. The selection of alternate measurements plays an important role in alternate testing since they must provide, at least, all the information provided by the classical specification based testing method yet keeping their easy to obtain quality. This dissertation targets the proposal of selection algorithms to achieve a suitable subset of alternate measurements for analog and mixed-signal testing.

## 1.3 Thesis Organization and Contributions

The dissertation is organized in seven chapters as sketched in the thesis roadmap shown in Figure 1.1 and Figure 1.2. The diagrams also contain the published results contributing to each of the chapters. The keys used in the references refer to those listed in Appendix A, page 165. The following paragraphs describe the structure

of the dissertation and provide a peek on the contents of each chapter. For easy reference, each chapter contents are described based on the two most significant published results in which it is based.

**Chapter 2** presents the challenges in alternate test and binning of mixed-signal circuits. Special care is taken in framing the thesis in the context of the issues derived from process variations due to the extreme miniaturization. Considerable emphasis is devoted to the existing alternate test methods, specially taking care of the challenges encountered when indirect measurements are used to take the test decision. The chapter focuses on the most commonly used regression and classification techniques in the field. As will be shown later, one of the most challenging issues in alternate mixed-signal testing is the encoding of the test acceptance/rejection regions. This makes circuit classification techniques of relevant importance in this thesis.

**Chapter 3** introduces a novel methodology to encode the test acceptance/rejection regions in the alternate measurement space. The proposed technique relies on tessellating the space using $2^n$-ary trees. Such binary tessellation is convenient because of its simplicity and straightforward digital implementation. Also, it has the great advantage of being able to encode the space very fast since the tree resolution is increased just where it is needed, i.e. in the surroundings of the test decision boundary. The tree data structure is also advantageous for high volume production testing since the test decision is achieved within a few comparisons due to the fast traversal of the resulting sparse tree. The published results in which Chapter 3 is based on are listed on the roadmap shown in Figure 1.1.

The application of octree data structures to encode the test acceptance/rejection regions was proposed in the paper *M-S Test Based on Specification Validation Using Octrees in the Measure Space* presented at the *European Test Symposium* in May 2013. The publication corresponds to reference [C11] in the list shown on page 165. The paper introduces the octree encoding methodology and applies it to test a second order filter affected by parametric variations. The method comprises two phases, namely, training and testing phases. In the former phase, circuit samples are generated based on Monte Carlo simulations, mathematical models or actual production data. The acceptance/rejection region is then encoded using octrees. The latter phase corresponds to the actual high volume production test using the previously encoded octree data structure. The benefits of the methods are discussed based on test escapes and test yield loss metrics as well as the test application time.

The proposed methodology of using octrees to encode the test acceptance/rejection regions can be extended to the more general concept of quality binning of analog and mixed-signal circuits. After volume production, fabricated circuits may present several levels of specification compliance. The manufacturer can take advantage of such levels by selling the fabricated ICs at different price rates according to their respective specification compliance levels. It turns out that octree based space tessellation becomes extremely adequate in such task since just a single tree is able to manage an arbitrary number of disjoint bins with exactly the same advantages shown for the test application.

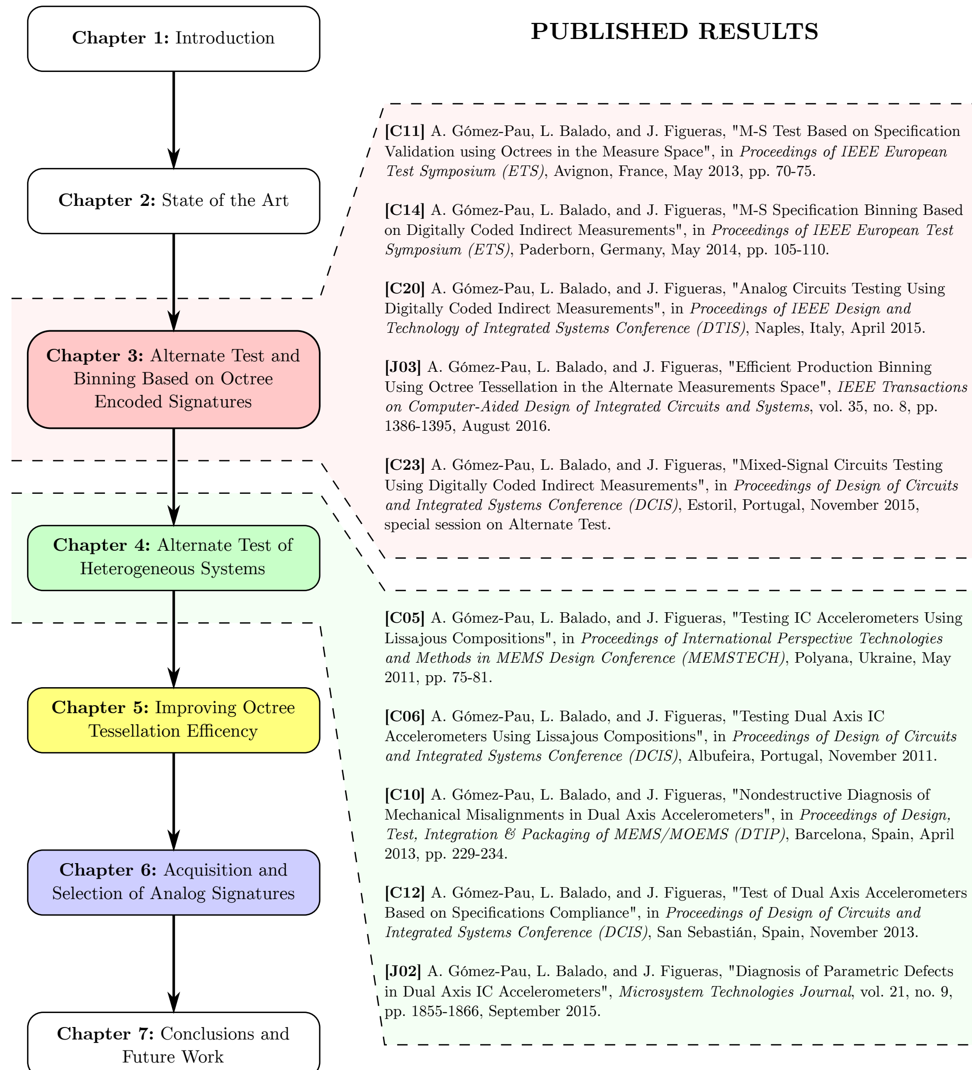


**Figure 1.1:** Thesis roadmap together with the published results contributing to chapters 3 and 4. Refer to Appendix A in page 165 for a complete list of publications.

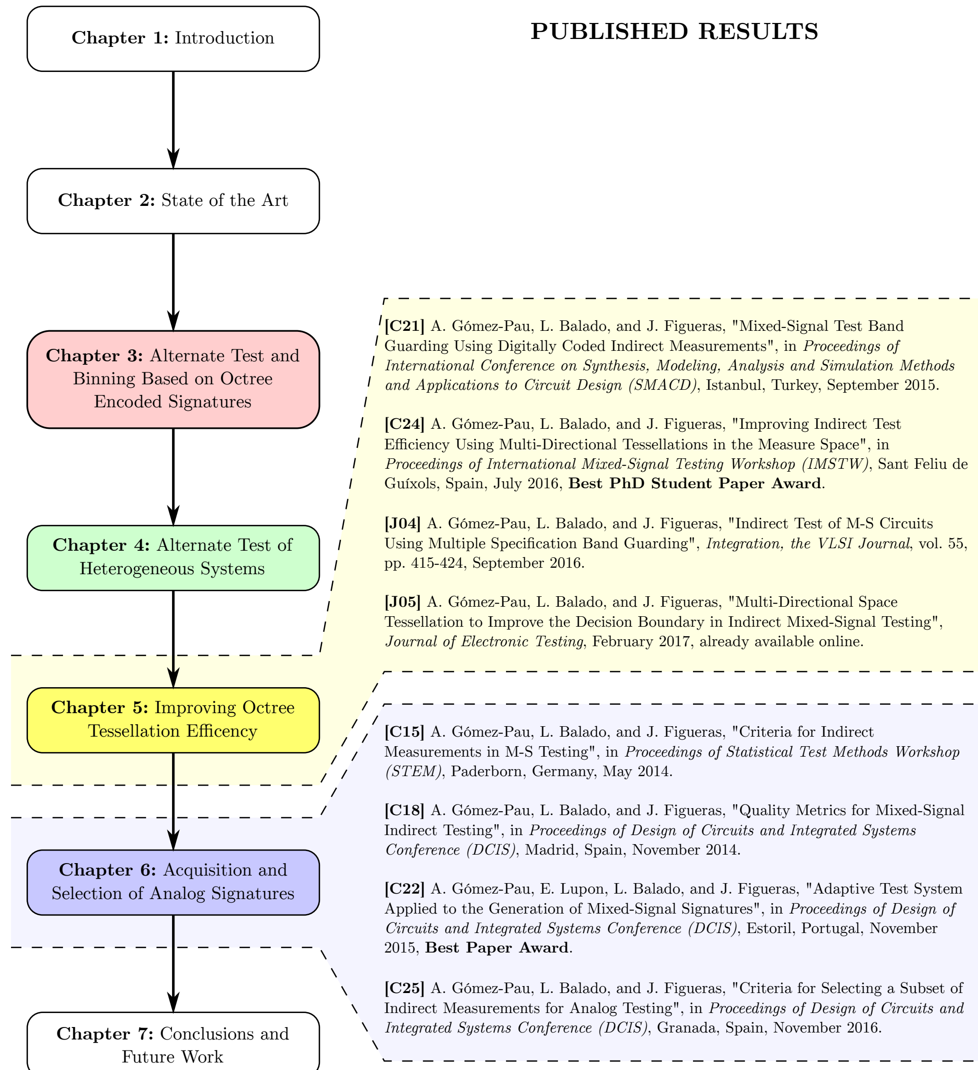


**Figure 1.2:** Thesis roadmap together with the published results contributing to chapters 5 and 6. Refer to Appendix A in page 165 for a complete list of publications.

High volume production binning of mixed-signal circuits using octrees was proposed in the article *Efficient Production Binning Using Octree Tessellation in the Alternate Measurements Space* published in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, volume 35, issue 8, in 2016. The publication corresponds to reference [J03] in the list shown on page 165. The method relies on the same principles mentioned earlier but considering and arbitrary number of bins, which are encoded accordingly, using an octree data structure. In order to illustrate the proposal, the method has been applied to a band-pass Butterworth filter considering three specification bins as a proof of concept. Successful simulation results are reported showing considerable advantages as compared to a SVM based classifier. Similar bin misclassifications are obtained with both methods while the binning time is 5 times faster when using octrees than when using the SVM based classifier.

**Chapter 4** is devoted to test heterogeneous systems, and more concisely, to MEMS accelerometers testing. As previously mentioned, testing heterogeneous systems is even more challenging than testing classical mixed-signal circuits due to their inherently non electrical nature. For the case of MEMS accelerometers, their mechanical subsystem must be mechanically excited in order to emulate the actual device operating conditions. Chapter 4 presents a novel methodology for testing MEMS accelerometers by using a vertical spinning wheel setup. This provides a rich kinematic excitation to the DUT as well as being able to capture parametric and catastrophic defects via the orthogonal composition of device outputs. Such composition conforms the alternate measurement space which is then tessellated using the octree encoding technique introduced in Chapter 3. Alternatively, the analog signature can be processed and compacted to extract the necessary information which allows the testing of the device. The published results in which Chapter 4 is based on are listed on the roadmap shown in Figure 1.1.

Testing MEMS accelerometers using octree tessellation was proposed in the paper *Test of Dual Axis Accelerometers Based on Specifications Compliance* presented at the *Design of Circuits and Integrated Systems Conference* in November 2013. The publication corresponds to reference [C12] in the list of publications shown on page 165. The paper uses the aforementioned kinematic excitation and encodes the Lissajous alternate space using octrees following the methodology presented in Chapter 3.

The vertical spinning wheel excitation comprises three different accelerations which are sensed by the DUT, namely, gravity, tangential, and centripetal accelerations. Such complex kinematic excitation makes the test setup undoubtedly sensitive to parametric deviations within the subsystems conforming the device. The inspection of the Lissajous patterns generated by the DUT and its test setup can then be used to identify the deviated parameter if a defect catalog is available. Although the whole Lissajous picture comes in handy when identifying a deviation by simple inspection, it is not that useful if the deviation level needs to be quantified. For that reason, a method for compacting the trace into a representative finite set of points is proposed as well as a metric to rate the sensitivity or diagnosis efficiency of

each of the selected trace points. Using this information, the deviation level can be inferred and therefore the test decision taken. The proposed vertical spinning wheel excitation, together with the signature compaction and metric efficiency evaluation has been experimentally applied to test a MEMS accelerometer.

The vertical spinning wheel test and diagnosis methodology was proposed in the article *Diagnosis of Parametric Defects in Dual Axis IC Accelerometers* published in *Microsystem Technologies Journal*, volume 21, issue 9, in 2015. The publication corresponds to reference [J02] in the list shown on page 165. Several device parameters have been studied and characterized under different deviation levels. The definition of a metric and the evaluation of its diagnosis efficiency is used to optimize the diagnosis procedure against noisy measurements. The method has been experimentally applied to diagnose the misalignment degree in a commercial dual axis accelerometer. The Lissajous characterization of the defect is illustrated and experimental results are reported. Misalignment diagnosis results show the viability of the proposal.

**Chapter 5** focuses on two major improvements that have been developed in the frame of the proposed octree encoding strategy presented in Chapter 3. A test strategy efficiency is usually evaluated in terms of false positives and false negatives test outcomes, which directly impact the costs of the whole test procedure as well as the final product. Depending on the actual IC, fab or customer requirements, these analog test metrics are usually bounded or restricted in some sense. Because of that reason, two major octree tessellation improvements have been proposed, namely, an ensemble of rotated octrees and a guard banding strategy. The former developed improvement is based on encoding different octrees at different angles and combine their individual information to yield to better misclassification levels. The latter technique corresponds to a multiple specification guard banding methodology implemented with octrees in order to balance the test yield loss and test escapes as desired. The leverage of analog test metrics becomes a useful feature in mixed-signal testing since it allows the accommodation to fab and customer requirements. The published results in which Chapter 5 is based on are listed on the roadmap shown in Figure 1.2.

The multi-directional tessellation based on an octree ensemble was proposed in the paper *Improving Indirect Test Efficiency Using Multi-Directional Tessellations in the Measure Space* presented at the *International Mixed-Signal Testing Workshop* in July 2016. An enhanced version of the work was published in the article *Multi-Directional Space Tessellation to Improve the Decision Boundary in Indirect Mixed-Signal Testing.* in *Journal of Electronic Testing* in February 2017. The publications correspond to references [C24] and [J05], respectively, in the list shown on page 165. The work in [C24] was honored with the **Best PhD Student Paper Award** distinction at the conference.

The articles prospect the possibilities of using space tessellations along multiple directions in order to improve the test decision boundary definition in the alternate measure space. The proposed method is able to reduce false positive test outcomes, with acceptable penalty in test yield loss metric, or vice-versa. The key idea presented in this work is to use an ensemble of octrees, each of them tessellating the plane along different directions. Such tessellations create a refinement in the non

linear test decision boundaries without the need of including extra circuit samples. The tree ensemble, together with a strict test decision criterion, serve as a classifier during the production testing phase. The proposed multi-directional ensemble tessellation strategy has been applied to test a band-pass Biquad filter affected by parametric variations. The proposed method has shown to be effective in lowering the test escapes metric as compared to a single octree classifier. The computational overhead of evaluating several octrees is insignificant since $2^n$-ary tree data structures can be efficiently traversed to yield a test decision. The octree ensemble technique has also been compared against a classic specification guard-banding technique reporting better test yield loss metrics for the same test escape target.

The multiple specification guard banding methodology using octrees was proposed in the paper *Mixed-Signal Test Band Guarding Using Digitally Coded Indirect Measurements* presented at the *International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* in September 2015. An enhanced version of the work can be found in *Indirect Test of M-S Circuits Using Multiple Specification Band Guarding* published in *Integration, the VLSI Journal* in September 2016. The publications correspond to references [C21] and [J04], respectively, in the list shown on page 165.

The papers propose a multiple specification band guarding technique as a method to achieve a test target of misclassified circuits. The acceptance/rejection test regions are encoded using octrees in the measurement space, where the band guarding factors precisely tune the test decision boundary according to the required analog test metrics targets. The generated octree data structure serves to cluster the forthcoming circuits in the production testing phase by solely relying on indirect measurements. The combined use of octree based encoding and multiple specification band guarding makes the testing procedure fast, efficient and highly tunable. The proposed band guarding methodology has been applied to test a band-pass Butterworth filter under parametric variations. Simulation results are reported showing noteworthy improvements when the multiple specification band guarding criterion is used.

**Chapter 6** focuses on a topic of major concern in the field of alternate testing, selection and acquisition of indirect measurements. Special care is devoted to an adequate selection of indirect measurements using statistical methods that yield to better and less costly test results. Throughout the chapter, the details of the design and application of an adaptive test system for mixed-signal circuits are presented as well the experimental results derived from its application to an analog system. The published results in which Chapter 6 is based on are listed on the roadmap shown in Figure 1.2.

An algorithm for selecting a subset of alternate measurements was proposed in *Criteria for Selecting a Subset of Indirect Measurements for Analog Testing* presented at the *Design of Circuits and Integrated Systems Conference* in November 2016. The publication corresponds to reference [C25] in the list of publications shown on page 165.

The work proposes a criterion to select a subset of indirect measurements avoiding

redundant information. The key idea of the proposal is to reduce the actual number of measurements to be performed to those strictly providing relevant information to the testing procedure, therefore keeping the incurred test misclassifications at acceptable levels. The method selects the measurements presenting minimum mean and spread of the correlations between all the possible pairs formed by the measurements within the target subset. In order to show the viability of the proposal, the method has been applied to select a subset of indirect measurements in several analog filters being affected by parametric variations. The obtained misclassification levels using the subset of measurements indicated by the proposed method are considerably low, therefore highlighting the benefits of the proposed selection methodology.

A system for acquiring analog signatures was proposed in the paper *Adaptive Test System Applied to the Generation of Mixed-Signal Signatures* presented at the *Design of Circuits and Integrated Systems Conference* in November 2015, honored with the **Best Paper Award** distinction at the conference. The publication corresponds to reference [C22] in the list of publications shown on page 165.

The work proposes an adaptive test system to measure and generate indirect digital signatures. The system is composed by an integrated digital signature generator and a digital control and acquisition subsystem. The signature generator is based on a converter architecture in which the analog range can be adapted. Also, the internal references are implemented using an active voltage divider, what yields to a compact and adaptive design since the actual resolution is increased as the signal range to be converted is reduced. The digital subsystem controls the proposed architecture as well as captures and stores the digital codes sent by the digital signature generator. The digital signature generator has been designed and fabricated in an industrial 65 nm CMOS technology while the digital control and acquisition subsystem has been implemented in an FPGA. The whole system has been applied to test a Biquad filter affected by parametric shifts. Results are reported showing the capabilities of the proposed adaptive test system.

Finally, **Chapter 7** is devoted to summarize the conclusions and contributions of the dissertation as well give some future research guidelines.

Chapter 2

# State of the Art

In this chapter, the state of the art in alternate test and binning of mixed-signal circuits is reviewed. One of the main challenges in alternate analog and mixed-signal testing is the representation or encoding of the test acceptance/rejection regions in order to take the test decision in a high volume production test program. This thesis is framed within the aforementioned challenging scenario, so special emphasis is devoted to focus this chapter in such particular issue and the related methods found in the literature of the field.

Chapter 2 is organized as follows. First, a general view of the challenges existing in alternate analog and mixed-signal testing is given with special emphasis in showing how such indirect procedures serve as a promising solution to battle against the ever increasing analog and mixed-signal testing costs [1]. Then, some of the methods found in the literature to overcome these challenges are briefly reviewed and explained. Basically, two different techniques can be distinguished, namely, regressors and classifiers. Amongst the first group, multi-adaptive regression splines (MARS) plays an important role in the field, while artificial intelligence (AI) techniques dominate the methods within the second group [2]. Subsequently, the challenges and advancements in alternate test of heterogeneous systems with particular attention to MEMS systems are reviewed. Then, the concept of quality binning for analog and mixed-signal is introduced and the benefits it may provide are highlighted [3]. Some works making usage of mixed-signal quality binning are commented. Finally, the chapter closes with an overview of the guidelines proposed in the literature to overcome the problem of selecting an adequate subset of alternate measurements for analog and mixed-signal testin.

## 2.1 Alternate Test of Mixed-Signal Circuits

Production testing of analog and mixed-signal circuits is an increasingly challenging task due to the presence of statistical variations related with the manufacturing process which directly affect circuit specifications [1,4]. High amount of resources are solely dedicated to test and diagnose such devices to ensure that only specification compliant circuits are shipped to customers [1, 5].

Semiconductor industry is demanding close to zero defect level devices, specially for those applications considered as safety critical, such as automobile and aeronautics [6]. The continuous miniaturization of technology nodes and the ever increasing device verification costs, together with the challenges encountered in analog/RF and mixed-signal testing makes this topic a crucial focus of research [1, 7]. The incurred costs in classic specification based test are not acceptable in high volume productions batches. These costs can be reduced when using non specification based procedures, usually referred as alternate or indirect test techniques [8,9]. Instead of directly measuring the functional specification to be validated, alternate test proposes to measure other easy to measure parameters and use them to predict the actual specification and/or to decide whether the circuit is within specifications or not.

When indirect measurements are used to validate circuit performances, lots of factors affect test metrics results. Test yield loss, i.e. good circuits failing the test, and specially test escapes, i.e. bad circuits passing the test, are of major concern for the acceptance of such procedures in a production test program development [7]. The main problem is how to use these alternate data in order to take the test decision without incurring in a prohibited number of misclassified circuits. Regression and machine learning techniques have been widely accepted for such a purpose [10]. For instance, in [7,11] a two tier approach is proposed to retest those circuits with chances of not being correctly classified by the first tier. The work in [12] uses copula theory in order to estimate the tails of distributions and therefore tune the process to achieve the required analog test metrics.

Alternate testing using classifiers implies a clustering process in which the main goal is to obtain a reliable boundary definition to separate circuits fulfilling the specifications from circuits violating them. When such clustering is made with indirect measurements, i.e. different from the actual specifications, getting the correct test decision boundary may become a difficult and challenging task. The benefits of using easy to obtain measures is worth only if the resulting analog test metrics fit the specified test targets [11].

The proposed technique in this thesis relies on tessellating the space using binary trees coming from the field of computer graphics [13] and data clustering [14]. The procedure is referred as $2^n$-ary tree space tessellation or in some cases octree tessellation due to its 3D computer graphics connection. In this technique the space is encoded using octrees to determine the test acceptance/rejection regions and such data structre is later used in the actual production testing phase to decide whether a circuit is classified as pass or fail.

## 2.2 State of The Art Methods in Alternate Test

In an alternate test program, once the alternate measurements have been performed, the test decision must be taken by solely relying on the set of measurements. Basically, two main approaches can be identified in the literature to such purpose, regression based techniques and classifier based techniques.

**Regression based approach:** Relies on constructing a mathematical model to map the actual circuit performances to the set of alternate measurements. This way, for every tuple of circuit measurements the functional specifications can be obtained by simple evaluating them in the regressor function that was previously trained, and the test decision is actually taken in the inferred circuit performance space. This approach requires a regressor to be trained for every functional specification that needs to be validated.

**Classifier based approach:** Uses state of the art data clustering methods to train (using different procedures) a classifier capable of representing the arbitrary test acceptance/rejection regions within the alternate measurements space. The test decision is take by evaluating the set of alternate measurements in the trained classifier. Oppositely to the regression based approach, classifiers directly yield to the test decision in the alternate measurements space.

Each of these two approaches present different particular methods. For the case of regression based approaches, one can identify linear and nonlinear regression techniques. Within the nonlinear regression techniques, MARS regression plays an important role in the field. For the case of classifier based approaches, one can identify a vast variety of methods, most of them within the artificial intelligence domain such as artificial neural networks (ANN) or support vector machines (SVM).

### 2.2.1 Regression Techniques

The underlying idea using regressions is to find a mapping function (the regressor) able to predict circuit performances as a function of certain set of indirect measurements. To this purpose, a regression function is needed for each functional specification. Once the regressors are trained, the functional specifications are obtained and therefore the test procedure is reduced to a naive specification based test to see whether each of the specs lie in its test acceptance region or not.

A huge variety of regression functions and methods in the statistical literature, but here, just the most commonly extended and used methods in alternate test of mixed-signal circuits are reviewed. The simplest and easy to understand regression method is the classical linear regression in which the independent or explanatory variables are fitted to a linear variety, i.e. straight line, plane, hyperplane, etc..., to construct a linear model for the response variable. Of course, the previous simple approach can be extended to arbitrary nonlinear functions if a certain mapping is known to fit

well to a certain nonlinear relationship. The multivariate adaptive regression splines (MARS) approach has been extensively used in alternate test of mixed-signal circuits. The MARS model is constructed similarly to linear regression but using what are called "basis functions", which can be linear or nonlinear, and their interactions. The subsequent sections briefly describe all these methods and point to some works that have used them serving to alternate test purposes.

### Linear Regression

Probably, linear regression is the most naive form of regression but still serves as a suitable tool for mapping the indirect measurements to functional specifications in the frame of alternate test. In this section, the term linear regression refers to multivariate linear regression. There are situations in which the indirect measurements clearly present a linear relationship between each of the functional specifications to validate. In such scenarios, linear regressions play a crucial role in inferring the desired circuit specifications. It is worth to mention that a proper statistical analysis of the residues is needed in order to assess the correctness of the linear regression. If the residuals do not present a normal distribution, then a more advanced regression technique must be used such as MARS regression or any other nonlinear regression model.

The way of tackling the general problem of multivariate linear regression is a well known method in statistics which relies on the solution of the so called *normal equations*. The *normal equations* derive from the concept of *leasts squares* fitting. These equations relate the response variable with the explanatory variables through the regression model parameters. The well established linear algebra methods allow a fast solution to the problem.

Many references and application can be found in the literature using linear regression in order to predict the functional specifications as a function of the alternate indirect measurements. For instance, Natarajan makes usage of linear regression in order to predict the damping factor, inertial mass and spring constant of a capacitive MEMS accelerometer [15]. The method is based on exciting the DUT using a multitone stimulus via the self test input pin. The measurement space corresponds to the response of the device to the applied stimuli which is in turn used to generate the mapping between the alternate measurement space and the specifications.

### Non Linear Regression: MARS Regression

Non linear regression based testing keeps the same concepts, objectives and principles of operation of linear regression but entangling the difficulties of fitting data to non linear functions. To such purpose, the usual way to proceed is to set and solve the problem using the so called *generalized leasts squares*. The method converges to the solution by iteration departing on a guess of the regression parameters. On each iteration the nonlinear regressor function is localy approximated with its 1st order Taylor expansion. Then, the classical linear *leasts squares* method can be applied and solve the normal equations similarly to linear regression.

In the field of alterante testing, the general non linear regression approach has been improved by the generalization capabilities of MARS regression, which is able to smartly add non linear terms to the resulting prediction function as required. The main drawback of classic multivariate linear regression, beyond the fitting of the parameters, is the selection of the non linear function to be fitted using the training data. This inconvenience makes classic non linear regression not as useful as MARS since the function relating the alternate measurements space to the actual circuit performances is not known a priori.

Te multiadaptive regression splines method was developed and proposed by Jerome H. Friedman in 1991 [16]. The basic idea on MARS regression is to add a series of basis function to construct a nonlinear model for the response variable [17]. These basis function may be linear or nonlinear as well as they may have what is called a knot. The knot prevents the function from contributing to the response variable within a certain domain. The knot is constructed using the so called hinge function involving the non differentiable $\max(\cdot)$ function. Figure 2.1 shows an example of a hinge function.

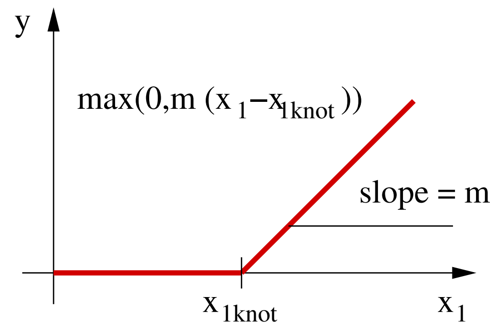


**Figure 2.1:** Example of MARS basis function using its associated hinge function with a knot.

Numerous research has been published taking advantage of MARS regression models. For instance, Hsiao uses a MARS model to test a phase-lock loop in [18]. Several functional specifications of the PLL are validated, such as the charge pump current, phase margin, bandwidth, locking time and several gains by using a MARS regressor based approach on alternate DC signatures. The underlying idea of the method is to integrate time varying voltages to get DC levels which are strongly correlated with the functional specifications to validate. The paper presents reasonable specs predictions using the trained MARS model.

Similarly, Abdallah presents a non intrusive sensor for extracting DC signatures from RF circuits in [19]. The used test vehicle is a low noise amplifier (LNA) whose functional specifications are modeled using a MARS regressor based on the aforementioned low cost DC measurements. The usage of the multi adaptive regression splines algorithm allows the prediction of the LNA specs within a reasonable misprediction error in the order of few percentage units.

Larguech presents a generic methodology for building efficient alternate test prediction models in [20]. The work focuses on the selection of those indirect measurements which are relevant to predict the desired functional specifications yet keeping the prediction error at low levels.

### 2.2.2 Classification Techniques

It is not deniable that artificial intelligence (AI) techniques have played a remarkable effort in solving engineering problems that, otherwise, would have been impossible to tackle. Electrical engineering, and, in particular, analog and RF testing is not an exception [21–23]. In the last years, the amount of research on analog and mixed-signal testing based on AI has seen a considerable ramp up. In this section, the most used AI methods in the field of analog and mixed-signal alternate testing are reviewed, i.e. artifical neural networks and support vector machines.

#### Artificial Neural Networks

Probably, one of the most representative AI methods are artificial neural networks (ANN). Artificial neural networks try to emulate the behavior of human brain synapse process to connect neurons to each other. The AI approach to such neuron cell connection is based on perceptron layers connected together forming a whole entity able to predict responses after a training process. The perceptron structure was first proposed by McCulloch back in 1943 [24]. The underlying idea is to sum a series of weighed inputs feed into the so called activation function. Figure 2.2 depicts the perceptron architecture within an ANN. This function is in charge of emulating the synapse firing process that takes place in the human brain. Firing function may be linear, polynomial or, the most commonly used, sigmoidal function. The artificial neural network is formed by several layers of perceptrons. The first layer is referred as the input layer while the last layer is referred to as the output layer. The inner layers are simply referred to as hidden layers since they remain unseen between the input and output layers. The number of hidden layers strongly decides the capability of the neural network to be able to classify inputs with non linear separation boundaries [2, 25].

Artificial neural networks correctly function after a nontrivial training process. The training for the case of neural networks is always a *supervised* training. The term *supervised* means that during the training process the input patterns are applied to the net and the weights are adjusted to get the desired, previously known, output. Otherwise, the training process is called *unsupervised*. One of the most successful and easy to apply training algorithms is the so called back-propagation training. The terms stands for the way the weights in each perceptron are computed and updated in each epoch until the desired error condition is met [25]. Artificial neural networks are not easy to train, specially if it is conformed by a large number of neurons (or hidden layers). The resulting network strongly depends on the chosen initial weight values and the convergence process may be slow. Also, depending on the training

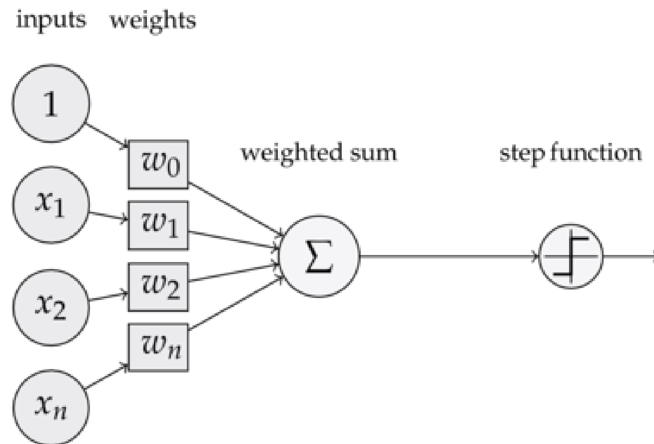


**Figure 2.2:** Example of a perceptron unit using a step firing function. Parameters $w_0, w_1, \ldots, w_n$ are the weighs computed during the training procedure.

procedure, it may occur the solution converges to a local minimum, what certainly questions the optimality of the resulting ANN.

In the context of alternate test of analog and mixed-signal circuits, several AI based works have been proposed to tackle the challenges behind the PASS/FAIL decision in the measure space. For instance, Stratigopoulos studies and demonstrates the feasibility of using an on chip artificial neural network for analog/RF built-in testing in [26]. The used network is composed of several hidden layers and implemented in a 0.5 $\mu$m CMOS technology. The VLSI implementation of the network itself is based on summing branch currents using current mirrors and bit configurable current sources acting as artificial axon weights. The performance of the hardware implemented neural net classifier is compared with its software counterpart for several numbers of hidden layers using a LNA as a test vehicle. The obtained results match each other showing the feasibility of the implementation for analog built-in test.

Stratigopoulos proposed a two tier based testing procedure relying on band guards using an ontogenic neural network and genetic algorithm in [7]. The used of band guards together with the two tier based testing procedure allows a practical tuning of test costs and test accuracy since a large amount of the tested circuits not relying within the band guards can be confidently tested using a single tier. Otherwise, the circuits within the guards are diverted to the second tier. Tuning the parameters related to such AI structures translates in the modulation of the cost/accuracy trade off.

The research cited earlier demonstrates the remarkable role of artificial neural networks in analog and mixed-signal alternate test to facilitate the PASS/FAIL decision.

### Support Vector Machines

Amongst the whole spectrum of statistical classification methods, support vector machine classifiers are one of the most widely used and one of the best techniques available in the literature presenting less misclassification rates. Support vector machines where first proposed by Cortés and Vapnick in 1995 [27]. The underlying idea of linear support vectors is not only to achieve a correct classification using the training set, but also to achieve a maximum margin classifier. That means the method targets to generate the separation boundary by locating the boundary itself at the maximum distance from the closest cluster elements, i.e. the support vectors. Such conditions yield to a quadratic program which can be easily solved using classical optimization algorithms such as Lagrange multipliers. Figure 2.3 shows and example of linear SVM classifier separating two linearly separable data clusters. As can be observed, the separation margin is the maxium possible for the given data distribution.

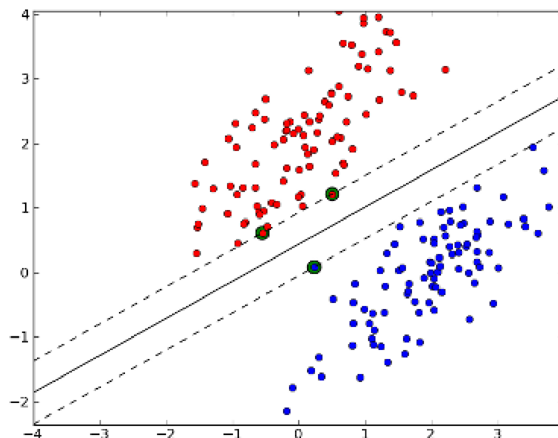


**Figure 2.3:** Example of linear SVM machine separator and the generated boundary with maximum margin separation. The support vectors are also highlighted.

For non linearly separable clusters, the dimensionality of the space is increased by using a non linear functions referred to as *kernel function*. The transformation of the input space to the so called *transformed space* or *feature space* yields to a more easy linearly separable data sets. Figure 2.4 shows the transformed input space after the aplication of a kernel function. SVM kernel functions may be functions of different nature such as linear functions, polynomials, radial basis function (RBF), sigmoidal functions,. . .

SVM classifiers are a popular choice when it comes to select an AI classification technique, but it comes together with some drawbacks such as the difficulty entangled

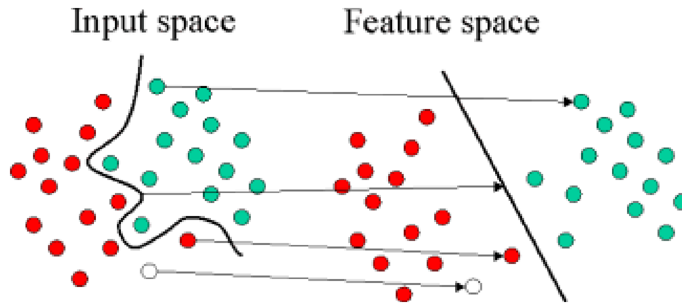


**Figure 2.4:** Example of a non linear SVM machine separator after the transformation of the input space using a non linear kernel function.

within the training process. First, a kernel function has to be chosen. Despite the appearance of the data may suggest what is the most suitable option, it is not immediate what kind of kernel may yield the best results. Given such situation, the practical option is to train several kernels, evaluate them, and select the one with the best performance, which does not seem to be optimal. Also, each of the possible kernel functions present some parameter which can not be determined a priori. Again, the way to proceed is by bruteforcing the training of different classifiers and selecting the one performing the best. The proper statistical approach to train a SVM is to use cross validation folds in order to avoid overfitting, fact that, together with the previously mentioned issues, increases the overall training time. Additionally, SVM classifiers only function with two class data sets, what entails the computation of several SVMs classifiers if more than two clusters need to be separated. The implementation of SVM, both the training and the evaluation, is not easy to achieve as a stand-alone or built-in solution.

Ke Huang used support vector machines in an alternate test procedure in [28] to identify counterfeit integrated circuits that are illegitimately pretended to be sold in the IC market. In this dissertation, the proposed space tessellation method to encode the test acceptance/rejection regions is compared against support vector machines classifier in Chapter 3.

## 2.3 Alternate Test of MEMS Systems

Diagnosis, test and quality control during fabrication are critical issues in the development of reliable MEMS devices [29]. Premature identification of possible failure sources becomes imperative to reduce the time to market of new units [30–32]. Fault diagnosis in MEMS systems presents similar challenges to those encountered in mixed-signal circuits. In addition, such devices require non electrical excitations inherent to their exploited transduction principle for sensors and actuators [33]. Costly automatic test equipment is needed because new features are added to the already expensive analog equipment such as vibration tables, spinning wheels, deflection measurements

or advanced microscopy techniques for optical microsystems.

Reliability of MEMS devices for safety critical applications require novel test and diagnosis strategies to achieve allowable production yields. Failures of MEMS structures have been studied for different architectures and materials [30, 31, 34]. The failure mechanisms mainly include stiction, fatigue, moisture contamination, process variations or electrostatic discharges. Such mechanisms result on catastrophic or parametric defects that need to be tested and diagnosed efficiently [32, 35].

For MEMS accelerometers, several studies have been proposed in the past as DFT (design for testability) and BIST (built-in self-test) techniques. As an example, there is a commercial digital test pin solution implemented in Analog Devices accelerometers [36]. Controlled with a digital input pin, an electrostatic force over specific outer combs mimics the inertial action of acceleration force. This way, makes online functional validation possible as a built-in test technique. Other proposals use similar outer comb actuators controlled with analog signals to evaluate different sensor parameters for capacitive and thermal devices [33, 37, 38].

Several techniques have been proposed for diagnosing MEMS accelerometers [39–44]. A calibration method based on device models is presented in [45] while a pseudo random generator in order to obtain the input-output transfer function is used in [46]. The work in [47] targets device calibration by performing different sets of measurements considering several device orientations. The work in [48] uses electrostatic actuation to excite the device and perform a set of measures which allow the test decision. An indirect diagnosis method is proposed in [15] using the regression techniques mentioned earlier to map the parameters space to the measures space.

In this dissertation, Chapter 4 presents an alternate testing setup to test and diagnose MEMS accelerometers using a vertical spinning wheel. The proposed method is able to manifest parametric and catastrophic faults.

## 2.4 Binning of Mixed-Signal Circuits

Fabricated ICs may present different degrees of specification compliance due to manufacturing process variations. Some devices exhibit excellent performance, therefore they are closer to nominal specifications, while others present worse performance, indicating they are far away from nominal specs. Specification based binning has been used as an efficient way of increasing production profit for digital circuits [21, 49–52]. To this purpose, several binning goals are considered, traditionally, power consumption and speed [3, 53]. Similar concept has been applied for binning analog and mixed-signal circuits [3, 54].

Production testing of analog and mixed-signal circuits is an increasingly challenging task due to the presence of statistical variations related with the manufacturing process which directly affect circuit specifications [1, 4]. High amount of resources are solely dedicated to test and diagnose such devices to ensure that only specification compliant circuits are shipped to customers [1, 5]. One possible option to reduce these

costs is to perform a specification based binning [3]. This allows the manufacturer to classify devices according to a quality criterion depending on how close the circuit is to nominal specifications [3]. See Figure 2.5 for an example of performance distribution for an analog circuit. As can be observed, the bandiwdth distributes accordingly to certain statatistical distribution. In such illustrating example, the higher the bandwidth, the best the circuit, therefore the circuits lying in this *super high quality bin* may be sold at a higher price. All the obtained performances may be binned in a similar way according to fab and customer requirements, therefore going beyond the binary test decision and taking profit of the actual distribution of performances.

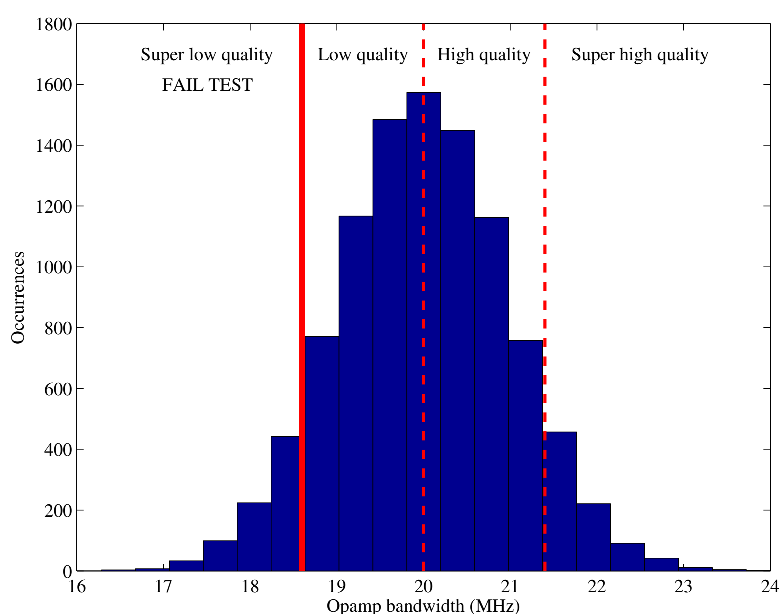


**Figure 2.5:** Example of performance bins for alternate analog and mixed-signal quality binning.

Binning of mixed-signal circuits can be achieved by simply measuring the specifications as in classic specification based testing or by performing alternate measurements that correlate to actual specifications [55, 56]. Alternate testing techniques require a mapping between the specification space and the measurements space in order to allow the test decision to be performed. Artificial intelligence [7] and regression techniques [11, 56, 57] have been used with successful results to this purpose, as well as using octrees to represent the pass/fail regions [58, 59]. Chapter 3 in this thesis, presents the usage of $2^n$-ary tree data structures to encode the specification bins in the alternate measurements space.

## 2.5 Selection of Alternate Measurements

Indirect testing strategies require the selection of a set of easy to measure parameters to be used in the alternate test procedure. To that purpose, many options exist, some of them entirely relying on designer's expertise and experience. The selection of alternate measurements for analog and mixed-signal circuits is an important aspect which is directly related to the test efficiency as well as to the incurred test costs.

ChatterjeeSome proposed the use of the sensitivity matrix between circuit's functional specifications and indirect measurements with the goal of maximizing its rank in [60]. This allows the avoidance of redundant information. Statistical methods have been also proposed, most of them relying on correlations and regressions techniques between the set of functional specifications and the set of indirect measurements [61]. For instance, Barragan proposed the usage of *Brownian distance correlation* together with a greedy algorithm in order to select a meaningful subset of measures adequate for analog/RF circuits testing in [62, 63].

In this thesis, Chapter 6 proposes a generic selection algorithm to conduct the selection of a subset of alternate measurements for mixed-signal testing. The method relies on a pairwise correlation statistic and a selection statistic which promotes the selection of those measurements subset presenting the maximum CUT information while avoiding redundancy within the subset.

Chapter 3

# Alternate Test and Binning Based on Octree Encoded Signatures

One of the most challenging aspects in alternate test of mixed-signal circuits is encountered when representing the test acceptance/rejection regions in the alternate measurements space. In this space, the test regions may be highly non linear, with arbitrary shapes and even present non connected regions, what greatly difficults the task of characterizing and representing them. As discussed in Chapter 2, machine learning techniques have been used in order to deal with such endeavor. Nevertheless, there are still many challenges to tackle in the field. This chapter proposes a novel methodology to encode the test decision regions using digitally encoded signatures. The technique presented in this chapter is based on a recursive tessellation of the space using octrees. Octrees derive from the field of computer graphics, where they where firstly proposed to represent arbitrary 3D objects with low computational resources [13]. The application of such recursive space tessellation technique can be easily generalized to several clusters and therefore extended to quality binning of mixed-signal circuits. The chapter focuses on using octrees to testing and binning of mixed-signal circuits showing its viability throughout several case studies.

## 3.1 Test of Mixed-Signal Circuits Using Digitally Encoded Signatures

In this section, the fundamentals of octree based encoding as well the way of using these data structures in analog and mixed-signal testing are explained. The algorithms that allow such encoding and evaluation are given as well as a few practical notes on its implementation. The efficiency metrics to evaluate the performance of the proposed method are defined and studied as well as the benefits such digital

encoding present in terms of computational effort are discussed.

The procedure of testing analog and mixed-signal circuits after high volume production can be formalized as the classification of any candidate circuit into a pass or fail cluster, according to certain circuit performances. Such clustering is performed according to parameters of different nature. The most common space for testing mixed-signal circuits is the *specifications space* in which circuit performances are directly measured and classified accordingly. Process variations may cause some circuits to violate or not fulfill the set of functional specifications. The effect of the uncertainties in the manufacturing process are modeled in this chapter by the statistical distributions offered by the technology process design kit (PDK) in the *components space*. As stated in Chapter 1 and Chapter 2, direct measurement of circuit specifications, i.e. specification based test, is difficult and time consuming [1]. Alternate measurements techiques are widely adopted as an indirect and effective solution to test analog and mixed-signal ICs [56]. Throughout this dissertation, the term *measurements space* will be used to designate the alternate measurements which will facilitate the testing process in the context of alternate mixed-signal testing. Figure 3.1 sketches these three spaces and the test boundaries defined according to certain specification levels.

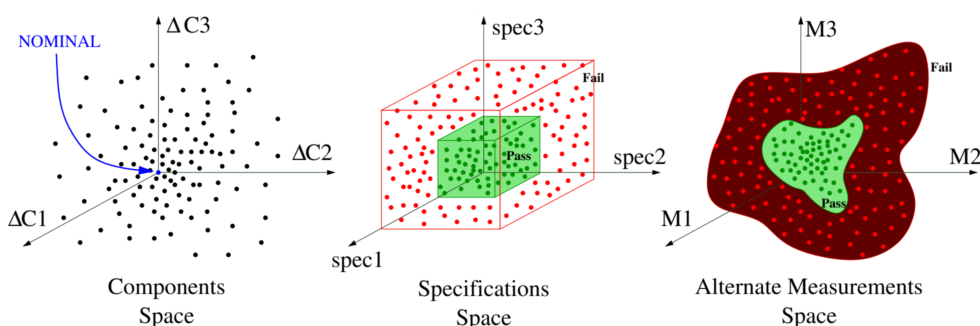


**Figure 3.1:** Sketch of the three spaces considered in this chapter. Components space variability induce deviations in the specifications space as well as in the alternate measurements space in which the testing process takes place.

The alternate measurements space almost never presents an easy to define test acceptance region. This is the actual challenge in alternate testing of mixed-signal circuits. For instance, Figure 3.2 shows an example of indirect measurements space for an analog circuit where the test acceptance region is an arbitrary shape. This fact becomes the starting point in alternate test of mixed-signal circuits using octrees.

### 3.1.1 Octree Encoding Fundamentals

The use of octrees to define arbitrary object shapes comes from the field of computer graphics as proposed in [13]. Their main applications include object identification, color quantization, rendering, and data clustering [64]. The successful usage of octree structures in electronic testing to classify mixed-signal circuit specifications comes

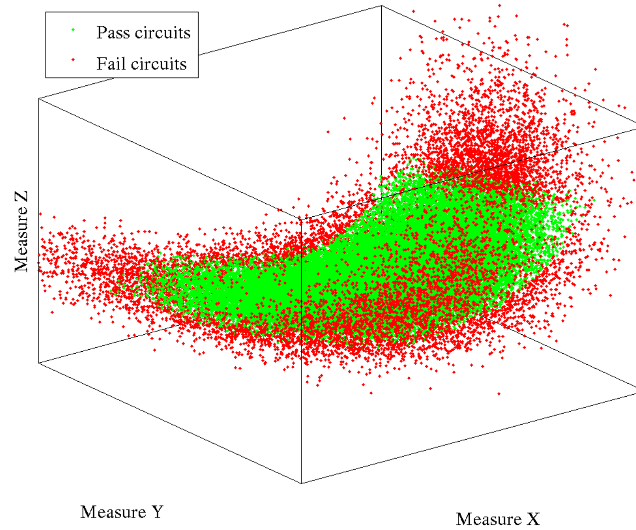


**Figure 3.2:** Example of alternate measures space and the pass/fail regions formed.

from the research developed in this dissertation and published in [58, 65]. In this section, the main ideas on $2^n$-tree data structures are reviewed, specially focusing in their applications in testing of mixed-signal circuits.

A $2^n$-tree data structure of dimension $n$ represents a geometric partition of an $n$-dimensional space. This representation is made by means of a tree in which each node has exactly $2^n$ branches, i.e. children branches, until the arrival to the latter nodes that do not have branches, i.e. tree leaves. Since one of their first applications were 3D computer graphics, each node has $2^3 = 8$ children. That is the reason that gives the most used name octree (8-tree) to this structure. For the case of 2-dimensional applications, they also receive the name of quadtrees (4-tree). See Figure 3.3 for an example of a 2-dimensional $2^2$-ary tree or quadtree.

To represent the contour of an object one needs to classify the data points to be inside or outside the shape boundary. This way, the procedure to obtain the boundary is solely based on the colored data points. To exemplify how a $2^n$-tree works to define a shape of one color object on a plane, let us consider a reduced set of bivariate data points of a green shape over a red background shown in Figure 3.4. The first step is to consider the square (an $n$-hypercube in $n$-dimensions) containing all the data points. By halving each dimension, the plane is tessellated in four equal size regions. If each of the resulting smaller squares exclusively contains single color data points, the square is tagged accordingly to that color class and no further partitioning is performed. Otherwise, the square is marked as decision pending (non colored parent nodes in Figure 3.4). This procedure adds new branch levels to the tree and continues

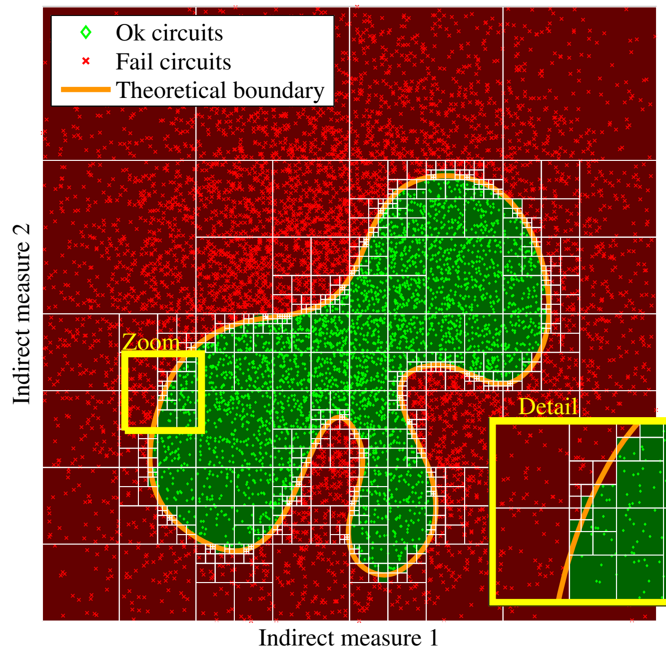


**Figure 3.3:** Quadtree generated using a few thousands data samples encoding an arbitrary 2D shape. As can be observed, the boundary refinement level increases as the number of available data in the training process increases.

until all the generated squares only contain equal color data.

In deep octree levels, depending on the number of data points and the statistical distributions of the available data, it may occur some squares do not contain points inside. This situation is solved by taking a decision according to the color of their neighboring squares. The number of levels achieved depends on the number of the available data points and their distribution. The tessellation of the plane is finer near the test decision boundary where different color data are the closest to each other. Here is where the octree algorithm performs the plane tessellation. When this process is accomplished, the configuration of the tree is totally defined and the boundary of the shape is approximated by means of straight lines or steps as can be observed in the zoom view of Figure 3.3.

In the next section, the way the octree data structure is evaluated using the alternate measurements obtained from a freshly fabricated circuit to yield a fast test decision is explained.

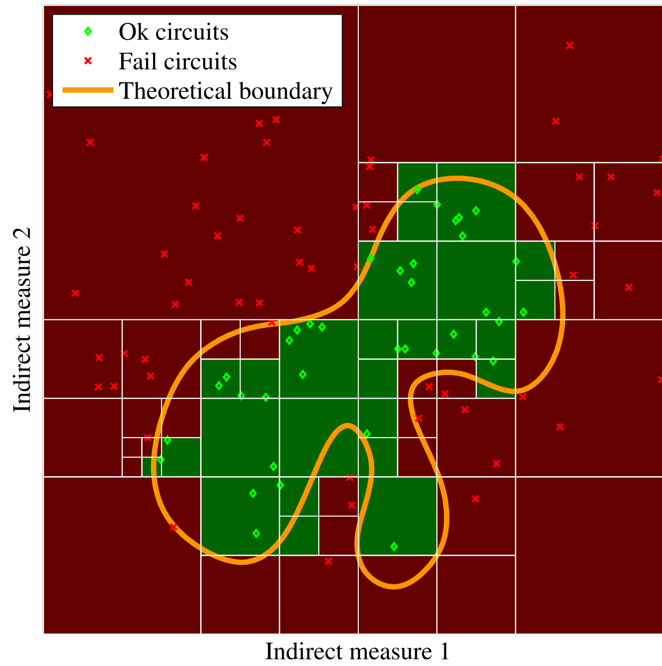


**Figure 3.4:** Two dimensional octree encoded. To simplify the exposition, just a few circuit samples have been considered. The obtained quadtree is 5 levels deep and has 81 nodes.

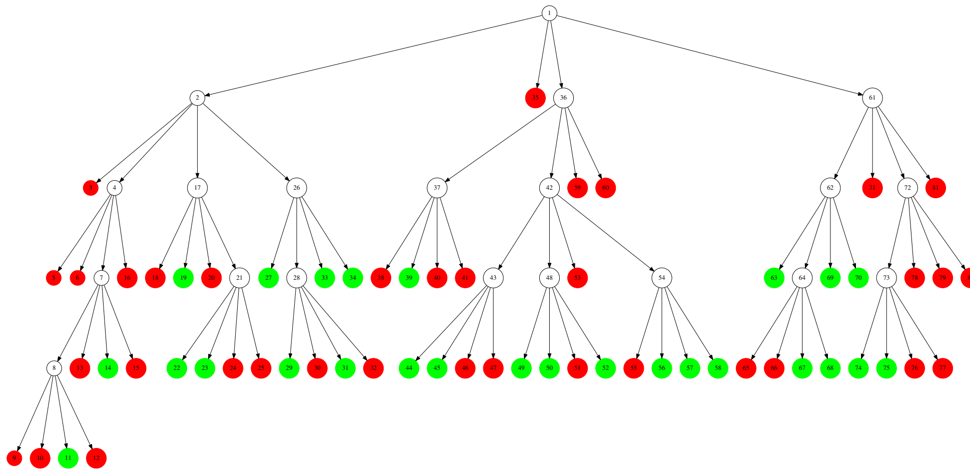

**Figure 3.5:** Graph of the octree depicted in Figure 3.4. White nodes correspond to parent octree cells.

### 3.1.2 Test Using Octree Data Structures

The dimension of the aforementioned octree data structure represent the number of alterante measurments in order to apply the test procedure whereas the colors represent the cluster in which a certain circuit is classified, i.e. pass or fail. The classification of a circuit merely consists in the evaluation of the obtained $2^n$-ary tree data structure.

To exemplify this classification process, consider the octree depicted in Figure 3.4 and a pair of circuit measures, $(M_1, M_2)$ in a 2-dimensional hypercube coming from a circuit that needs to be tested. The clustering procedure is performed using the octree graph representation of Figure 3.4. The algorithm used for circuit evaluation is listed in Figure 3.6. Assuming the $(M_1, M_2)$ data point is within the initial square, the algorithm checks to which quadrant it belongs to (SW, NW, SE or NE) by making one comparison per coordinate. This decision brings the candidate circuit to a new branch of the tree thus a deeper octree level is achieved. If the current node is colored, the point is mapped to that color and the evaluation finishes. If it is a non colored node, the evaluation algorithm repeats the decision operation through the graph until a tagged node is found and the circuit is finally classified.

```
1: function EvalMeasurements(N, M)
2:     Precond: N is an octree node data structure
3:     Precond: M is a vector of alternate measurements
4:     if N.label ≠ NULL then
5:         return N.label
6:     else
7:         idchild ← compare(M, N.center)
8:         N ← N.child[idchild]
9:         return EvalMeasurements(N, M)
10:    end if
11: end function
```

**Figure 3.6:** Pseudocode of a recursive implementation of the testing procedure using octrees in the alternate measurements space. Note that octree evaluation is efficient since only one comparison per coordinate and level traversed is required.

### 3.1.3 Efficiency Metrics

#### Test Efficiency Metrics

Any test method has certain probabilities of mispredicting some circuits, i.e. false positives and false negatives, also referred to test escapes and test yield loss. Reducing the misclassification levels is of crucial importance in high volume production testing of analog and mixed-signal circuits [6]. When using octrees, the training phase encodes the indirect measure space up to certain resolution which is actually

limited by the available sample density. When octrees are used to encode the space, the highly non linear test decision boundaries are difficult to resemble, specially in those regions where the boundary slopes differ from the orthogonal directions along which the octree is constructed. In this dissertation, the test efficiency metrics to evaluate the test preocedure are:

**Test escapes** Circuits that violate at least one specification but are classified as pass by the test method.

**Test yield loss** Circuits that certainly fulfill all the specifications but are classified as fail by the test method.

As a rule of thumb, higher costs are incurred if circuits not accomplishing the specified test limits are shipped to the customer, i.e. false positive circuits. This is why the test escape metric usually becomes the main concern when improving any test method although both metrics may be taken in account and leveraged according to several cost related criteria. In Chapter 5 some improvements regarding these issues will be presented as well as techniques that allow the leveraging of these both analog test metrics.

#### Test Complexity Estimation

The process of alternate testing of analog and mixed-signal circuits using octrees can be formalized as the application between the $n$-dimensional alternate measurements space and natural numbers. These natural numbers represent the test acceptance/rejection regions or quality bins as will be show later. That is, for any vector of alternate measurements, $M \in \mathbb{R}^n$, the octree maps it to a certain cluster $b$. For the case of test, $b \in \{1, 2\}$, 1 for pass and 2 for fail. Using the whole tree data structure $\mathcal{T}$, the testing procedure becomes $b = \mathcal{T}(M) \in \mathbb{N}$,

$$\begin{aligned} \mathcal{T} : \mathbb{R}^n &\to \mathbb{N} \\ M &\mapsto b \end{aligned} \tag{3.1}$$

Similarly, let $h(M)$ be the application mapping any vector of alternate measurements, $M \in \mathbb{R}^n$, to the maximum octree depth (or height) at that exact location. Under such definitions and according to the concepts and the algorithm given in previous sections, the number of comparisons, $N_c$, to test a circuit using a vector of alternate measurements, $M$, turns to be $N_c = n\,h(M)$, i.e. one comparison per coordinate and level traversed. Moreover, if $\mathcal{P}(M)$ denotes the joint probability density distribution in the alternate measurements sample space $\Omega \subset \mathbb{R}^n$, the average number of comparisons to test a circuit using the octree data structure turns out to be,

$$\overline{N_c} = n \int_{\Omega} h(M)\ \mathcal{P}(M)\, dM \ll n h_{\max} \tag{3.2}$$

Despite of the fact that the number of nodes of a sparse $2^n$-tree grows exponentially with the dimensionality of the measurements space, because of such inherent sparsity [58] that the average number of required comparisons is far below the theoretical upper bound $nh_{\max}$. This fact makes octree evaluation time efficient and easy to be digitally implemented as the algorithm listed in Figure 3.6 clearly states and the forthcoming test application case studies confirm.

### Computational Efficiency and Implementation

It is worth to mention a few words on some octree computational aspects. Octree encoding can be carried out efficiently using recursion. The recurrent function is the tessellation process itself which receives the current hypercube information as well as the data inside such hypercube. The function tests for data class uniqueness within the hypercube. If equal class data points are found, the current node is updated accordingly and the tessellation process finishes on this branch. On the contrary, if more than one class data points are found, the recurrent function is called for the $2^n$ newly generated children. Such implementation is memory efficient and can be easily implemented in a programmable device as an embedded system (i.e. microcontroller or FPGA). It is worth to note that stack overflow is unlikely to happen during the tessellation process since, at each level, the resolution increases exponentially what implies that, with only a few levels, the achieved resolution is far beyond the actual resolution offered by any high quality measurement instrument.

Octree evaluation is also a very efficient procedure due to the way the octree data structure is stored in memory. Again, the inherently recurrent data structure provides a number of benefits when it comes to evaluate a new circuit candidate in the computed octree. The information of each node (coordinates, level,...) is stored in memory together with pointers to node's children and parent node [66]. Such indirect addressing scheme is very common in storing binary trees in a linear fashion memory organization. The evaluation of a freshly fabricated circuit in the trained octree is achieved by simply comparing the actual data point coordinates with the ones of the center of the hypercube. This allows descending along the tree until a leaf node is achieved and therefore the test decision taken, as reviewed in previous section. Throughout the clustering procedure no expensive mathematical operations are involved beyond simple bit to bit comparisons and program flow indirection.

### Noise and Octree Depth

Under realistic conditions, any circuit measurements is subjected to certain level of uncertainty, mainly due to the noise present in the measurements. Assume a voltage range $V_{\text{range}}$ and a maximum uncertainty level in the measure of $V_{\text{noise}}$, what gives the dynamic range of the measurement, $\text{DNR} = V_{\text{range}}/V_{\text{noise}}$. Since each octree level halves the range, it is clear that the resolution is $V_{\text{range}}/2^{h_{\max}}$, being $h_{\max}$ the maximum octree height. Given the previous definitions, it is clear that the maximum required octree depth is $h_{\max} = \lceil \log_2 \text{DNR} \rceil$.

```
typedef struct Node{
  struct Node *child[NCHILD];
  struct Node *parent;
  int index;
  int level;
  int data;
}Node;
```

**Figure 3.7:** Example of octree node data structure defined in ANSI C. As can be observed, each node has information of its parent and its $2^n$ children, as well as level, child index, and the cluster which is mapped to.

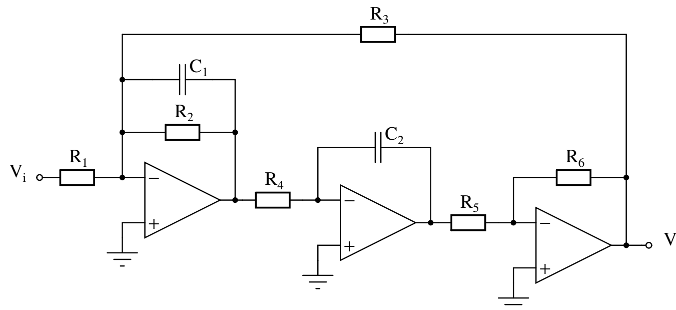


**Figure 3.8:** Band-pass state variable filter schematic. Filter components have been assumed to vary according to a normal distribution.

If octree computation is stopped at level $h_{\max}$, even when circuit data is available to continue tessellating the space beyond level $h_{\max}$, the impact of noise can be quantified as the ratio of the decision pending cells hypervolume and the root node hypervolume. Of course, test escapes and test yield loss will also reflect the noise impact. In the subsequently presented case study the impact of noise in the testing efficiency is also explored.

## 3.2 Test Application: Band-Pass Biquad Filter

In order to illustrate the usage of octrees both for encoding the test acceptance regions and using the resulting tree data structure for production testing, the method has been applied to test a band-pass Biquad filter under realistic variability conditions. The schematic of the filter is shown in Figure 3.8.

### 3.2.1 Filter Design and Test Specifications

The circuit depicted in Figure 3.8 is a second order system composed of three operational amplifiers and several passive components. Circuit specifications, as well as

**Table 3.1:** Band-pass Biquad filter test limits.

| Specification | Nominal | Lower Limit | Upper Limit |
|---|---|---|---|
| Natural frequency, $f_0$ | 1.00 MHz | 0.98 MHz | 1.02 MHz |
| Quality factor, $Q$ | 1.67 | 1.63 | 1.70 |
| DC gain, $G$ | 2.00 V/V | 1.94 V/V | 2.06 V/V |

test limits, are shown in Table 3.1. The measure space used in this work corresponds to those metrics defined in [67], which are based on the Lissajous composition of input/output signals when a multi tone excitation is applied to the filter [68, 69]. These input/output compositions turn to be quite sensitive to parametric defects, as Figure 3.9 depicts, and determine the analog signature of the circuit.

### 3.2.2 Alternate Measurements Space

In this case study, the alterante set of indirect measurements are going to be extracted from signal composition via Lissajous curves. Such compositions are a suitable option to be considered due to their sensitivity to catastrophic and parametric defects [68, 70]. Lissajous curves are obtained by composing two periodic signals, $x(t)$ and $y(t)$, usually the input excitation and the output response of the CUT, as Figure 3.10 sketches.

Lissajous curves can be considered as an analog signature of the system allowing to identify and quantify a large spectrum of defects and deviations. As an example of previous successful application to mixed-signal circuits, consider the test of an analog filter. Figure 3.11 depicts the obtained Lissajous traces for a defective and non defective circuit when it is excited with a multitone signal. As can be observed, the differences between both signatures are clear.

Lissajous compositions have been used for testing and diagnosing mixed-signal circuits with successful results. Brosa et al. used Lissajous compositions together with zone detection procedures to create a built-in self-test solution for mixed-signal circuits [70]. Balado et al. explored the possibilities of using three dimensional Lissajous curves and zone crossing counters to perform a test decision on analog circuits via regression techniques [68]. Some other works used the Lissajous based testing method to diagnose capacitors values in a continuous-time filter [71] while the combination of Lissajous compositions and digital signatures allows the test of a low-pass filter in the works found in [69]. In this chapter, Lissajous traces are used to characterize and test analog filters affected by parametric defects [72].

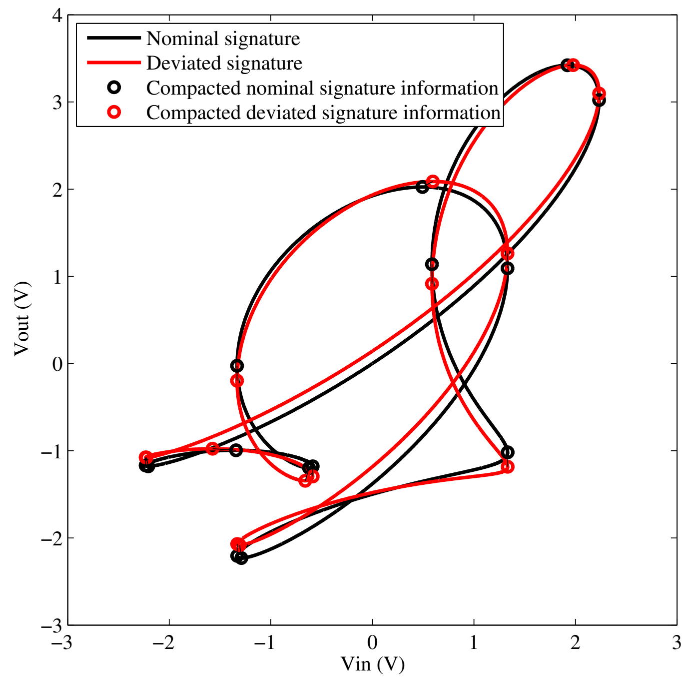


**Figure 3.9:** Filter's analog signature generated by composing input/output signals when excited with a multitone input. Trace information is compacted to the extrema values of the analog signal for further processing.

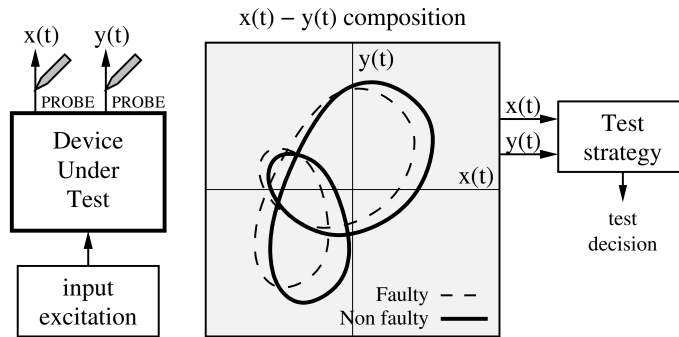


**Figure 3.10:** Diagram showing how Lissajous compositions are obtained by composing two periodic signals. Trace information allows the diagnosis procedure due to their sensitivity to parametric defects.

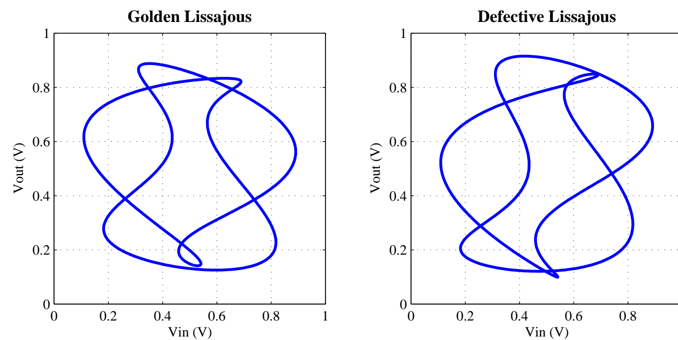


**Figure 3.11:** Example of Lissajous compositions as analog signatures. The trace on the left corresponds to a fault-free analog filter while the trace on the right corresponds to a filter out of specifications.

### 3.2.3 Statistical Training Phase

The method previously described has been applied to test a band-pass Biquad filter. As a proof of concept, only variations in the passive components have been considered, albeit it can be naturally extended to take into account the whole variability offered by the design kit or rely on experimental measurements coming from high volume production. In further examples, the variability included in the process design kit (PDK) is used to evaluate the octree encoding methodology.

Filter's gain has been considered to be constant therefore only two functional specifications are varying simultaneously, namely, the natural frequency and the quality factor. This decision has been take for the sake of allowing an easy interpretation and visualization of the data. Monte Carlo simulations have been carried out considering independent Gaussian distributions in the components space despite the method allows to include any known joint parametric distribution for circuit parameters. The

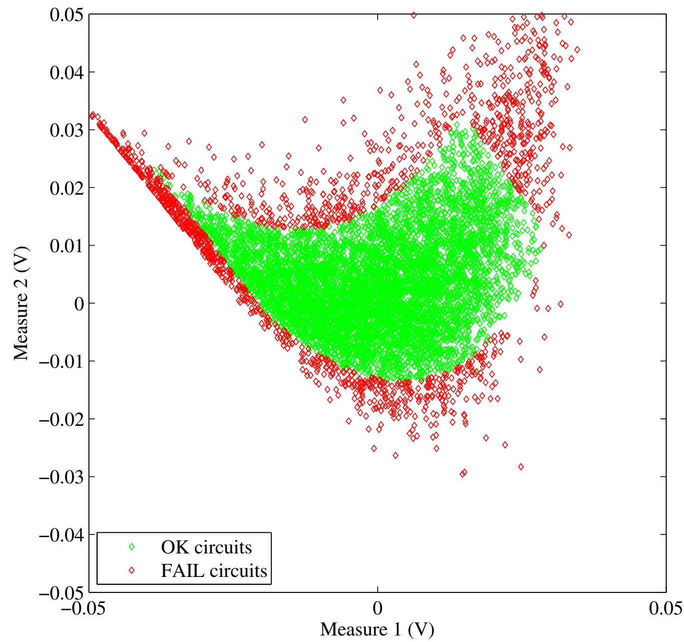


**Figure 3.12:** Band-pass Biquad filter samples in the measure space. The circuits have been generated using Gaussian Monte Carlo simulations and colored according to the test limits defined in Table 3.1.

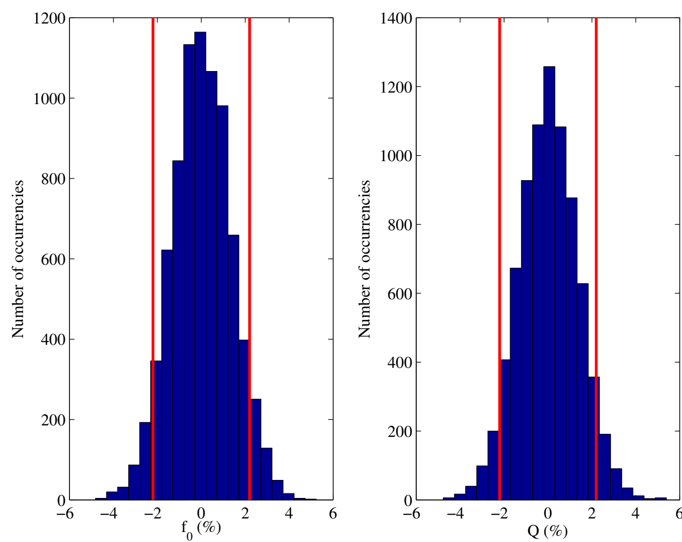


**Figure 3.13:** Histograms of the Monte Carlo samples showing the distribution of filter's natural frequency and quality factor. Test limits are represented by red vertical lines.

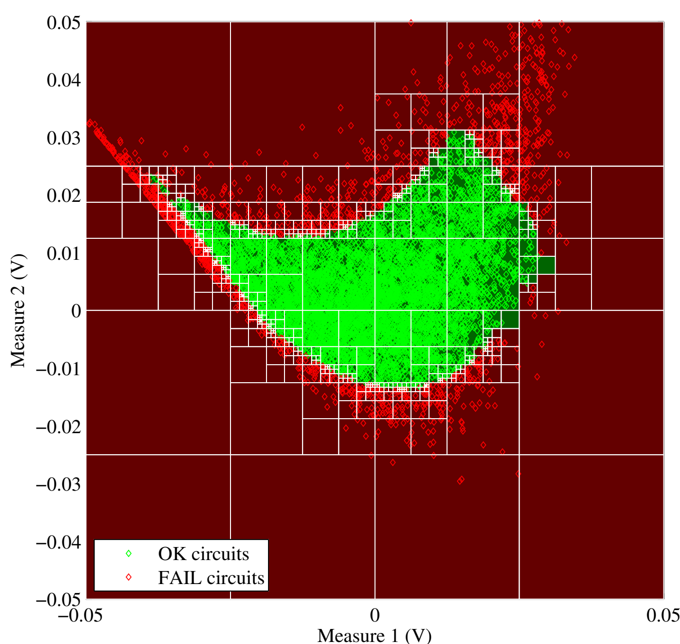


**Figure 3.14:** Resulting octree after the application of the training phase to the set of Biquad circuit samples shown in Figure 3.12. As can be observed, high octree levels concentrate in the test decision boundary.

assumed $3\sigma$ spread is 2% and 5% of the nominal value for resistors and capacitors, respectively. The effects of component variability over the functional specifications can be observed in Figure 3.13. Figure 3.14 shows the resulting 10 levels octree encoding of the acceptance/rejection regions colored in Figure 3.12.

Figure 3.15 shows the resulting levels distribution for the octree depicted in Figure 3.14. As can be appreciated, the vast majority of nodes correspond to levels 6, 7 and 8 despite the maximum node level is 10. Further details will be given in the forthcoming sections, but this fact implies a considerable advantage in terms of test application time.

### 3.2.4 Simulation Results

#### Testing Using Octrees

In order to evaluate the proposed testing procedure using octrees, a set of $50 \times 10^3$ Biquad filters have been generated using Monte Carlo simulations and evaluated using octrees. The results of the evaluation can be observed in Figure 3.16. Correctly classified circuits are drawn using green and red colors, which respectively correspond to pass and fail circuits. Circuits that have not been correctly clustered are circled

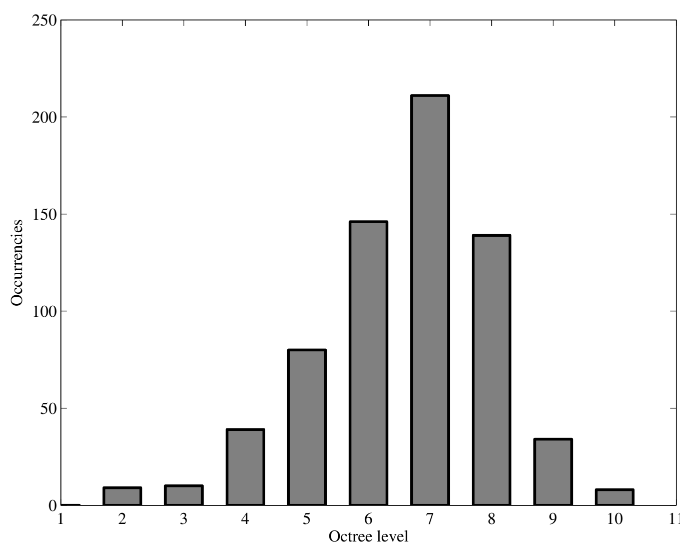


**Figure 3.15:** Levels distribution for the octree shown in Figure 3.14. Despite the maximum octree level is 10, the vast majority of octree cells correspond to levels 6, 7 and 8, what greatly facilitates its evaluation in the testing phase.

using dark green for pass circuits classified as fail and dark red for fail circuits classified as pass. Table 3.2 shows the *test escapes* and *yield loss* circuits as a function of the number of Monte Carlo samples used in the training phase. As expected, since the resolution is improved, the method improves as the number of samples increases.

In order to study the time efficiency of evaluating the octree, all the required comparisons have been stored for the generated set of $50 \times 10^3$ circuits. Figure 3.17 shows the percentage of test circuits as a function of the required number of comparisons of certain level. As can be observed, more than 95% of the circuits are clustered performing only 6 comparisons despite the octree has 10 levels. This implies a consid-

**Table 3.2:** Analog test metrics as a function of the number of Monte Carlo samples used in the training phase.

| $N_{\mathrm{ckts}}$ | Escapes (%) | Yield Loss (%) |
|---|---|---|
| $1 \times 10^3$ | 1.04 | 2.48 |
| $2 \times 10^3$ | 0.92 | 1.58 |
| $5 \times 10^3$ | 0.79 | 0.82 |
| $10 \times 10^3$ | 0.46 | 0.65 |
| $20 \times 10^3$ | 0.36 | 0.44 |
| $50 \times 10^3$ | 0.23 | 0.25 |

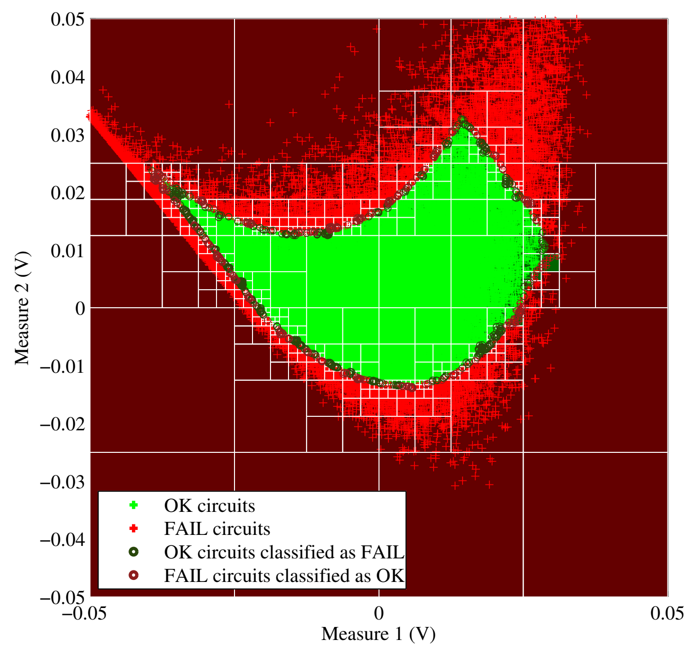


**Figure 3.16:** Testing phase results for the set of $50 \times 10^3$ Monte Carlo circuit samples using the octree presented in Figure 3.14 and generated in the former training phase. Circled circuits are those that have been misclassified.

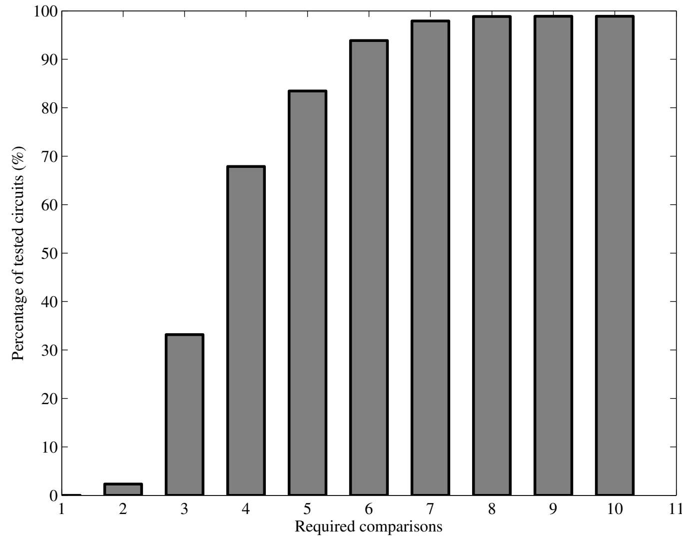


**Figure 3.17:** Cumulative required comparisons distribution for the testing phase according to the set of $50 \times 10^3$ Biquad filter samples. As can be observed, about 95% of the circuits are clustered performing only 6 comparisons.

erable benefit in terms of test application time since the octree data structure adapts its shape to the irregular boundaries in the measure space, only where a refinement is needed.

#### Noise Impact Evaluation

It has been already mentioned that there are two main sources for the existence of misclassification, namely, finite octree resolution and noise. The former issue has already been studied and simulation results have been reported. It basically depends on the required resolution which is also related with the number of samples used in the training phase. The latter issue, noise, is also of crucial importance thus resolution strictly depends on the DNR in a real world application. When noise is added, similar results to those presented in Figure 3.16 are obtained.

Figure 3.18 shows the *test escapes* and *yield loss* analog metrics for several scenarios. Results depend on the standard deviation of Gaussian noise added to the measures for several initial sample sizes used in the training phase. As can be observed, misclassifications increase with the noise level. Also, sample size is not a crucial parameter in the presence of noise since no higher resolution can be obtained beyond the noise level.

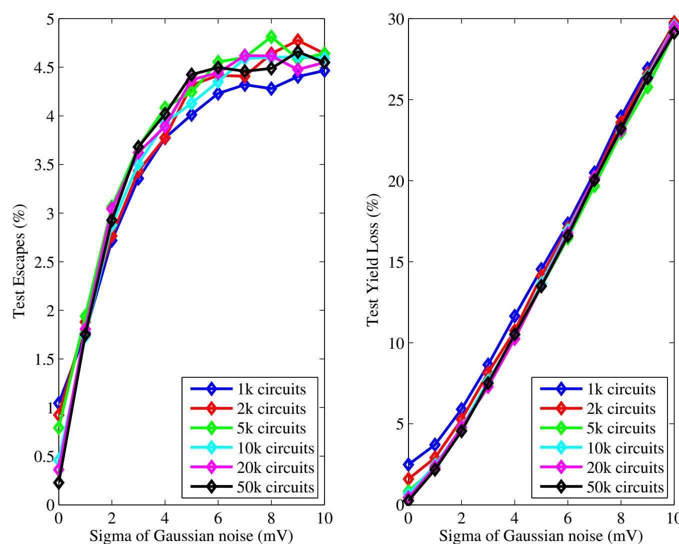


**Figure 3.18:** Analog test metrics (*test escapes* and *test yield loss*) as a function of the standard deviation of the noise distribution added to the measures and the number of initial Monte Carlo samples used in the training phase.

## 3.3 Test Application: Low-Pass Biquad Filter with Boundary Densification

The previously presented case study was devoted to test a band-pass Biquad filter. It is clear that the number of circuit samples lying in the surroundings of the test decision boundary is a crucial aspect to allow the octree tessellation procedure to increase the resolution near the pass/fail boundary. Because of that reason, a densification strategy based on statistical blockade technique [73, 74] in order to obtain more circuit samples near the test decision region has been developed. In this section, the octree encoding methodology, aided with the boundary densification strategy, is applied to a Tow-Thomas Biquad filter.

### 3.3.1 Statistical Training Phase with Boundary Densification

#### Boundary Densification Algorithm

The classical methods for accurately defining the test decision boundary for analog and mixed-signal circuits present the drawback of simulating large amounts of circuits in order to get a representative sample of the statistical distribution tails where the test limits are encountered. For that reason, some accelerating methods have been proposed in the literature during the last years. Among them, statistical blockade [73] blocks the simulation of those circuits not significantly contributing to the

characterization of distribution tails.

In this case study, a strategy based on the well known statistical blockade technique is used. Figure 3.19 describes the algorithm which allows the densification of the test decision boundary based on an initial data set of $N_0$ Monte Carlo simulations. Then, the circuits are simulated and their functional specifications are obtained identifying the circuits lying near the boundary and used as a reference for selecting $N_{\text{extra}}$ circuits from a new and much larger $N_1$ samples data set. The whole algorithm allows to get an extra densification of samples near the test decision boundary.

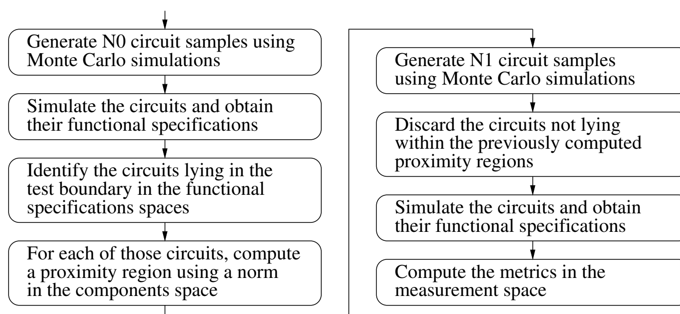


**Figure 3.19:** Densification algorithm to increase the number of circuits near the test boundary. It is based on the statistical blockade technique [73] which allows to get rid of samples not lying in the distribution tails.

Figure 3.20 corresponds to a 2000 Monte Carlo circuit metrics samples of a Biquad low-pass filter. Green points encode circuits within specifications and red points encode circuits out of specifications. Clearly, there exist a test decision boundary in the metrics space which is blurred due to the lack of sample density in the surroundings of the acceptance region boundary. Black points in the data correspond to the set of identified circuits lying near the test boundary.

In order to obtain a boundary with better precision more samples are required. Figure 3.21 corresponds to the same data sample shown in Figure 3.20 but having applied the described densification algorithm. Here, a new Monte Carlo data set consisting on $N_1 = 2 \times 10^6$ samples has been generated. From this set, the neighboring data lying in the surroundings of the previously identified black points are extracted and the rest are discarded. For the presented case example that implies an extra densification of $N_{\text{extra}} = 11195$ samples giving a total of 13195 circuits. As can be seen, the improvement is quite large thus the algorithm gets rid of lots of circuits in the center of the distribution.

Then, using the achieved extra densification, the acceptance region has to be encoded in order to perform the test and be able to cluster a circuit as functional or non functional. Such encoding is performed using octrees which will be subsequently described. Then, the production testing phase can be applied.

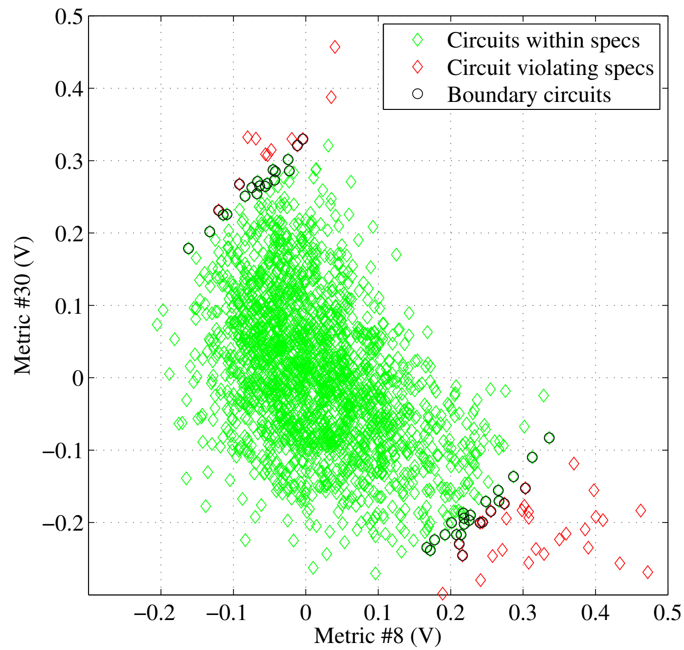


**Figure 3.20:** Monte Carlo simulations of the Biquad filter depicted in Figure 3.23 showing the spread of the chosen metrics when $N_0 = 2000$ simulations are performed. Black points correspond to the circuits lying in the test decision boundary identified in the functional specifications space.

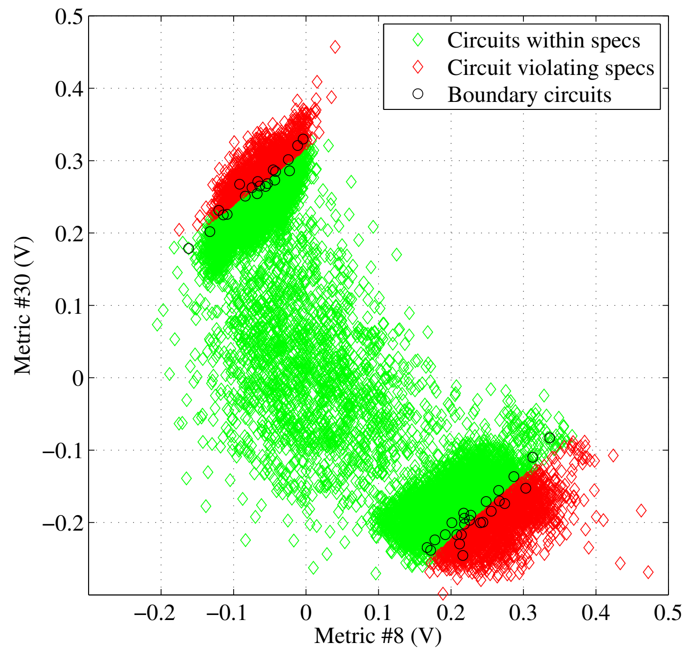


**Figure 3.21:** Monte Carlo simulations of the Biquad filter after the application of the densification procedure described in Figure 3.19. The procedure starts with $N_0 = 2000$ samples and is capable of generating $N_{\text{extra}} = 11195$ extra samples near the test boundary.

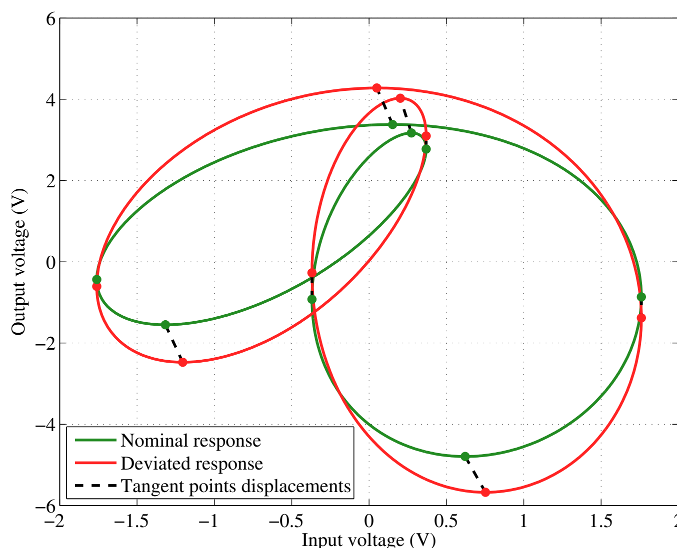


**Figure 3.22:** Lissajous compositions of the nominal and deviated responses when a multitone signal is applied to a low-pass filter. The metrics correspond to the set of displacements $(\Delta x_i, \Delta y_i)$ of the horizontal and vertical tangent points of the shifted trace with respect to the nominal curve.

### Alternate Measurements Space

As mentioned earlier, Lissajous compositions can be considered as an analog signature due to their sensitivity to parametric defects. Figure 3.22 shows the output of the Biquad filter when it is excited using a multitone input. The difference between faulty and non faulty traces can be easily appreciated at a glance [68–70].

In order to quantify the amount of deviation, a discrepancy metric has been defined. Considering a reference and a deviated Lissajous traces, the metric is defined as the set of $(\Delta x_i, \Delta y_i)$ displacements of the shifted curve with respect to the reference one. The points taken in consideration are the tangency points of vertical and horizontal tangent lines to the Lissajous composition as Figure 3.22 depicts. The selection of these points allows an easy and systematic approach facilitating further data processing. A subset of these set of features conform the alternate measurements to be used in the testing procedure.

### Filter Design and Test Specifications

The method described in the previous sections has been applied to test the low-pass Biquad filter depicted in Figure 3.23. The circuit is a second order system composed of three operational amplifiers, six resistors and two capacitors. Current work only considers parametric variations in resistors and capacitors albeit the study can be

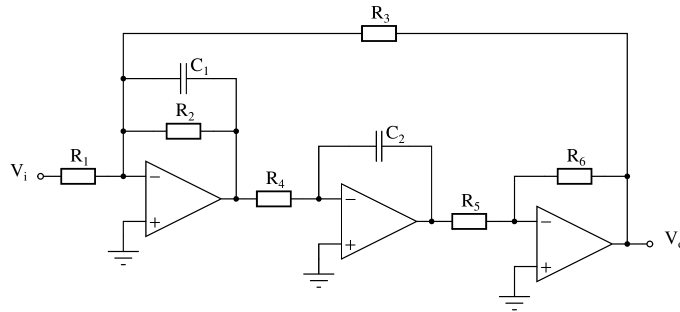


**Figure 3.23:** Low-pass state variable filter schematic. Filter components have been assumed to vary according to a normal distribution. For the Monte Carlo distributions generation, different standard deviations have been considered for resistors and capacitors.

**Table 3.3:** Biquad filter functional specifications.

| Specification | Nominal | Lower Limit | Upper Limit |
|---|---|---|---|
| DC gain, $G$ | −1.20 V/V | −1.26 V/V | −1.14 V/V |
| Natural frequency, $f_0$ | 18.800 kHz | 18.236 kHz | 19.364 kHz |
| Quality factor, $Q$ | 3.00 | 2.70 | 3.30 |

naturally extended to take into account the whole variability offered by the design kit.

Functional parameters for the filter can be easily derived in terms of component values. The DC voltage gain turns to be $G = -\frac{R_3}{R_1}$, the natural frequency $f_0 = \frac{1}{2\pi}\sqrt{\frac{R_6}{R_3R_4R_5C_1C_2}}$ and the quality factor $Q = R_2\sqrt{\frac{R_6C_1}{R_3R_4R_5C_2}}$. In order to allow an easy interpretation and visualization of the data, the DC gain has been considered to be constant and therefore only 2 functional parameters are considered. This fact allows performing the test with only two measures. Such measures have selected to be the most sensitive and less cross-correlated set of $(\Delta x_i, \Delta y_i)$ metrics.

The set of functional specifications for the low-pass filter is shown in Table 3.3. First column lists the name of the spec, second shows its nominal value and the latter ones establish the adopted test decision interval. Test limits correspond to a ±5%, ±3% and ±10% of the nominal value for the three listed parameters respectively.

### Statistical Training Phase

Monte Carlo simulations have been carried out considering independent Gaussian distributions in the components space despite the method allows to include any known joint parametric distribution of the CUT parameters. The $3\sigma$ spread for resistors has

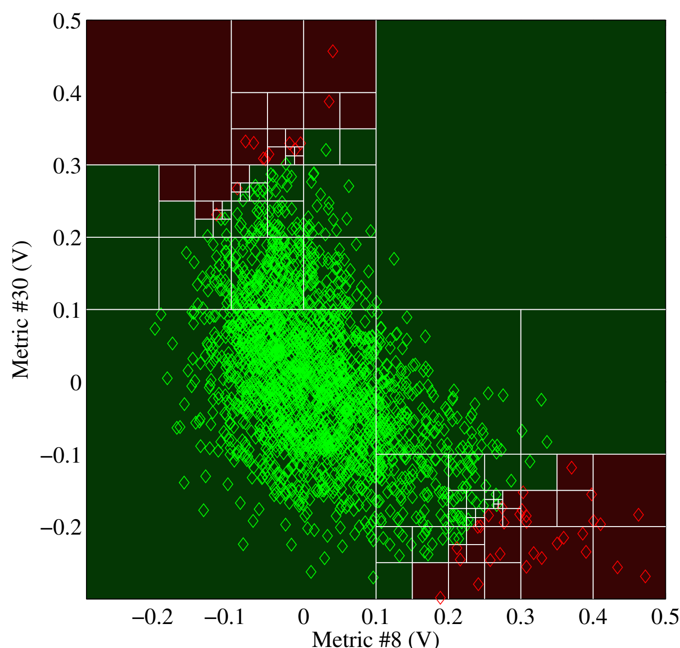


**Figure 3.24:** Quadtree encoding of the acceptance region using the initial data sample depicted in Figure 3.20. The maximum depth level is 7. Due to the sparse representation of the octree data structure its computation is completed in a fraction of a second.

been established to 2% of their nominal value while a 5% $3\sigma$ spread has been chosen for capacitors. Using an initial sample of $N_0 = 2000$ circuits, the octree depicted in Figure 3.24 is obtained. Depending on the underlying data distribution, some octree cells may not contain any data sample and therefore further partitioning does not provide any benefit. Such cases are treated differently using a neighboring criteria to properly cluster the cell.

According to the densification algorithm listed in Figure 3.19, a second and larger data set of $N_1 = 2 \times 10^6$ samples has been generated. From these 2 million samples, only $N_{\text{extra}} = 11195$ circuits are identified to be in the test decision boundary and then added to the early 2000 samples. Thus, a total sum of 13195 samples including test boundary densification are available to generate a denser octree. Figure 3.25 shows the outcome of the octree generation algorithm over such set. As can be appreciated, the density of the latter octree is much higher than the one shown in Figure 3.24. Combining this fact and the benefits regarding computational time of octree data structure evaluation, it guarantees a better test performance as the next section highlights.

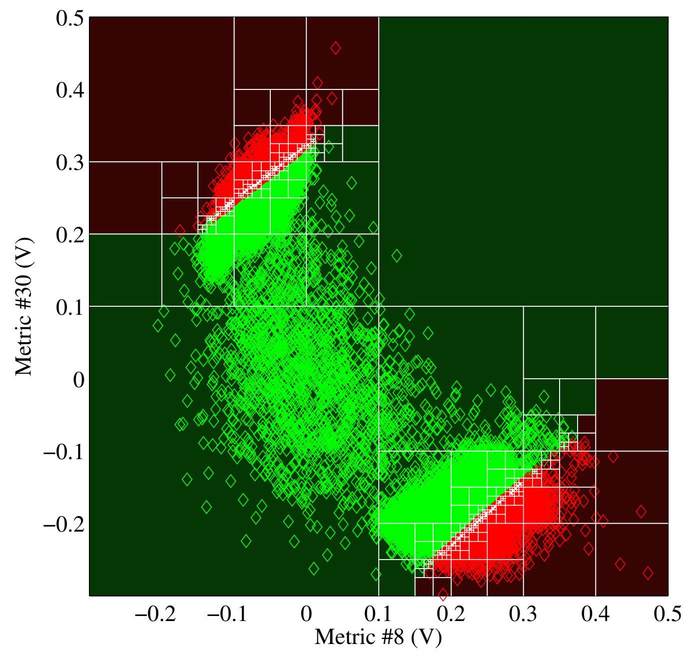


**Figure 3.25:** Quadtree encoding of the boundary densification shown in Figure 3.21. The $N_1$ samples value was 2 million resulting in an extra densification of 11195 samples. The maximum quadtree level is 11, achieved in the test decision boundary.

**Table 3.4:** Biquad filter testing simulation results.

| | $N_1/N_0 = 100$ | | | $N_1/N_0 = 500$ | | |
|---|---|---|---|---|---|---|
| $N_0$ | TYL ppm | TE ppm | Level | TYL ppm | TE ppm | Level |
| **100** | 6380 | 4944 | 4 | 2828 | 6360 | 4 |
| **200** | 1996 | 5848 | 5 | 1744 | 4484 | 7 |
| **500** | 2248 | 3928 | 6 | 1872 | 2816 | 9 |
| **1000** | 1652 | 2952 | 7 | 1172 | 1808 | 10 |
| **2000** | 600 | 1520 | 10 | 400 | 908 | 11 |
| **5000** | 368 | 896 | 13 | 236 | 736 | 13 |
| **10000** | 252 | 844 | 13 | 144 | 680 | 15 |
| **20000** | 108 | 736 | 13 | 72 | 648 | 16 |
| **50000** | 68 | 636 | 15 | 20 | 620 | 16 |
| **100000** | 40 | 620 | 16 | n/a | n/a | n/a |

### 3.3.2 Simulation Results

In order to validate the proposal, several simulations have been performed considering different conditions as the size $N_0$ of the initial data samples and the size $N_1$ of the densification set. Of course, these parameters play a crucial role in the performance of the presented testing technique thus, depending on such sizes, the resulting octrees will encode the test acceptance region with different precision.

Two different cases have been considered, namely: (i) fixing the $N_1/N_0$ ratio to 100 and (ii) fixing the $N_1/N_0$ ratio to 500. For each of these scenarios, different $N_0$ samples has been generated: 100, 200, 500, 1000, 2000, 5000, 10000, 20000 and 50000. Boundary $N_{\text{extra}}$ samples, test yield loss, test escapes, mean computational time and octree depth and its distribution are the studied parameters via Monte Carlo simulations. For this purpose, a test data set of 250000 circuits has been considered and evaluated using the presented testing technique based on the octree encoding of the acceptance region in the measure space.

Figures 3.26 and 3.27 show the results of the statistical distribution of the octree depth for $N_1/N_0 = 100$ and $N_1/N_0 = 500$ respectively. Each of them show the distribution for the cases $N_0 = 1000$ and $N_0 = 10000$. It is worth to note the crucial importance of the initial data sample size as the bar plots of Figure 3.26 reveal. Starting from $N_0$ of 1000 circuits, a coarse octree mesh is obtained presenting only 7 levels in depth. On the contrary, when the initial sample size is enlarged to 10000 the resulting octree is 13 levels depth. This is so because in the first approach, the number of identified samples lying near the test boundary is small and therefore no considerable benefit is obtained in the second pass.

Similar conclusions are derived from the distributions shown in Figure 3.27. In this case, the initial data set is also 1000 in size but the large amount of extra samples in the densification stage allows to achieve much better results than its $N_1/N_0 = 100$

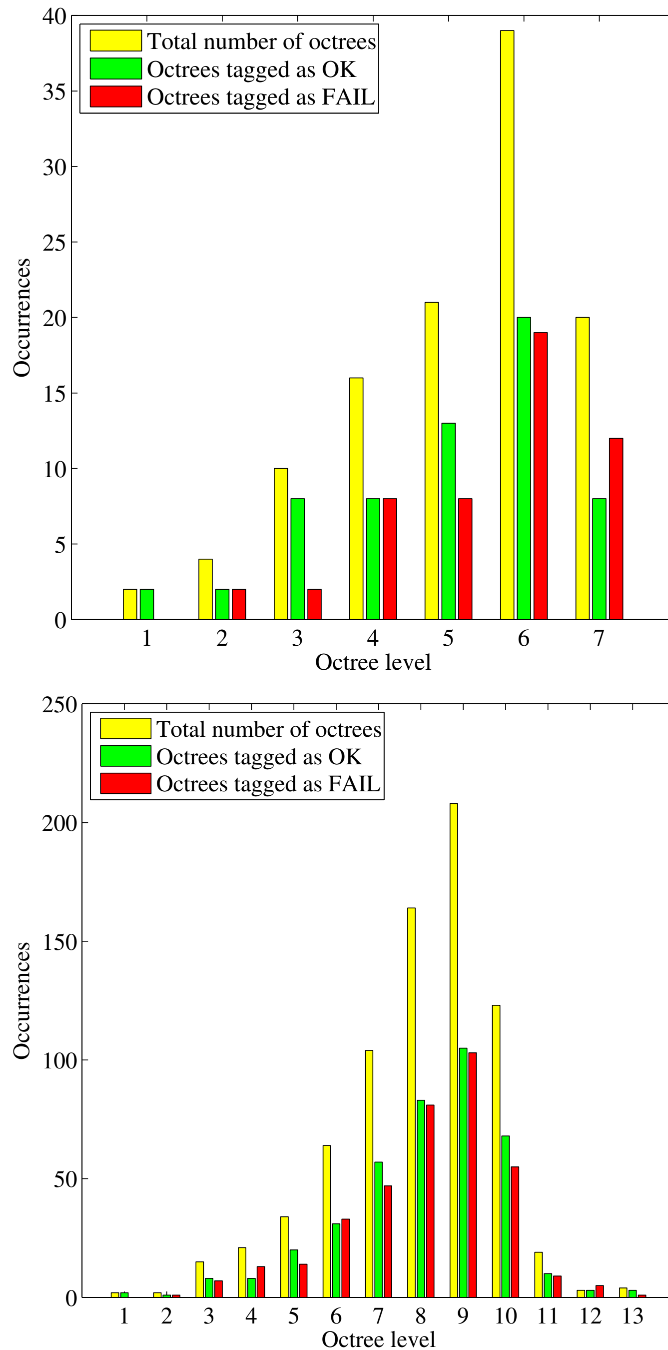


**Figure 3.26:** Bar plots showing the distribution of the octree levels with different initial sample sizes. The plot on the left uses an initial sample size of 1000 circuits while 10000 circuits are used on the right. The $N_1/N_0$ ratio has been fixed to 100.

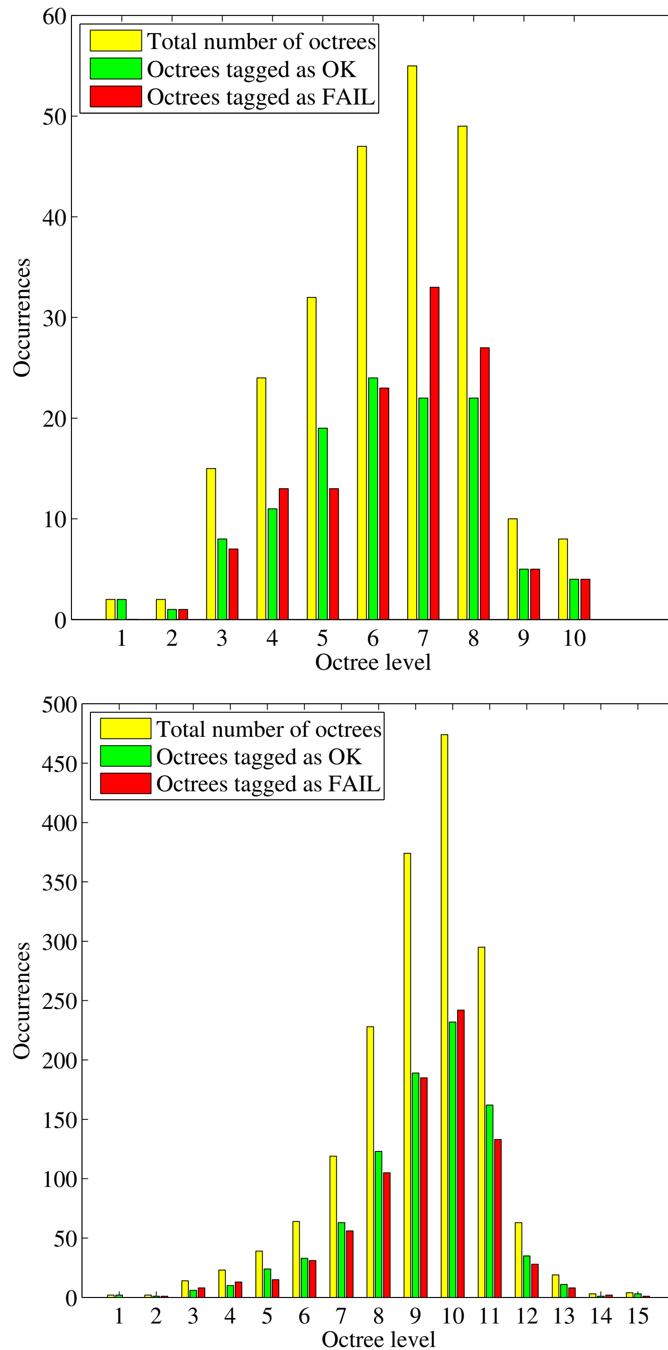


**Figure 3.27:** Bar plots showing the distribution of the octree levels with different initial sample sizes. The plot on the left uses an initial sample size of 1000 circuits while 10000 circuits are used on the right. The $N_1/N_0$ ratio has been fixed to 500.

counterpart. For $N_0 = 1000$, 10 levels are obtained while 15 levels are achieved in the $N_0 = 10000$ case.

All the bar plots depicted in Figures 3.26 and 3.27 present an equitable number of occurrences of OK and FAIL octree cells. This behavior is reasonable thus in each iteration of the octree generation algorithm, the cell is tessellated if it contains samples from different clusters. The octree cell size reduces as it approaches the test boundary, then achieves a peak which correspond to the mean density of the samples and then the number of finer cells rapidly reduces because they only encode abnormally dense regions.

Simulations results reveal test yield loss and test escapes keep a decreasing tendency as the number of initial data samples increase. Such observation states in both studied scenarios as can be observed in Figure 3.28. It is important to note that no significant difference is appreciated when the ratio $N_1/N_0$ raises from 100 to 500 what leads to remark the number of initial circuits is a crucial parameter thus strongly determines the number of samples generated in the next pass.

Table 3.4 lists the numerical values resulting from the performed simulations, namely, test yield loss, test escapes, $N_{\text{extra}}$ samples and maximum octree level as a function of the $N_0$ samples and for both commented scenarios. In both situations and for all the studied $N_0$ values, test escapes line remains over the test yield loss line. The lowest values are obtained when an initial data set of 50000 circuits is considered and a 500 times larger $N_1$ data set is generated. These values are 40 ppm for test yield loss and 620 ppm for test escapes.

The number of extra samples generated by the densification algorithm listed in Figure 3.19 and maximum octree levels results are also reported in Table 3.4. The $N_{\text{extra}}$ samples increase exponentially as the linear plot suggests in Figure 3.28. The maximum octree depth seems to increase logarithmically as well as the mean computational time for the evaluation of one circuit.

The case study presented in this section is using just two clusters, corresponding to the classical pass/fail bins in mixed-signal testing. This concept can be generalized to an arbitrary number of bins, therefore yielding to the quality binning procedure presented in the forthcoming chapter. As will be seen, octree tessellation can be also used to encode more then two clusters within the alternate measurements space.

## 3.4 Binning of Mixed-Signal Circuits Using Digitally Encoded Signatures

Binning after volume production is a widely accepted technique to classify fabricated ICs into different clusters depending on different degrees of specification compliance. This allows the manufacturer to sell non optimal devices at lower rates, so adapting to customer's quality-price requirements. The binning procedure can be carried out by measuring every single circuit performances, but this approach is costly and time

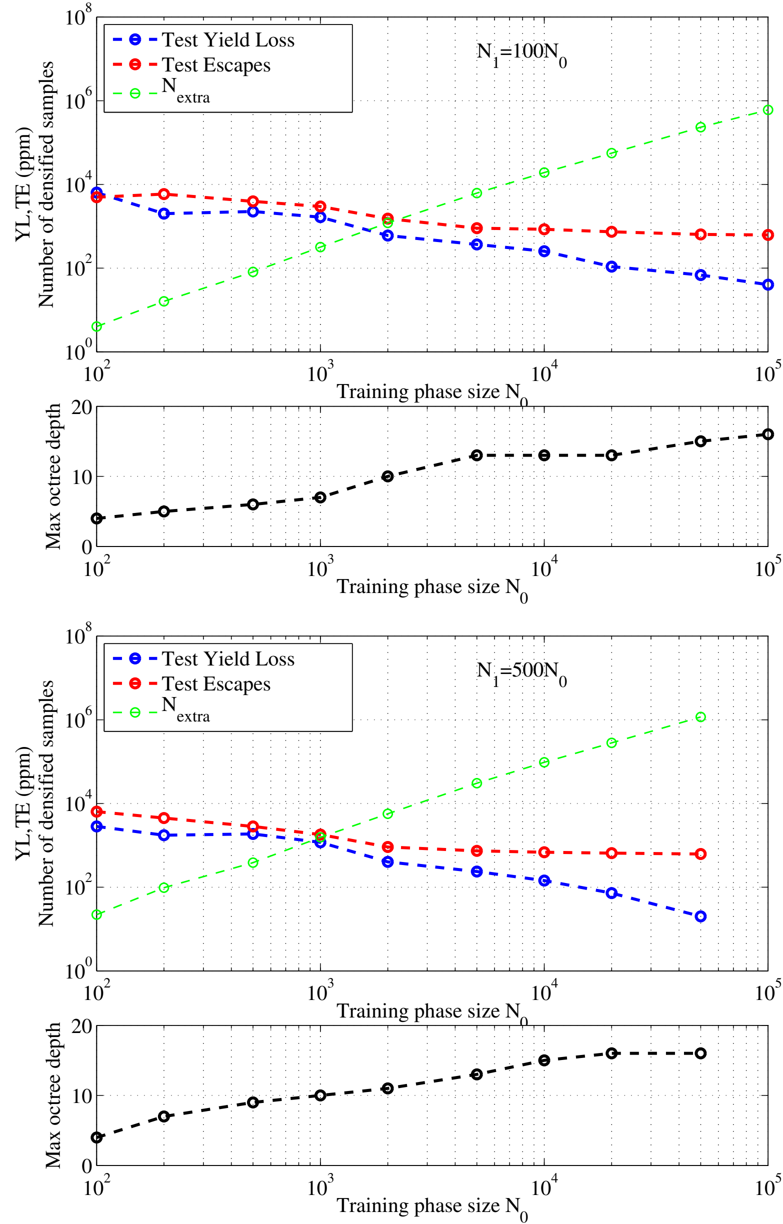


**Figure 3.28:** Test yield loss, test escapes, $N_{\mathrm{extra}}$ samples and maximum octree depth as a function of the training phase length $N_0$. The $N_1/N_0$ ratio has been fixed to 100 for the plot on the left and 500 for the plot on the right. The analog test metrics have been tested using 250000 candidate circuits.

consuming. On the contrary, if alternate measurements are used to characterize the bins, the procedure is considerably enhanced. In such a case, the specification bin boundaries become arbitrary shape regions due to the highly non linear mappings between the specifications space and the alternate measurements space. The alternate binning strategy proposed in this chapter functions with the same efficiency regardless of these shapes. The digital encoding of the bins in the alternate measurements space using octrees is the key idea of the chapter. The proposed strategy has two phases, as mentioned before. The training phase and the binning phase. In the training phase, the specification bins are encoded using octrees. This first phase requires sufficient samples of each class to generate the octree under realistic variations, but it only needs to be performed once. The binning phase corresponds to the actual production binning of the fabricated ICs. This is achieved by evaluating the alternate measurements in the previously generated octree. The binning phase is fast due to the inherent sparsity of the octree data structure.

Similarly to test, the procedure of binning analog and mixed-signal circuits after volume production can be formalized as the classification of any candidate circuit into a cluster, according to certain circuit performances, among several possible disjoint bins. Such clustering is performed according to parameters of different nature.

The most common space for binning mixed-signal circuits is the *specifications space* in which circuit performances are directly measured and binned accordingly. Process variations may cause some circuits to violate or not fulfill the set of functional specifications related to certain bins. The effect of the uncertainties in the manufacturing process are modeled in this chapter by the statistical distributions offered by technology's process design kit in the *components space*. Direct measurement of circuit specifications is difficult and time consuming [1]. To overcome these drawbacks, the use of alternate measurements is widely adopted as an indirect and effective solution to test analog and mixed-signal ICs [56]. In this chapter, the term *measurements space* will be used to designate the alternate measurements which will facilitate the binning process. Figure 3.29 sketches these three spaces and the bin boundaries defined according to certain specification levels.

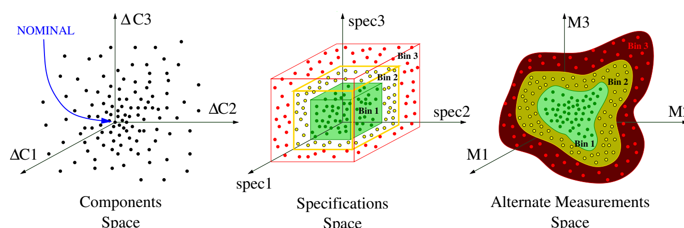


**Figure 3.29:** Sketch of the three spaces considered in this chapter. Components space variability induce deviations in the specifications space as well as in the alternate measurements space in which the binning process takes place.

The proposed production binning methodology is performed in two phases, namely, training and binning phases. First, the training phase encodes the specification bins in the measurements space using octrees relying on circuit samples obtained by sim-

ulation, model evaluation or actual production data. After the training phase, the production binning is achieved by evaluating the alternate measurements of a candidate circuit in the previously trained octree data structure.

### 3.4.1 Octree Encoding for Quality Binning

In this section, the previously presented octree encoding algorithm is generalized for an arbitrary number of quality bins. In this section, the octree data structure will be used to encode the specification bins in the alternate measurements space.

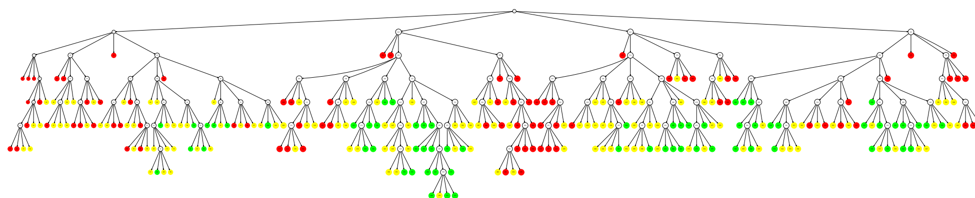

**Figure 3.30:** Graph representation of the quadtree depicted in Figure 3.31. The resulting tree is 8 levels deep and has 369 nodes.

As an example of data encoding using octrees, consider the set of two dimensional alternate measurements shown in Figure 3.31. The color of each pair of measurements indicate they belong to bin 1 (green), bin 2 (yellow) or bin 3 (red). Initially, and also during the whole process, the theoretical boundary separating both bins is unknown, so the presented algorithm is solely based on the alternate measurements. The encoding algorithm starts with the definition of a square cell (root node) including all the data to be considered in the training phase. Then, the square is tessellated in 4 equal regions by halving each dimension. Each of these 4 generated regions is further examined. If it exclusively contains single bin measurements, the square is tagged accordingly to that class and no further partitioning is needed. Otherwise, the square is marked as decision pending (white parent nodes in Figure 3.30) and the tessellation/labeling procedure continues until all the generated squares only contain equal class measurements.

Depending on the underlying statistical distributions of the available alternate measurements, octree cells containing no data may occur in deep levels. In this case, unknown octree cells are labeled accordingly to the bin assigned to the majority of their neighboring cells.

It is worth noting that the encoding procedure using octrees does not change as the number of bins increases. This is a major advantage over other state of the art methods which are only capable of separating two clusters at a time. The graph generation and encoding algorithm simply creates a new tag for every newly encountered bin.

In order to encode the bins in the measurements space, a considerable amount of representative data needs to be generated. This can be done entirely relying on simulations, circuit models or by using available data on the production run with

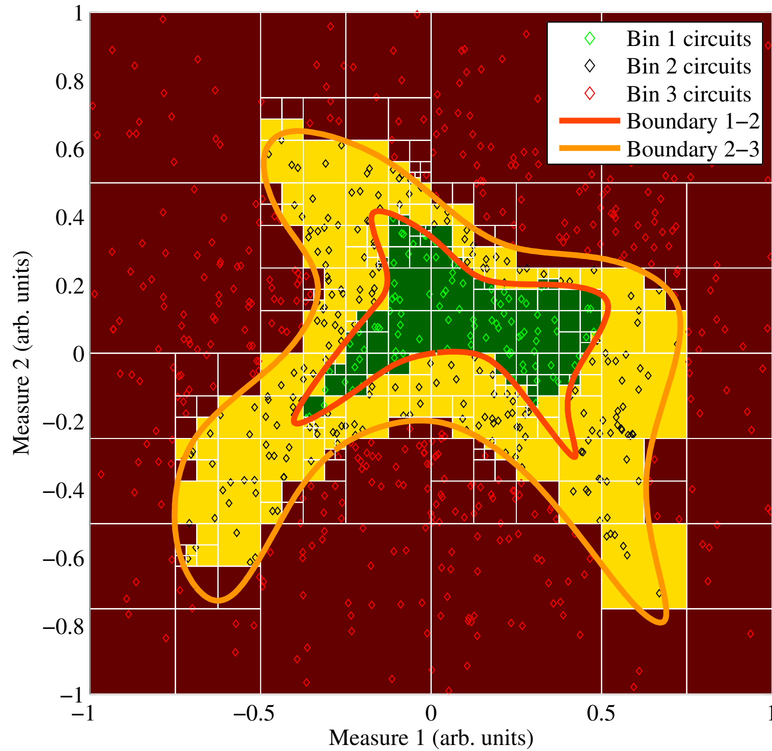


**Figure 3.31:** Example of a quadtree generated using 100 bivariate Gaussian samples and three bins. The actual boundary separating both bins is represented by the thick orange line. The resulting quadtree is 8 levels deep and has the graph representation depicted in Figure 3.30.

already binned ICs. Of course, accelerating techniques for obtaining representative bin border circuits can also be used, such us statistical blockade [74], stratified sampling [75], copula theory [12] or estimating the probability density function using kernels [76]. The defined bins in the specification space will map to arbitrary regions in the measurements space which will be used for binning the forthcoming circuits.

As an example of circuit data generation in the measurements space, $10^4$ Monte Carlo circuit samples of a 4th order band-pass Butterworth filter have been generated relying on HSPICE simulations. Figure 3.32 shows these circuits in the measurements space where green points encode circuits fulfilling the specifications (bin 1), yellow points indicate circuits presenting marginal specifications (bin 2) and red points indicate circuits not satisfying all the specifications (bin 3).

Once circuit data are generated, they need to be digitally encoded using an octree data structure. This data structure presents the advantage of being able to represent arbitrary $n$-dimensional regions and the capability of controlling its resolution by just limiting the maximum level depth. Such tree structures can be digitally represented

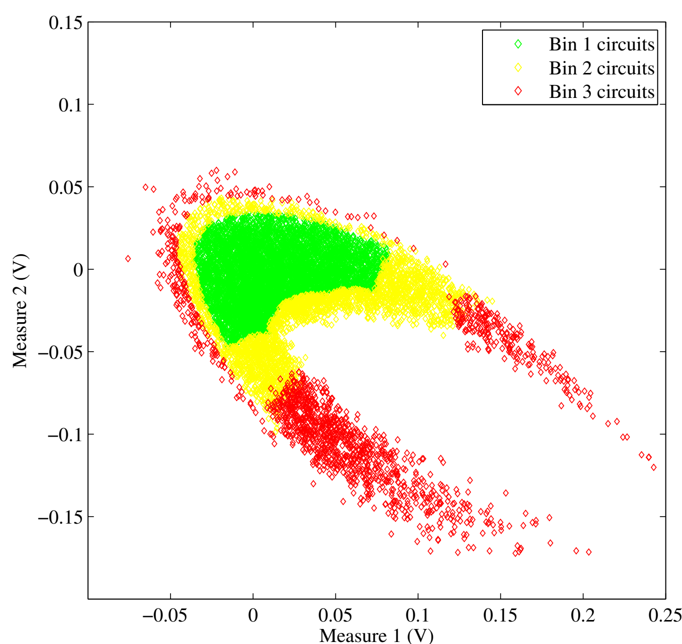


**Figure 3.32:** Monte Carlo samples of a 4th order band-pass Butterworth filter in the measurements space. The circuit has been designed and simulated using an industrial 65 nm CMOS technology.

and are easily evaluated using recursion. Next section describes how octrees can be created using circuit data samples.

### 3.4.2 Binning Using Octree Data Structures

As mentioned earlier, the binning phase corresponds to the actual production binning of the fabricated ICs using the octree data structure encoded in the former training phase. The binning procedure is time efficient due to the sparsity of the octree as will be shown later.

Consider a pair of alternate circuit measurements, $(M_1, M_2)$, corresponding to a fabricated circuit aiming to be binned using, for instance, the octree depicted in Figure 3.31. The binning procedure is performed using the graph of Figure 3.30. Assuming the pair of alternate measurements are within the initial square box (root node), the binning algorithm computes to which of the four quadrants the measurements belong to by performing one comparison per coordinate. This decision brings the candidate circuit to a new bound hence a new and deeper octree level is achieved. If the current node is labeled, the circuit is mapped to that bin and the evaluation finishes. If not, the evaluation algorithm repeats the comparison operation through the graph until a labeled node is found (tree leafs) and the circuit is binned. The

pseudocode of the binning algorithm using octrees is listed in Figure 3.6.

### 3.4.3 Efficiency Metrics: Bin Escapes

As pointed before, the binning phase consists on the evaluation of a candidate circuit in the octree generated in the training phase, $b = \mathcal{T}(M)$, according to previously introduced notations. Certain circuits may be incorrectly binned due to insufficient octree resolution or noise in the measurements. Similarly to test escapes and test yield loss, a new metric to measure the quality of the binning procedure needs to be defined. Here forth, these circuits will be referred as *bin escapes*. In order to quantify this metric, let $p$ denote the number of bins and let us define a $p \times p$ matrix $E = (e_{ij})$ referred from now on as the *bin escapes matrix*. Element $e_{ij}$ in *bin escapes matrix* indicates how many circuits certainly belonging to bin $i$ have been clustered into bin $j$. Then, the *global bin escapes* metric, denoted as GBE, can be naturally defined as the sum of all the misclassified circuits as follows,

$$\text{GBE} = \sum_{\substack{i,j=1 \\ i \neq j}}^{p} e_{ij} \tag{3.3}$$

Then, it is clear that the circuits accounted in the diagonal of the bin escapes matrix correspond to correctly binned circuits. On the contrary, circuits accounted above or below the diagonal of the bin escapes matrix are circuits that have been misclassified. Circuits above the diagonal are circuits classified in a worse performance bin than the actual circuits. On the contrary, elements located below the diagonal correspond to circuits classified in a bin being representative of better circuit performances than the actual circuit. Bin escapes matrix is being used in to evaluate the efficiency of the proposed binning procedure.

## 3.5 Binning Application: 4th Order Band-Pass Butterworth Filter

### 3.5.1 Filter Design and Bin Specifications

In order to illustrate the proposed binning methodology using octrees, it has been applied to bin a 4th order band-pass Butterworth filter in the alternate measurements space. The Butterworth filter has been designed and simulated in an industrial 65 nm N-well bulk CMOS technology from ST-Microelectronics [77] as illustrated in the schematic shown in Figure 3.33. The variability in the circuit has been provided by the process design kit offered by ST Microelectronics. The used topology corresponds to a multiple feedforward implementation [78] according to the design specifications shown in Table 3.5.

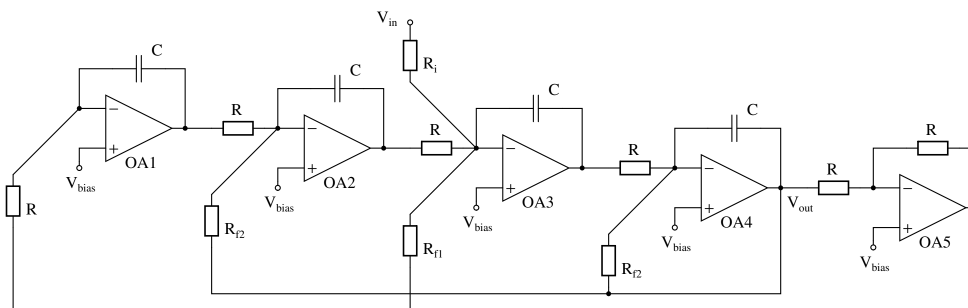


**Figure 3.33:** Schematic of the 4th order band-pass Butterworth filter used as case study. The chosen topology corresponds to a multiple feedforward implementation [78]. The filter has been designed and simulated using a low-power standard-Vt 65 nm CMOS technology from ST-Microelectronics. Passive elements correspond to fixed width high resistance polysilicon resistors (rhiporpo) and metal-insulator-metal capacitors (mim). Components values are $R = 10$ kΩ, $R_i = 4R$, $R_{f1} = 0.444R$, $R_{f2} = 1.414R$ and $C = 15.9$ pF. Power supply for this technology is 1.2 V.

The designed Butterworth filter has been tuned at 1 MHz with a 500 kHz bandwidth. Circuit components have been chosen to meet the aforementioned specifications and implemented using technology specific passive components as illustrated in Figure 3.33. Resistors have been implemented using fixed width high resistance polysilicon resistors and capacitors using metal-insulator-metal capacitors. The sheet resistance of the used polysilicon resistors is approximately, $R_s = 6$ kΩ/□, while the capacitance of the used metal-insulator-metal capacitors is about 5 fF/$\mu$m$^2$.

**Table 3.5:** Butterworth filter design specifications.

| Design Specification | Symbol | Value | Units |
|---|---|---|---|
| Filter order | $n$ | 4 | |
| Center frequency | $f_0$ | 1 | MHz |
| Bandwidth (−3 dB) | BW | 500 | kHz |
| Band-pass gain | $G$ | −3 | dB |

Even though the presented methodology can be naturally extended to an arbitrary number of bins, in this chapter only three bins have been considered as a proof of concept. Table 3.6 defines bin boundaries based on frequency/gain performances of every sample circuit. For instance, a circuit will be classified in bin 1 if and only if all the following conditions are satisfied: (1) the filter presents a gain less than −1.8 dB within the 262.8 kHz band-pass bandwidth, (2) it attenuates no more than −4.2 dB within the 262.8 kHz band-pass bandwidth and (3) it attenuates more than −49.0 dB at the stop-band corner frequencies (9.9 MHz bandwidth). Analogous reasoning applies for bins 2 and 3 according to the information shown in Table 3.6.

**Table 3.6:** Butterworth filter bin limits.

| Specification | Bins 1–2 | Bins 2–3 | Units |
|---|---|---|---|
| Pass-band bandwidth | 262.8 | 530.8 | kHz |
| Stop-band bandwidth | 9.9 | 14.9 | MHz |
| Max pass-band gain | −1.8 | −1.4 | dB |
| Min pass-band gain | −4.2 | −10.8 | dB |
| Min stop-band gain | −49.0 | −56.0 | dB |

### 3.5.2 Alternate Measurements Space

Circuit excitation is achieved by applying a single 3 tone input stimulus. The chosen tones correspond to filter's center frequency, an octave lower and an octave higher. The input-output composition can be considered as an analog signature characterizing the filter and its level of specification compliance [68, 69, 79]. Figure 3.34 shows the input-output Lissajous composition for a nominal filter when it is excited using the aforementioned 3 tone stimulus as well as the Lissajous trace when the stimulus is applied to a filter affected by process variability. As demonstrated in previous works [68], Lissajous compositions serve as an indicator of circuit parametric deviations in linear analog filters.

Continuous trace information is compacted to a set of 10 evenly spaced (in time) voltage samples of filter response to the mentioned multitone stimulus as Figure 3.34 illustrates. The selection of such points allows an easy and systematic approach facilitating further data processing while keeping most of the Lissajous trace information available to the forthcoming measurements selection criterion [67]. The actual alternate measurements correspond to the difference of the samples of the deviated response with respect to the nominal response.

Last paragraph defined the set of possible alternate measurements to be used during the binning procedure. As Figure 3.34 illustrates, there are a total of 10 candidate alternate measurements to be considered. It is clear that a set of alternate measurements to be used for binning purposes has to satisfy two main properties: (1) the measurements need to reflect circuit's performances variability in order to allow the binning to be performed efficiently and (2) an adequate set of measurements should not be redundant to avoid incurring in extra binning costs [62, 63, 80]. The first condition is achieved by means of a sensitivity analysis of candidate alternate measurements. Regarding the second condition, Kendall's Tau rank correlation coefficient [81] is used to rate the most adequate pair of measurements with the aim of reducing redundant information [82]. Chapter 6 is devoted to present and assess the Kendall's Tau based selection criterion. Kendall's Tau rank correlation coefficient computed between all the possible alternate measurements pairs of the Butterworth filter under study is shown in Figure 3.35. The minimum absolute value of Kendall's Tau is 0.1126, highlighted in a white border and corresponds to measurements ids 9

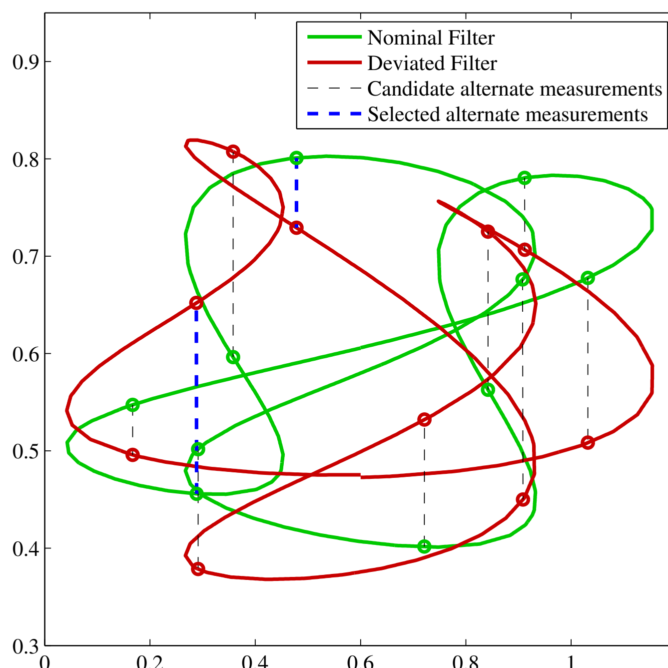


**Figure 3.34:** Input-output composition when a 3 tone signal is applied to the band-pass Butterworth filter. Evenly spaced (in time) voltage samples form the candidate set of alternate measurements to be used in the binning process.

and 7. Here forth, these measurements will define the alternate measurements space for the case study.

### 3.5.3 Statistical Training Phase

The proposed binning strategy using octrees has been applied to bin a 4th order band-pass Butterworth filter under the presence of process variations. As mentioned earlier, the circuit has been designed using and industrial 65 nm CMOS technology and simulated using HSPICE simulator. Monte Carlo simulations have been conducted relying on technology's process design kit (statcrolles corner) [77]. The set of obtained circuits clearly present different degrees of specification compliance. Figure 3.36 shows in detail the obtained magnitude Bode plots together with the bin boundaries defined in Table 3.6.

The training phase uses the measurements selected in previous section to encode the bins in the alternate measurements space using octrees. Figure 3.37 shows the resulting encoding of the circuits shown in Figure 3.32. Green, yellow and red octree cells correspond to bin 1, bin 2 and bin 3, respectively. The resulting octree has 14 levels in depth, i.e. $h_{\max} = 14$.

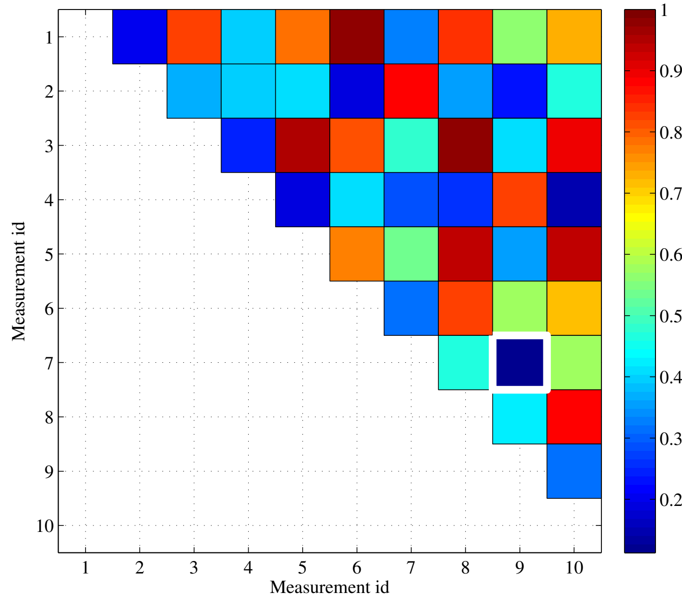


**Figure 3.35:** Kendall's Tau rank correlation coefficients between all the possible pairs of candidate alternate measurements. The minimum absolute value is highlighted in white. Warm colors indicate high correlation while cold colors indicate low correlation. More details in Chapter 6.

The resulting levels distribution for the encoded octree representing the alternate measurements space of the Butterworth filter is shown in Figure 3.38. As can be appreciated, the vast majority of nodes correspond to levels 6, 7, 8, and 9 despite the maximum node level is 14. Further details will be given in the forthcoming sections, but this fact implies a considerable advantage in terms of binning time since a considerable amount of circuit samples will be binned without achieving a deep recursion level.

### 3.5.4 Simulation Results

In order to evaluate the binning procedure using octrees, a new set of $50 \times 10^3$ Butterworth filters has been generated using Monte Carlo simulations and evaluated in the octree generated in the training phase. The results of the evaluation can be observed in Figure 3.39. Correctly binned circuits are drawn using green, yellow and red colors, which respectively correspond to bins 1, 2, and 3. Circuits that have not been correctly binned are circled using different colors according to the legend shown in Figure 3.39. Table 3.7 reports the data characterizing the bin escapes matrix for the case study. As expected, the vast majority of bin escapes takes place between contiguous bins. Global bin escapes for this case study is 1.676% out of the $50 \times 10^3$ that form the binning set. The worst adjacent bin misclassification is 0.494%.

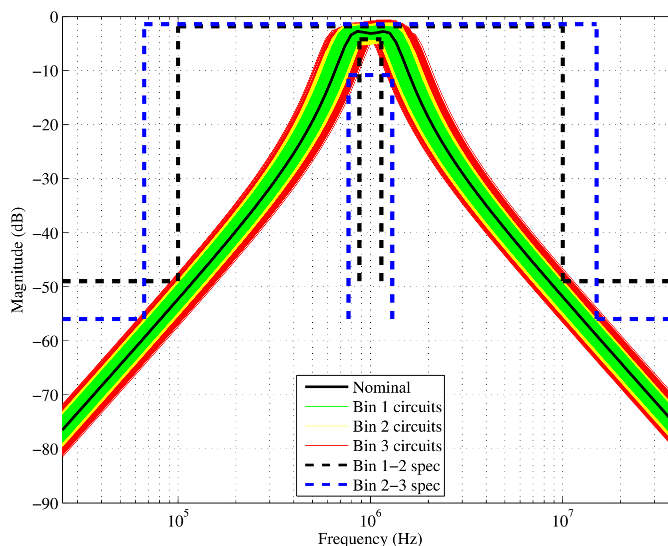


**Figure 3.36:** Detail of the magnitude Bode plots generated using HSPICE Monte Carlo simulations of the Butterworth filter used as case study. The specifications boundaries defining each of the bins are also shown using discontinuous traces.

**Table 3.7:** Bin escapes matrix for octrees based binning (%).

| | Without noise | | | Gaussian noise $\sigma = 3$ mV | | |
|---|---|---|---|---|---|---|
| | **Bin 1** | **Bin 2** | **Bin 3** | **Bin 1** | **Bin 2** | **Bin 3** |
| **Bin 1** | 56.580 | 0.494 | 0.000 | 53.970 | 3.084 | 0.020 |
| **Bin 2** | 0.328 | 26.750 | 0.436 | 2.288 | 23.902 | 1.324 |
| **Bin 3** | 0.000 | 0.418 | 14.994 | 0.004 | 1.006 | 14.402 |
| **GBE** | 1.676% | | | 7.726% | | |

In order to study the time efficiency of evaluating the octree presented in previous section, all the required comparisons have been stored for the generated set of $50 \times 10^3$ circuits. Figure 3.40 shows the cumulative percentage of binned circuits as a function of the required number of comparisons at a certain level. As can be observed, about 95% of the circuits are clustered by just performing 7 two-dimensional comparisons despite the octree is 14 levels deep. As suggested earlier, this implies a considerable benefit in terms of binning time since the octree data structure adapts its shape to the irregular bin boundaries generated in the alternate measurements space, only where a refinement is needed.

It has been mentioned that there are two main sources of bin escapes, namely, finite octree resolution and noise. The former issue has already been studied and simulation results have been reported. It basically depends on the required resolution which is also related with the number of samples used in the training phase. The latter

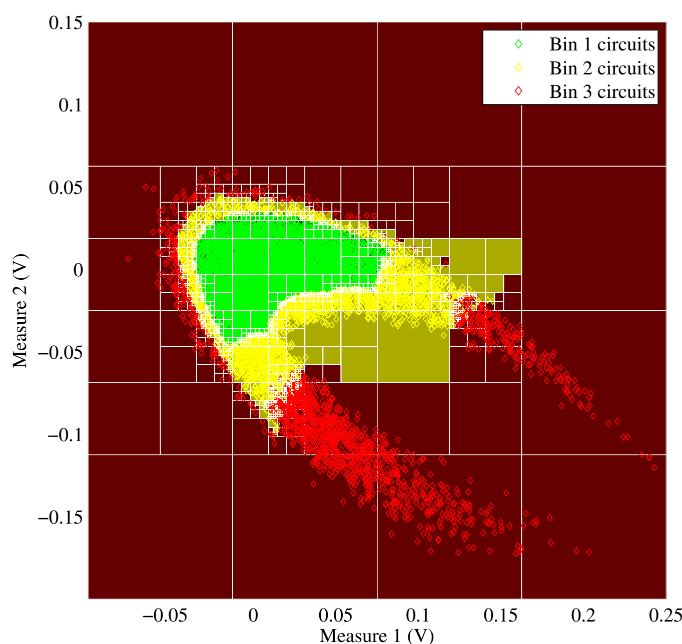


**Figure 3.37:** Resulting octree after the application of the training phase to the set of $10^4$ Butterworth filter samples shown in Figure 3.32. As can be appreciated, high octree levels concentrate in bin boundaries, where a refinement is needed.

issue, noise, is also of crucial importance thus resolution strictly depends on the DNR in a real world application. When noise is added, similar results to those presented in Figure 3.39 are obtained, but numbers get degraded. Table 3.7 also reports information on a noisy binning scenario, where Gaussian noise has been added to the alternate measurements. In this case, the global bin escapes rises up to 7.726% being the worst adjacent bin misclassification 3.084% out of the total set of considered circuits.

Binning results for different noise levels added to the alternate measurements and different sizes of the training set are reported in Figure 3.41. Global bin escapes is considerably affected when noise levels are increased, clearly showing a direct relationship between noise and GBE. Training set size also plays a noticeable role with respect to bin escapes. For the presented case study, if the training set consists of $10^3$ circuits, the resulting octree represents the alternate measurements space poorly what translates in high GBE. On the contrary, if sample size is in the order of $10^4$ or larger, the octree is sufficient to encode the bins in the measurements space.

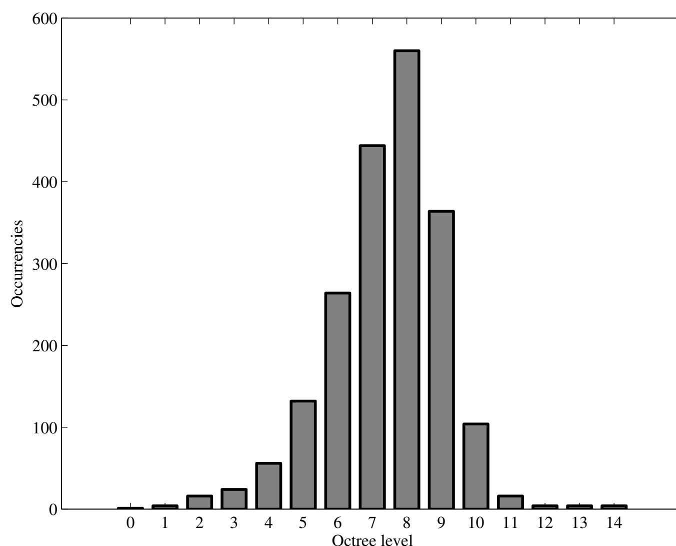


**Figure 3.38:** Levels distribution for the octree shown in Figure 3.37. Despite the maximum octree level is 14, the vast majority of octree cells correspond to levels 6, 7, 8, and 9, what greatly facilitates its evaluation in terms of binning efficiency.

### 3.5.5 Comparison with Support Vector Machines Classifier

In order to compare the proposed method for binning mixed-signal ICs with state of the art tools and techniques, a support vector machine (SVM) classifier has been trained using exactly the same set of circuits used for octrees which is depicted in Figure 3.32. The training procedure has been carried out using Matlab and the sequential minimal optimization training method. The kernel used in the procedure is a radial basis function (RBF), which is a standard choice in the field [27, 28, 83]. The SVM training has been carried out using an 5-fold cross validation together with a grid search to determine the optimum kernel spread, $\sigma$, as well as the optimum soft margin parameter, $C$. A single SVM classifier is capable of dealing with two classes only, so for binning circuits in $p$ bins, $p-1$ support vector machines need to be trained. In this chapter, two SVM classifiers have been trained, one for separating bins 1-2 and one for separating bins 2-3. The results for the grid search can be seen in Figure 3.42.

The cross validation procedure together with the grid search method to determine the best $\sigma$ and $C$ parameters yields to the optimum support vector machines to be used. Table 3.8 reports the training results for the two SVM classifiers trained using the same training set as used with octrees ($10^4$ samples). The whole SVM training process takes 1.5 h. The resulting optimum SVM classifiers boundaries are shown in Figure 3.43.

Table 3.9 summarizes the results of the comparison between the production binning

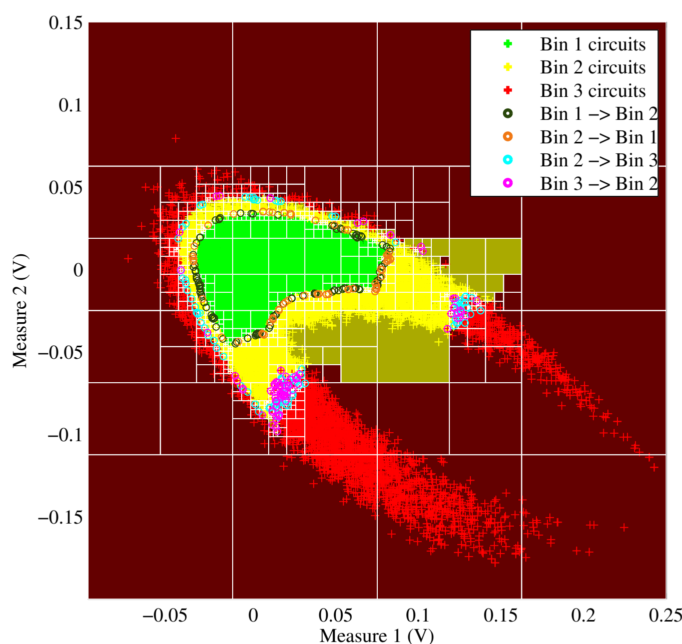


**Figure 3.39:** Binning results using the testing set of $50 \times 10^3$ Monte Carlo circuit samples by means of the octree illustrated in Figure 3.37 and generated in the former training phase. Misclassified circuits concentrate in bin boundaries.

using octrees and using support vector machines. Regarding the training phase, the training using SVM is considerably longer, specially if the cross validation and grid search needs to be performed. The global bin escapes for octrees and SVM are similar, accounting for 1.676% if octrees are used and 1.828% if SVM classifiers are used. The time needed to achieve the binning for the $50 \times 10^3$ circuits was around 5 times faster using octrees than support vector machines classifiers. This strictly depends on the number of support vectors resulting after the training phase for the case of SVM classifiers while it only depends on the average octree level for the case of octree classifiers.

Table 3.10 reports the bin escapes matrix for the binning procedure using the trained SVMs. The left hand side table corresponds to the ideal classification with no noise while the right hand side table reports the bin escapes matrix when Gaussian noise is added. Under the presence of noise, octree global bin escapes represent the 7.726% out of the total circuits while SVM wrongly bins the 7.660%, showing almost equivalent performances. It is important to note that non linear support vector machines rely on a minimization algorithm which may not converge immediately. Furthermore, SVM classifiers depend on several tuning parameters which require specific parameter selection and may result in non optimal classifiers. On the contrary, the octree encoding algorithm is straightforward to implement and solely relies on the available

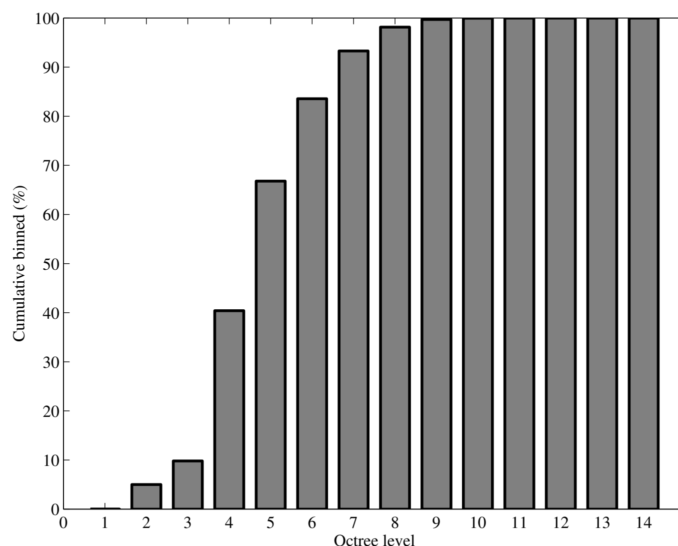


**Figure 3.40:** Cumulative percentage of binned circuits as a function of the achieved octree level for the binning phase using $50 \times 10^3$ Butterworth filters. As can be observed, about 95% of the circuits are binned by just performing 7 comparisons.

data.

## 3.6 Summary and Comments

A considerable number of challenges exist in alternate test of analog and mixed-signal circuits ranging from the selection of the actual set of indirect measurements to the actual test efficiency metrics reduction passing through the computational effort required to take the test decision. Amongst these challenges, the representation of the arbitrary test acceptance regions in the alternate measure space is an issue of major importance since it directly impacts on the test results.

In this chapter, a novel testing strategy aimed for mixed-signal circuits using octree tessellation in the alternate measurement space has been proposed. The method relies on two phases, namely training phase and testing phase. The training phase digitally encodes the test acceptance/rejection regions in the alternate measurements space using octrees. Such encoding is based on a set of circuits obtained from Monte Carlo simulations, model evaluation or available data on the production test run. The testing phase corresponds to the actual production testing using the previously computed octree.

Such digital encoding approach presents a number of benefits, specially in terms of computational efficiency since the obtained octree data structures are inherently

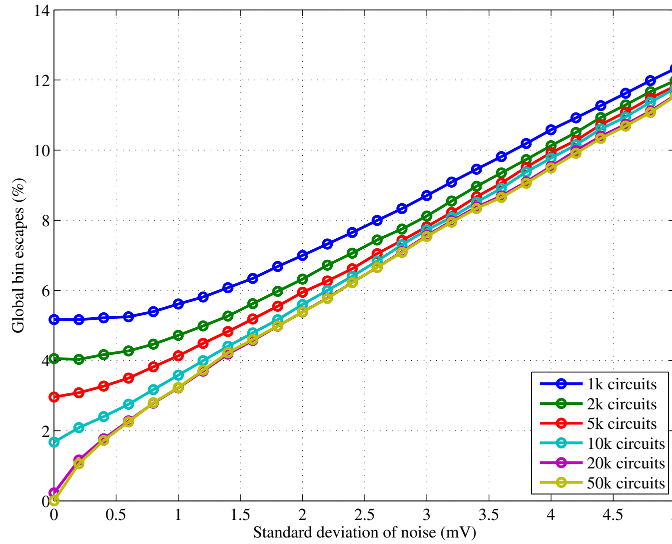


**Figure 3.41:** Global bin escapes as a function of the number of circuit samples used in the training phase and the noise present in the alternate measurements. As expected, global bin escapes metric increases as noise level increases.

sparse, what greatly facilitates fast training and testing times. Also, octrees have the great advantage of being generalized to an arbitrary number of dimensions without any extra issue beyond the well known curse of dimensionality. Regarding these generalization capabilities, octrees are sensitive to extend their clustering capabilities to more than two clusters, therefore facilitating the presented quality binning approach without any extra overhead. Further, the octree encoding algorithm is deterministic hence not relying on a minimization algorithm as many of the state of the art clustering methods do. This is a desirable feature since the resulting encoding does not depend on the chosen minimization algorithm, convergence issues or the considered initial conditions. Also, the simplistic recursive implementation, both for training and testing, of such data structures make them quite affordable and easy to implement in stand alone systems such as embedded systems (microcontroller, FPGAs,. . . ) as well as convenient for BIST implementations.

The proposed method has been applied to test a band-pass Biquad filter as a proof of concept. In order to show the viability the proposal, electrical simulations have been conducted to evaluate the incurred test escapes and test yield loss metrics, as a function of the number of circuits considered in the training phase and the noise level present in the measurements. Simulation results reveal that the proposed strategy is viable in terms of test efficiency metrics as well as have been also proven to be time efficient since only one comparison per coordinate and level traversed is needed in order to halve the uncertainty of classifying a circuit in the corresponding acceptance/rejection regions. This chapter has also proposed a procedure to increase the number of circuit samples in the surroundings of the test decision boundary.

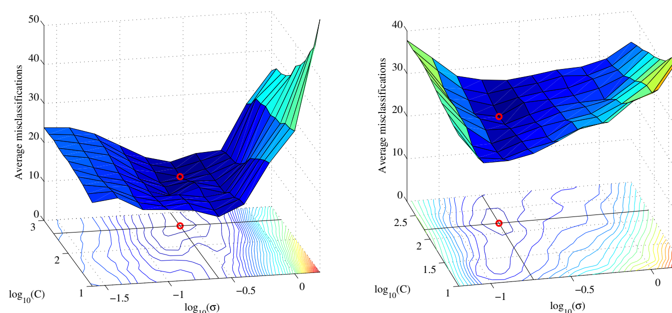


**Figure 3.42:** Results of the grid search in the $(\sigma, C)$ space using 5-fold cross validation technique with the training set presented in Figure 3.32. The plot on the left corresponds to the SVM between bins 1-2 while the plot on the right corresponds to the SVM between bins 2-3.

**Table 3.8:** SVM classifiers training information.

| Aspect | SVM 1-2 | SVM 2-3 | Units |
|---|---|---|---|
| Training set size | 10k | 10k | ckts |
| Number of grid search points | 110 | 100 | |
| Cross validation folds | 5 | 5 | |
| Optimum $\sigma$ parameter | 0.2512 | 0.1848 | |
| Optimum $C$ parameter | 398.1 | 158.5 | |
| Average misclassification | 12.6 | 25.0 | ckts |
| Number of support vectors | 180 | 623 | |
| Single SVM training time | 6.64 | 6.44 | s |
| Total training time | 53.7 | 38.7 | min |

Such circuit sample densification procedure implies a much better encoding of the test regions and therefore a considerable reduction in the penalty metrics.

Aiming to evaluate the performance of the proposal in the field of quality binning, a Butterworth filter has been designed in an industrial 65 nm CMOS technology affected by parametric variations and binned using octrees. In order to evaluate the binning application, a new metric has been defined to that purpose, i.e. global bin escapes (GBE). Monte Carlo simulations have been conducted to evaluate the GBE metric as a function of several parameters such as the training set size and noise levels. Simulation results reveal that bin misclassification metrics can be controlled depending on the number of circuits used in the training phase. The octree binning procedure has been compared against state of the art support vector machines classifiers revealing considerable advantages in terms of evaluation complexity and showing a speedup of $\times 5$ and slightly better misclassification results for the considered two-dimensional case study.

The next chapter focuses on the also challenging issue of testing heterogeneous systems and how an alternate test approach is able to enhance and facilitate the test

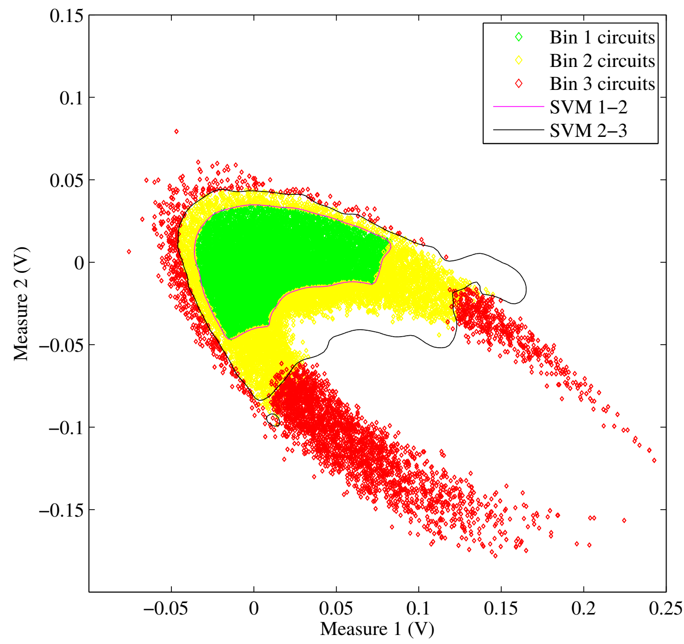


**Figure 3.43:** Best SVM classifiers using the training set of $10^4$ circuits shown in Figure 3.32. The SVM has been trained using sequential minimal optimization method and radial basis functions (RBF) as kernel.

and identification of parametric variations in such non classical systems.

**Table 3.9:** Comparison between octrees and support vector machines.

| Aspect | Octree | SVM |
|---|---|---|
| Grid search and cross validation time | not needed | 1.5 h |
| Single classifier training time | 1.3 s | 13 s |
| Production binning time | 19.2 s | 99.8 s |
| Global bin escapes | 1.676 % | 1.828 % |

**Table 3.10:** Bin escapes matrix for SVM classifier (%).

| | Without noise | | | Gaussian noise $\sigma = 3$ mV | | |
|---|---|---|---|---|---|---|
| | **Bin 1** | **Bin 2** | **Bin 3** | **Bin 1** | **Bin 2** | **Bin 3** |
| **Bin 1** | 56.688 | 0.3860 | 0.000 | 54.078 | 2.980 | 0.016 |
| **Bin 2** | 0.204 | 26.234 | 1.076 | 2.244 | 23.464 | 1.806 |
| **Bin 3** | 0.000 | 0.162 | 15.250 | 0.004 | 0.610 | 14.798 |
| **GBE** | 1.828% | | | 7.660% | | |

Chapter 4

# Alternate Test of Heterogeneous Systems

As seen in previous chapter, octree tessellation is an efficient way of encoding the alternate pass/fail regions for alternate mixed-signal testing. The applicability of the method is not restricted to mixed-signal circuits, hence it can be also applied to test heterogeneous systems. Microelectromechanical systems (MEMS) fabrication and packaging may induce parametric defects which have to be efficiently tested to improve fabrication yield and device reliability. Traditionally, due to the non inherently electrical transduction principle in heterogeneous systems, testing such devices is an issue of major concern. In this chapter, the possibilities of testing single parametric defects in dual axis IC accelerometers are explored. The proposed method uses a mixed-signal test strategy based on Lissajous compositions. It consists of a dynamic correlation of the two orthogonal output signals from the device. This leads to a Lissajous trace which is able to manifest parametric deviations. Several device parameters have been studied and characterized under different deviation levels. The definition of a metric and the evaluation of its test efficiency is used to optimize the testing procedure against noisy measurements. The method has been experimentally applied to test the misalignment degree in a commercial dual axis accelerometer.

## 4.1 Integrated MEMS Capacitive Accelerometers

MEMS capacitive accelerometers are widely used and under increasing demand. They can be found in basic consumer electronics as well as in safety critical applications like in the automotive industry or in aerospace navigation systems. Such devices consist of three functional subsystems as depicted in Figure 4.1. First and middle subsystems correspond to the mechanical and structural parts of the accelerometer device where

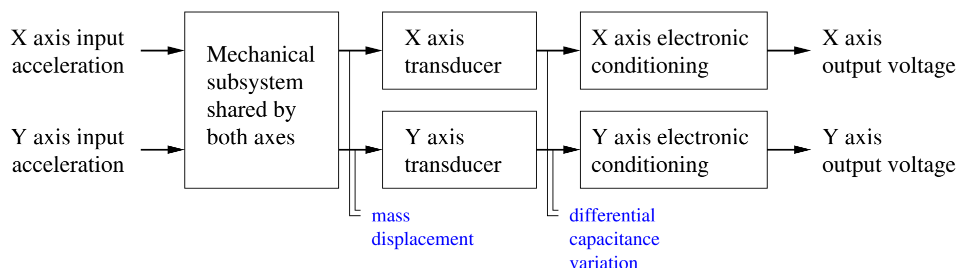


**Figure 4.1:** Stages of the acceleration to voltage transduction chain for integrated capacitive accelerometers and the magnitudes involved in the process.

the transduction from acceleration to electrical signal takes places. The latter stage performs the electronic signal conditioning according to device specifications.

MEMS accelerometers manufacturers constantly deal with challenging specifications. For instance, designing for the mitigation of process variations, the achievement of more precise, reliable and compact devices or targeting high sensitivity devices for safety critical applications. Because of such reasons, these devices need to be precisely diagnosed to ensure device parameters lie within specification ranges. This chapter proposes a testing strategy focusing on single parametric defects affecting mechanical and transducer subsystems. In the following sections, some modeling considerations are explained for both functional blocks.

### 4.1.1 Mechanical Subsystem

The sensing principle for capacitive MEMS accelerometers is based on the displacement of an inertial mass, $m$, attached by means of beams to the fixed substrate as Figure 4.2 illustrates. The dynamics of such structures are complex, therefore the need of using computational methods as finite elements analysis (FEA) to precisely characterize them [84]. Under small displacements, beams behavior can be approximated by linear differential equations thus being treated as a damped mass attached to spring elements.

As a first order approximation, the model of the mechanical subsystem of an accelerometer is the well known second order system $\ddot{x} + \frac{b}{m}\dot{x} + \frac{k}{m}x = a_{\text{in}}$. Variables $a_{\text{in}}$ and $x$ represent the input acceleration and inertial mass displacement respectively. Parameter $k$ is the spring constant, related with structure stiffness. It can be shown that the spring constant of a single loaded cantilever beam with constrained rotations in both ends is $k = 12EI_z/\ell^3$, where $E$ is the Young's modulus of the material, $I_z$ corresponds to the moment of inertia of the section with respect to the bending axis and $\ell$ is the length of the beam. For more detailed information regarding different mechanical configurations see reference [84].

Parameter $b$ corresponds to the damping factor which takes into account the effects of the so called Couette's flow. Damping occurs when the whole structure moves over

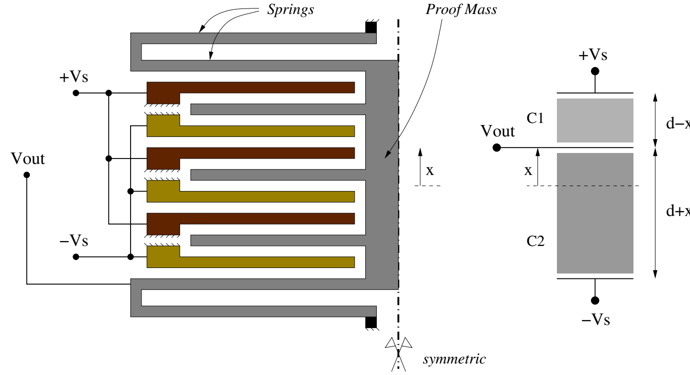


**Figure 4.2:** Sketch of capacitive accelerometer inertial mass and comb fingers. Inertial mass and fingers move along $x$ direction by means of the anchoring springs, thus generating different capacitances in the voltage divider.

a viscous fluid, air in most cases. This creates a shear stress which is translated into a force opposite to displacement, proportional to fluid dynamic viscosity and contact area and inversely proportional to the gap between the structure and the substrate. Coefficient $b$ is extremely small in MEMS accelerometers and does not affect device response, but plays an important role when working near the natural frequency [84].

MEMS fabrication and packaging processes may present misalignments which result in an improper placement of the internal microstructures or dies. For such reason, axis misalignment is taken into consideration as a possible defect. In this chapter, a rotation angle $\beta$ is defined to contemplate such kind of defects. Non defective devices have $\beta = 0$. For misalignment angles $\beta \neq 0$, different acceleration measures are obtained.

### 4.1.2 Capacitive Transducer Subsystem

The capacitive transducer subsystem is formed by a set of interdigitated fingers attached to the inertial mass as Figure 4.2 depicts [84]. Fingers movement, translate in a capacitance variation in the two sides of the differential capacitive voltage divider being proportional to the inertial mass displacement. The capacitive transducer is supplied with a high frequency signal $\pm V_\text{s}$ in order to reduce resistive effects. Device output is denoted as $V_\text{out}$. Sensor output voltage depends on both capacitances $C_1$ and $C_2$ as illustrated in Figure 4.2. Such capacitances are functions of plate areas, $A_1$ and $A_2$, medium permittivities, $\varepsilon_1$ and $\varepsilon_2$ and rest distances between plates, $d_1$ and $d_2$. Therefore, device output can be written as,

$$V_\text{out} = \frac{C_1 - C_2}{C_1 + C_2} V_\text{s}, \quad C_1 = \frac{\varepsilon_1 A_1}{d_1 - x}, \quad C_2 = \frac{\varepsilon_2 A_2}{d_2 + x} \tag{4.1}$$

Where subindexes 1 and 2 correspond to the upper and lower capacitances shown

in Figure 4.2 respectively. If no defects are present in the capacitive voltage divider subsystem, output voltage simplifies to $V_{\text{out}} = \frac{x}{d} V_{\text{s}}$.

In the following section, the characterization of dual axis capacitive accelerometers using Lissajous compositions is presented. Different single defects are studied taking into account the presented model of the sensor.

### 4.1.3 Electronic Conditioning Subsystem

The electronic conditioning subsystem accommodates the output signal according to device specifications. As mentioned, it is usual to supply the capacitive transducer with a high frequency AC signal for mitigating resistive effects, so the electronic conditioning subsystem also performs the demodulation and filtering of the analog signal coming out from the capacitive transducer subsystem.

For the case of analog output accelerometers and assuming an ideal AC signal demodulation, the electronic conditioning subsystem can be supposed to act as a signal boosting stage with a certain gain $G$, therefore, $V_{\text{out}} = G\, V_{\text{c}}$.

The output signal is normally affected by an offset voltage $V_{\text{off}}$, which is also added in the electronic conditioning subsystem. Gathering the contribution of each of the subsystems in one single expression yields device output voltage, $V_{\text{out}}$, to a given input acceleration, $a_{\text{in}}$,

$$V_{\text{out}} = V_{\text{off}} + \underbrace{G \frac{V_{\text{s}}}{d} \frac{m}{k}}_{\text{Sensitivity}} \; a_{\text{in}} \tag{4.2}$$

The term $S = G \frac{V_{\text{s}}}{d} \frac{m}{k}$ is the sensitivity of the device. Sensitivity is the most important functional parameter of an accelerometer and it distributes following a normal distribution as can be checked in different Analog Devices products datasheets [85]. In this chapter, both axes sensitivities are considered as functional specifications.

## 4.2 Analog Characterization and Excitation of Dual Axis Capacitive Accelerometers

Accelerometers target magnitude is acceleration so the applied kinematics to achieve a good characterization are crucial. To this purpose, both axes need to be excited at the same time with a wide range of accelerations. Of course, the use of a low-cost setup is desirable as well as to be able to characterize several devices presenting different parametric deviations in a single experimental run.

In the following sections the Lissajous based characterization setup is presented for dual axis IC accelerometers and discussed in terms of the applied kinematics. Simula-

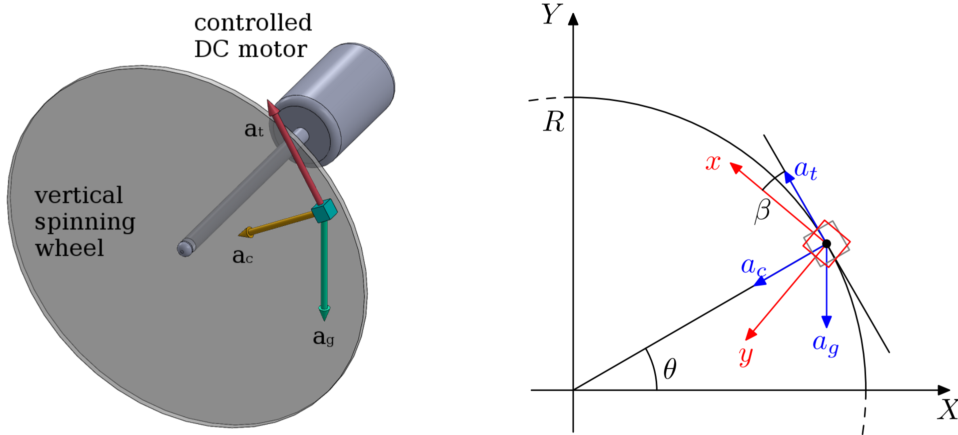


**Figure 4.3:** Sketch of a dual axis accelerometer mounted in a vertical spinning wheel and the accelerations involved in the kinematics when the wheel is spun following an arbitrary angular velocity profile $\dot{\theta}(t)$.

tions considering different parametric shifts in the parameters forming the mechanical and the capacitive transducer subsystems are also presented.

### 4.2.1 Vertical Spinning Proposal

Conventional IC accelerometer testing is carried out by means of horizontal spinning tables or tilt tables. Horizontal spinning method uses centripetal acceleration as input excitation. Such acceleration only depends on the angular velocity and rotation radius and therefore becomes a well controlled input signal. On the other hand, tilt tables take advantage of gravity acceleration to apply a static excitation by projecting it along the sensitive axes.

In this proposal, both centripetal and gravity accelerations, as well as tangential acceleration are combined [72]. To this purpose, the accelerometer is spun in vertical position with the aid of a controlled DC motor as Figure 4.3 sketches. The imposed angular velocity profile, $\dot{\theta}(t)$, follows a sinusoidal function of $\Omega_M$ rad/s offset and $\Omega_A$ rad/s amplitude. The kinematics are $T$-periodic of the form,

$$\dot{\theta}(t) = \Omega_M + \Omega_A \sin\left(\frac{2\pi}{T}t\right) \tag{4.3}$$

Setting the angular velocity $\dot{\theta}(t)$ to be a sinusoidal profile, the angular position $\theta(t)$ and angular acceleration $\ddot{\theta}(t)$ of the spinning wheel can be determined as well. Then, each of the orthogonal acceleration components sensed by device axes can be obtained.

### 4.2.2 Lissajous Compositions Under Parametric Defects

The particular acceleration scheme shown previously yields to a rich set of Lissajous compositions, therefore highlighting the possible deviations in the model parameters. As stated, the spun device experiments three different accelerations, namely, gravity, $a_g$, centripetal, $a_c$, and tangential, $a_t$. Under such vertical spinning assumptions, the overall acceleration vector $a_{\text{tot}}(t)$, becomes the sum of each of these three accelerations,

$$a_g = \begin{pmatrix} -g\cos\theta(t) \\ g\sin\theta(t) \end{pmatrix} \quad a_c = \begin{pmatrix} 0 \\ R\dot{\theta}(t)^2 \end{pmatrix} \quad a_t = \begin{pmatrix} R\ddot{\theta}(t) \\ 0 \end{pmatrix} \tag{4.4}$$

Where $\theta(t)$ and $\ddot{\theta}(t)$ correspond to the integration and differentiation of the angular velocity profile indicated in equation (4.3). The projections of these accelerations define the Lissajous composition in terms of different parametric defects. According to the models presented earlier, a set of simulations have been conducted considering single parametric defects in each of the following parameters:

- Mechanical subsystem: inertial mass ($m$), spring constant ($k$), axis misalignment ($\beta$)
- Transducer subsystem: medium permittivity ($\varepsilon$), overall plate area ($A$), rest distance between plates ($d$)

For instance, parametric defects affecting the inertial mass shared by both axes yield to the Lissajous composition shown in Figure 4.4. The behavior is different when considering defects in the spring constant of $y$ axis as Figure 4.5 illustrates. It can be seen that mass and spring constant deviate the Lissajous composition in opposite directions. This behavior is understandable since the steady state response of the mechanical subsystem depends on the quotient $m/k$.

If axis misalignment is present, the obtained Lissajous compositions can be seen in Figure 4.6. As can be appreciated, the traces seem to rotate with respect to a common point. This behavior is reasonable thus sensed accelerations project differently in each of the axes.

When the capacitive subsystem is affected by parametric defects the obtained Lissajous compositions experiment a translation along the defective axis. In Figure 4.7, medium permittivity of the upper capacitor of $y$ axis has been studied under several parametric defects. On the contrary, in Figure 4.8, the rest distance between plates is varied. As can be observed, the behavior is also in opposite directions as the modeling equation for output voltage suggests.

An interesting observation is that the sensitivity to parametric defects of mechanical and capacitive transducer parameters is different. It is shown that capacitive transducer subsystem parameters are much more sensitive to deviations than those in the mechanical subsystem as the scales and applied defects clearly show.

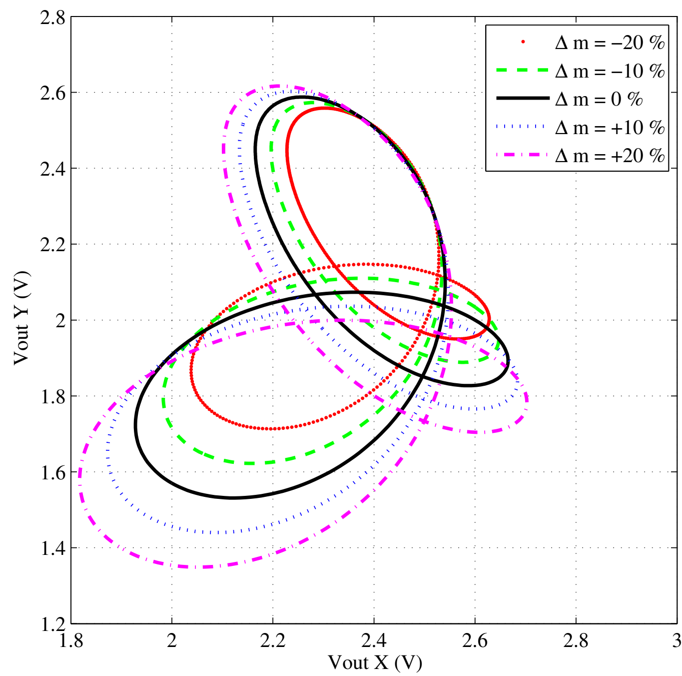


**Figure 4.4:** Simulated Lissajous compositions of a dual axis IC accelerometer for different defect levels in the inertial mass. Both axes masses have been considered to be correlated.

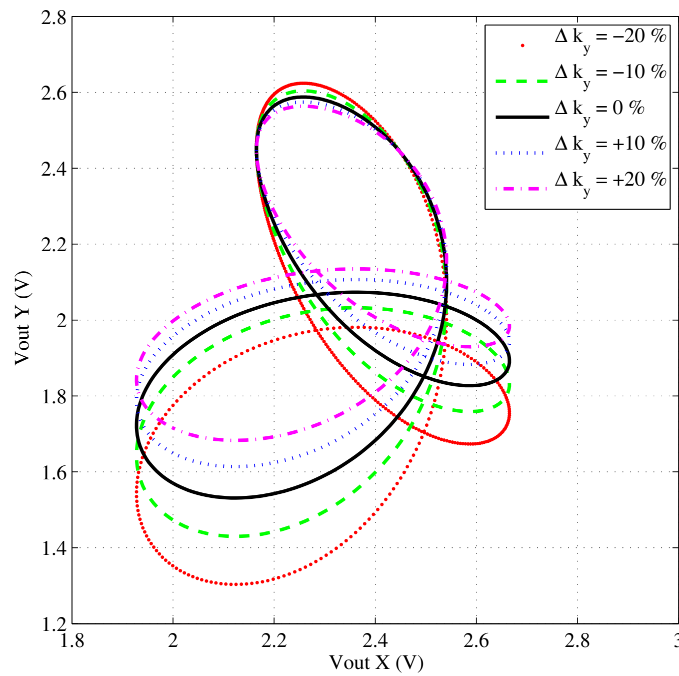


**Figure 4.5:** Simulated Lissajous compositions of a dual axis IC accelerometer for different defect levels in the spring constant. The deviated spring constant is the one on $y$ axis.

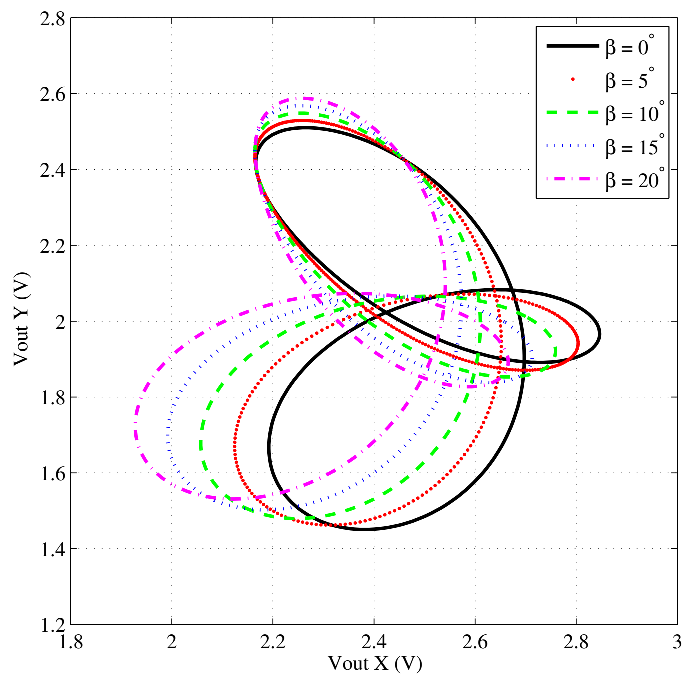


**Figure 4.6:** Simulated Lissajous compositions of a dual axis IC accelerometer for different defect levels in axes misalignment.

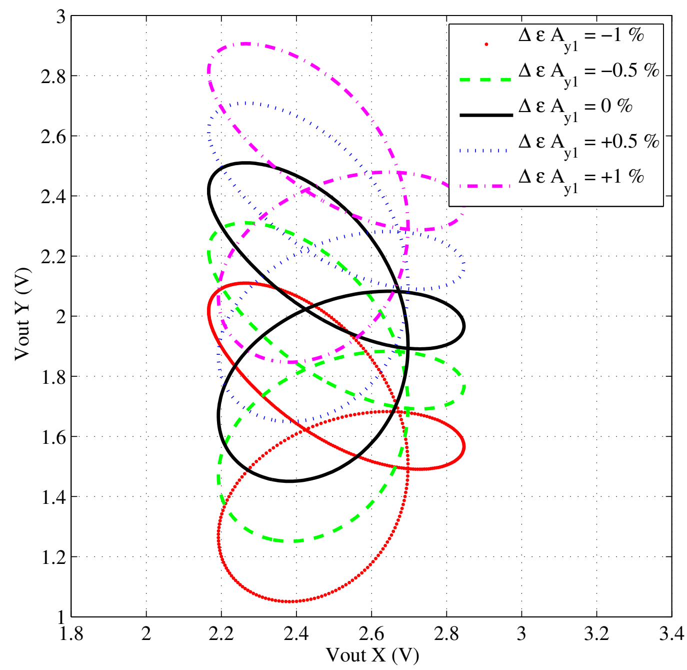


**Figure 4.7:** Simulated Lissajous compositions of a dual axis IC accelerometer for different defect levels in the medium permittivity or plate area. The deviated parameter is in the upper capacitor of $y$ axis.

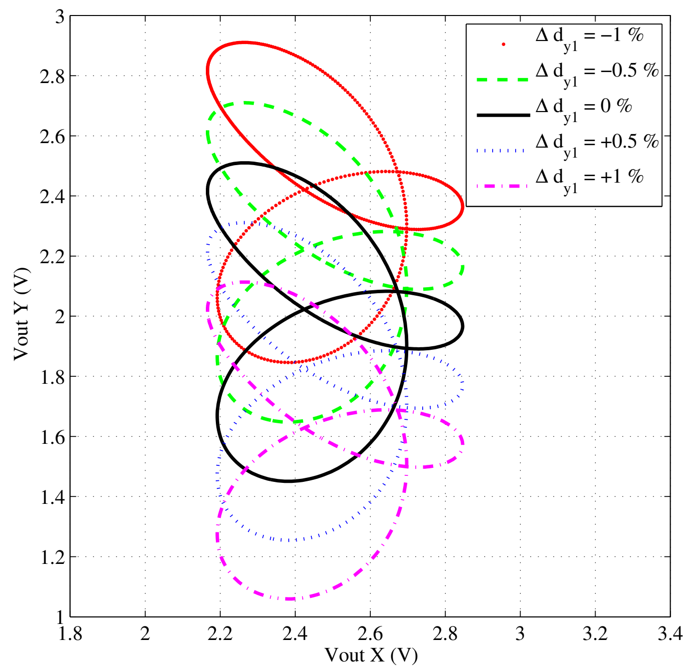


**Figure 4.8:** Simulated Lissajous compositions of a dual axis IC accelerometer for different defect levels in the rest distance between plates. The deviated parameter is in the upper capacitor of $y$ axis.

### 4.2.3 Metric Definition

In order to quantify the amount of deviation, a discrepancy metric is defined. Continuous trace information is compacted by taking into consideration the tangency points of vertical and horizontal tangent lines to the Lissajous composition as Figure 4.18 illustrates. The selection of such points allows an easy and systematic approach facilitating further data processing while keeping Lissajous trace information. In general, given a Lissajous composition of two signals, $\mathcal{L}(x(t), y(t))$, its set of tangency points is defined as,

$$T_{\mathcal{L}} = \{(x, y) \in \mathcal{L} \mid \dot{x}(t) = 0 \text{ or } \dot{y}(t) = 0\} \quad (4.5)$$

Then, the metric is defined as the set of $\Delta X_i$ and $\Delta Y_i$ displacements of the deviated curve with respect to the reference one, see Figure 4.18. Rigorously, given two Lissajous traces, one defective, $\mathcal{L}_d$, and one reference, $\mathcal{L}_r$, the metric is defined as,

$$M_{(\mathcal{L}_d, \mathcal{L}_r)} = \{s_1 - s_2 \in \mathbb{R}^2, s_1 \in T_{\mathcal{L}_d} \text{ and } s_2 \in T_{\mathcal{L}_r}\} \quad (4.6)$$

The diagnosis procedure starts with a set of measured Lissajous tangency points displacements, $(\Delta X_i, \Delta Y_i)$. Such displacements are plotted in the calibration curves and then the closest point of the calibration curve is chosen as the diagnosed value. Further details will be given when reporting the experimental results of the diagnosis strategy. In the following section, the methodology for evaluating the diagnosis efficiency of each of these metrics with respect to the defect level is discussed and justified.

### 4.2.4 Diagnosis Efficiency Evaluation

It is clear that not all the tangency points will displace equally if the device presents a defective parameter. For such reason, it would be desirable to quantify the sensitivity of each of the selected tangency points to device parameters variations. To this purpose, a diagnosis efficiency (DE) function is defined as the ratio between the norm of the displacement and the considered absolute value of deviation, $r$, as,

$$\mathrm{DE}(r) = \frac{\|(\Delta X_i, \Delta Y_i)\|}{|r|} \quad (4.7)$$

As shown in Figure 4.18, some points may be spotted as better diagnosis candidates than others depending on the amount of displacement they present when a defect is considered. Function $\mathrm{DE}(r)$ takes into account the variation ratio of tangency points displacements with respect to the actual amount of defect. In order to quantify such aspect in the considered parametric defect interval, a figure of merit is defined as the average value of the diagnosis efficiency function, $\mathrm{DE}(r)$, over the interval ranging from $r_{\min}$ to $r_{\max}$, as,

$$\text{FOM} = \frac{1}{r_{\max} - r_{\min}} \int_{r_{\min}}^{r_{\max}} \text{DE}(r)\, dr \tag{4.8}$$

The defined figure of merit quantifies the suitability of the tangency point to be used in the diagnosis procedure. Such FOMs will serve as weighting parameters when performing parameter diagnosis. Also, such methodology allows a better noise immunity in the final diagnosis result.

## 4.3 Application to Accelerometer Sensitivity Test Using Octrees

As mentioned earlier, conventional integrated accelerometers testing is carried out by means of horizontal spinning tables or tilt tables. Horizontal spinning tables use centripetal acceleration as input excitation since it is a well controlled parameter due to its dependence on the angular velocity and spinning radius. On the other hand, tilt tables take advantage of gravity acceleration to apply a static excitation to the device. Previous works derived from the research presented in this dissertation have explored the possibilities of testing and diagnosing dual axis accelerometers using a vertical spinning setup [72, 86].

The vertical spinning proposal consists on rotating the device in a vertical plane following an arbitrary angular velocity profile, $\dot{\theta}(t)$, as Figure 4.3 illustrates. While the device is rotating, both orthogonal device outputs are sensed and composed to yield a Lissajous composition. These traces are sensitive to catastrophic and parametric defects the device under test (DUT) may present and therefore become a suitable tool for testing such devices.

The test proposal departs from a Lissajous composition generated by the previously presented vertical spinning setup. Therefore, the classification of pass/fail devices is translated in taking the decision if a given Lissajous composition corresponds to a device which fulfills functional specifications or not. To this purpose, the proposed testing methodology is divided into two phases. The former corresponds to a training phase in which the specifications compliance region is computed using statistical and corner samples with the aid of octrees. The latter is related to the testing procedure itself. Figure 4.9 shows an overview of the method which is described in detail in the following two sections.

### 4.3.1 Statistical Training Phase

As stated before, the training phase consists on the generation and encoding of the specifications compliance region for further usage in the testing phase. The training phase may be computationally intense since the computation time is exponentially related to the data dimensionality and the required number of bits (upper bound),

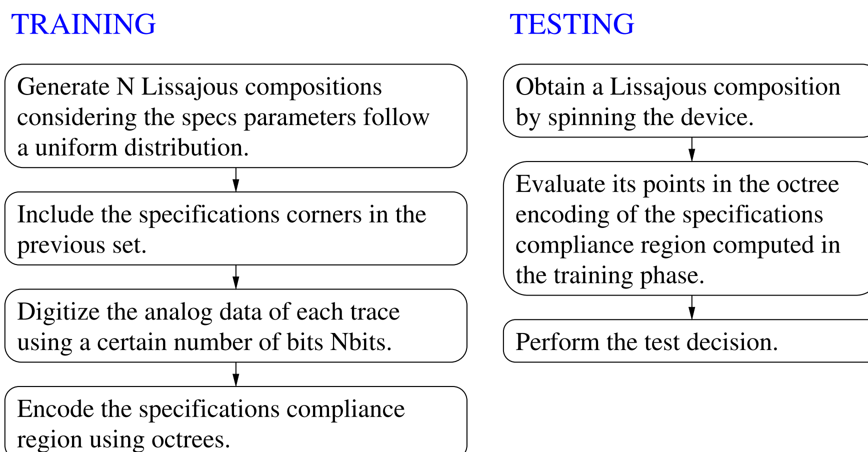


**Figure 4.9:** Flow diagram showing an overview of the steps that characterize the training and testing phases. The training phase, which may be computationally intense, only needs to be performed once.

but it only needs to be computed once. Given a device with sensitivities $S_x$ and $S_y$ for each of its axes, it is called to be within (functional) specifications if and only if,

$$S_{\min} \leq S_x \leq S_{\max}, \quad S_{\min} \leq S_y \leq S_{\max} \tag{4.9}$$

The previous subset of devices can be visualized in the Lissajous composition space by performing a statistical sampling of specifications compliance devices among all the possible ones and representing them in the XY plane. In Figure 4.10, 50 Lissajous compositions are plotted. Devices sensitivities have been drawn from non correlated uniform distributions. Voltage outputs can be easily computed using equation (4.2).

Test limits have been established to $\pm 5\%$ of the nominal value of 0.29 V/g ($S_{\min} = 0.2755$ V/g and $S_{\max} = 0.3045$ V/g). In order to accurately determine the specification compliance region, the four corners have been also included in the dataset.

In order to encode the analog data of Figure 4.10 using octrees, a digitization process has to be performed. For illustration purposes, Figure 4.11 shows the resulting digitization of the previous set of Lissajous compositions using 6 bits. As can be seen, the digitization process allows getting rid of a large number of redundant data points which do not provide any extra information according to the required resolution or noise level.

After digitization, the octree algorithm detailed in the previous section can be applied to pass/fail data points. Figure 4.12 shows the resulting octree encoding using 6 bits. Note that the maximum achieved octree level matches the number of bits since each new level corresponds to a bisection operation.

If the number of bits is increased, the maximum number of levels also increases and

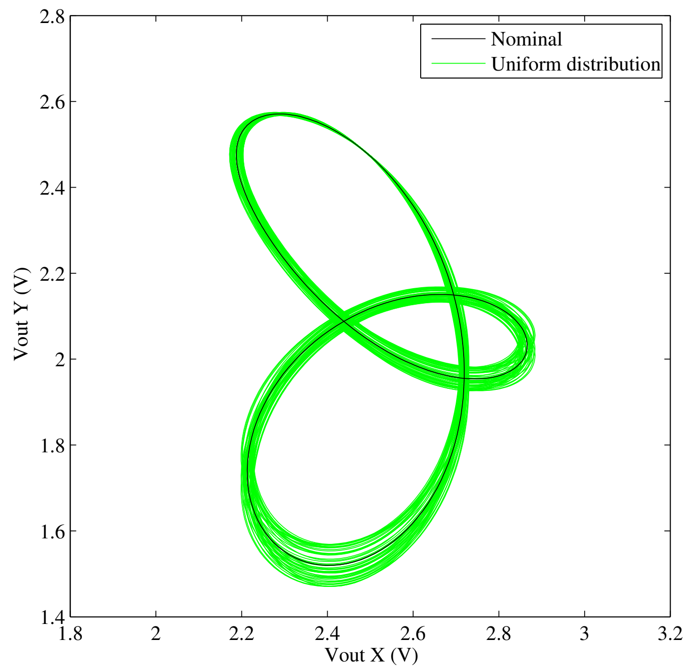


**Figure 4.10:** Set of 50 Lissajous compositions generated with devices which sensitivities have been drawn from non correlated uniform distributions. Distributions spread has been assumed to be ±5% of the nominal value.

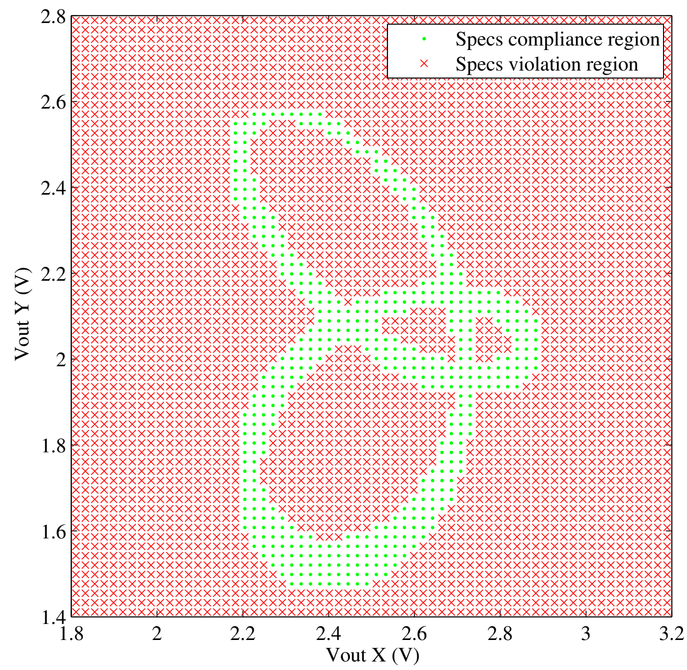


**Figure 4.11:** Resulting specifications compliance and violation regions after digitizing the analog information of the Lissajous compositions shown in Figure 4.10. The digitization has been carried out using 6 bits.

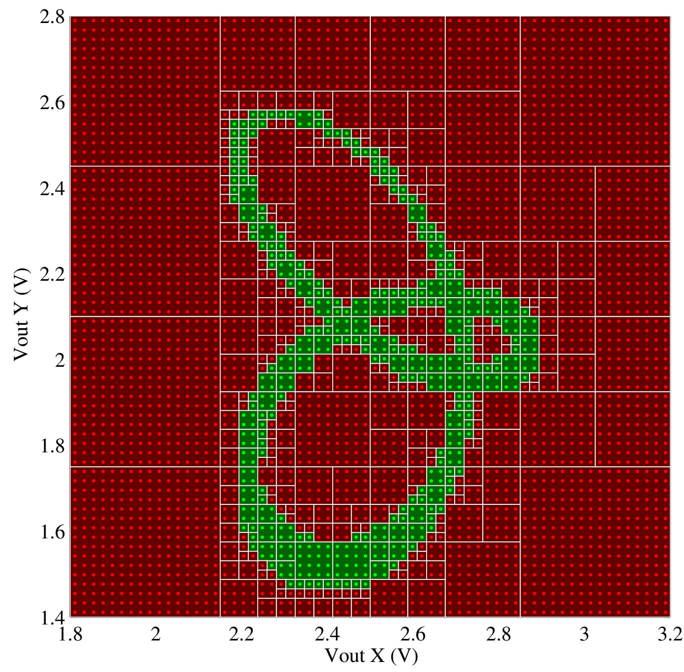


**Figure 4.12:** Octree encoding of the specifications compliance/violation regions for the case study presented in Figure 4.11 using 6 bits. The maximum octree level achieved is 6.

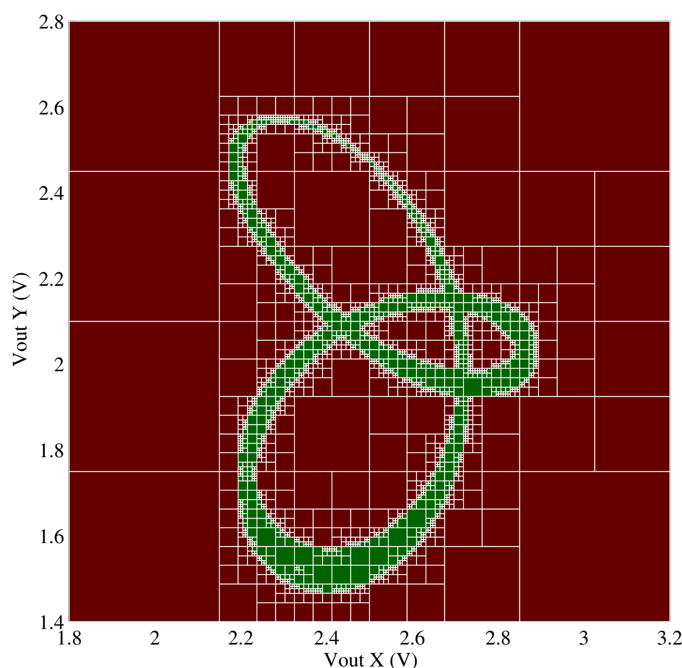


**Figure 4.13:** Octree encoding of the specifications compliance/violation regions for the case study presented in Figure 4.12 with 8 bits. The maximum octree level achieved is 8.

therefore the number of octree cells. Such situation can be checked in Figure 4.13 in which the Lissajous information of Figure 4.10 has been encoded using an 8 bits octree.

### 4.3.2 Simulation Results

Octree data structures are time efficient to evaluate as shown in Chapter 3. This is so because the probability of having a device near the test decision boundary is quite small. Additionally, the octree depth is only higher in the boundary region so the average time to perform an evaluation is far from the maximum theoretical exponential upper bound. The proposal presents an advantage over other clustering methods since the required number of operations to evaluate the device is highly decreased.

The test strategy consists on the evaluation of a Lissajous composition in the previously computed octree encoding the specifications compliance region. To this purpose, only a few points of the trace are chosen to be evaluated in the octree improving this way the test application time.

Consider the Lissajous composition of Figure 4.14. The points taken in consideration

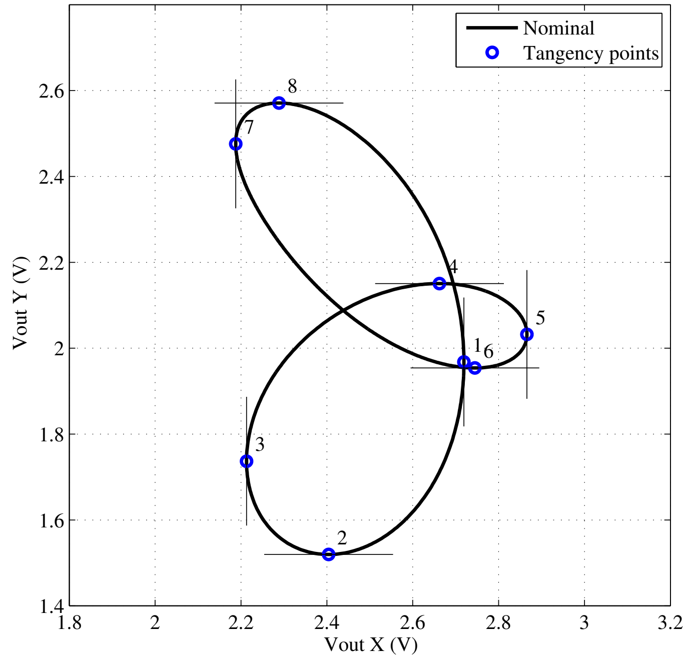


**Figure 4.14:** Lissajous trace information is replaced by its points of tangency with vertical and horizontal tangent lines. These set of points are used to perform the test decision by evaluating them in the octree data structure.

correspond to the tangency points of vertical and horizontal tangent lines to the Lissajous composition. The selection of such points allows an easy and systematic approach, therefore facilitating further data processing while keeping the information of the Lissajous trace [72].

Given a set of $n$ Lissajous data points, the test strategy establishes a device as PASS if all the $n$ points are clustered as specification compliant by the octree data structure, otherwise, the device is classified as FAIL.

In order to validate the proposal, several simulations have been performed as a function of the number of bits. To that purpose, a set of 10000 device samples have been generated considering their sensitivities distribute as normal and non correlated random variables.

As shown in previous chapter, testing techniques are evaluated using *test yield loss* and *test escape* metrics. *Test yield loss* is defined as the probability of classifying a functional device as non functional and therefore being discarded. *Test escapes* is defined as the probability of classifying a non functional device as functional and therefore being served to the customer. If the number of simulations is high enough, these indicators can be estimated.

Test escapes values are upper bounded by 2.4% as Figure 4.15 illustrates. As ex-

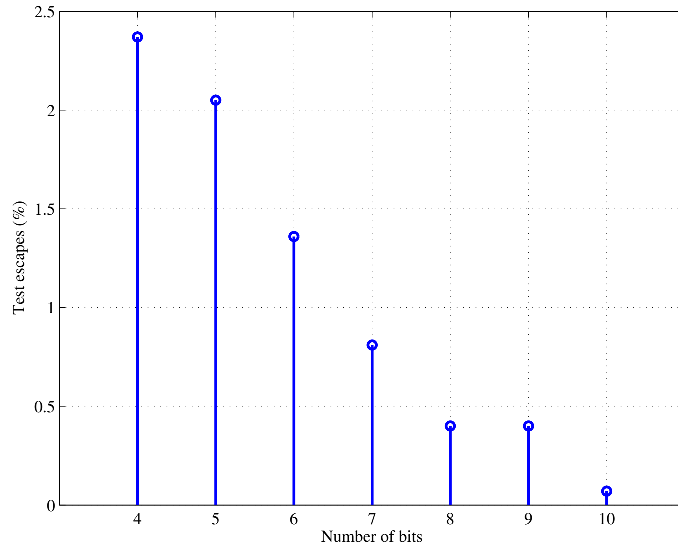


**Figure 4.15:** Test escapes as a function of the number of bits used to encode the octree data structure. The finer the encoding, the probability of classifying a non functional device as functional decreases.

pected, the number of non functional devices passing the test decreases as the resolution (i.e. the number of bits) of the octree increases. Of course, there is a trade off between the required resolution and required test escapes level since they strongly affect the octree computation time.

Regarding test yield loss, simulation results can be seen in Figure 4.16. As can be observed, the maximum value does not exceed 0.05%. The increase of test yield loss as the number of bits increase is because a finer approximation of the specifications compliance region boundary is achieved. This fact increases the probability of classifying a functional device as non functional, situation reflected in Figure 4.16.

Figure 4.17 shows the test application time considered as the computational time used to evaluate the octree for a given candidate device. As can be observed, the largest time is about 5 ms using 10 bits for octree encoding. It is important to note that the computational time logarithmically depends on the number of bits. This fact makes the octree data structure an interesting option in terms of time efficiency.

## 4.4 Application to Accelerometer Axis Misalignment Diagnosis

As stated, Lissajous based characterization of dual axis accelerometers using vertical spinning is a generic method for highlighting single parametric defects in such devices.

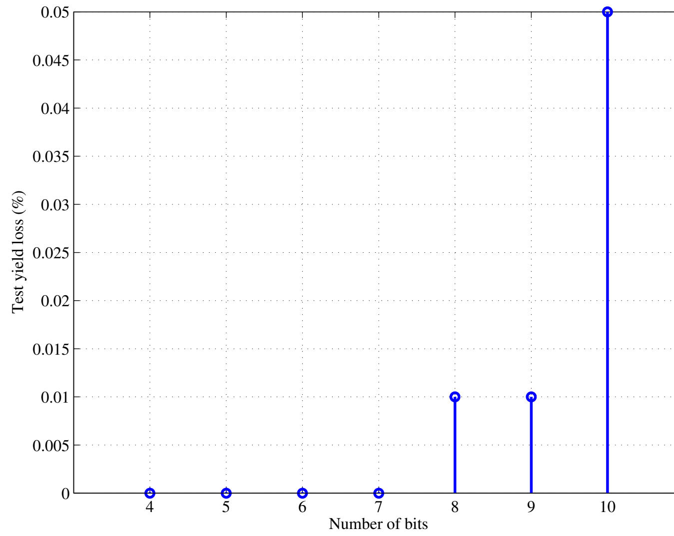


**Figure 4.16:** Test yield loss as a function of the number of bits used to encode the octree data structure. The finer the encoding, the larger the probability of classifying a functional device as non functional.

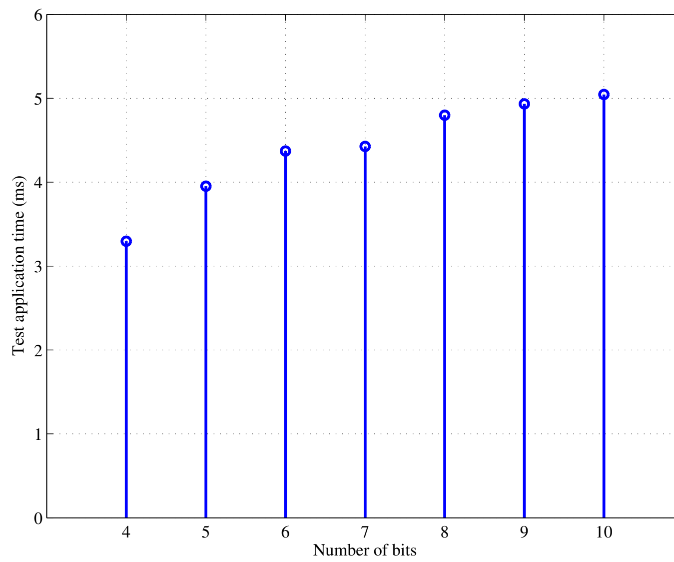


**Figure 4.17:** Test application time as a function of the number of bits used to encode the octree data structure. As can be checked, increasing the resolution does not implies a significant overhead in evaluating the octree.

**Table 4.1:** Metrics for 10° misalignment.

| | $\Delta X_i$ (V) | $\Delta Y_i$ (V) | | $\Delta X_i$ (V) | $\Delta Y_i$ (V) |
|---|---|---|---|---|---|
| **Point 1** | −0.096 | 0.038 | **Point 5** | −0.090 | −0.084 |
| **Point 2** | −0.192 | −0.051 | **Point 6** | −0.054 | −0.071 |
| **Point 3** | −0.152 | −0.099 | **Point 7** | −0.005 | 0.036 |
| **Point 4** | −0.106 | −0.088 | **Point 8** | −0.025 | 0.015 |

In order to validate the proposal, a particular study focusing on misalignments will be carried out. Here forth, the considered defects will be axis misalignment denoted by angle $\beta$ in Figure 4.3.

### 4.4.1 Misalignment Metric Evaluation

According to the metric definition given in equation (4.6) and considering the Lissajous compositions shown in Figure 4.18, the resulting metric values for the case $\beta = 10°$ are shown in Table 4.1.

As expected, some tangency points are more sensitive to misalignment defects than others. In the following section this fact will be quantified by means of the diagnosis efficiency function and the FOMs.

### 4.4.2 Misalignment Diagnosis Efficiency Evaluation

Taking into consideration previous definitions regarding metrics and diagnosis efficiency evaluation, such measures can be easily computed for the particular case of axis misalignment. Figure 4.19 shows the calibration curves considering misalignment defects. Calibration curves represent the locus of the tangency point for different misalignment levels ranging from $-20°$ to $+20°$.

Regarding the definition given in equation (4.7) for the diagnosis efficiency function, Figure 4.20 shows the resulting functions for each of the tangency points when $\beta$ is varied from $-20°$ to $+20°$. As can be observed, DE functions clearly reveals the sensitivity of the considered tangency points.

The defined FOMs values in equation (4.8) are shown in Table 4.2 and observed as a bar plot in Figure 4.21. The underlying conclusion is that, for instance, point 7 is not sensitive to the considered deviation because of its proximity to the supposed "rotation center" when the Lissajous trace deviates from its reference shape.

The performed diagnosis efficiency analysis allows parameter estimation knowing a priory the confidence on each of the tangency points. This study endows reliability and robustness to the presented diagnosis procedure as will be shown when discussing the experimental results.

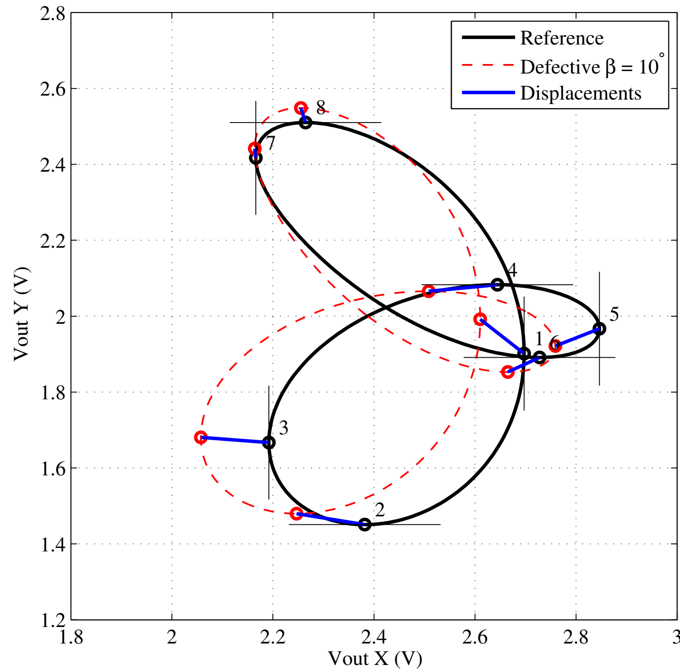


**Figure 4.18:** Lissajous trace information is replaced by its points of tangency with vertical and horizontal tangent lines. The metric is defined as the set of $(\Delta X_i, \Delta Y_i)$ displacements with respect to the reference curve.

**Table 4.2:** FOMs for diagnosis efficiency functions considering different misalignment levels.

| | **FOM** (mV/°) | | **FOM** (mV/°) |
|---|---|---|---|
| **Point 1** | 12.14 | **Point 5** | 9.82 |
| **Point 2** | 13.87 | **Point 6** | 6.73 |
| **Point 3** | 13.52 | **Point 7** | 2.65 |
| **Point 4** | 13.10 | **Point 8** | 4.23 |

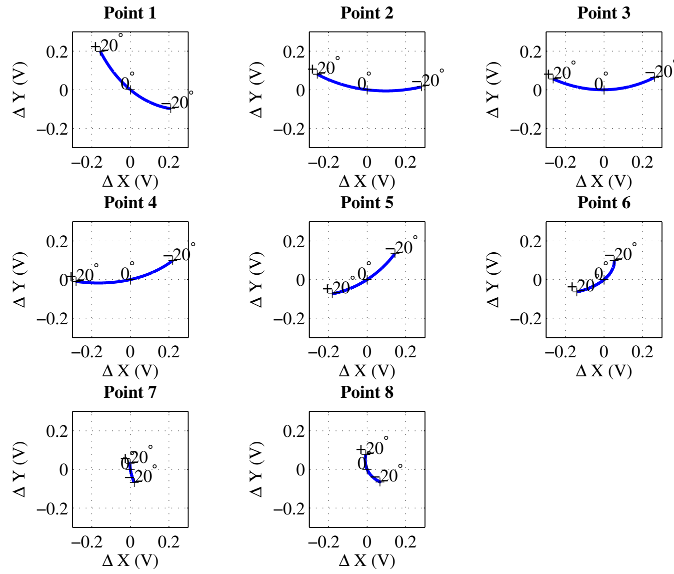


**Figure 4.19:** Calibration curves for $\beta$ angle ranging from $-20°$ to $+20°$. These curves allow the diagnosis procedure based on the experimental $(\Delta X_i, \Delta Y_i)$ metric values.

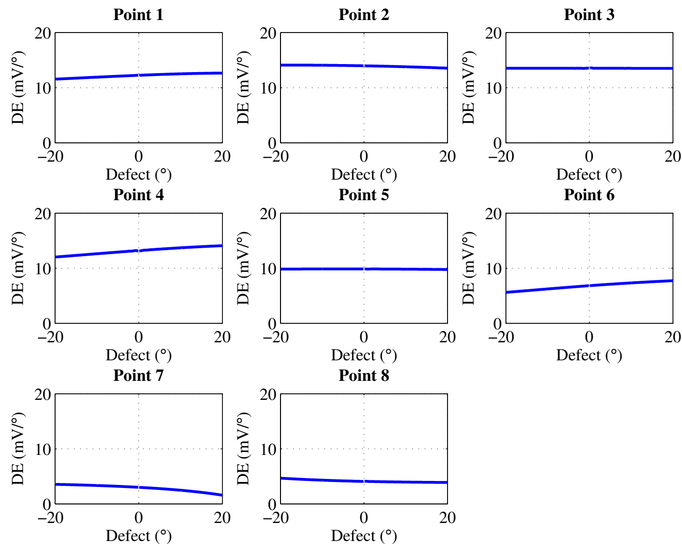


**Figure 4.20:** Diagnosis efficiency for each of the tangent points as a function of misalignment level. They are computed as the quotient $\mathrm{DE}(\beta) = \|(\Delta X, \Delta Y)\|/|\beta|$.

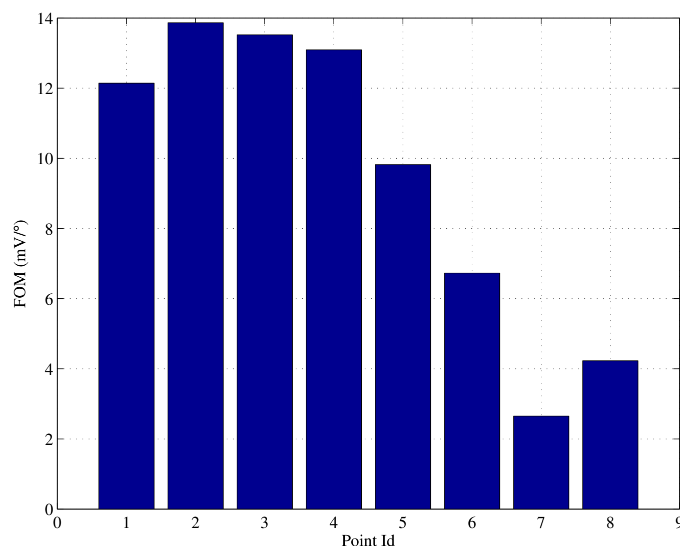


**Figure 4.21:** Diagnosis efficiency FOMs for each of the tangent points identified in the Lissajous curve. FOMs values correspond to the average of the plots shown in Figure 4.20 over the considered misalignment range.

### 4.4.3 Experimental Setup

An experimental test bench for diagnosing dual axis IC accelerometers has been constructed. A photography of the setup can be seen in Figure 4.22. The setup consists in a vertical spinning wheel in which the device under diagnosis is mounted. The spinning wheel has different positions to plug the device in, all of them adequately wired to capture device output signals. The spinning wheel is driven by a controlled DC motor which follows the sinusoidal profile indicated in equation (4.3).

The test bench is fully managed by a Microchip microcontroller which takes care of the captured signals transmission to the computer for further processing. The data is transferred using an IR serial transmission protocol using CRC error detector algorithm therefore assessing the robustness of the optical communication. The microcontroller also implements the angular velocity control scheme. The simulated and measured signals of such kinematics are shown in Figure 4.23.

Completing the test bench, a Matlab GUI has been developed as a front-end to the hardware setup for evaluating the experimental Lissajous traces. Data acquisition process, post-acquisition signal conditioning and diagnosis algorithms have been embedded in such software platform allowing a quick and efficient diagnosis procedure.

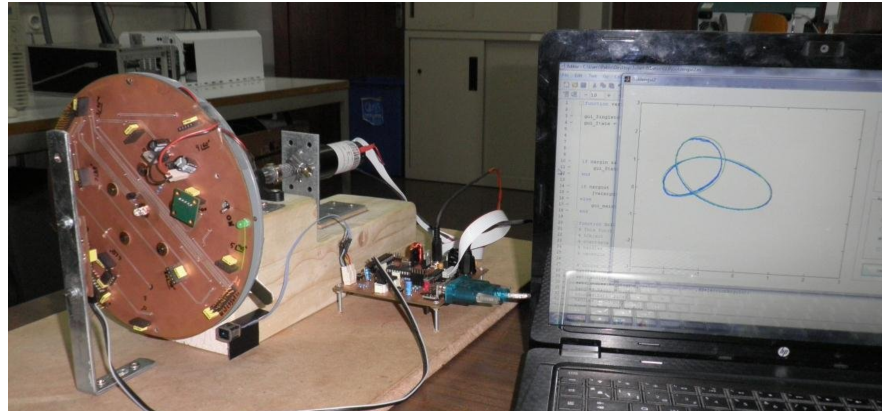

**Figure 4.22:** Photography of the experimental setup where the device is mounted. An IR serial transmission with CRC error detector allows the communication with the PC. The test bench is fully managed by a Microchip microcontroller.

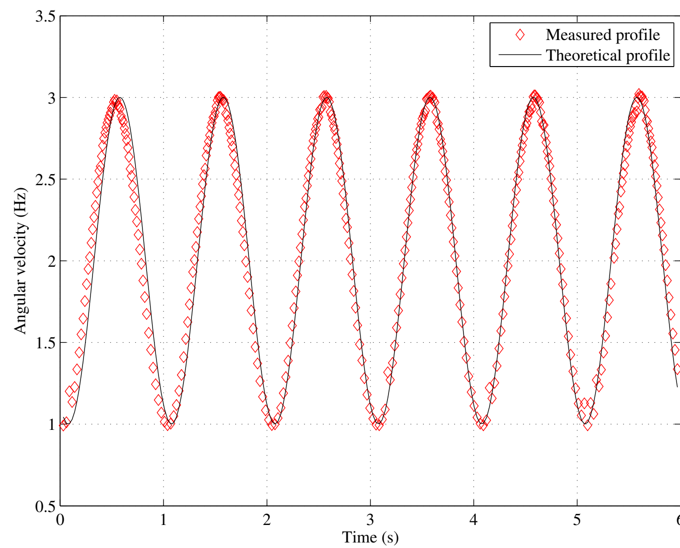


**Figure 4.23:** Simulated and measured angular velocity profiles at the motor shaft. The angular velocity has been imposed to $4\pi$ rad/s offset and $2\pi$ rad/s amplitude. The signal is 1 s periodic.

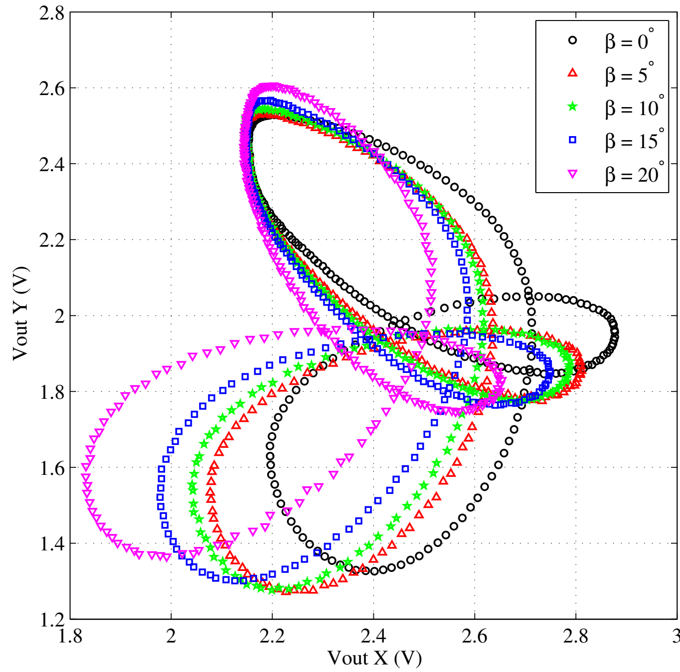


**Figure 4.24:** Experimental Lissajous compositions of a dual axis IC accelerometer for $\{0, 5, 10, 15, 20\}^\circ$ misalignment angles. Experimental traces match those shown in Figure 4.6.

### 4.4.4 Experimental Results

Using the previously described setup, experimental Lissajous compositions have been obtained using a commercial Analog Devices ADXL320 accelerometer. Figure 4.24 shows the resulting traces for different levels of misalignment ranging from 0° to 20° in steps of 5°. Experimental Lissajous traces match those simulated and displayed in Figure 4.6.

The diagnosis procedure consists on a post-acquisition signal conditioning phase and the misalignment level estimation phase. Firstly, using the developed hardware/-software platform, signals $x(t)$ and $y(t)$ composing the Lissajous trace are captured. Such acquisition is extended over a number of periods in order to smooth out the data (10 periods for the traces shown in Figure 4.24). The signals are filtered to attenuate noise levels and finally the extrema information is extracted using a robust peak detector algorithm coded ad hoc for this purpose. Metrics values for each of the tangent points are computed and processed.

Misalignment level estimation consists on the plotting of the obtained metrics in the calibration curves previously calculated as shown in Figure 4.19. Figure 4.25 shows the details of this operation for the first tangency point when a misalignment of

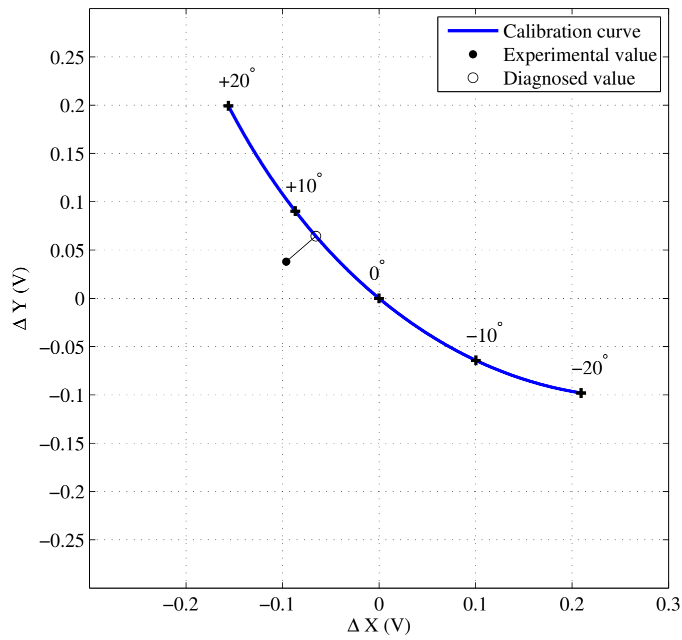


**Figure 4.25:** Detail on how the experimental diagnosis procedure is carried out for tangency point 1. The metrics for point 1 are plotted in its calibration curve (black dot). The closest point of the calibration curves determines the diagnosed value (black circle).

**Table 4.3:** Experimental diagnosis results and discrepancies.

| | $\beta$ (°) | $\varepsilon$ (%) | | $\beta$ (°) | $\varepsilon$ (%) |
|---|---|---|---|---|---|
| **Point 1** | 7.37 | −26.3 | **Point 5** | 11.62 | 16.2 |
| **Point 2** | 12.03 | 20.3 | **Point 6** | 10.72 | 7.2 |
| **Point 3** | 9.61 | −3.9 | **Point 7** | 17.31 | 73.1 |
| **Point 4** | 8.27 | −17.3 | **Point 8** | 5.17 | −48.3 |

$\beta = 10°$ is present. The diagnosed misalignment level by each of the 8 Lissajous tangency points is the corresponding calibration curve closest point. This is achieved by simply tracing straight lines departing from the experimental metrics normally crossing the calibration curve. The cross point becomes the diagnosed value. This procedure has been applied for all the tangency points as Table 4.3 reflects and Figure 4.26 depicts. Diagnosed $\beta$ angles and relative errors $\varepsilon$ with respect to the actual known deviation of 10° are reported.

Diagnosed misalignment values can be averaged to obtain the final diagnosis result but the former metric efficiency analysis dissuades such procedure. Figure 4.21 reveals not every tangency point presents the same efficiency to misalignment angle estimation. This fact can be corroborated in the obtained experimental results as shown in Figure 4.26, where less sensitive points yield to less accurate estimations. Because of that, a weighted average is taken as diagnosis result. The weights correspond to the FOMs values. The diagnosed misalignment level is 9.84° which is 1.5% far from the actual known value of $10° \pm 1°$.

The presented case study on diagnosing dual axis accelerometers under misalignment defects reflects the viability of the proposal. In this chapter, the methodology has been experimentally applied to misalignment diagnosis but it can be applied to any functional device parameter affected by parametric shifts due to process variations. The obtained diagnosis results are in good agreement with the actual known misalignment value.

## 4.5 Summary and Comments

Testing heterogeneous devices entangles a series of non trivial challenges which are even harder to cope than the ones existing in traditional CMOS circuits. This is so because of their inherently non electrical nature, which is the base of the transduction principle of such devices. For the particular case of MEMS accelerometers, a mechanical excitation stimuli is needed in order to emulate their in field operation. In this chapter, a method consisting on a variable speed vertical spinning wheel where the devices is mounted has been proposed. The method combines three types of accelerations, namely, gravity, centripetal, and tangential accelerations. Such a kinematic excitation provides a rich set of excitation which are sensed by the devices and therefore its response can be analyzed. Both outputs composition yields to the analog signature able to manifest and characterize parametric deviations.

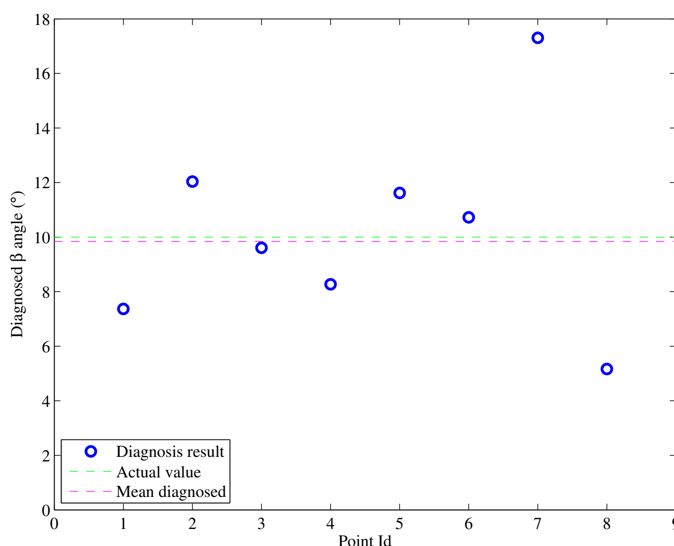


**Figure 4.26:** Diagnosed misalignments for each of the Lissajous tangency points and the weighted averaged diagnosis result. The actual misalignment angle is known to be $10^\circ \pm 1^\circ$.

Using the vertical spinning wheel excitation setup, a test strategy based on validating the DUT specifications using octrees has been proposed. The method relies on a training phase aiming the generation of the specifications compliance region using statistical samples. In this chapter, the method has been applied to test a dual axis accelerometer with promising results. The test is performed by simply checking in which octree region the candidate device lies on as explained in Chapter 3. The test is performed using data samples from a Lissajous composition sensitive to parametric defects. To such purpose, the octree representation has many benefits due to its sparse data structure what makes its evaluation time efficient as observed in the previous mixed-signal application. Several simulation have been conducted in order to evaluate the incurred test yield loss and test escapes of the testing proposal. The reported results indicate the digital octree encoding proposal is also applicable to test heterogeneous devices.

In this chapter, the Lissajous based characterization method has been used to diagnose the defect level for a single parameter. To this purpose, a metric between reference and faulty Lissajous curves has been defined. The computation of calibration curves allows the estimation of parametric shifts. The suitability of the tangency points for diagnosis purposes has been studied in terms of a diagnosis efficiency function. The method endows robustness to the diagnosis procedure against noisy measurements. The presented procedure has been applied to axes misalignment diagnosis reporting successful experimental results.

The next chapter focuses on two strategies able to improve the test efficiency as

well as serving as a technique for leveraging the analog test metrics using octrees. This subject is of significant importance in any testing procedure because it allows adapting the analog test program to customer specifications.

Chapter 5

# Improving Octree Tessellation Efficiency

In chapter 3 and chapter 4, a deterministic classification approach using octrees in the alternate measurement space has been proposed to test and diagnose analog and mixed-signal circuits as well as heterogeneous systems [65]. The technique relies on tessellating the space using binary trees. The procedure is referred as $2^n$-ary tree space tessellation or simply octree tessellation. There are some safety critical applications where the analog test metrics are gradually demanding tighter bounds and/or methods to increase the test yield, hence, the refinement of the test decision boundary without a significant test time penalty is an interesting topic of research. This chapter explores the possibilities of using multi-directional tessellations in the indirect measure space as well as multiple specification band guarding methodology is presented to optimize, achieve or leverage the targeted analog test metrics.

## 5.1 Octree Ensemble

When indirect measurements are used to validate circuit performances, lots of factors affect test metrics results. Test yield loss and specially test escapes are of major concern for the acceptance of such procedures in a production test program development. Regression and machine learning techniques have been widely accepted for such a purpose [10]. In this section, a novel multi-directional tessellation technique using octrees in the measure space is proposed.

### 5.1.1 Multi-Directional Tessellations in the Measurements Space

The use of $2^n$-ary trees to encode the indirect measure space has reported good results both in the field of mixed-signal testing [58] as well in the field of quality binning [65]. Using octree data structures to encode the space has the advantage of being able to represent arbitrary $n$-dimensional regions. Also, these data structures have the capability of controlling the encoding resolution by simply limiting the maximum octree depth. Such structures are easy to generate and evaluate due to their inherently sparse structure as shown in chapter 3. A $2^n$-ary tree can be stored as an array of pointers to memory locations what greatly facilitates its traversal from the root node to the leaf nodes, where the test decision is taken. Refer to chapter 3 for further details on generating and evaluating $2^n$-ary trees.

Any test method has certain probabilities of mispredicting some circuits, i.e. false positives and false negatives, also referred to test escapes and test yield loss. Reducing the misclassification levels is of crucial importance in high volume production testing of analog and mixed-signal circuits [6]. When using octrees, the training phase encodes the indirect measure space up to certain resolution which is actually limited by the available sample density. When a single octree is used to encode the space, the highly non linear test decision boundaries are difficult to resemble, specially in those regions where the boundary slopes differ from the orthogonal directions along which the octree is constructed. Because of that reason, the proposed novelty in this work is to consider several octrees to encode the space, each of them constructed along multiple directions. From here on, $N_{\text{octrees}}$ will indicate the number of octrees used in the space tessellation procedure. Each of the $N_{\text{octrees}}$ can be obtained by applying the octree encoding algorithm but using a different orthogonal base which results from a rotation of the original base. Without loss of generality, for the case of 2 dimensional spaces, each of the basis rotation angles are determined by,

$$\theta_k = \frac{\pi/2}{N_{\text{octrees}}} k, \quad k = 0, 1, 2, \ldots, N_{\text{octrees}} - 1 \tag{5.1}$$

For the sake of better clarifying the ideas, consider the synthetic data set shown in the top-left corner of Figure 5.1. This set of random points may represent pass/fail circuits in the indirect measure space. Consider that the desired number of octrees has been set to $N_{\text{octrees}} = 3$. Then, according to Equation (5.1), the rotation angles to be applied to the original base are $0°$, $30°$ and $60°$. The constructed octree data structures encoded with the previous angles are the other plots shown in Figure 5.1. A detailed view of the encoding can be observed in Figure 5.2.

The octree ensemble as a whole is better capable of resembling the non linearities of the test decision boundary as Figure 5.3 depicts. The two left-side figures correspond to a single octree while the two right-side figures correspond to a multi-directional tessellation with $N_{\text{octrees}} = 5$. This improvement in encoding accuracy results in a reduction of test escapes if the information provided by each of the $2^n$-ary trees is ANDed with respect to the clause of being a pass circuit. Consequently, the proposed production testing procedure evaluates all the considered octrees and labels the circuit

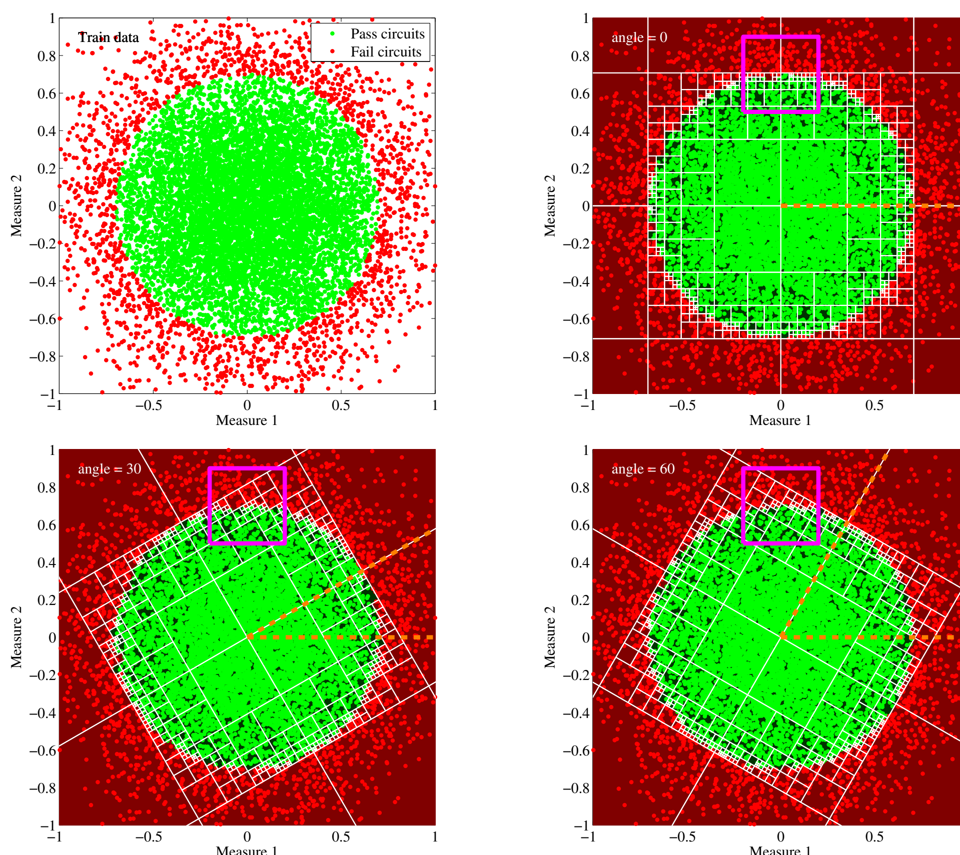


**Figure 5.1:** Example of a synthetic training set of indirect measurements and the corresponding octree encodings when $N_{\text{octrees}} = 3$. The considered rotation angles in this example are 0°, 30° and 60°. A zoomed version of these octrees can be seen in Figure 5.2.

as pass if and only if all the evaluated octrees have yielded to a pass test decision. This ensures the test escapes metric is reduced as the number of octrees used in the training phase is increased since the criterion gets more strict.

### 5.1.2 Test Application: Band-Pass Biquad Filter

In order to show the viability of the proposed multi-directional tessellation strategy, it has been applied to test a band-pass Biquad filter in the indirect measure space. Subsequent sections describe the CUT topology and its design and test specifications, the applied excitation as well as the considered set of indirect measurements in order to carry out the test procedure.

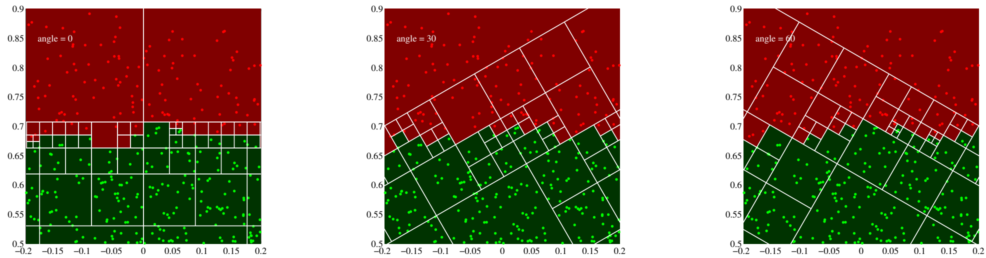


**Figure 5.2:** Detail of the three rotated octrees depicted in Figure 5.1. The overlap of these trees define the test acceptance and rejection regions for the synthetic case with $N_{\text{octrees}} = 3$.

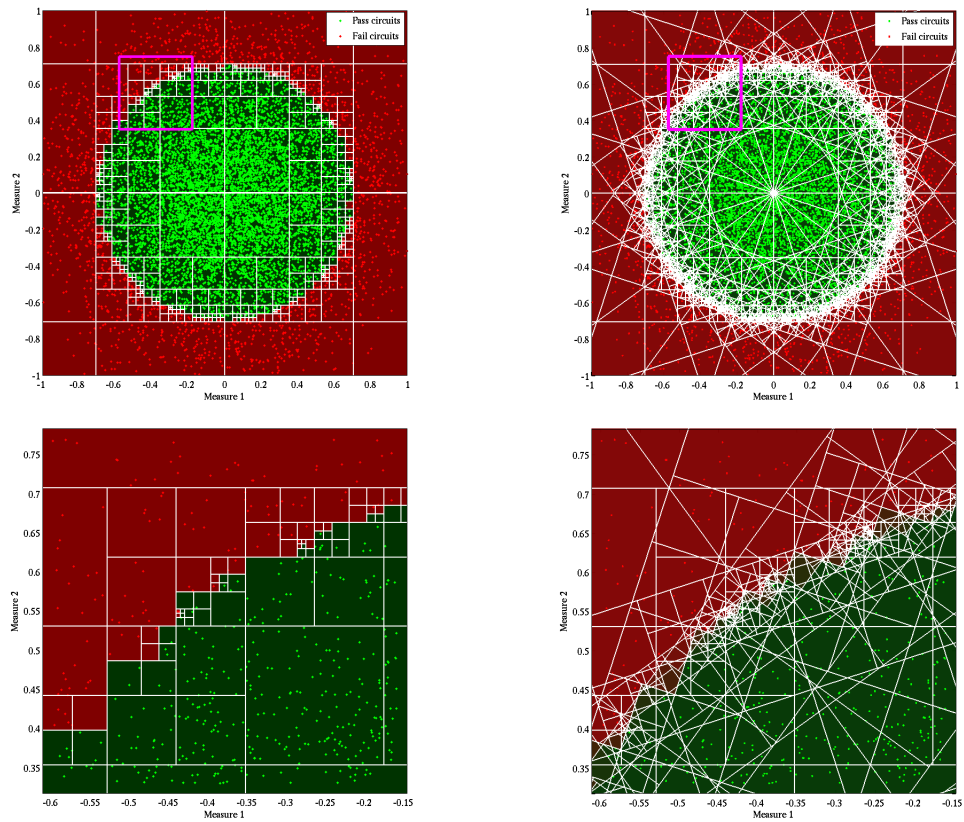


**Figure 5.3:** Example of multi-directional tessellation with $N_{\text{octrees}} = 1$ (left) and $N_{\text{octrees}} = 5$ (right) using the synthetic data set shown in Figure 5.1. As can be appreciated, when using 5 octrees, the test acceptance/rejection regions are better encoded.

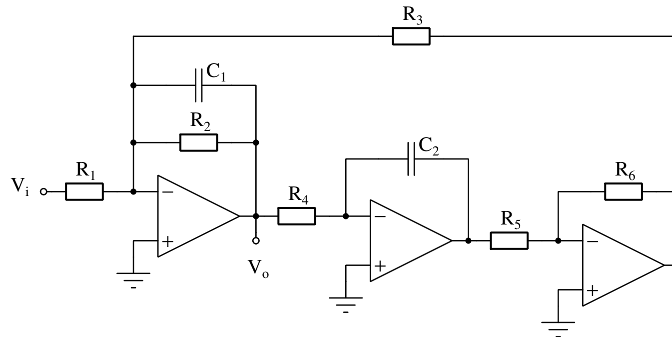


**Figure 5.4:** Schematic of the Tow-Thomas Biquad filter used as case study [87]. The node of interest corresponds to the band-pass output of the filter. The filter is composed of three operational amplifiers and passive components.

**Table 5.1:** Band-pass Biquad filter specifications and test limits.

| Specification | Symbol | Value | Units | Test Limits |
|---|---|---|---|---|
| Center frequency | $f_0$ | 1.00 | MHz | ±5% |
| Bandwidth (−3 dB) | BW | 700 | kHz | |
| Quality factor | $Q$ | 1.43 | – | ±4% |
| Pass-band gain | $G_{\mathrm{BP}}$ | 2.00 | – | ±3% |

#### Filter Design and Test Specifications

The chosen topology is a Tow-Thomas Biquad filter [87] in which the node of interest is the band-pass output, as depicted in Figure 5.4. As a proof of concept, circuit components have been considered to vary according to independent normal distributions. Filter design and test specifications are listed in Table 5.1. The filter has been tuned at 1 MHz with 700 kHz bandwidth. The nominal gain of the filter at 1 MHz is 2 V/V. Test specifications are as follow. Center frequency has to be within ±5%, quality factor has to be within ±4% and gain has to be within ±3%. All the given tolerance percentages refer to the corresponding nominal value of the considered specification. In order to tag a circuit as pass it must not violate any of the aforementioned test specifications.

According to the parametric variations affecting each of the components of the Biquad filter, a batch of Monte Carlo simulation have been carried out, including transient and AC analyses. Figure 5.5 shows a few magnitude Bode plots for the considered band-pass output of the filter. The nominal transfer function is plotted using a thick black trace while the the green and red traces correspond to pass and fail circuits, respectively.

The chosen excitation for the filter is a multitone signal composed of 3 different tones, namely, the central frequency of the filter (1 MHz), one octave higher (2 MHz) and

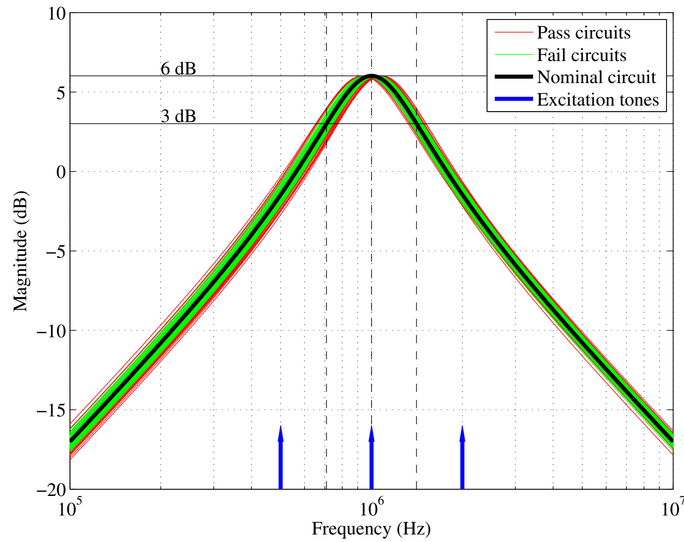


**Figure 5.5:** Magnitude Bode diagrams of the band-pass Biquad filter used as case study. Green traces correspond to circuits fulfilling the specifications while red traces correspond to circuits violating, at least, one specification.

one octave lower (500 kHz). Such a stimulus has been proven to be effective, both in terms of fault coverage and test application time [65, 68]. The three tones forming the input stimulus are indicated in Figure 5.5 as blue arrows. Figure 5.6 shows one period of the sinusoidal steady state response of the filter. The black dashed trace corresponds to the applied multitone stimulus while the solid black trace corresponds to the nominal filter response to the multitone input stimulus. The chronogram also shows some Monte Carlo transient responses of the Biquad filter using green traces for circuits fulfilling the specifications listed in Table 5.1 and red traces for circuits violating them.

### Alternate Measurements Space

As introduced earlier, this work is framed in the context of indirect or alternate test. Based on previous works from the authors [65, 68], a set of indirect measurements have been selected in order to perform the test. The chronogram shown in Figure 5.6 depicts the two indirect measurements considered for every simulated circuit, indicated with blue and magenta circles. These measurements correspond to the positive and negative peaks of the transient response of the filter when it is excited using the aforesaid multitone signal.

The test of the considered band-pass Biquad filter entirely relies on the presented set of indirect measurements. Figure 5.7 shows a scatter plot of $10^4$ measurements forming the so called indirect measure space. As usual, green and red points cor-

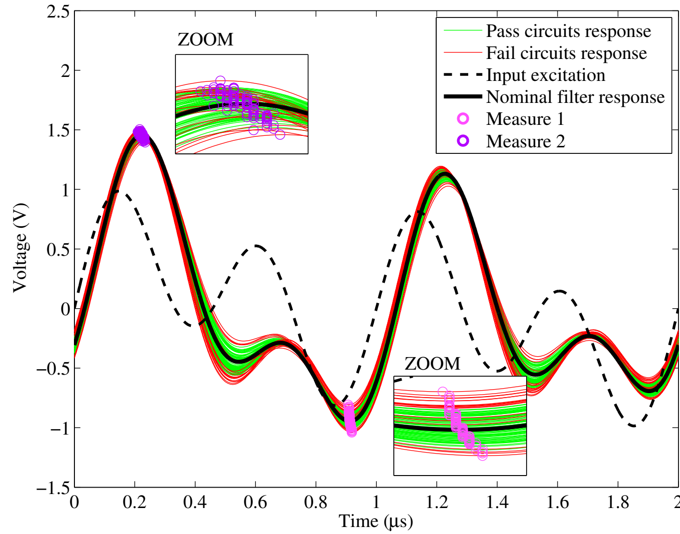


**Figure 5.6:** Response of the band-pass Biquad filter when is excited with a multitone signal [68]. The indirect measurements used in this example correspond to the peak values of the sinusoidal steady state response.

respond to circuits accomplishing and violating the specifications, respectively. The application of the proposed multi-directional tessellation technique is carried out in the indirect measure space as the next section details.

## 5.1.3 Simulation Results

This section reports the simulation results obtained when the proposed multi-directional tessellation technique introduced earlier is applied to the Biquad filter case study. The following sections discuss the results for the training and testing phases.

### Statistical Training Phase

Using the data shown in Figure 5.7, the indirect measurement space has been encoded using several rotated octrees along multiple directions. For instance, the resulting octree for $N_{\text{octrees}} = 1$ is depicted in Figure 5.8. As can be observed, finer octree cells concentrate at the surroundings of the test decision boundary. Despite of this fact, misclassification errors occur due to the difficulties of straight and orthogonal edges to adapt to the non linear test decision boundary.

The proposed method of using multi-directional octree encodings provides better adaption to arbitrary test decision boundaries and the noticeable benefit of not requiring to include more circuit samples to the training set. The method is able to keep reducing the false positive circuits as the number of included octrees is increased.

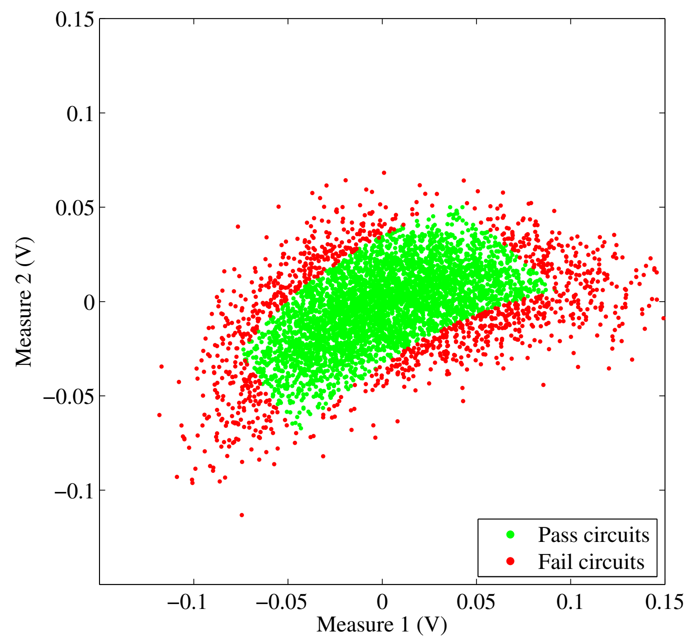


**Figure 5.7:** Indirect measure space showing $10^4$ Monte Carlo circuit samples before applying the proposed multi-directional octree encoding technique. Green and red points correspond to pass and fail circuits, respectively.

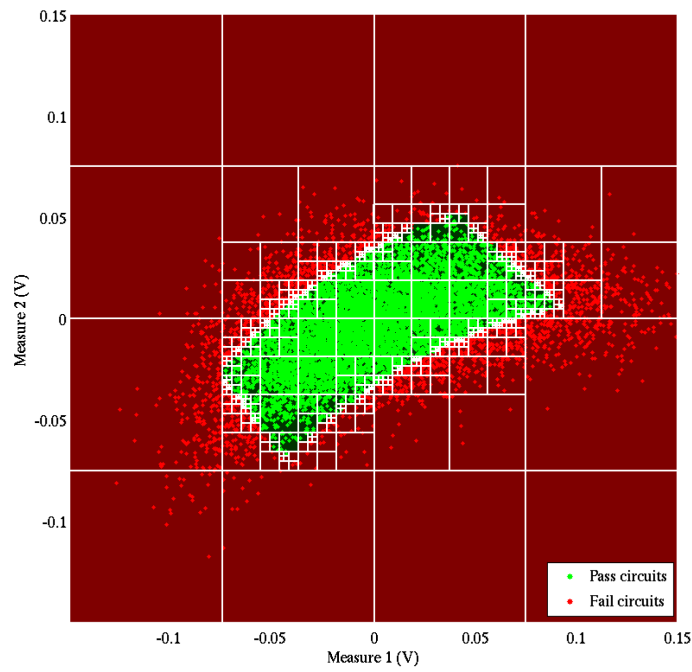


**Figure 5.8:** Indirect measure space encoded using a single octree. Despite finer octree cells concentrate at the test decision boundary, test errors may occur due to the adaption difficulties when using a single tree.

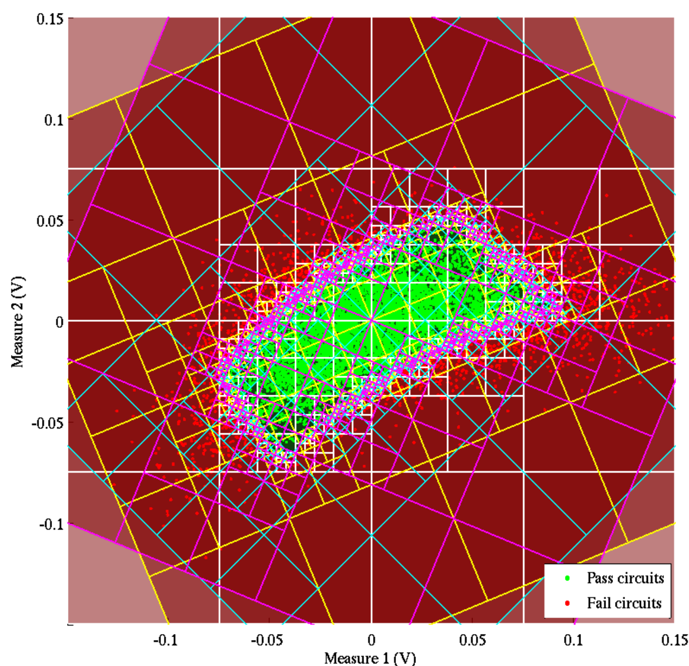


**Figure 5.9:** Indirect measure space encoded using 4 octrees. The rotation angles of the trees are 0° (white), 22.5° (yellow), 45° (cyan) and 67.5° (magenta). The combination of these 4 encodings along multiple directions, i.e. tree overlapping, allows a much finer resolution to be achieved.

For example, Figure 5.9 shows the case when $N_{\text{octrees}} = 4$. As can be seen, the test decision boundary adaption is better than the one shown in Figure 5.8. The octrees in this figure have been rotated 0°, 22.5°, 45° and 67.5°, which correspond to the tessellations drawn in white, yellow, cyan and magenta, respectively. In the next section, the benefits of the approach will be clearer.

### Production Testing Phase

Once the training phase has been applied, i.e. all the octrees along the selected directions have been properly trained, the actual production testing phase can be engaged. The test procedure uses a strict criterion aiming to reduce false positive test outcomes as previously outlined. The procedure evaluates all the considered octrees and labels the circuit as pass if and only if all the evaluated octrees have yielded to a pass test decision. For further details on octree evaluation, refer to [65]. Such a test decision procedure guarantees the test escapes metric is reduced as the number of octrees used in the training phase is increased, i.e. the criterion gets more and more strict.

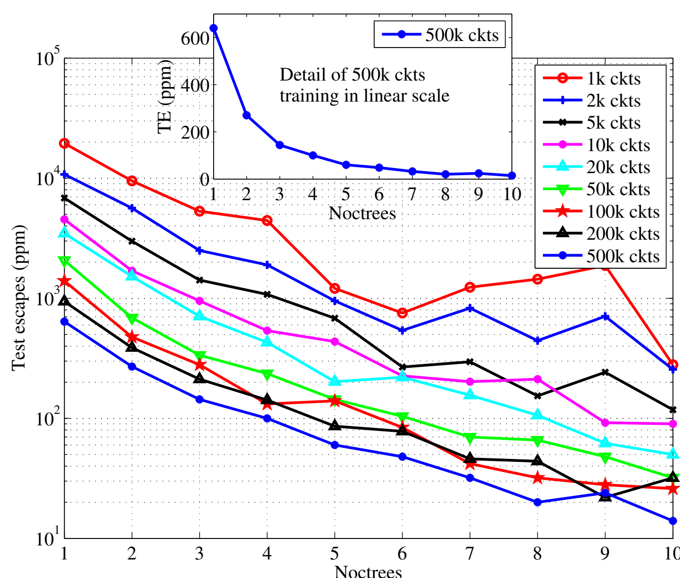


**Figure 5.10:** Incurred test escapes metric resulting from the application of the proposed multi-directional tessellation technique as a function of the number of octrees used for several training set sizes. The test escapes metric is reduced as the number of the tessellating octrees is increased.

In order to achieve a fair evaluation of the proposed technique, 500k new Monte Carlo circuits have been generated and tested using a varying number of octrees as well as training set sizes. Figure 5.10 shows the obtained results for the band-pass Biquad filter used as test vehicle. The plot shows the test escapes metric (in parts per million) as a function of the number of octrees considered in the former training phase, ranging from 1 to 10. The different traces correspond to different training set sizes ranging from 1k circuits to 500k circuits. As the number of circuits used in the training phase increases, the number of false positives decreases. Likewise, the number of test escapes is greatly reduced as the number of octrees used in the tessellation rise up. The plot reveals the test escapes can be considerably reduced down to a few tenths of ppm. As the detailed plot of the 500k circuits trace suggests, the test escape metric asymptotically approaches to zero. On the contrary, Figure 5.11 shows the incurred test yield loss metric as a function of the same parameters shown for the test escapes metric. As expected, the yield loss metric increases as the number of the tessellations used in the testing procedure increases.

In favor of better understand the benefits of the proposed multi-directional tessellation technique, the average test escape reduction factor and average test yield loss increasing factor have been computed with respect to the reference case using a single octree, i.e. along 2 directions. Figure 5.12 shows such factors as a function of the number of octrees used in the tessellation together with the corresponding standard deviation intervals. As can be observed, the average test escape reduction factor is

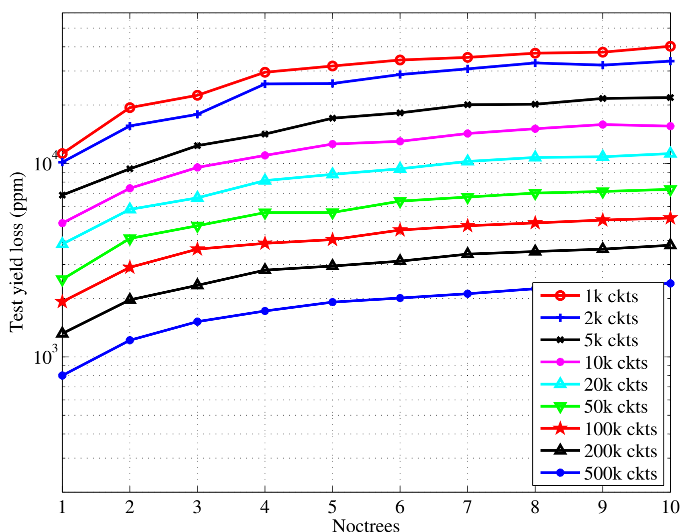


**Figure 5.11:** Incurred test yield loss metric resulting from the application of the proposed multi-directional tessellation technique as a function of the number of octrees used for several training set sizes. The test yield loss metric increases as the number of the tessellating octrees is increased.

greatly increased as the number of octrees is increased. When using 10 octrees, the false positives get a reduction of 50 times in average as compared to the case with $N_{\text{octrees}} = 1$. Conversely, the test yield loss metric is increased by a factor of 3 times in average for $N_{\text{octrees}} = 10$. The proposed multi-directional methodology is able to reduce the test escape metric at the expense of slightly increasing the test yield loss metric.

#### Performance Evaluation

In order to provide some performance comparison and overhead of the proposed multi-directional tessellation strategy, the computation times of the training and testing processes have been annotated. The machine used in the benchmarking is an 8 core Intel Pentium i7 processor at 3.4 GHz with 16 Gbytes of RAM. The employed electrical simulator is Synopsis HSPICE version 2010.03 without exploiting its multiprocessing capabilities, i.e. all the simulations have been carried out using a single processor core. The algorithms for octree encoding and evaluation have been ad hoc implemented in ANSI C using a recursive data structure as reported in [88], while the postprocessing has been done using MATLAB R2012a.

Table 5.2 shows the results of the performance and overhead evaluation. The absolute times, as well as the incurred overhead with respect to a single octree encoding, have been tabulated. The training phase performance has been evaluated using 1k and 500k circuits. The data within the *Total Time* column is divided into two fields. The

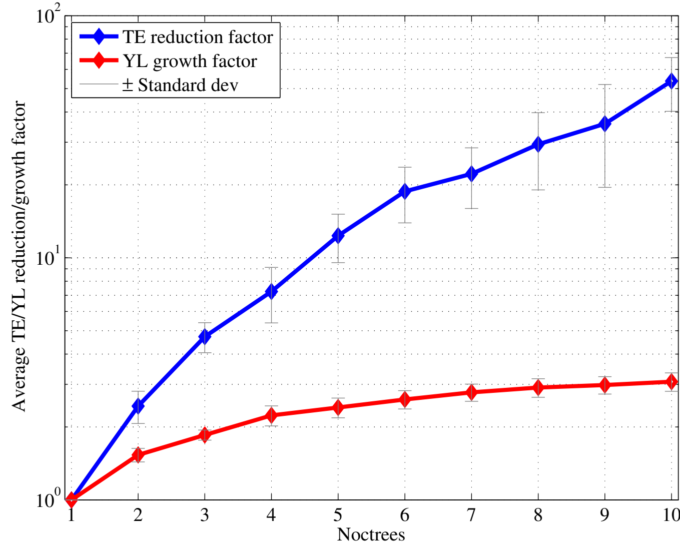


**Figure 5.12:** Average reduction and growth factors for the incurred false positive and false negatives test outcomes with respect to a single octree encoding as a function of the number of octrees used throughout the tessellation process.

value before the "+" sign correspond to electrical simulator times while the value after it corresponds to the actual multi-directional encoding process. The immediate conclusion regarding the training phase is that the incurred overhead of using $N_{\text{octrees}}$ along multiple directions is negligible. The bottleneck of the training phase is, in this case, the required simulation times, which would become even longer if the complexity of the CUT increases. The incurred overheads for the testing phase linearly increase with the number of considered octrees. Regardless of this fact, the testing times are small enough to consider octree evaluation reasonably time efficient. Note that the required time to evaluate a single circuit is below 1 $\mu$s. A performance comparison with support vector machines can be found in Chapter 3 as well as in reference [65].

### Comparison with Band-Guarding

With the aim of providing a comparison with other misclassification control technique, the proposed method has been compared against the band-guarding technique used in [88] which will be the object of the second part of current chapter. Despite targeting the same goal, both methods differ considerably. The following methodology has been carried out in order to achieve the comparison. First, certain test escape target metric has been fixed. Using the data provided in the test escapes plots (see Figure 5.10) the adequate number of octrees to be used in order to guarantee the test escape target has been determined. Similar procedure has been carried out for the band-guarding method but in this case, to determine the adequate band-guarding factor to guarantee the required test escape level. Then, the incurred test yield loss

**Table 5.2:** Performance and overhead evaluation.

| | $N_{\text{octrees}}$ | Total Time | Overhead |
|---|---|---|---|
| **Train 1k** | 1 | 12s + 3ms | REF |
| | 2 | 12s + 6ms | 0.025% |
| | 5 | 12s + 15ms | 0.100% |
| | 10 | 12s + 30ms | 0.225% |
| **Train 500k** | 1 | 1h 40m + 0.54s | REF |
| | 2 | 1h 40m + 1.09s | 0.009% |
| | 5 | 1h 40m + 2.72s | 0.036% |
| | 10 | 1h 40m + 5.44s | 0.082% |
| **Test 500k** | 1 | 0.401s | REF |
| | 2 | 0.802s | 100% |
| | 5 | 2.005s | 400% |
| | 10 | 4.010s | 900% |

metric can be derived from the data shown in Figure 5.11. The results of the comparison can be observed in Figure 5.13 in which the incurred test yield loss is plotted as a function of the target test escape metric for both methods. The discrete nature of the proposed multi-directional tessellation technique makes the plots to look like steps, but being able to keep test yield loss metrics below those resulting from the band-guarding methodology.

## 5.2 Multiple Specification Band Guarding

A multiple specification band guarding methodology is presented to optimize or achieve the targeted analog test metrics [89]. As developed in Chapter 3,the indirect test method using octrees comprises two phases, namely, the training phase and the testing phase. In the training phase, a representative amount of circuit samples is generated and the acceptance/rejection regions are encoded using octrees in the indirect measurement space. In the former phase, the proposed band guarding strategy is applied by tuning a set of factors which modify the test specifications and therefore the number of misclassified circuits. The latter phase corresponds to the actual production testing of the incoming ICs using the previously generated octree data structure. Octree encoded pass/fail regions facilitate an efficient and fast circuit clustering due to the inherent sparsity of such data structures [58].

The procedure of testing analog and mixed-signal is just a classification of a candidate circuit into pass/fail clusters. Such classification is usually performed in the *specifications space* or *performance space* in which circuit specifications/performances are directly measured. This procedure is referred as the well known *specification based test* as opposed to the *indirect test* or *alternate test*. Indirect testing aims

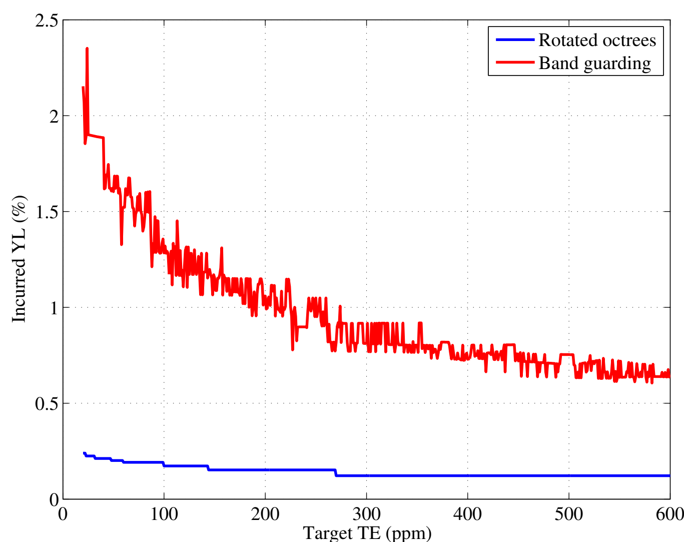


**Figure 5.13:** Incurred test yield loss metric as a function of a given test escape target for the proposed multi-directional tessellation using octrees and the band-guarding method used in [88].

to battle against the drawbacks of specification based test such as the need for high end technical resources or the difficulties in validating every single test specification. The indirect test procedure used throughout this chapter is formed by two phases, namely, the training phase and the testing phase as introduced in chapter 3. The former phase is in charge of generating the circuit data and encode them using an octree data structure which will be used in the latter phase to test the freshly fabricated ICs.

### 5.2.1 Multiple Specification Band Guarding in the Indirect Measurements Space

Test specification band guarding can be used to improve test outcomes depending on the established test escapes and test yield loss trade offs or targets. The underlying idea is to create a series of band guards along the test decision boundaries. The actual purpose of these guards is to displace the test limits with the objective of bypassing the mispredictions or uncertainties carried out by the actual test procedure, therefore achieving less misclassified circuits [89].

The proposed band guarding procedure is performed in the indirect measurement space using a set of factors $r_1, r_2, \ldots, r_p$, which are in charge of shrinking or enlarging the test specification cube and so the test decision boundary in the indirect measurement space. From now on, these factors will be referred as *band guarding factors*. Each of the factors is responsible of modifying one or more test specifications

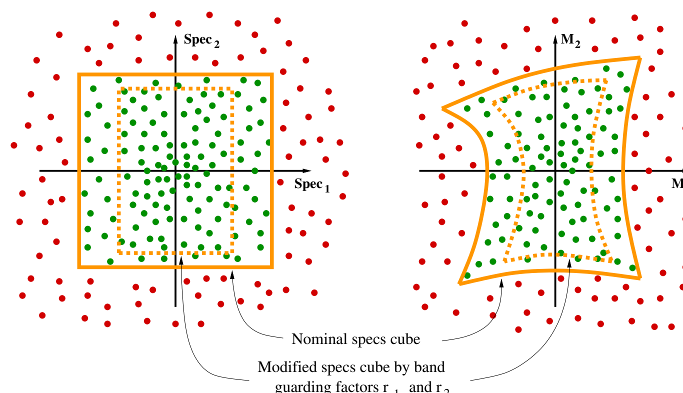


**Figure 5.14:** Example of multiple specification band guarding in the specifications space and the resulting non linear mapping in the indirect measurement space. The applied shrink helps to reduce test escapes metric.

as sketched in Figure 5.14.

If all the band guarding factors are less than 1, the acceptance region will be shrunk, what immediately translates into tighter test specifications. This implies that the probability of classifying an actual fail circuit into the pass cluster will be reduced, i.e. the test escape metric will be reduced. On the contrary, if all the band guarding factors are greater than 1, the acceptance region will be enlarged, what implies the relaxation of tests specifications and therefore the probability of classifying an actual pass circuit into the fail cluster gets reduced, i.e. the test yield loss metric will be reduced. Of course, according to the desired trade off between the test efficiency metrics or the needs for tightening or relaxing any of the circuit performances, a whole space of possibilities is available for the test engineer. It is worth to note that the case $r_1 = r_2 = \cdots = r_p = 1$ results in a test scenario with no band guarding at all.

As a proof of concept, two band guarding factors are in charge of tuning the test specifications of a continuous time filter. The following section describes the case study and explains in which manner the test specifications are varied according to each of the factors.

### 5.2.2 Test Application: Band-Pass Butterworth Filter

#### Filter Design and Test Specifications

In order to demonstrate the viability of the proposed multiple specification band guarding technique, it has been applied to test a 6th order band-pass Butterworth filter in the indirect measurement space [90]. The schematic of the CUT is shown in Figure 5.15. Filter's topology corresponds to a ladder filter realized with operational transconductance amplifiers (OTA) implementing the inductances and MiM

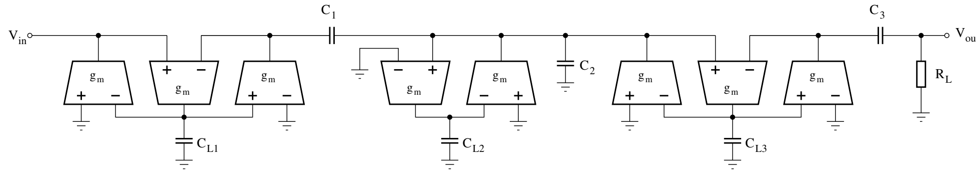


**Figure 5.15:** Schematic of the 6th order band-pass Butterworth filter used as a case study. The filter has been designed and simulated using an industrial 65 nm technology from ST-Microelectronics. Filter topology corresponds to a ladder filter implemented with operational transconductance amplifiers (OTA).

**Table 5.3:** Butterworth filter components values.

| Comp | Value | Units | Comp | Value | Units |
|---|---|---|---|---|---|
| $C_1$ | 2.12 | pF | $C_{L1}$ | 74.94 | pF |
| $C_2$ | 4.24 | pF | $C_{L2}$ | 37.47 | pF |
| $C_3$ | 6.37 | pF | $C_{L3}$ | 24.98 | pF |
| $g_m$ | 79.24 | $\mu$A/V | $R_L$ | 50.00 | kΩ |

capacitors. The Butterworth filter has been designed in an industrial 65 nm N-well bulk CMOS technology from ST-Microelectronics [77]. Filter design components are listed in Table 5.3.

Filter design specifications are listed in Table 5.4. As can be appreciated, the Butterworth band-pass filter has been tuned at 1 MHz with a 1 MHz bandwidth and 0 dB gain. The $Q$-factor resulting for such combination is $Q = 1$, what ensures a wide flat band in the pass-band. A series of test specifications have been imposed over the filter as listed in Table 5.5. The test limits have been defined using boxes in the magnitude Bode plot as Figure 5.16 depicts in blue dashed lines. As can be observed, test specifications regard to both bandwidth and gain, what makes the testing of the filter a non trivial task. The filter has been simulated using HSPICE and the 65 nm technology models from ST-Microelectronics. Figure 5.16 shows some Monte Carlo simulations when the statistical corner (statcrolles) of the process design kit is used.

The band guarding factors are referred to $r_1$ and $r_2$. The way the band guarding

**Table 5.4:** Band-pass Butterworth filter specifications.

| Specification | Symbol | Value | Units |
|---|---|---|---|
| Center frequency | $f_0$ | 1.0 | MHz |
| Bandwidth (−3 dB) | BW | 1.0 | MHz |
| Quality factor | $Q$ | 1.0 | |
| Pass-band gain | $G_{\text{BP}}$ | 0.0 | dB |

**Table 5.5:** Butterworth filter test limits.

| Specification | Test Spec | Units |
|---|---|---|
| Minimum pass-band bandwidth | 745.6 | kHz |
| Maximum stop-band bandwidth | 11.0 | MHz |
| Maximum pass-band gain | 1.2 | dB |
| Minimum pass-band gain | −3.0 | dB |
| Minimum stop-band attenuation | −59.0 | dB |

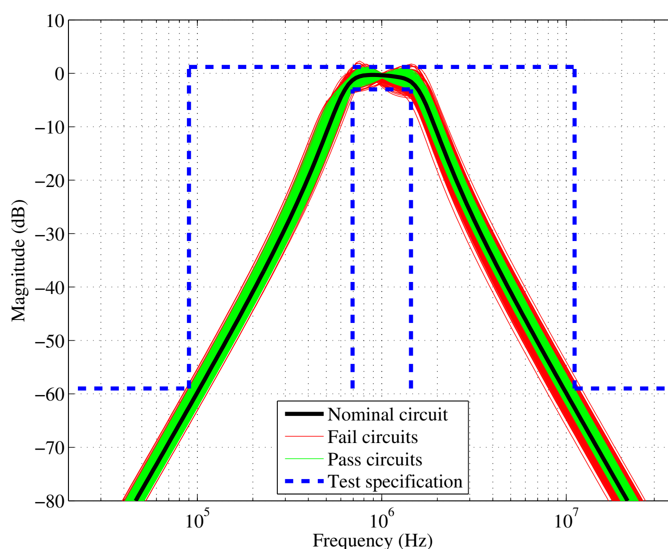


**Figure 5.16:** Magnitude Bode diagrams obtained by Monte Carlo simulations using technology statistical corner (statcrolles). The test limits listed in Table 5.5 are also drawn in blue dashed line.

factors control the test limits is as follows. Factor $r_1$ contributes to the maximum and minimum allowable gains in the pass-band of the filter. If $r_1 > 1$ means that the two upper gain lines move away from the 0 dB line. On the contrary, factor $r_2$ contributes to the bandwidth of the filter. If $r_2 > 1$, the test specification related to filter's bandwidth is relaxed, what implies the band-pass corner frequencies get closer to $f_0$.

### Alternate Measurements Space

The presented 6th order band-pass Butterworth filter has been excited with a multitone stimulus. The input signal is composed of 3 tones corresponding to filter's center frequency, an octave higher and an octave lower. Such stimulus has been

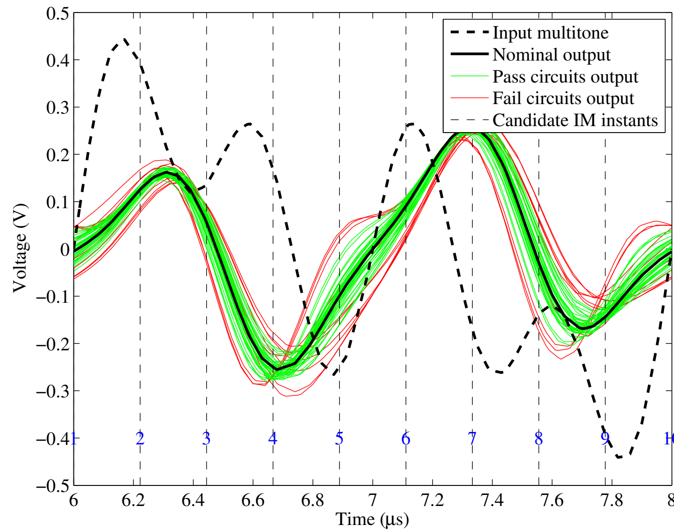


**Figure 5.17:** Response of the Butterworth filter when it is excited with a multitone signal. The candidate indirect measurements correspond to equally spaced samples of filter's output.

proven to be effective for analog and mixed-signal testing purposes since it concentrates in a single stimulus the excitation of three single tones, making the whole process faster [65, 67–69]. Figure 5.17 shows the applied multitone input signal and the corresponding output responses for a few Monte Carlo samples. Green traces correspond to circuits fulfilling the test specifications listed in Table 5.5 while red traces correspond to circuits violating, at least, one of the test specifications.

The candidate set of indirect measurements will be formed by several samples of filter's response to the aforementioned multitone input signal. The samples are taken at evenly spaced time intervals as indicated with the dashed vertical lines in Figure 5.17. Such procedure yields to a set of 10 candidate indirect measurements from which a final subset needs to be selected. As intuition suggests, a good subset of indirect measurements has to satisfy two requirements. The measurements need to reflect circuit's performance variability and should not be redundant to avoid incurring in extra test costs.

Having a look at the Bode diagrams shown in Figure 5.16 and the steady state transient responses depicted in Figure 5.17, it is clear that the candidate measurements are correlated with circuit performances. Regarding the second condition, Kendall's Tau rank correlation coefficient is used to quantify the correlation level among the final subset of indirect measurements [81]. Since the aim is to reduce redundant information, the pair presenting the lowest Kendall's Tau correlation is included in the target subset.

Table 5.6 shows the absolute values of Kendall's Tau rank correlation coefficient

**Table 5.6:** Kendall's Tau rank correlation coefficient between candidate indirect measurement pairs.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1.000 | | | | | | | | | |
| 2 | 0.688 | 1.000 | | | | | | | | |
| 3 | 0.910 | 0.620 | 1.000 | | | | | | | |
| 4 | 0.835 | 0.576 | 0.830 | 1.000 | | | | | | |
| 5 | 0.658 | 0.626 | 0.645 | 0.501 | 1.000 | | | | | |
| 6 | 0.766 | 0.712 | 0.755 | 0.633 | 0.812 | 1.000 | | | | |
| 7 | 0.331 | 0.272 | 0.313 | 0.171 | 0.587 | 0.425 | 1.000 | | | |
| 8 | 0.705 | 0.706 | 0.689 | 0.550 | 0.916 | 0.865 | 0.520 | 1.000 | | |
| 9 | 0.240 | 0.033 | 0.256 | 0.308 | 0.053 | **0.015** | 0.130 | 0.046 | 1.000 | |
| 10 | 0.981 | 0.689 | 0.912 | 0.835 | 0.658 | 0.768 | 0.331 | 0.706 | 0.240 | 1.000 |

among the 10 candidate indirect measurements under consideration. The pair of measurements presenting the lowest correlation is the one formed by measurements 9 and 6 with a correlation value of 0.015. Here forth, these measurements will define the indirect measurement space for the presented Butterworth filter.

It is worth to note that for the present case study two indirect measurements are enough to define the test decision boundary. If two measurements were not enough, Kendall's Tau rank correlation coefficient is also useful for such scenario [65]. The underlying idea is to add indirect measurements to the final subset while keeping the sum of all their Kendall's Tau the smallest possible. This is a general procedure based on a similar concept in order to make an appropriate selection when more than two measurements are needed.

### 5.2.3 Simulation Results

#### Statistical Training Phase

Taking into account the previously selected subset of indirect measurements, $10^4$ Monte Carlo samples of the Butterworth filter have been simulated resulting in the samples shown in Figure **??**. The application of the octree encoding algorithm results in the octree depicted in Figure 5.18. As can observed the octree gets finer exactly where it is needed, i.e. in the surroundings of the test decision boundary. The resulting octree is 12 levels deep.

As shown in Chapter 3, octree based classifiers present considerable benefits in terms of test application time. It is worth to take a look at the levels distribution of the octree cells forming the octree data structure. Figure 5.19 shows such distribution for the octree depicted in Figure 5.18. As can be stated, the vast majority of octree cells concentrate at levels 7, 8, and 9 despite the maximum level is 12. This fact implies a considerable advantage in terms of test application time since most of the circuits will be resolved without the need of traversing the tree down to its maximum level

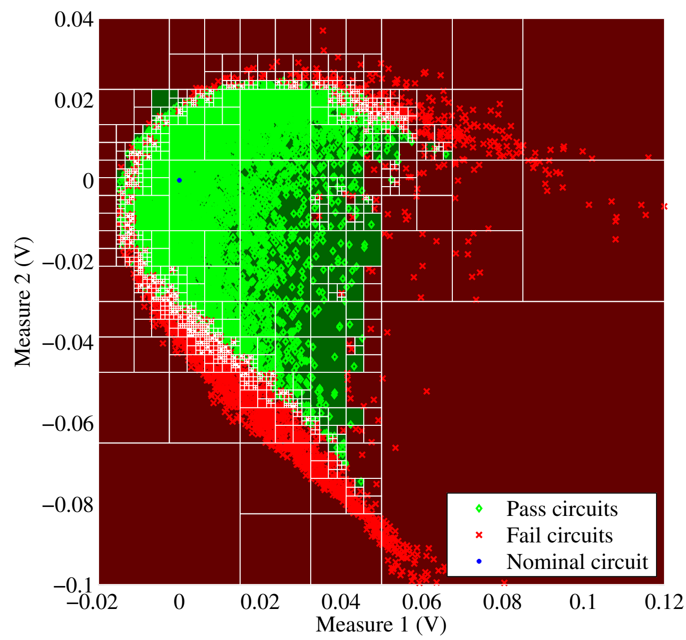


**Figure 5.18:** Resulting octree after the application of the training phase to the set of $10^4$ Butterworth circuit samples shown in Figure ??. As can be observed, high octree levels concentrate in the test decision boundary.

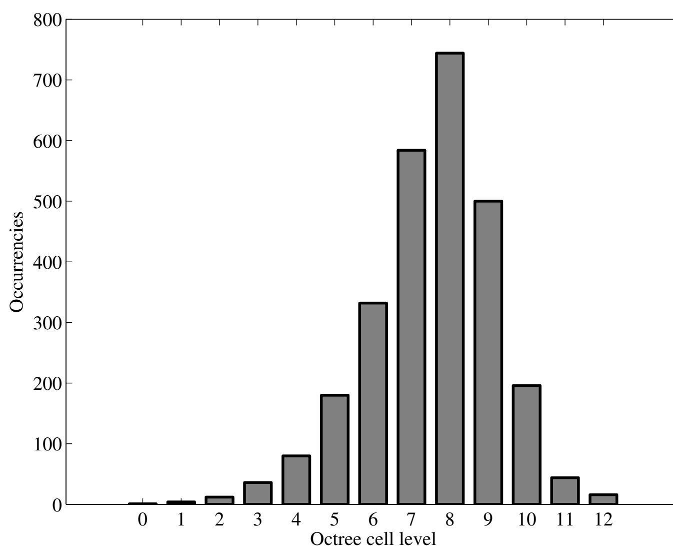


**Figure 5.19:** Levels distribution for the octree shown in Figure 5.18. Despite the maximum level is 12, the vast majority of octree cells correspond to levels 7, 8 and 9, what greatly facilitates its evaluation in the forthcoming testing phase.

as will be shown in the following section where the simulation results are presented.

### Analog Test Metrics Evaluation

In order to evaluate the proposed testing procedure using octrees, a set of $10^5$ Butterworth filters have been generated using Monte Carlo simulations and evaluated using the octrees generated in the training phase. For the case $r_1 = r_2 = 1$, the results of the evaluation can be observed in Figure 5.20. Correctly classified circuits are drawn using green and red colors, which respectively correspond to pass and fail circuits. Circuits that have not been correctly clustered are circled using dark green for pass circuits classified as fail and dark red for fail circuits classified as pass. As can be appreciated, the misclassified circuits lie in the boundary of the test decision regions, which is the most prone area to misclassification.

Special attention needs the bar chart depicted in Figure 5.21. It is showing the cumulative distribution of the required number of traversed levels in order to cluster every single circuit out of the $10^5$ that have been generated. As can be observed, despite the maximum octree level is 12 (plus the root node), more than 95% or the circuits are classified by just descending down to level 7. Recalling the algorithm listed in Figure **??**, it turns that with only $2 \times 7 = 14$ float number comparisons most of the circuits are clustered. This fact contrast with other classifier methodologies, such as support vector machines (SVM), which require the evaluation of multiple dot

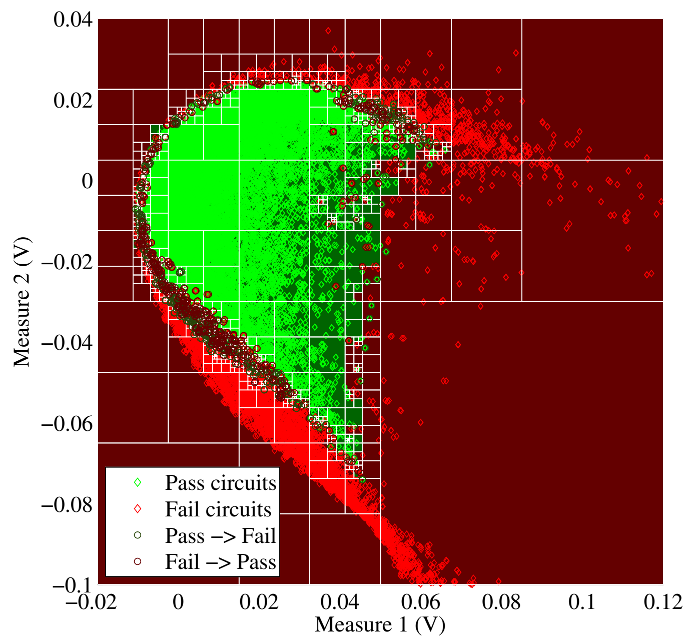


**Figure 5.20:** Testing phase results using the octree shown in Figure 5.18 with band guarding factors of $r_1 = r_2 = 1$. Circled circuits correspond to circuits being misclassified by the octree, i.e. test escapes and test yield loss.

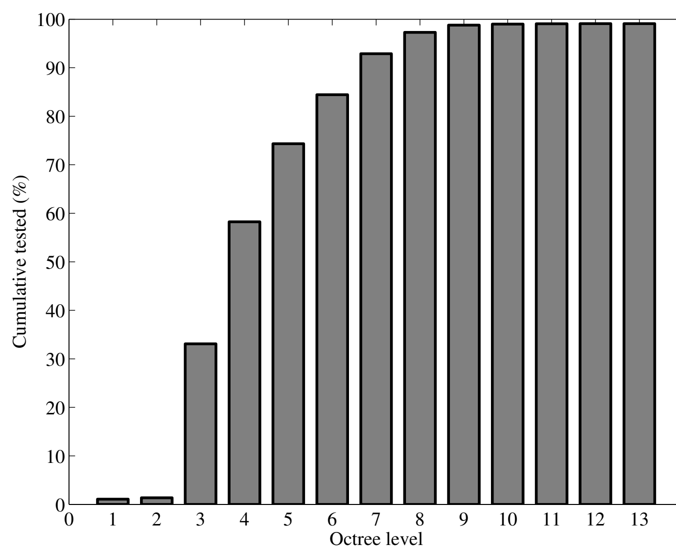


**Figure 5.21:** Cumulative percentage of tested circuits as a function of the achieved octree level for the testing phase. As can be appreciated, more than 90% of circuits are tested in just 7 levels recursions.

products plus a complex kernel function [65].

The training and testing procedures have been performed using different octrees with different levels of band guarding factors. The band guarding factor related to gain specifications, $r_1$, has been varied from 0.5 to 1.78 in steps of 0.04. Similarly, the band guarding factor related to bandwidth specifications, $r_2$, has been varied from 0.85 to 1.49 in steps of 0.02. Such ranges result in grid of size $33 \times 33$, which allows to explore the $r_1 - r_2$ space. The resulting analog test metrics, i.e. test escapes and test yield loss, are shown in Figure 5.22 as function of factors $r_1$ and $r_2$. As mentioned before, the case $r_1 = r_2 = 1$ corresponds to the nominal case with no band guarding used. As can be appreciated, analog test metrics are drastically reduced down to zero as the band guarding factors vary along certain directions, while it is increased if opposite directions are taken.

As a rule of thumb, higher costs are incurred if circuits not accomplishing the specified test limits are shipped to the customer, i.e. false positive circuits. For that reason, fixing a test escape target and tune the test strategy to achieve it becomes a common practice in the test industry. For instance, let us assume the test escapes ratio must be below 1000 ppm (0.1%). In order to better elucidate the concepts throughout the example, Figure 5.23 shows the test escapes contour levels in the $r_1 - r_2$ plane. The established test escape level of 1000 ppm has been highlighted using a thick blue line. This means that any combination of band guarding factors lying on this level will result in a test especifications with an associated test escape metric of 0.1%.

The counterpart metric to test escapes is the test yield loss. Test yield loss is defined

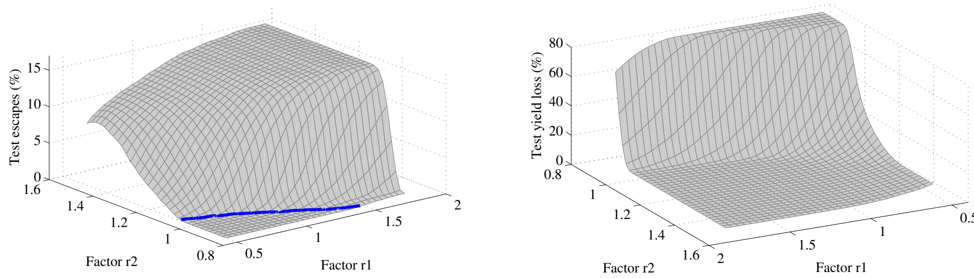


**Figure 5.22:** Test escapes (left) and test yield loss (right) metrics as a function of the band guarding factors $r_1$ and $r_2$ evaluated using the set of $10^5$ circuit samples in the testing phase. The test escapes target of 1000 ppm level is plotted in blue.

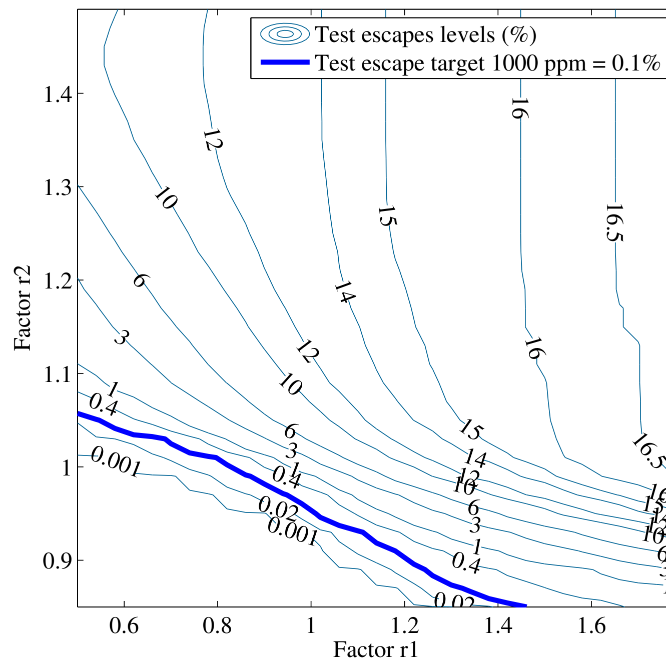


**Figure 5.23:** Test escapes contour levels in the $r_1 - r_2$ plane. The test escapes target of 1000 ppm level is highlighted in blue. Any band guarding factor pair lying on the thick blue level guarantees a test escape of 1000 ppm.

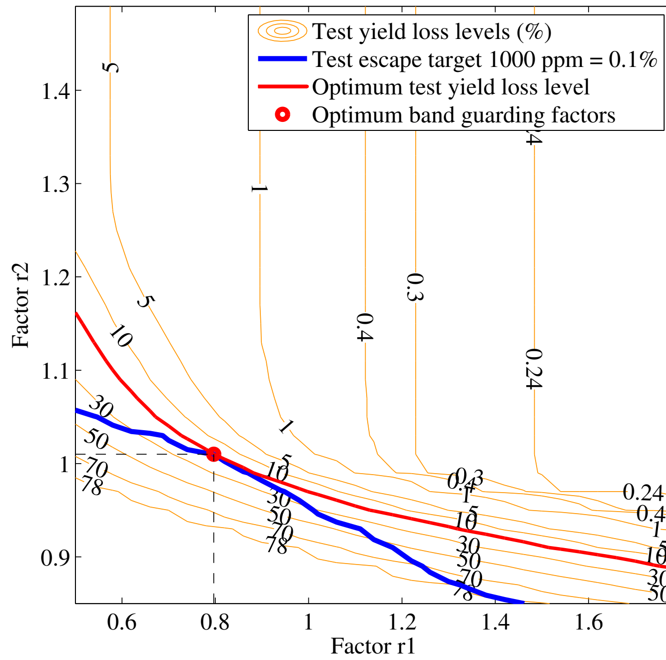


**Figure 5.24:** Test yield loss contour levels in the $r_1 - r_2$ plane together with the resulting 1000 ppm test escape level from Figure 5.23. The optimum band guarding factors are selected by choosing the minimum test yield loss level.

as the ratio of circuits certainly accomplishing the test specifications but classified as fail by the test strategy, i.e. false negatives. In the used example, the test yield loss will serve to determine which is the optimum pair of $(r_1, r_2)$ band guarding factors. Figure 5.24 shows the contour levels of the yield loss metric in the $r_1 - r_2$ plane together with the 0.1% test escape level elucidated from Figure 5.23. The optimum band guarding factors would be the ones with the minimum test yield loss but still maintaining the test escapes target. It is clear that the contour level to choose is the one being tangent to the test escapes contour. Such yield loss contour level is highlighted with a thick red line in Figure 5.24. The contour corresponds to a test yield loss of 16.77% and the needed band guarding factors to achieve the target are $r_1 = 0.797$ and $r_2 = 1.010$.

The results of the optimization process are listed in Table 5.7. Initially, when no band guarding was used, the test escapes and yield loss were 2.05% and 3.11%, respectively. When using the proposed multiple specification band guarding method, the test escapes metric has been reduced by a factor of 20.5 at the expense of increasing the test yield loss metric by a factor of 5.4. In the presented example, test escapes has been fixed as a target, but a different approach can be carried out using importance weights. For instance, an objective function $f(r_1, r_2)$ can be formed as a linear combination (or whatever) of the test escapes and test yield loss functions

**Table 5.7:** Multiple specification band guarding results.

| | Without Band Guarding | With Band Guarding | Factor |
|---|---|---|---|
| **TE (%)** | 2.05 | 0.10 | ÷ 20.5 |
| **YL (%)** | 3.11 | 16.77 | × 5.4 |
| $r_1$ | 1.000 | 0.797 | |
| $r_2$ | 1.000 | 1.010 | |

**Table 5.8:** Multiple specification band guarding results when Gaussian noise is added to the indirect measurements.

| | Without Band Guarding | With Band Guarding | Factor |
|---|---|---|---|
| **TE (%)** | 3.21 | 0.50 | ÷ 6.4 |
| **YL (%)** | 7.68 | 20.18 | × 2.6 |
| $r_1$ | 1.000 | 0.989 | |
| $r_2$ | 1.000 | 0.970 | |

as follows, $f(r_1, r_2) = w_{\text{TE}} \cdot \text{TE}(r_1, r_2) + w_{\text{YL}} \cdot \text{YL}(r_1, r_2)$. Where $w_{\text{TE}}$ and $w_{\text{YL}}$ are the weights assigned, for instance, proportionally to the incurred costs of false positives and false negatives, respectively. Such a function can be numerically optimized without even the need of exploring the whole $r_1 - r_2$ plane.

#### Noise Impact

It is clear that noisy indirect measurements may affect the test efficiency. The proposed multiple specification band guarding methodology is also capable of greatly improving one of the metrics at the expense of worsening the other in the presence of noise. In order to study such scenario, simulations using Gaussian noise in the measurements have been carried out. Table 5.8 shows the analog test metrics under the influence of Gaussian noise with a $\sigma$ spread of 2 mV. As expected, results are worsened with respect to the results shown in Table 5.7, but the method is still able to provide some benefits by just choosing the right band guarding factors depending on the desired targets. Here, a test escapes target has been fixed to 5000 ppm (i.e. 0.5%). The best obtained yield loss metric to achieve the target is 20.18%, what means that the method has been able to reduce the test escapes by a factor of 6.4 while increasing the test yield loss metric by a factor of 2.6. Results get affected by the noise but the method is still usable under such conditions.

## 5.3 Summary and Comments

This chapter has proposed a method to improve indirect test efficiency for analog and mixed-signal circuits based on octree tessellation. The method relies on tesselating the indirect measure space along multiple directions using an octree ensemble. The use of several rotated octree data structures allows the test decision boundary to be encoded with higher resolution and therefore better resemble the actual pass-fail boundary. The production testing phase uses these previously generated tessellations together with a strict test decision criterion to reduce false positive test outcomes. The proposed multi-directional tessellation technique has been applied to test a band-bass Biquad filter with promising results. Simulations conducted under the presence of parametric variations reveal that the proposed methodology is able to lower false positive circuits by an average factor of 50 as compared to a single octree tessellation. Conversely, the test yield loss metric is increased by an average factor of 3. The computational effort of the proposed method for the testing phase linearly increases with the number of octrees used in the tessellation. Despite of this, the actual testing times are acceptable. Regarding the training phase, the incurred computational overhead is insignificant. The proposed multi-directional methodology has been compared against a band-guarding technique revealing better test yield loss for the same test escapes target.

Also, a multiple specification band guarding technique for testing mixed-signal circuits in the indirect measurement space has been proposed. The method is based on a set of factors which are in charge of shrinking or enlarging the CUT specifications cube. An adequate tuning of the band guarding factors allows the optimization of any test target involving the number of misclassified circuits by the test methodology. The test method comprises two phases. The training phase encodes the indirect measurement using octrees to represent the acceptance/rejection test regions. In this phase, the multiple specification band guarding methodology tunes the CUT specifications. The production testing phase uses the octree data structure in order to efficiently test the forthcoming circuits taking advantage of the inherent octree sparsity. The proposed multiple specification band guarding methodology has been applied to test a band-pass Butterworth filter with promising results. The band guarding factors have been set to act over the gain and bandwidth specifications of the CUT. The optimum selection of band guarding factors has allowed the achievement of the initially fixed test targets. Simulations conducted under the presence of noise have revealed the proposed band guarding methodology is also usable under noisy indirect measurements.

Both methods present the great advantage of being able to leverage the analog test metrics. The trade off existing between false positive and false negative circuits within the test industry makes of vital importance the capability of adapting to customer requirements, which are usually given in terms of test escapes or test yield loss targets.

The forthcoming chapter is devoted to the selection and acquisition of analog signatures for alternate mixed-signal testing. A generic algorithm to achieve a good subset

of indirect measurements is presented as well as a novel built-in acquisition system using a low cost integrated approach.

# Chapter 6

# Selection and Acquisition of Analog Signatures

Previous Chapters focused on how octree tessellations may serve to encode the indirect measure space in the frame of indirect mixed-signal testing. In the context of specification based test, it is quite straightforward how to perform the measurements of the specifications. Conversely, under the umbrella of alternate or indirect testing, the way to proceed is not that clear nor straightforward. If the used method to acquire the measurements is not sufficiently fast and reliable, both in terms of measurement costs and time, it may spoil the benefits provided by the alternate test.

Equally important is the selection of a subset of indirect measurements to be used in the alternate test procedure. Some solutions have been lately proposed in order to achieve a reliable set of indirect measurements. The work in [63] proposes an incremental procedure for constructing the target subset based on the information which is missing and can be provided by an extra feature inclusion. Statistical methods have been also proposed, most of them relying on correlations techniques between the set of functional specifications and the set of indirect measurements [61]. For instance, Barragan et al. use the *Brownian distance correlation* together with a greedy algorithm in order to select a meaningful subset of measures adequate for analog/RF circuits testing [62]. The work in [65, 88] uses the *Kendall's Tau rank correlation* in order to select a subset of measurements by avoiding redundancy in the resulting subset.

This Chapter focuses on the two aforementioned topics, i.e. the acquisition and selection of analog signatures. Regarding the acquisition of measurements, an adaptive acquisition system is proposed, designed and validated with experimental results. The proposed adaptive test system grabs its concepts from orthogonal signal composition, but is perfectly extendable to any scenario requiring and adaptive acquisition within certain voltage windows. Regarding the selection of indirect measurements,

an algorithm based on Kendall's Tau rank correlation coefficient is proposed and validated.

## 6.1 Selection of Analog Signatures for Mixed-Signal Testing

Alternate testing strategies require the selection of a set of easy to measure parameters to be used as indirect measurements. To that purpose, many options exist, some of them entirely relying on designer's expertise and experience. Some authors have proposed the use of the sensitivity matrix between circuit's functional specifications and indirect measurements with the goal of maximizing its rank [60]. This allows the avoidance of redundant information. Statistical methods have been also proposed, most of them relying on correlations and regressions techniques between the set of functional specifications and the set of indirect measurements. For instance, in [62, 91], the authors use the Brownian distance correlation together with a greedy algorithm in order to select a meaningful subset of measurements adequate for analog/RF circuits testing.

In this chapter, the concepts and procedures for selecting a suitable subset of indirect measurements are extended to choose an arbitrary number of measurements avoiding or minimizing redundancy within the target subset. Proceeding this way allows to maximize test efficiency while keeping incurred test costs at acceptable levels. The proposal is validated by applying the proposed selection methodology to several Biquad filters.

### 6.1.1 Criterion for Selecting a Subset of Alternate Measurements for Mixed-Signal Testing

This section introduces the new statistic to perform the selection of a subset of indirect measurements. It will be referred as the *selection statistic* or the *$\alpha$-statistic*. Then, the procedure to select a subset of indirect measurements based on the previously defined $\alpha$-statistic is presented. The algorithm to achieve an adequate selection aiming to avoid redundancy within the target subset is explained. Also, a brief introduction to the correlation statistic employed in this work is given.

#### Selection Procedure

The selection of indirect measurements is a challenging issue since the relationship of the information provided by the indirect measurements to the actual functional performances to validate is not straightforward. The key idea of this work is to perform the selection trying to avoid or reduce redundancy between the measurements. This fact implies the achievement of a balance between the amount of relevant circuit information available at testing time and the incurred tests costs tied to redundant

measurements. According to this reasoning, a subset of indirect measurements for analog and mixed-signal testing should accomplish the following two properties. The measurements need to reflect circuit's functional specifications variability in order to allow the test to be performed efficiently and should not be redundant to avoid incurring in extra tests costs yet providing the crucial information. Of course, the latter condition may be relaxed if the objective is to improve test robustness against noisy measurements.

Based on previous research from this dissertation have proposed some ideas for selecting a pair of indirect measurements for mixed-signal testing [65,82]. The objective of this chapter is to extend the concepts when more than two indirect measurements are required to perform the test. The algorithm listed in Figure 6.1 describes the required steps to select an adequate subset of $k$ indirect measurements out of a candidate set of $n$ measurements according to the criteria discussed above. In order to achieve this goal, the method relies on a pairwise correlation statistic, as will be discussed in the forthcoming section. These pairwise correlations are computed and stored in matrix $T_\mu$, being $\mu$ a set of the two indexes of measurements involved in the correlation computation. Then, all the possible combinations of $k$ indirect measurements are explored and for every subset the selection statistic or $\alpha$-statistic is computed. Each of the subsets is formed by the $k$ indexes within the $\nu$ set. As introduced before, the $\alpha$-statistic is computed by adding the expectancy and standard deviation of all the pairwise correlations within the current subset of indirect measurements. Finally, the subset of indexes, $\bar{\nu}$, presenting the minimum $\alpha$-statistic is returned. In order to select the minimum $\alpha$-statistic, $\bar{\alpha}$ is initialized to a large value at the very beginning of the algorithm.

Note that the computational complexity of the algorithm reduces, in practice, to the computation of the correlation matrix (line 5 in the algorithm listed in Figure 6.1). All further steps present no computational effort since they are just memory access to the previously computed $T_\mu$ matrix.

### Selection Statistic

The proposed selection procedure for mixed-signal indirect testing is based on a selection statistic which serves for rating the suitability of a subset of measurements. Here forth, it will be referred as the $\alpha$-statistic or the selection statistic. Let $M_i$ be a subset of indirect measurements for $i = 1, \ldots, k$ aimed to be used for mixed-signal testing. Then, the $\alpha$-statistic is simply defined as, $\alpha = \alpha_m + \alpha_s$, where the addends $\alpha_m$ and $\alpha_s$ correspond to the mean and standard deviation values of all the possible correlation pairs formed by the measurements within the subset as Equation (6.1) and Equation (6.2) state.

```
 1: function SelectMeasurements(M, n, k)
 2:     Precond: M is a candidate set of n measurements
 3:     Precond: k is the number of measurements to choose
 4:     for μ ← AllCombinations(n, 2) do
 5:         T_μ ← KendallTau(M_μ)
 6:     end for
 7:     ᾱ ← ∞
 8:     for ν ← AllCombinations(n, k) do
 9:         Γ ← ∅
10:         for μ ← AllCombinations(ν, 2) do
11:             push(Γ, T_μ)
12:         end for
13:         α ← Mean(Γ) + Stdev(Γ)
14:         if α < ᾱ then
15:             ᾱ ← α
16:             ν̄ ← ν
17:         end if
18:     end for
19:     return ν̄
20:     Postcond: ν̄ contains the indexes of the selected k
21:               indirect measurements
22: end function
```

**Figure 6.1:** Algorithm to select a subset of indirect measurements for mixed-signal testing. The measurements within the resulting subset minimize the average value and spread of their pairwise Kendall's Tau statistic.

$$\alpha_m = \frac{1}{\frac{1}{2}k(k-1)} \sum_{1 \leq i < j \leq k} \mathrm{corr}(M_i, M_j) \tag{6.1}$$

$$\alpha_s = \left( \frac{1}{\frac{1}{2}k(k-1)} \sum_{1 \leq i < j \leq k} \mathrm{corr}(M_i, M_j)^2 - \alpha_m^2 \right)^{\frac{1}{2}} \tag{6.2}$$

Operator corr() refers to any correlation metric between measurements pairs. The forthcoming sections will describe the possibilities for measuring the correlation between measure pairs and the rank correlation coefficient used in this work for such purpose will be described.

#### Correlation Statistic

As pointed out in the previous section, the criterion to select a subset of $k$ indirect measurements out of a candidate set of $n$ measurements requires a correlation statistic. The concepts introduced earlier are perfectly meaningful with any measure of correlation such as statistical covariance, Pearson's linear coefficient or Brownian distance correlation, among others. Albeit many possibilities exist, previous works from the authors have yielded to successful results when Kendall's Tau rank correlation coefficient has been used [82]. Kendall's Tau rank correlation coefficient will be used in this work as a measure of pairwise correlation between indirect measurements [81].

Kendall's Tau rank correlation coefficient is easy to understand and compute. Let $(x_1, y_1), (x_2, y_2), \ldots, (x_r, y_r)$ be a set of bivariate data for $i, j = 1, \ldots, r$. Prior to the definition of Kendall's Tau coefficient, the concept of *concordant* and *discordant* data points must be clarified. Given two bivariate data points, $P_i = (x_i, y_i)$ and $P_j = (x_j, y_j)$, they are said to be *concordant* when $x_i < x_j$ and $y_i < y_j$ or $x_i > x_j$ and $y_i > y_j$. Or alternatively, when the components of the difference vector $P_i - P_j$ have the same sign or even when $(x_i - x_j)(y_i - y_j) > 0$. Otherwise, the two pairs are said to be *discordant*. Under such context, Kendall's Tau rank correlation coefficient is defined as the difference of the number of concordant pairs and the number of discordant pairs of all the possible pairs formed with the aforementioned $r$ samples [81]. The definition of Kendall's Tau rank correlation coefficient explicitly becomes,

$$\tau_{xy} = \frac{\displaystyle\sum_{1 \leq i < j \leq r} \text{sign}[(x_i - x_j)(y_i - y_j)]}{\frac{1}{2} r(r-1)} \tag{6.3}$$

Note that $-1 \leq \tau_{xy} \leq 1$ since the denominator corresponds to the total number of possible pairs given $r$ bivariate data points. Kendall's Tau is a suitable indicator of correlation of any nature since it does not require the data to be linear to present high correlation values. This feature is remarkably desired since the mapping between the functional specifications space and the indirect measurements space may be highly nonlinear. In this work, Kendall's Tau correlation coefficient is used to compute the pairwise correlation between indirect measurements aiming to avoid redundancy, as indicated in the algorithm shown in Figure 6.1.

### 6.1.2 Test Application: Band-Pass Biquad Filter

In order to validate the proposal, the criterion previously presented has been applied to select a subset of indirect measurements to test a Biquad filter. In subsequent sections, design and test specifications of the CUT are described, as well as the excitation applied and the candidate set of indirect measurements.

**Table 6.1:** Band-pass Biquad filter specifications.

| Specification | Symbol | Value | Units | Test |
|---|---|---|---|---|
| Center frequency | $f_0$ | 1 | MHz | ±5% |
| Bandwidth (−3 dB) | BW | 500 | kHz | |
| Quality factor | $Q$ | 2 | | ±5% |
| Band-pass gain | $G_{\mathrm{BP}}$ | 2 | V/V | ±5% |

### Filter Design and Test Specifications

The functional specifications of the band-pass Biquad filter are listed in Table 6.1. The filter has been tuned at 1 MHz with a −3 dB bandwidth of 500 kHz. The voltage gain of the filter at 1 MHz has been set to 2 V/V. The chosen topology is a KHN implementation of a second order state space filter as shown in Figure 6.2. The Biquad filter is composed of several passive components and three operational amplifiers. Despite its simplicity, the Biquad filter is used as a proof of concept of the novelties presented in this work.

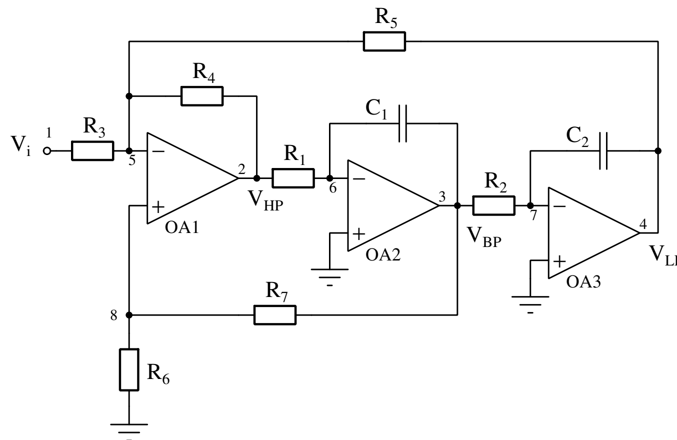


**Figure 6.2:** Schematic of the KHN Biquad filter used in the case study. Table 6.1 shows filter's functional specifications as well as the test acceptance limits. The filter is composed of passive components and operational amplifiers.

Regarding the test specifications, a filter is considered to pass the test if and only if its center frequency, quality factor and band-pass gain are within the ±5% bands of their nominal values. Conversely, if one of the three specifications is violated, the circuit is considered to fail the test.

### Alternate Measurements Space

The presented Biquad filter has been excited with a multitone stimulus. The input signal is composed of 3 in-phase tones corresponding to filter's center frequency (1 MHz), an octave higher (2 MHz) and an octave lower (500 kHz), what yields to a periodic signal of period 2 $\mu$s. Such stimulus has been proven to be effective for analog and mixed-signal testing purposes since it concentrates in a single stimulus the excitation of three single tones, making the whole process faster [65,68,69]. Figure 6.3 shows the applied multitone input signal and the corresponding output responses for a few Monte Carlo samples once the sinusoidal steady state has been reached. Green traces correspond to circuits fulfilling the test specifications listed in Table 6.1 while red traces correspond to circuits violating, at least, one of the test specifications.

In this work, the candidate set of indirect measurements are formed by several samples of filter's response to the aforementioned multitone input signal. The candidate set of samples are taken at evenly spaced time intervals as indicated with the dashed vertical lines in Figure 6.3. Such approach yields to a set of 10 candidate indirect measurements from which a final subset needs to be selected. As intuition suggests, a good subset of indirect measurements has to satisfy two requirements. The measurements need to reflect circuit's performance variability and should not be redundant to avoid incurring in extra test costs.

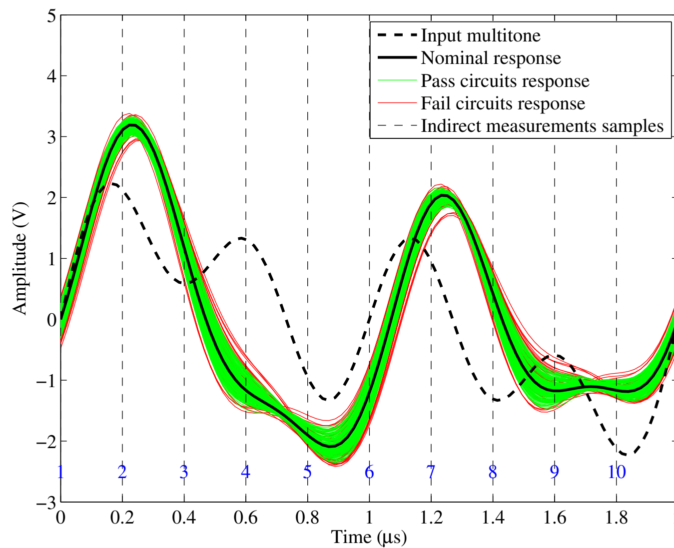


**Figure 6.3:** Steady state transient response of the Biquad filter when it is excited with a multitone signal. The candidate set of indirect measurements correspond to 10 evenly spaced samples of filter's response.

### 6.1.3 Simulation Results

In this section, the results obtained after applying the proposed selection criterion to the Biquad filter introduced earlier are reported. Firstly, a population of Monte Carlo circuit samples is generated and excited with a multitone signal in order to obtain the candidate set of indirect measurements. Then, according to the procedure presented in earlier, a subset of measurements are selected to perform the test. The procedure is carried out using octrees as described in [65]. The former phase corresponds to training an octree using the selected indirect measurements. The latter phase corresponds to the actual production testing in which a freshly generated set of Monte Carlo circuits are evaluated using the previously computed octree. The test misclassifications obtained using the subset of indirect measurements indicated by the proposed method are compared and discussed against any other arbitrary selection of indirect measurements.

#### Monte Carlo Simulations

With the purpose of obtaining a representative sample of circuit population, $10^5$ Monte Carlo simulations have been carried out assuming passive components values distribute according to independent normal distributions with different $3\sigma$ spreads for resistors and capacitors. The generated set of Monte Carlo simulations is split into two equal size sets for the training and testing phases [65]. A sample of frequency and transient response of the circuits within the training set can be observed in Figure 6.4 and Figure 6.3 in which the thick black traces represent the nominal response of the filter while the green and red thin traces represent the response of pass and fail circuits, respectively.

The resulting functional specifications of the Monte Carlo circuits within the training set, as well as their pairwise scatter plots, are depicted in Figure 6.5. As can be inferred all three functional specifications are normally distributed according to Anderson-Darling normality test [92]. Also, no significant correlations between specifications can be appreciated, what clearly suggests that 2 measurements will not be enough to perform the test.

#### Alternate Measurements Selection

The distribution of functional specifications obtained via Monte Carlo simulations, see Figure 6.5, suggest that no significant correlations exist between any of the three considered performances. This fact suggests that, at least, 3 indirect measurements will be needed in order to perform the test. That means that 3 indirect measurements need to be selected out from the 10 indirect measurements conforming the candidate set. According to the proposed method of selection previously proposed, the first step is to compute all the pairwise correlations between the candidate set of indirect measurements. In this work, Kendall's Tau rank correlation coefficient will serve to that purpose [81]. Table 6.2 lists the absolute values of Kendall's Tau coefficients for

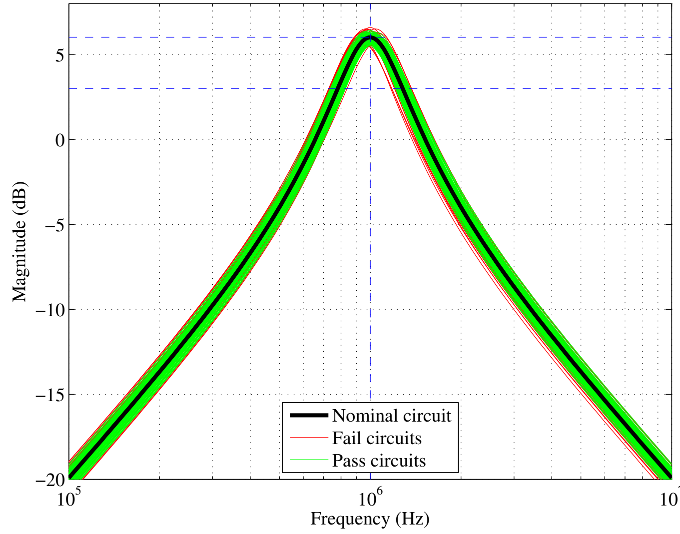


**Figure 6.4:** Filter's frequency response obtained by Monte Carlo simulation. Green traces correspond to circuits satisfying all the specifications listed in Table 6.1 while red traces correspond to circuits violating, at least, one specification.

all the measurements within the candidate set.

Then, in order to avoid redundancy within the training set, the proposed selection method is used. This means to explore all the $\binom{10}{3} = 120$ tuples formed by 3 indirect measurements and select the one with the minimum $\alpha$-statistic. Given the Kendall's Tau pairs shown in Table 6.2, the measurements presenting the minimum $\alpha$-statistic are M02, M04 and M10 with a value of $\alpha = 0.6154$. For this 3-tuple of measurements, the mean value of Taus is 0.4269 and the standard deviation of Taus is 0.1885.

### Test Application Results

In order to validate the proposal, the acceptance and rejection regions will be encoded using octrees in the indirect measurement space. As introduced earlier this comprises two phases, namely, the training phase and the testing phase. The training phase is in charge of encoding the indirect measurement space by means of octree tessellations while the testing phase corresponds to the actual production testing procedure in which the freshly fabricated circuits are evaluated in the previously computed octree. The evaluation of a circuit in the octree yields to its clustering in pass or fail regions.

In this work, $10^5$ circuits have been simulated, $50 \times 10^3$ for each phase. The 3-dimensional octree resulting from the training phase when measurements M02, M04 and M10 are considered is shown in Figure 6.6. In order to facilitate its interpretation, fail circuits, as well as the cells encoding them, have been omitted. Figure 6.6 shows

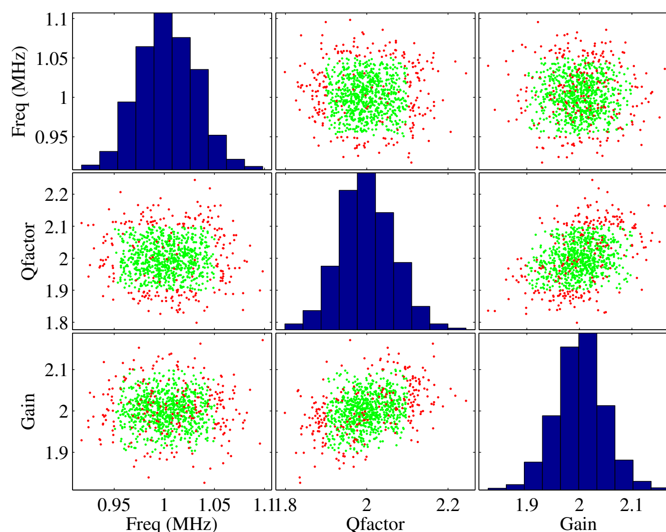


**Figure 6.5:** Pairwise scatter plots and distributions of filter performances obtained by Monte Carlo simulation. As can be appreciated, no significant correlations exist between functional specifications.

the 3-dimensional acceptance region encoded using octrees as well as the pass circuits forming the training set in green color. The green core is actually surrounded by red octree cells encoding the rejection region.

The previously encoded octree using measurements M02, M04 and M10 have been used to test $50 \times 10^3$ Biquad filters. The test results for such selection is that 3.070% of the circuits have been incorrectly clustered. Test escapes and test yield loss analog metrics corresponds to 1.496% and 1.574% of the testing set size, respectively. In order to evaluate the performance of the selected subset of indirect measurements, all the remaining 3-tuples have also been used in the training/testing procedure. Figure 6.7 shows the misclassification rate as a function of the selection statistic. As can be observed in the scatter plot, the less mean and spread of Kendall's Taus, the less misclassifications are obtained. In other words, the misclassification obtained with the tuple of measurements suggested by the proposed method is 3.070% while the extreme values of the misclassification population are 2.736% as a lower bound and 30.606% as an upper bound. Therefore, the selected subset of indirect measurements is very close to the best misclassification value.

Aiming to explore the behavior of the selection statistic in different case studies, it has also been applied to select a subset of indirect measurements in several Biquad filters. The two explored topologies are KHN and Tow-Thomas Biquads. Regarding the former one, low-pass, band-pass and high-pass have been studied. The outputs studied in the latter topology are low-pass and band-pass. Figure 6.8 shows the results obtained for these cases. The conclusion is similar to the previously drawn from the band-pass filter using the KHN topology. Both the selection statistic and

**Table 6.2:** Kendall's Tau rank correlation coefficients between candidate indirect measurements for the band-pass KHN Biquad filter.

| | **M02** | **M03** | **M04** | **M05** | **M06** | **M07** | **M08** | **M09** | **M10** |
|---|---|---|---|---|---|---|---|---|---|
| **M01** | 0.469 | 0.921 | 0.877 | 0.659 | 0.903 | 0.767 | 0.867 | 0.889 | 0.658 |
| **M02** | 1.000 | 0.403 | 0.534 | 0.164 | 0.383 | 0.650 | 0.446 | 0.558 | 0.209 |
| **M03** | | 1.000 | 0.802 | 0.737 | 0.909 | 0.690 | 0.892 | 0.811 | 0.731 |
| **M04** | | | 1.000 | 0.543 | 0.833 | 0.873 | 0.756 | 0.957 | 0.536 |
| **M05** | | | | 1.000 | 0.693 | 0.427 | 0.717 | 0.549 | 0.891 |
| **M06** | | | | | 1.000 | 0.708 | 0.805 | 0.822 | 0.660 |
| **M07** | | | | | | 1.000 | 0.672 | 0.877 | 0.434 |
| **M08** | | | | | | | 1.000 | 0.783 | 0.753 |
| **M09** | | | | | | | | 1.000 | 0.552 |

the misclassification rate show to be moderately correlated, or at least, the tuple presenting the minimum $\alpha$-statistic always presents reasonably low misclassifications, what makes it a good statistic to guide the selection of indirect measurements.

## 6.2 Acquisition of Analog Signatures for Mixed-Signal Testing

Indirect testing strategies solely rely in easy to measure parameters to perform the test. The set of indirect measurements present certain correlation level with the circuit performances to be validated.

The use of analog signal composition has been proposed for alternate mixed-signal testing as shown in Chapter 3. As can be seen in Figure 6.9, the green trace corresponds to the nominal signature generated when the filter used as a CUT is excited with a periodic signal. The red trace corresponds to the same composition but being affected by a parametric shift. Throughout this Chapter, the concept of XY signal monitoring is reused [68] serving as an application example of the proposed adaptive signature generator system for testing and diagnosis.

### 6.2.1 Adaptive Signature Generator System

Testing analog circuits in mixed-signal ICs is an arduous and costly task because of test time targets. Testing the analog part of a circuit, which represents a small portion of the total silicon area, results in large test costs due to time consumption and non standardized test techniques. One possibility to cope with these problems is to use indirect testing strategies together with analog signal monitoring. This allows the generation of a set of digital signals characterizing the CUT which are delivered

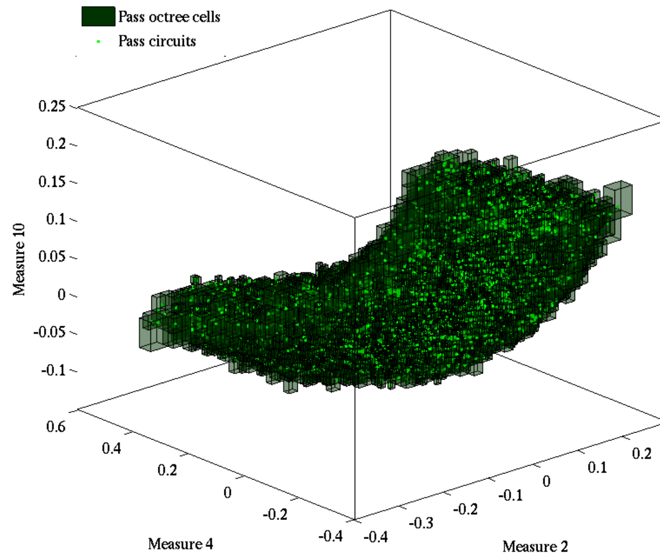


**Figure 6.6:** Octree generated in the training phase encoding pass/fail circuits using the indirect measurements M02, M04 and M10 with the minimum $\alpha$-statistic. In order to facilitate the interpretation, octree cells encoding fail circuits have been omitted.

to the digital automatic test equipment. The digital output can be a pass/fail signal or a more complex digitally encoded analog measurement. Figure 6.10 shows a complex mixed-signal IC structure including six of such monitors capable of generating signatures of the analog circuitry. A digital processing module is in charge of combining and generating the required information for testing the analog circuitry using, for instance, a JTAG output.

The new approach presented in this section is based on an adaptive monitor, intended for testing and diagnosis purposes. The presented monitor samples two analog signals within an *acceptance/observation window* and delivers a digital signature of these signals in two different ways. Firstly, it acts as an indicator stating whether the signal is inside or outside the acceptance window. Secondly, when the signal is inside the acceptance window, the monitor delivers an $n$-bit resolution digital measurement of the analog signals being monitored. This idea comes from the fact that, in a testing scenario, the values to be measured are known to be close to the values measured in the golden circuit. Since the accepted tolerances due to parametric deviation are also known, it is possible to design, as part of the testing system, a specific converter that can be adapted to these known ranges.

For the particular case of XY testing, the resulting XY composition becomes the analog signature of the CUT/CUD. Variations in circuit parameters will shift and twist the curve resulting in the red trace shown in Figure 6.9, as opposed to the nominal green trace. The location of the observation windows are determined by

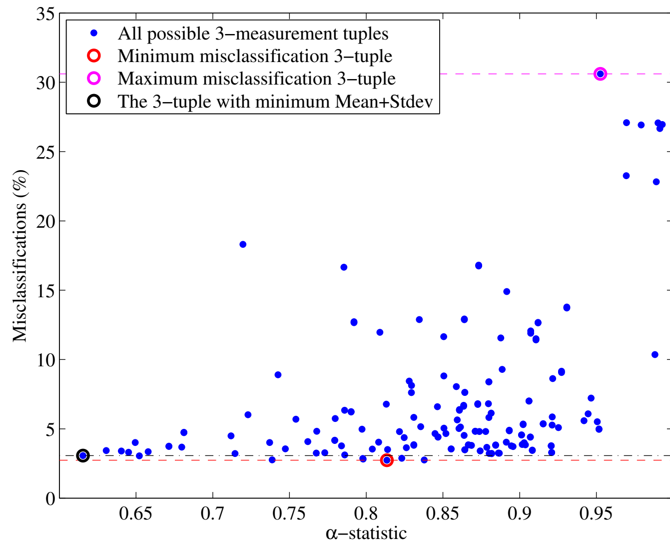


**Figure 6.7:** Scatter plot of test misclassifications as a function of the selection statistic for the band-pass KHN Biquad filter for each of the 120 3-tuples formed using the 10 indirect measurement candidate set.

the selection of the more sensitive trace points or the ones with higher correlation with specifications. Figure 6.11 represents four of such windows. To implement the proposed signature generator, two adaptive ADC converters are needed. These converters digitize the signals with $n$-bit resolution within the range of the observation windows, which may be different for each of the axis. Outside the observation window the converter is out of scale and yields all zeroes or all ones depending whether the value is below or above the observation window. Within the window range, the converter delivers the digitized values of the analog signals being monitored. It can be easily understood as a zoom of the signal within the acceptance window. Therefore a converter with less resolution and with less complexity and size can be used for this purpose since the actual resolution is increased as the window range is shrunk.

The complete architecture of the signature generator is shown in Figure 6.12. Besides the two adaptive flash converters, a digital control subsystem is also needed to manage the converters, establish the adaptive observation windows references and process the generated digital signatures. The interface between the digital and the analog part is a single bit serial transmission carrying the digitized values of the two analog signals being monitored. This information is decoded and stored or transferred for internal digital post processing or delivered to external ATE resources.

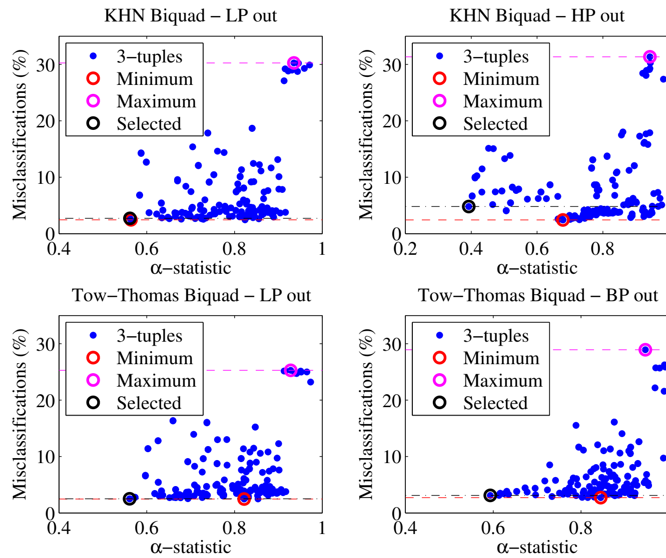


**Figure 6.8:** Scatter plot of test misclassifications as a function of the selection statistic for several Biquad topologies and filter outputs. The two upper scatters correspond to the low-pass and high-pass outputs of a KHN Biquad while the two lower scatters correspond to the low-pass and band-pass outputs of a Tow-Thomas Biquad.

## 6.2.2 Adaptive Signature Generator System Setup

### Integrated Signature Generator Subsystem

The integrated digital signature generator subsystem is in charge of providing the digitized information of the two analog traces being monitored within the observation windows. Figure 6.13 shows the architecture of one of the channels conforming the integrated signature generator proposed in this Chapter. It is formed by a flash ADC structure with serial output capabilities. The flash ADC references are generated by an active voltage divider constructed using isolated well PMOS transistors, what yields to a low power structure as well as a compact design, as opposed to the classical polysilicon resistors.

The integrated signature generator subsystem functions as follows. Each of the comparators compare the analog input signal with respect to the voltage references generated by the established observation window limits and the active voltage divider. Every time the load signal, NLD, is activated at a rising clock edge, the digital thermometric code is stored in the flip-flops and the first LSB bit is flushed to the output. Ever since, every rising edge clock pulse makes the shift register continue flushing its contents until all the thermometric information is sent. Then, the cycle starts over.

The integrated digital signature generator subsystem has been designed and fabri-

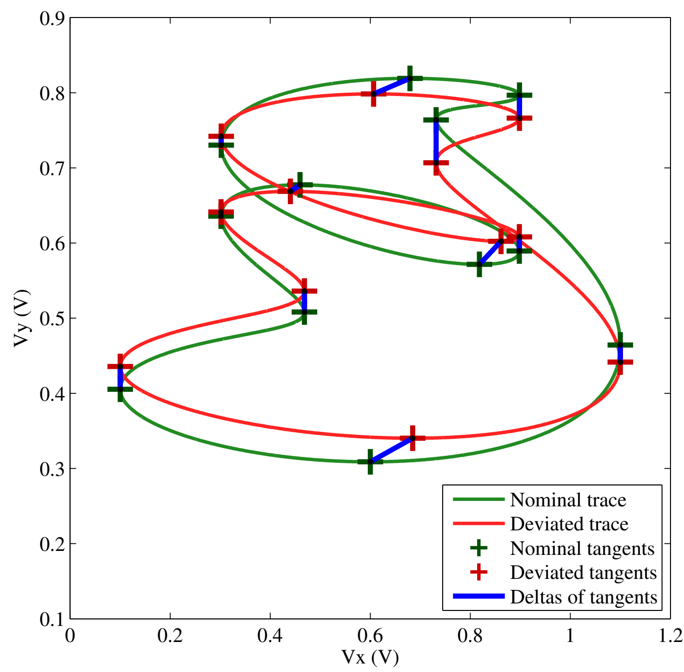


**Figure 6.9:** Nominal and deviated analog signatures resulting from an XY signal composition. The extreme points of the traces contain the signal information which serves for test/diagnosis purposes [58, 67, 68].

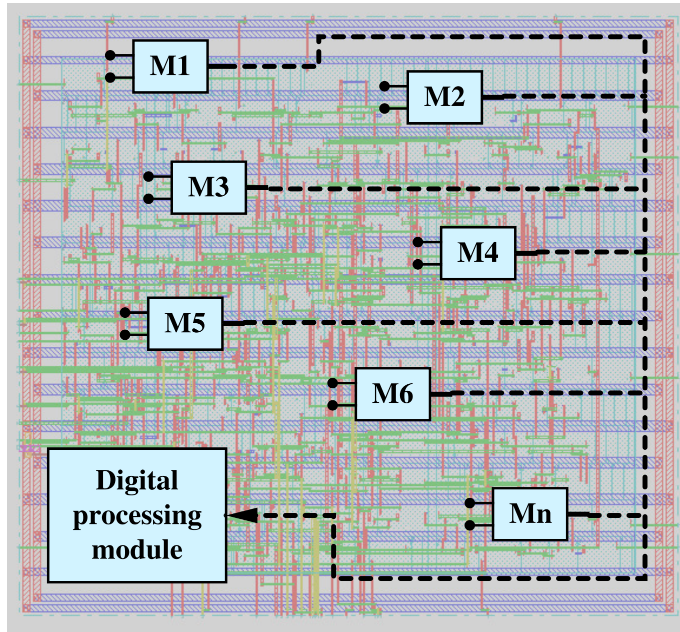


**Figure 6.10:** Integrated analog signal monitoring and digital signature generation. The digital processing module facilitates the test/diagnosis decision based on the digital information provided by the monitors.

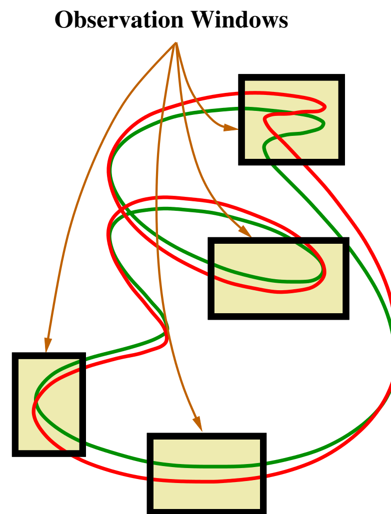


**Figure 6.11:** Composition of two analog signals and four possible observation windows. Each observation window focuses on a certain area of interest, based on a previous sensitivity/correlation analysis [82].

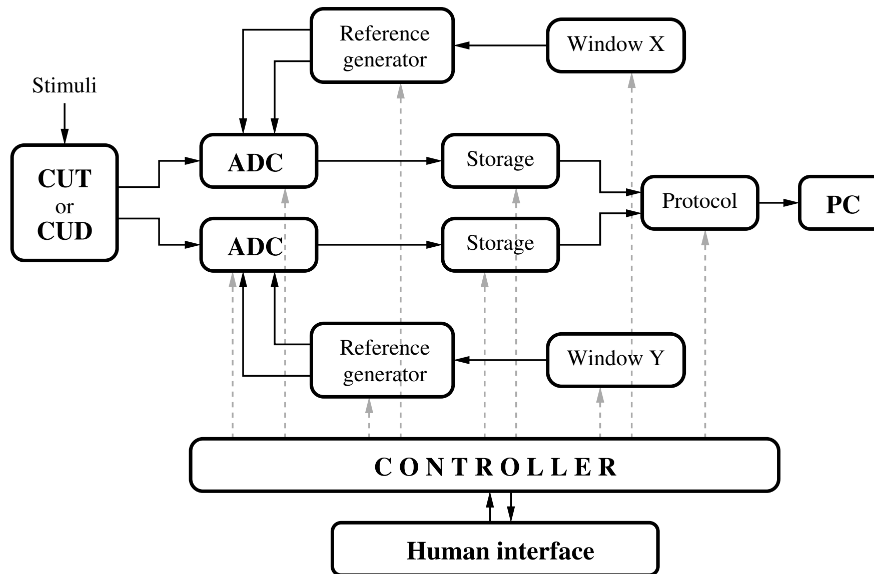


**Figure 6.12:** Basic architecture of the signature generator system. CUT/CUD analog signals are monitored and digitized within the observation window limits established by the controller. The data are stored and transferred to a PC for further processing.

cated in an industrial 65 nm CMOS technology. Figure 6.14 shows the layout of the signature generator which is 170 $\mu$m wide and 62 $\mu$m high, resulting in a total silicon area of 10540 $\mu m^2$. Figure 6.15 shows a photograph of the fabricated bare die in which the integrated digital signature generator subsystem can be identified.

### FPGA Based Digital Control and Acquisition Subsystem

The digital control and acquisition subsystem aims to serve as a suitable interface between the integrated signature generator digitizing XY pairs and a computer. The computer will be in charge of analyzing the data of the consecutive XY pairs captured within an observation window. To this purpose, the digital control and acquisition subsystem performs the following tasks:

- Establish the observation window.
- Control the digital signature generator serial transmission of the digitized XY pairs. Each pair consists in 30 bits of data (2 thermometric codes of 15 bits).
- Receive the XY pairs and compact them to natural binary code.
- Store the consecutive XY pairs related to the observation window.
- Send the stored XY pairs to the PC through a USB port for further analysis.

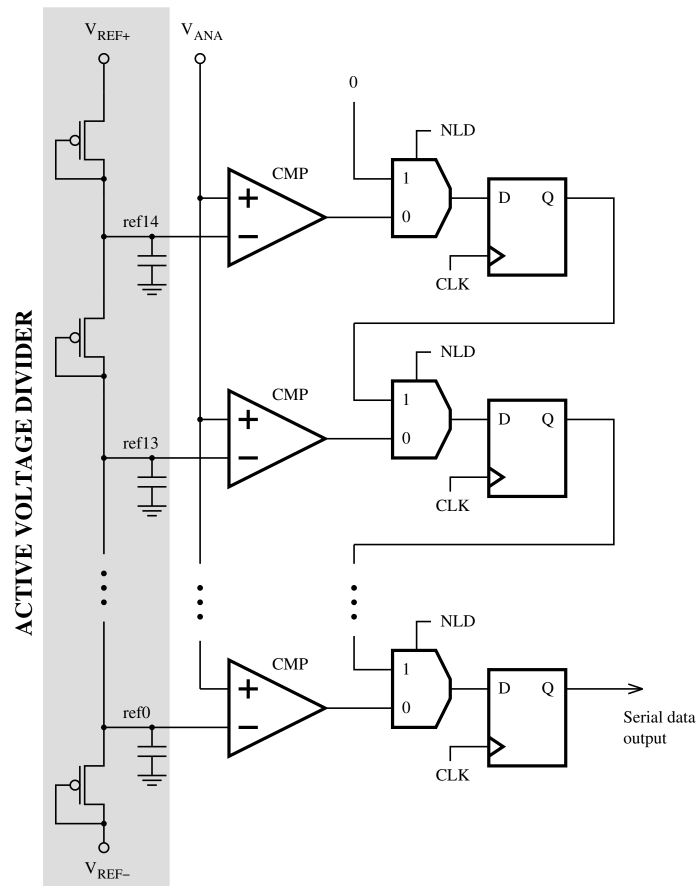


**Figure 6.13:** Schematic of the integrated signature generator subsystem. Internal ADC references are generated using a diode connected, isolated well, PMOS transistor ladder. Comparator outputs are serially transmitted to the FPGA based digital control and acquisition subsystem.

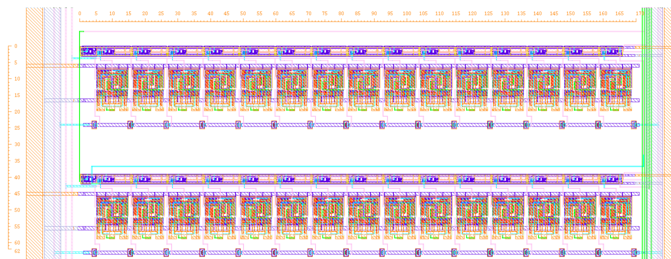

**Figure 6.14:** Layout of the integrated signature generator subsystem (both channels) where the array of comparators can be appreciated as well the active voltage divider and the shift register structure. The integrated signature generator subsystem is 170 $\mu$m wide and 62 $\mu$m high (10540 $\mu m^2$).

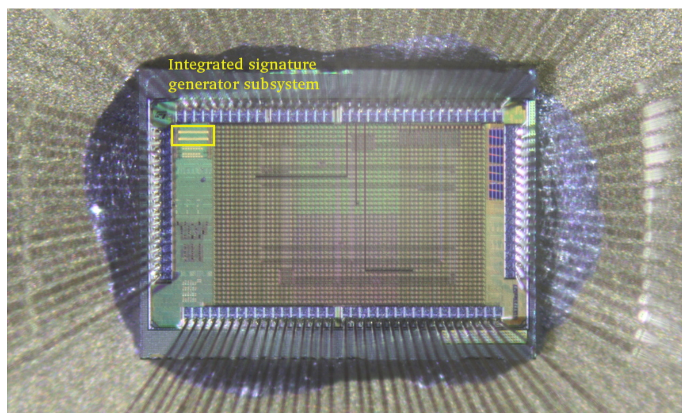


**Figure 6.15:** Photograph of the integrated signature generator subsystem fabricated in an industrial 65 nm CMOS technology. The integrated signature generator subsystem is 170 $\mu$m wide and 62 $\mu$m high (10540 $\mu m^2$).

All the logic required to perform these tasks has been designed over an FPGA using the VHDL hardware description language. To avoid designing a PCB to support the FPGA, a development board from Terasic/Altera including an Altera Cyclone III EP3C16F484C6 device has been used. The use of this board has additional advantages, because it already includes a 50 MHz oscillator generating the clock signal driving the FPGA, a USB connection to a PC, and a user interface integrated by 10 switches, 3 push buttons, 10 LEDs, 4 seven-segments and, if desired, a 2 line $\times$ 16 characters LCD. Also, it has some drawbacks, because the FPGA I/O power supply is fixed to 3.3 V, thus requiring logic level adjustments to 1.8 V (digital) and 1.2 V (analog) I/O power supply values used by the integrated digital signature generator subsystem.

An observation window is defined by four voltage references corresponding to the extreme values for the X and Y axis, respectively. These voltage references must be delivered to the digital signature generator and can be obtained through appropriate DACs controlled by the digital control and acquisition subsystem. Successive sets of these four values can be established on the fly through the above mentioned user interface and stored in RAM. Alternatively, they can be established at compilation time and stored in ROM.

In order to minimize the cost of the DACs, each DAC has been implemented as an inverted weight outputs (IWOC) digital pattern generator [93] followed by a first order low-pass filter. The IWOC digital pattern generator has an architecture similar to a PWM generator based on an $n$-bit binary counter and an $n$-bit comparator, but the weights of the counter output signals are inverted before being input to the comparator. Figure 6.16 shows the architecture of such DAC structure for $n$ = 6, allowing to define the voltage references for the observation window in steps of 18.75 mV. The frequency of the DAC clock is 50 MHz and the cut-off frequency of the low-pass filter is about 1.1 kHz, guaranteeing a ripple lower than 0.5 mV. Note

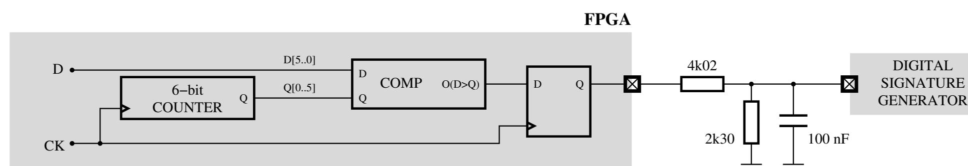


**Figure 6.16:** Architecture of the 6-bit DAC based on an IWOC digital pattern generator [93] as implemented in the digital control and acquisition subsystem. The use of four IWOC based DACs allows the generation of the analog limits for the observation windows as seen in Figure 6.20.

that the $n$-bit counter can be shared by the four DACs.

By means of a frequency divider by 50, a 1 MHz clock is generated by the FPGA for controlling the digital signature generator serial transmission of the sampled XY pairs. A negative pulse, referred as NLD, of a single clock period is also generated every 30 clock periods to allow loading the sampled XY pairs in a shift register for their serial transmission. These signals are used within the FPGA to receive the XY pairs in thermometric codes of 15 bits and, on the fly, convert them to natural binary code. A single 4-bit counter and two 4-bit registers are used to this purpose.

To store the consecutive XY pairs related to the observation window and send them to the PC through a USB port taking advantage of the SignalTap II Logic Analyzer tool available in Altera's design software. This debugging tool allows to include in the FPGA a logic analyzer that samples the desired signals, stores them in a RAM and sends the contents of this RAM to a PC through a USB connection for storing them in a file. Using this tool, it is just necessary to sample the 4-bit registers every 30 clock periods once the observation window is reached.

### 6.2.3 Experimental Results Testing a Biquad Filter

In order to validate the proposed adaptive test/diagnosis system, it has been applied to test a low-pass Biquad filter affected by parametric deviations. The filter has been tuned at $f_0 = 1$ kHz with unity DC gain and critical damping ratio. The applied stimulus is a multitone signal composed out of filter's characteristic frequency plus two extra tones, one octave higher and one octave lower. Such rich selection of tones is able to excite the pass band and the attenuation band of the filter, therefore being able to manifest parametric shifts in circuit components.

As mentioned before, a previous study needs to be carried out in order to explore the XY composition. The resulting analog signature information is compacted by means of its tangency points to horizontal and vertical lines, as depicted in Figure 6.9. The displacements of these tangency points with respect to the nominal trace form the set of indirect testing measures. Among all the possible measures, two of them are selected using a criterion based on Kendall's Tau rank correlation coefficient [82].

Once the indirect measures are selected, the observation windows ranges need to

**Table 6.3:** Measured observation windows limits.

| | Window 1 | | Window 2 | |
|---|---|---|---|---|
| | Low | High | Low | High |
| **X range (mV)** | 682 (0x24) | 870 (0x2E) | 663 (0x23) | 927 (0x31) |
| **Y range (mV)** | 699 (0x25) | 835 (0x2C) | 510 (0x1B) | 608 (0x20) |

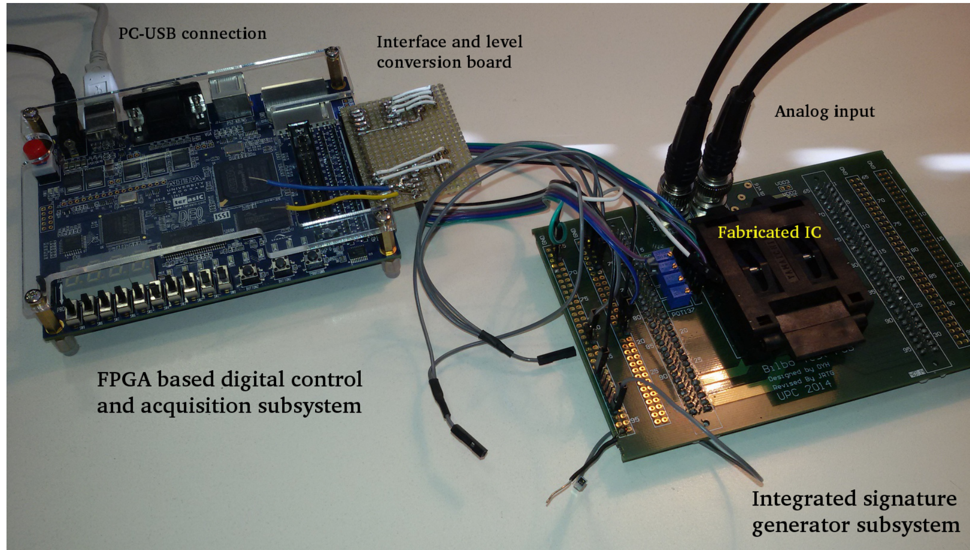


**Figure 6.17:** Photograph of the experimental setup. On the right, the board containing the fabricated IC implementing the integrated signature generator subsystem. On the left, the digital control and acquisition subsystem implemented on a Terasic/Altera Cyclone III FPGA board.

be established according to test specifications. The use of Monte Carlo simulations facilitate the appropriate selection acceptance/observation windows ranges according to the criteria shown previously. For the current case study, the selected observation window ranges are shown in Table 6.3 together with the digital code to be configured using the FPGA user interface.

The experimental setup is shown in Figure 6.17. The integrated signature generator subcircuit is mounted on an ad hoc board which receives the XY analog signals, the voltage references as well as the appropriate serial transmission control signals provided by the digital control and acquisition subsystem. The latter subsystem can be observed in left hand side of Figure 6.17. It has been implemented in a Cyclone III FPGA board and connected to a PC through a USB connection. The board between these two subsystems serves as a level conversion board as well as to physically support the first order filters for the IWOC DACs.

The digital signature generator system functions as expected as can be observed in

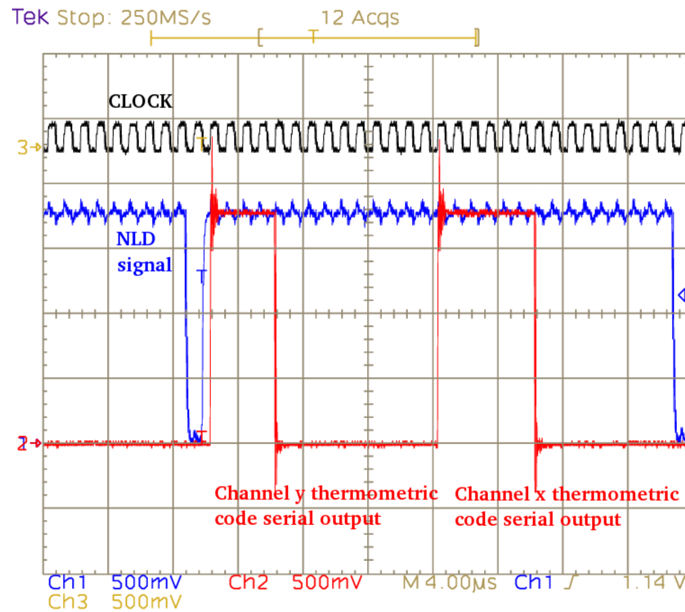


**Figure 6.18:** Oscilloscope chronograms of the signals involved in the serial transmission of the signature information. Once the load signal is activated the shift register flushes the 15-bit thermometric code of both channels.

the measured digital chronograms shown in Figure 6.18. Once the NLD signal is activated (low) at a rising clock edge, comparator outputs in Figure 6.13 are loaded into the shift register and the first LSB bit from channel Y is flushed to the output. Subsequent clock pulses continue flushing the digital data corresponding to channel Y and channel X, as shown in the chronograms of Figure 6.18. In Figure 6.19, the measured Lissajous composition as seen on the oscilloscope before impedance matching. The experimental trace matches the simulated trace shown in Figure 6.9.

The digital data captured within the two observation windows used in this case study are shown in Figure 6.20. As expected, the experimental traces match the simulated XY composition within the ranges established by the observation windows. It can be appreciated the way the digital values saturate indicating the trace is outside the observation windows, yet providing the digital information within the acceptance window.

In order to state the suitability of the developed adaptive signature generator system for test/diagnosis purposes, several amounts of deviations have been applied to filter's characteristic frequency ranging from 2.5% up to 15%. For each of these deviated filters, XY composition data has been captured and processed. With the aim of denoising the data, several periods have been sampled and averaged (few milliseconds). Using an ad hoc peak detection algorithm based on quadratic interpolation, the $\Delta y$ displacements of the Lissajous traces have been measured within each of the

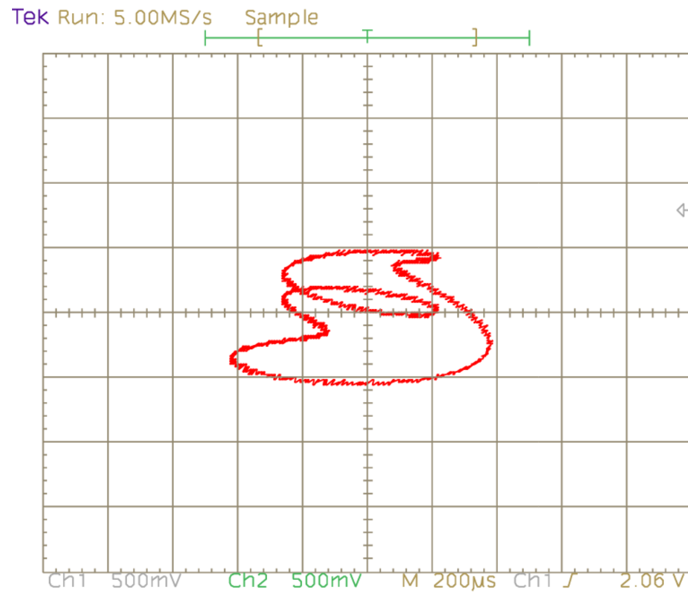


**Figure 6.19:** Measured Lissajous composition of the input/output signals when a multitone is applied to a low-pass Biquad filter. As can be observed, the experimental Lissajous trace matches the one shown in Figure 6.9.

observation windows. Table 6.4 shows these measurements and the inferred deviation level for each of the windows relying on the simulation data shown in Figure 6.21. Finally, the diagnosed deviations for each observation window can be averaged to yield the diagnosed deviation level in filter's $f_0$ frequency. Table 6.4 also shows the relative error in diagnosing each of the applied deviation levels. As can be stated, all these errors are in the order of 1%, therefore validating the proposed adaptive test/diagnosis signature generator system. Of course, the diagnosed value can be used to test the CUT by simply comparing it against the test limit, which is, in this particular case study, $\Delta f_{0\max} = 8\%$.

## 6.3 Summary and Comments

In this chapter, a criterion to select a subset of indirect measurements and a novel adaptive test system for mixed-signal testing have been proposed.

The selection algorithm is based on selecting a subset in a way redundancy is avoided, therefore maximizing the information provided by each of the measurements what immediately translates into better test results. The method relies on any pairwise correlation statistic such as Pearson linear correlation coefficient, Brownian distance correlation or Kendall's tau rank correlation coefficient. The proposed strategy selects the subset of indirect measurements based on those tuples of measurements

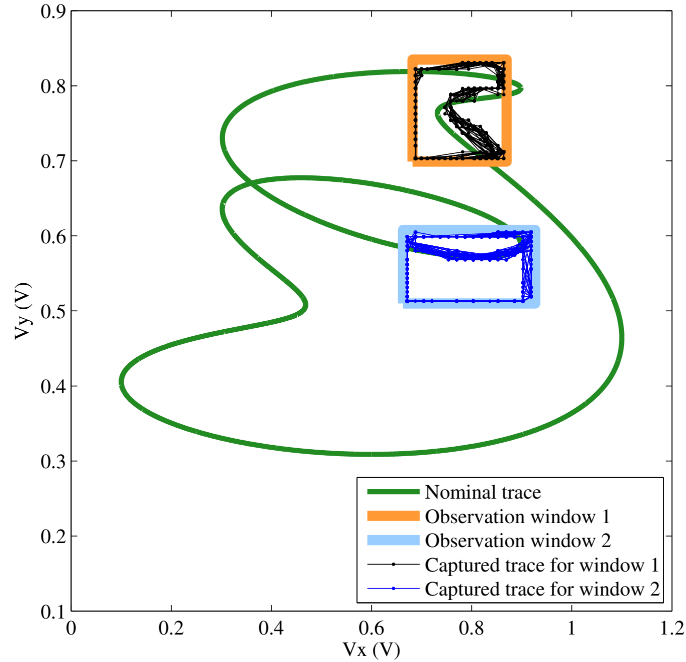


**Figure 6.20:** Simulated XY composition and the digitized experimental trace within the two observation windows considered in this case study as defined in Table 6.3. As can be observed, the experimental traces match the simulated trace within both observation windows.

**Table 6.4:** Measured $\Delta y$ displacements for several $\Delta f_0$ deviation levels and diagnosis and test results.

| | **Window 1** | | **Window 2** | | **Diag/test results** | | |
|---|---|---|---|---|---|---|---|
| $\Delta f_0$ (%) | $\Delta y_1$ (mV) | $\Delta f_{01}$ (%) | $\Delta y_2$ (mV) | $\Delta f_{02}$ (%) | $\Delta f_{0d}$ (%) | Error (%) | Test |
| 2.50 | 6.97 | 2.34 | −1.47 | 0.83 | 1.59 | −0.89 | Pass |
| 5.00 | 17.34 | 5.98 | −8.70 | 4.95 | 5.47 | 0.44 | Pass |
| 7.50 | 22.44 | 7.85 | −13.84 | 7.93 | 7.89 | 0.36 | Pass |
| 10.00 | 29.75 | 10.63 | −17.15 | 9.87 | 10.25 | 0.23 | Fail |
| 12.50 | 38.25 | 14.04 | −19.48 | 11.25 | 12.65 | 0.13 | Fail |
| 15.00 | 40.29 | 14.88 | −20.52 | 11.88 | 13.38 | −1.41 | Fail |

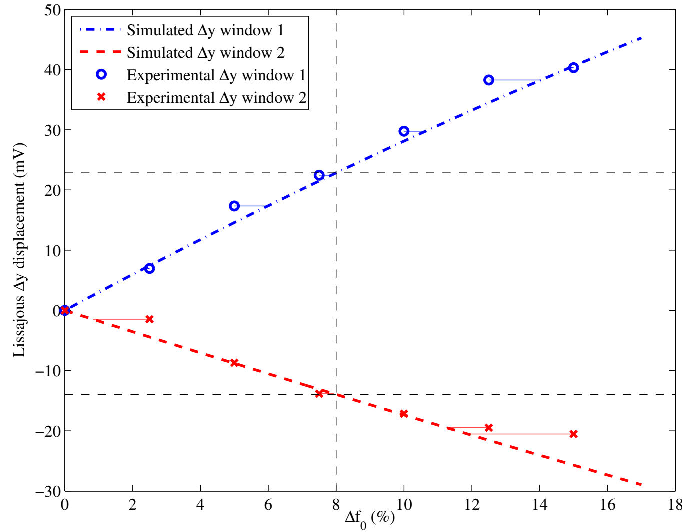


**Figure 6.21:** Simulated and experimental data of the $\Delta y$ displacements of the two tangency points within each of the two observation windows considered in this case study as the $f_0$ frequency of the filter varies from its nominal value.

presenting the lowest selection statistic, i.e. the lowest mean and spread of the pairwise measurements correlations. The proposed method has been applied to select a subset of indirect measurements for testing various Biquad filters under the presence of process variations. The test procedure has been carried out by means of octree tessellations in the indirect measurement space. Test misclassifications have been shown to be correlated with the proposed selection statistic in all the studied cases. Resulting misclassification rates are, in average, within the first 2.4% of the misclassification population obtained when all the possible subsets of measurements are explored.

A novel adaptive signature generator for test/diagnosis has been proposed and its feasibility has been experimentally demonstrated. The key idea of the method relies on the concept of signal monitoring within predefined observation or acceptance windows. These windows are established accordingly to golden circuit behavior and test limits. The system is formed by the integrated signature generator subsystem and the digital control and acquisition subsystem. The former is composed by two adaptive ADCs able to monitor the CUT/CUD within specified observation windows according to test specifications or the expected location of the analog traces. The latter subsystem is in charge of setting the observation windows references and controlling the serial transmission of the acquired data, which is later sent through a USB connection to a PC for further processing. The subsystems constituting the proposed adaptive signature generator have been fabricated and implemented in an industrial ST Microelectronics 65 nm N-well bulk CMOS technology and an Altera Cyclone III FPGA, respectively. The whole system has been applied to diagnose and test a low-

pass Biquad filter affected by parametric deviations. Successful experimental results are reported showing a diagnosis discrepancy in the order of 1%.

Chapter 7

# Conclusions and Future Work

This chapter summarizes and collects the contributions and conclusions derived from the dissertation. Also, some future research guidelines are given in order continue the research on the field.

## 7.1 Contributions and Conclusions

### Alternate Test and Binning Using $2^n$-ary Tree Digital Encoding

This dissertation proposes a novel methodology to digitally encode the test acceptance/rejection regions of analog and mixed-signal circuits within the alternate measurement space. The alternate test proposal comprises two phases, the training phase and the testing phase. The training phase encodes the test acceptance/rejection regions using a recursive digital tessellation procedure based on octrees or $2^n$-ary trees. The testing phase corresponds to the actual production testing using the octree data structure generated in the former phase.

The $2^n$-tree digital encoding approach presents a number of benefits, specially in terms of computational efficiency since the resulting octree data structures are inherently sparse, what greatly facilitates fast training and testing times. The test of a fresh circuit requires a single comparison per dimension and level traversed in order to successfully cluster the circuit. The alternate test decision boundaries may be highly non linear, with irregular shapes or even present non connected regions. Octrees are able to beat these drawbacks and adapt to any shape since the digital encoding algorithm refines the tessellation exactly where it is needed, i.e. in the surroundings of the test decision boundary. To that purpose, a boundary densification algorithm has been proposed in order to increase the number of circuit samples within the pass/fail boundary. Also, octrees have the great advantage of being able to be

generalized to an arbitrary number of dimensions without any extra issue beyond the well known curse of dimensionality. Regarding these generalization capabilities, octrees are sensitive to extend their clustering capabilities to more than two clusters, therefore facilitating the proposed quality binning approach without any extra overhead. Further, the octree encoding algorithm is deterministic hence not relying on a minimization algorithm as many of the state of the art clustering methods do. This is a desirable feature since the resulting encoding does not depend on the chosen minimization algorithm, convergence issues or the considered initial seed. Also, the simplistic recursive implementation, both for training and testing, of these data structures make them quite affordable and easy to implement in stand alone systems such as embedded systems as well as BIST implementations. The proposed octree based encoding methodology has been applied to test and bin various analog circuits under parametric variations with successful results. The method has also been compared against a state of the art clustering method such as a support vector machine based classifier reporting similar test efficiency but being able to cluster a circuit 5 times faster.

### Suitable for Testing Heterogeneous Systems

Heterogeneous systems testing is a specially challenging endeavor due to their non electrical nature according to the exploited transduction principle. For the particular case of MEMS accelerometers, a sufficiently rich mechanical excitation is required in order to push their internal mechanical subsystem into play and manifest all the parametric deviations related to such systems. This thesis proposes a variable speed vertical spinning strategy in order to excited the DUT. It has been applied to test a commercial MEMS accelerometer using the aforementioned excitation together with the octree encoding methodology presented in Chapter 3 to encode the analog signature characterizing the system. The vertical spinning wheel excitation methodology has reported great defect identification capabilities. The analog signature compaction and the definition of a diagnosis efficiency metric has reported successful axis misalignment diagnosis in a commercial accelerometer device.

### Analog Test Metrics Trade Off

The dissertation proposes two major improvements in order to endow the $2^n$-ary tree encoding procedure the capabilities of leveraging and controlling the analog test metrics. The trade off existing between false positive and false negative circuits in the test industry makes of vital importance the capability of adapting to customer or fab requirements. The proposed methods conform an octree ensemble classifier and a band guarding technique.

The first method relies on using an ensemble of rotated octrees in order to achieve a better adaption to the shape of the test decision boundary. The application of different criteria using the information of each of the rotated octrees to derive the test decision allows an adequate leverage test escapes and test yield loss metrics. The

second method is based on a multiple specification band guarding methodology which is capable of individually adjusting the guards of each of the functional specifications using a band guarding factor. The proposed method allows the selection of the appropriate set of band guarding factors to achieve the target imposed for one of the metrics while minimizing the other. Both the proposed boundary definition improvement techniques have been applied to several analog filters with good results. The methods successfully achieve the leverage and control of the analog test metrics according to the specified test goals without significant overhead.

### Selection of Alternate Measurements

The selection of alternate measurements for analog and mixed-signal circuits is an important aspect which is directly related to the test efficiency as well as to the incurred costs. In this thesis, a criterion to select a subset of indirect measurements for mixed-signal testing has been proposed. The proposal is based on selecting a subset of alternate measurements in which redundant information is avoided, therefore maximizing the effective information provided by each of the measurements. This immediately translates into better test results and lower test costs. The method may rely on any pairwise correlation statistic such as Pearson linear correlation coefficient, Brownian distance correlation or Kendall's tau rank correlation coefficient, which is the one chosen in this dissertation. The proposed strategy selects the subset of indirect measurements based on those tuples of measurements presenting the lowest selection statistic, i.e. the lowest mean and spread of the pairwise measurements correlations. The proposed method has been applied to select a subset of alternate measurements for testing various Biquad filters under the presence of process variations. The test procedure has been carried out by means of octree tessellations in the indirect measurement space. Test misclassifications have been shown to be correlated with the proposed selection statistic in all the studied cases. The selected measurements presenting the lowest misclassification rates are consistent with the ones offered by the selection algorithm.

## 7.2 Future Work

In this section, some future work guidelines are given with respect to the research presented throughout this dissertation. The forthcoming paragraphs spot some aspects or topics which may lead to such future research in the field.

### Challenges in Testing Very Large Circuits

If the circuit under test is large, the electric simulations to extract the alternate measurements which will allow the octree encoding may be unfeasible to perform. At this point, new challenges arise such as optimum circuit partitioning or the establishment of proper circuit hierarchies. This reasoning also leads to the interesting field

of higher level circuit modeling. Albeit there exist languages which allow such higher description modeling, i.e. Verilog-A, Verilog-AMS, VHDL-AMS,... there exist a considerable gap between them and low level SPICE simulation. The objective pursued in this thesis requires the best features of these two approaches, namely, the detail and accuracy of low level electrical simulations and the performance provided by compiled analog hardware description languages. Research targeting the symbiosis of these two aspects will lead to a paradigm shift in analog and mixed-signal circuit testing and simulation.

### New Methods to Improve the Test Decision Boundary Definition

Octree encoding has shown to be efficient both in terms of analog test metrics and computation time. Regarding the former aspect, it would be desirable to reduce even more the number of misclassified circuits which could undoubtedly be achieved by improving the definition of the test decision boundary. Actually, the octree ensemble and band guarding methods proposed in this thesis target, and quite successfully achieve, this specific objective as well as the leverage of between test escapes and test yield loss metrics. Two main sources of misclassification have been identified, one coming from poor circuit density in the surroundings of the test decision boundary and one coming from the coarseness of the octree cells, i.e. the non smooth octree cells corners. One possibility to cope with this drawback may be the combination of different classification methods. For instance, the use of octrees to perform a coarse encoding of the space by limiting the maximum allowed octree depth and then including any other classification method (ANN, SVM,...) to actually get a smooth separation between the different clusters.

### New Methods to Test Heterogeneous Systems

As spotted throughout the dissertation, the test of heterogeneous systems (particularly MEMS accelerometer devices) is an even more challenging issue than testing classical analog and mixed-signal circuits. This is so because of their inherently non electrical nature according to their transduction principle. Such situation implies an extra effort in generating and applying the excitation to test the device, as shown for the case of MEMS accelerometers. A whole spectrum of excitation possibilities is still in the need to be explored as well as extend the evaluation of alternate test methodologies applied to such non classical electronic devices.

### Selection of Input Stimuli Targeting Octree Based Encodings

The previously suggested future research guideline brings the more general concept of circuit excitation to discussion. This dissertation has used a multitone signal to excite the CUT and based on the test vehicles used, it seems to be a well suited option to the purpose. Now, could it be improved? It certainly would be the objective of

future research since the selection of the input stimuli absolutely determines the output of the circuit and therefore the alternate measurements in which the test decision relies on. It is clear the multitone approach is a reasonably general approach since adequately tuning the gain and phase of the included tones any arbitrary signal may be generated if a sufficient number of harmonics are considered. The question arises here to ask which are the most relevant tones to be included in order to greatly highlight the parametric deviations of the CUT and therefore make them noticeable in the alternate measurements. This is, of course, a matter of essential future research.

### Reuse of Parametric Defect Generated Octree to Catastrophic Defects Detection

This thesis has been framed within the challenges encountered in the current deep submicron CMOS technologies in which process variability (among PVTA variations) is probably the issue which motivates a vast percentage of the research performed today in the field of alternate test of analog and mixed-signal circuits. Such scenario makes researchers to focus most of their works on circuits affected by parametric variations. So this dissertation too, but what about using alternate test methods to identify catastrophic defects? It could be of great advantage to use all the existing knowledge on parametric defects to target catastrophic defects. Albeit this work focuses on test and binning, it could be easily extended to identify and diagnose classes of catastrophic defects, similarly to inductive fault analysis (IFA) but with the tools derived from parametric tests. Decision trees will certainly serve to that purpose since different regions of the alternate measurement space will concentrate the same type of catastrophic defects, i.e. shorts to ground or shorts to power supply will probably lie together. This guideline opens the window of analog and mixed-signal catastrophic defect testing and diagnosis using the tools specifically developed for parametric defects.

### Strategies to Deal with High Dimensional Spaces

Alternate test deals with a number of indirect measurements which are expected to contain enough circuit information in order to be able to correctly define the test acceptance/rejection regions and cluster the circuits from the production run. There exist a trade off between the resulting test efficiency and the selected features. Any alternate test method used to encode the test acceptance/rejection regions relies on a certain number of indirect measurements, but if the number is large, the method may be suffering from the well known issue in high dimensional spaces referred to as *the curse of dimensionality*. It basically states the great difficulties to keep the test efficiency at reasonable levels when the number of dimensions is increased, despite of increasing the size of training data set accordingly. This makes another important aspect to come into play. The adequate selection of alternate measurements is of vital importance to get reasonable test performances. It does not only affects the test efficiency but it also has a direct impact on test costs since any extra measure

to be performed rises up the test budget. The further exploration of new statistics as well as selection algorithms to improve such aspect of alternate test becomes a substantial necessity in the field.

Appendix A

# List of Publications

## Refereed Journals


**[J01]** E. I. Vatajelu, A. Gómez-Pau, M. Renovell, and J. Figueras, “SRAM Cell Stability Metric under Transient Voltage Noise,” *Microelectronics Journal*, vol. 45, no. 10, pp. 1348–1353, October 2014.

**[J02]** A. Gómez-Pau, L. Balado, and J. Figueras, “Diagnosis of Parametric Defects in Dual Axis IC Accelerometers,” *Microsystem Technologies Journal*, vol. 21, no. 9, pp. 1855–1866, September 2015.

**[J03]** A. Gómez-Pau, L. Balado, and J. Figueras, “Efficient Production Binning Using Octree Tessellation in the Alternate Measurements Space,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 8, pp. 1386–1395, August 2016.

**[J04]** A. Gómez-Pau, L. Balado, and J. Figueras, “Indirect Test of M-S Circuits Using Multiple Specification Band Guarding,” *Integration, the VLSI Journal*, vol. 55, pp. 415–424, September 2016.

**[J05]** A. Gómez-Pau, L. Balado, and J. Figueras, “Multi-Directional Space Tessellation to Improve the Decision Boundary in Indirect Mixed-Signal Testing,” *Journal of Electronic Testing*, February 2017, already available online.


## Refereed Conferences and Workshops


**[C01]** R. Sanahuja, A. Gómez, L. Balado, and J. Figueras, “Digital Signature Generator for Mixed-Signal Testing,” in *Proceedings of IEEE European Test Symposium (ETS)*, Seville, Spain, May 2009.

**[C02]** A. Gómez, R. Sanahuja, L. Balado, and J. Figueras, "Verifying Analog Circuits Based on a Digital Signature," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Zaragoza, Spain, November 2009.

**[C03]** A. Gómez, R. Sanahuja, L. Balado, and J. Figueras, "Analog Circuit Test Based on a Digital Signature," in *Proceedings of IEEE Design Automation and Test in Europe Conference (DATE)*, Dresden, Germany, March 2010, pp. 1641–1644.

**[C04]** A. Gómez-Pau, R. Sanahuja, L. Balado, and J. Figueras, "Identification of Component Deviations in Analog Circuits Using Digital Signatures," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Lanzarote, Spain, November 2010.

**[C05]** A. Gómez-Pau, L. Balado, and J. Figueras, "Testing IC Accelerometers Using Lissajous Compositions," in *Proceedings of International Perspective Technologies and Methods in MEMS Design Conference (MEMSTECH)*, Polyana, Ukraine, May 2011, pp. 75–81.

**[C06]** A. Gómez-Pau, L. Balado, and J. Figueras, "Testing Dual Axis IC Accelerometers Using Lissajous Compositions," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Albufeira, Portugal, November 2011.

**[C07]** E. I. Vatajelu, A. Gómez-Pau, M. Renovell, and J. Figueras, "Transient Noise Failures in SRAM Cells: Dynamic Noise Margin Metric," in *Proceedings of IEEE Asian Test Symposium (ATS)*, New Delhi, India, November 2011, pp. 413–418.

**[C08]** A. Gómez-Pau, R. Sanahuja, L. Balado, and J. Figueras, "Built-In Test of MEMS Capacitive Accelerometers for Field Failures and Aging Degradation," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Avignon, France, November 2012.

**[C09]** E. I. Vatajelu, A. Gómez-Pau, M. Renovell, and J. Figueras, "SRAM Stability Metric under Transient Noise," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Avignon, France, November 2012.

**[C10]** A. Gómez-Pau, L. Balado, and J. Figueras, "Nondestructive Diagnosis of Mechanical Misalignments in Dual Axis Accelerometers," in *Proceedings of Design, Test, Integration & Packaging of MEMS/MOEMS (DTIP)*, Barcelona, Spain, April 2013, pp. 229–234.

**[C11]** A. Gómez-Pau, L. Balado, and J. Figueras, "M-S Test Based on Specification Validation using Octrees in the Measure Space," in *Proceedings of IEEE European Test Symposium (ETS)*, Avignon, France, May 2013, pp. 70–75.

**[C12]** A. Gómez-Pau, L. Balado, and J. Figueras, "Test of Dual Axis Accelerometers Based on Specifications Compliance," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, San Sebastián, Spain, November 2013.

**[C13]** A. Gómez-Pau, L. Balado, and J. Figueras, "M-S Specification Binning Based on Digitally Coded Indirect Measurements," in *Proceedings of IEEE European Test Symposium (ETS)*, Paderborn, Germany, May 2014, pp. 105–110.

**[C14]** S. Banerjee, A. Gómez-Pau, and A. Chatterjee, "Design of Low Cost Fault Tolerant Analog Circuits Using Real-Time Learned Error Compensation," in *Proceedings of IEEE European Test Symposium (ETS)*, Paderborn, Germany, May 2014, pp. 229–230.

**[C15]** A. Gómez-Pau, L. Balado, and J. Figueras, "Criteria for Indirect Measurements in M-S Testing," in *Proceedings of Statistical Test Methods Workshop (STEM)*, Paderborn, Germany, May 2014.

**[C16]** A. Gómez-Pau, L. Balado, J. Figueras, and A. Chatterjee, "An Efficient Behavioral Description Frontend Tool for Mixed-Mode SPICE Simulation," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, 2014.

**[C17]** A. Gómez-Pau, S. Banerjee, and A. Chatterjee, "Real-Time Transient Error and Induced Noise Cancellation in Linear Analog Filters Using Learning-Asisted Adaptive Analog Checksums," in *Proceedings of IEEE International On-Line Testing Symposium (IOLTS)*, Platja d'Aro, Spain, July 2014, pp. 25–30.

**[C18]** A. Gómez-Pau, L. Balado, and J. Figueras, "Quality Metrics for Mixed-Signal Indirect Testing," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Madrid, Spain, November 2014.

**[C19]** S. Banerjee, A. Gómez-Pau, A. Chatterjee, and J. A. Abraham, "Error Resilient Real-Time State Variable Systems Signal Processing and Control," in *Proceedings of IEEE Asian Test Symposium (ATS)*, Hangzhou, China, November 2014, pp. 39–44, invited paper.

**[C20]** A. Gómez-Pau, L. Balado, and J. Figueras, "Analog Circuits Testing Using Digitally Coded Indirect Measurements," in *Proceedings of IEEE Design and Technology of Integrated Systems Conference (DTIS)*, Naples, Italy, April 2015.

**[C21]** A. Gómez-Pau, L. Balado, and J. Figueras, "Mixed-Signal Test Band Guarding Using Digitally Coded Indirect Measurements," in *Proceedings of International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, Istanbul, Turkey, September 2015.

**[C22]** A. Gómez-Pau, E. Lupon, L. Balado, and J. Figueras, "Adaptive Test System Applied to the Generation of Mixed-Signal Signatures," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Estoril, Portugal, November 2015, **Best Paper Award**.

**[C23]** A. Gómez-Pau, L. Balado, and J. Figueras, "Mixed-Signal Circuits Testing Using Digitally Coded Indirect Measurements," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Estoril, Portugal, November 2015, special session on Alternate Test.

**[C24]** A. Gómez-Pau, L. Balado, and J. Figueras, "Improving Indirect Test Efficiency Using Multi-Directional Tessellations in the Measure Space," in *Proceedings of International Mixed-Signal Testing Workshop (IMSTW)*, Sant Feliu de Guíxols, Spain, July 2016, **Best PhD Student Paper Award**.

**[C25]** A. Gómez-Pau, L. Balado, and J. Figueras, "Criteria for Selecting a Subset of Indirect Measurements for Analog Testing," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Granada, Spain, November 2016.

# Bibliography


[1] L. Milor, "A tutorial introduction to research on analog and mixed-signal circuit testing," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 45, no. 10, pp. 1389–1407, October 1998.

[2] T. J. Hastie, R. J. Tibshirani, and J. H. Friedman, *The elements of statistical learning : data mining, inference, and prediction*, ser. Springer series in statistics. New York: Springer, 2009.

[3] E. Yilmaz, S. Ozev, and K. Butler, "Adaptive quality binning for analog circuits," in *Test Symposium (ETS), 2013 18th IEEE European*, May 2013, pp. 1–6.

[4] S. Callegari, F. Pareschi, G. Setti, and M. Soma, "Complex oscillation-based test and its application to analog filters," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 57, no. 5, pp. 956–969, May 2010.

[5] F. Liu, E. Acar, and S. Ozev, "Test yield estimation for analog/rf circuits over multiple correlated measurements," in *Test Conference, 2007. ITC 2007. IEEE International*, October 2007, pp. 1–10.

[6] "International technology roadmap for semiconductors (update)," 2015, http://www.itrs2.net.

[7] H.-G. Stratigopoulos and Y. Makris, "Error moderation in low-cost machine-learning-based analog/rf testing," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 27, no. 2, pp. 339–351, 2008.

[8] P. Variyam and A. Chatterjee, "Enhancing test effectiveness for analog circuits using synthesized measurements," in *VLSI Test Symposium, 1998. Proceedings. 16th IEEE*, April 1998, pp. 132–137.

[9] P. N. Variyam and A. Chatterjee, "Specification-driven test generation for analog circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1189–1201, 2000.

[10] V. Stopjakova, P. Malosek, D. Micusik, M. Matej, and M. Margala, "Classification of defective analog integrated circuits using artificial neural networks," *Journal of Electronic Testing*, vol. 20, no. 1, pp. 25–37, 2004.

[11] H. G. Stratigopoulos and S. Mir, "Adaptive alternate analog test," *IEEE Design Test of Computers*, vol. 29, no. 4, pp. 71–79, August 2012.

[12] A. Bounceur, S. Mir, and H.-G. Stratigopoulos, "Estimation of analog parametric test metrics using copulas," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 30, no. 9, pp. 1400–1410, September 2011.

[13] D. Meagher, "Octree encoding: A new technique for the representation, manipulation and display of arbitrary 3-d objects by computer," Rensselaer Polytechnic Institute, New York, techreport, 1980.

[14] S. Biswas and R. D. Blanton, "Statistical test compaction using binary decision trees," *IEEE Design Test of Computers*, vol. 23, no. 6, pp. 452–462, June 2006.

[15] V. Natarajan, S. Bhattacharya, and A. Chatterjee, "Alternate electrical tests for extracting mechanical parameters of mems accelerometer sensors," in *VLSI Test Symposium, 2006. Proceedings. 24th IEEE*, May 2006, p. 6pp.

[16] J. H. Friedman, "Multivariate adaptive regression splines," *Ann. Statist.*, vol. 19, no. 1, pp. 1–67, 03 1991.

[17] J. H. Friedman, "Fast mars," Department of Statistics, Stanford University, techreport 110, 1993.

[18] S. W. Hsiao, X. Wang, and A. Chatterjee, "Analog sensor based testing of phase-locked loop dynamic performance parameters," in *2013 22nd Asian Test Symposium*, November 2013, pp. 50–55.

[19] L. Abdallah, H. G. Stratigopoulos, and S. Mir, "True non-intrusive sensors for rf built-in test," in *2013 IEEE International Test Conference (ITC)*, September 2013, pp. 1–10.

[20] S. Larguech, F. Azais, S. Bernard, M. Comte, V. Kerzerho, and M. Renovell, "A generic methodology for building efficient prediction models in the context of alternate testing," in *2015 IEEE 20th International Mixed-Signals Testing Workshop (IMSTW)*, June 2015, pp. 1–6.

[21] G. Gielen and R. Rutenbar, "Computer-aided design of analog and mixed-signal integrated circuits," *Proceedings of the IEEE*, vol. 88, no. 12, pp. 1825–1854, December 2000.

[22] D. Maliuk and Y. Makris, "A dual-mode weight storage analog neural network platform for on-chip applications," in *2012 IEEE International Symposium on Circuits and Systems*, May 2012, pp. 2889–2892.

[23] G. Volanis, A. Antonopoulos, A. A. Hatzopoulos, and Y. Makris, "Toward silicon-based cognitive neuromorphic ics - a survey," *IEEE Design Test*, vol. 33, no. 3, pp. 91–102, June 2016.

[24] W. S. Mcculloch and W. H. Pitts, "A logical calculus of the ideas immanent in nervous activity," *Bulletin of Mathematical Biophysics*, vol. 5, pp. 115–133, 1943.

[25] C. Moewes and A. Nürnberger, *Computational Intelligence in Intelligent Data Analysis*, ser. Studies in Computational Intelligence (SCI). Berlin Heidelberg: Springer-Verlag, 2013, vol. 445.

[26] H. G. D. Stratigopoulos and Y. Makris, "Nonlinear decision boundaries for testing analog circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, pp. 1760–1773, November 2005, issue 11.

[27] C. Cortes and V. Vapnik, "Support-vector networks," *Machine Learning*, vol. 20, no. 3, pp. 273–297, September 1995.

[28] K. Huang, J. Carulli, and Y. Makris, "Counterfeit electronics: A rising threat in the semiconductor manufacturing industry," in *Test Conference (ITC), 2013 IEEE International*, September 2013, pp. 1–4.

[29] N. Deb and R. D. Blanton, "Multi-modal built-in self-test for symmetric microsystems," in *Proceedings of the 22nd VLSI Test Symposium*, May 2004.

[30] N. Deb and R. Blanton, "Analysis of failure sources in surface-micromachined mems," in *Test Conference, 2000. Proceedings. International*, 2000, pp. 739–749.

[31] R. Rosing, A. Lechner, A. Richardson, and A. Dorey, "Fault simulation and modelling of microelectromechanical systems," *Computing and Control Engineering Journal*, vol. 11, no. 5, pp. 242–250, 2000.

[32] A. Castillejo, D. Veychard, S. Mir, J. M. Karam, and B. Courtois, "Failure mechanisms and fault classes for cmos-compatible microelectromechanical systems," in *Proceedings of the International Test Conference*, 1998, pp. 541–550.

[33] A. Rekik, F. Azais, N. Dumas, F. Mailly, and P. Nouet, "An electrical test method for mems convective accelerometers: Development and evaluation," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2011*, March 2011, pp. 1–6.

[34] A. Kolpekwar, T. Jiang, and R. Blanton, "Caramel: Contamination and reliability analysis of microelectromechanical layout," *Microelectromechanical Systems, Journal of*, vol. 8, no. 3, pp. 309–318, September 1999.

[35] A. Soma and G. De Pasquale, "Reliability of mems: Effects of different stress conditions and mechanical fatigue failure detection," in *Proceedings of International Perspective Technologies and Methods in MEMS Design Conference (MEMSTECH)*, 2010, pp. 72–80.

[36] L. Zimmermann and et. al., "Airbag application: a microsystem including a silicon capacitive accelerometer, cmos switched capacitor electronics and true self-test capability," *Sensors and Actuators*, vol. 1, no. 3, pp. 190–195, January 1995.

[37] A. A. Rekik, F. Azais, N. Dumas, F. Mailly, and P. Nouet, "Modeling the influence of etching defects on the sensitivity of mems convective accelerometers," in *Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW)*, June 2010, pp. 1–6.

[38] H. Weinberg, "Dual axis, low g fully integrated accelerometers," *Analogue Dialog*, vol. 33, no. 1, pp. 1–2, 1999.

[39] B. Charlot, S. Mir, F. Parrain, and B. Courtois, "Electrically induced stimuli for mems self-test," in *VLSI Test Symposium, 19th IEEE Proceedings on. VTS 2001*, 2001, pp. 210–215.

[40] R. Puers and S. Reynthens, "Rasta: Real-acceleration-for-self-test accelerometer: A new concept for self-testing accelerometers," *Journal of Sensors and Actuators*, vol. 97–98, pp. 97–98, April 2002.

[41] S. Mir, L. Rufer, and A. Dhayni, "Built-in-self-test techniques for mems," *Microelectronics Journal*, vol. 37, no. 12, pp. 1591–1597, December 2006.

[42] S. Dasnurkar and J. Abraham, "Characterization and testing of microelectromechnical accelerometers," in *Mixed-Signals, Sensors, and Systems Test Workshop, 2008. IMS3TW 2008. IEEE 14th International*, June 2008, pp. 1–6.

[43] X. Xiong, Y.-L. Wu, and W.-B. Jone, "A dual-mode built-in self-test technique for capacitive mems devices," in *VLSI Test Symposium, 2004. Proceedings. 22nd IEEE*, April 2004, pp. 148–153.

[44] L. Ciganda Brasca, P. Bernardi, M. Sonza Reorda, D. Barbieri, L. Bonaria, R. Losco, L. Marcigot, and M. Straiotto, "A parallel tester architecture for accelerometer and gyroscope mems calibration and test," *Journal of Electronic Testing*, vol. 27, no. 3, pp. 389–402, 2011.

[45] N. Dumas, F. Azais, F. Mailly, and P. Nouet, "Evaluation of a fully electrical test and calibration method for mems capacitive accelerometers," in *Proceedings of International Mixed-Signals, Sensors and Systems Test Workshop*, Vancouver, Canada, June 2008.

[46] L. Rufer, S. Mir, E. Simeu, and C. Domingues, "On-chip pseudorandom mems testing," *Journal of Electronic Testing: Theory and Applications*, vol. 21, no. 3, pp. 233–241, June 2005.

[47] J. Yang, W. Wu, Y. Wu, and J. Lian, "Thermal calibration for the accelerometer triad based on the sequential multiposition observation," *IEEE Transactions on Instrumentation and Measurement*, vol. 62, no. 2, pp. 467–482, February 2013.

[48] S. Kar, K. Swamy, B. Mukherjee, and S. Sen, “Testing of mems capacitive accelerometer structure through electro-static actuation,” *Microsystem Technologies*, vol. 19, no. 1, pp. 79–87, 2013.

[49] M. Gong, H. Zhou, L. Li, J. Tao, and X. Zeng, “Binning optimization for transparently-latched circuits,” *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 30, no. 2, pp. 270–283, February 2011.

[50] Z. Pan and M. Breuer, “Estimating error rate in defective logic using signature analysis,” *Computers, IEEE Transactions on*, vol. 56, no. 5, pp. 650–661, May 2007.

[51] A. Davoodi and A. Srivastava, “Variability driven gate sizing for binning yield optimization,” *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 16, no. 6, pp. 683–692, June 2008.

[52] S. Lichtensteiger and J. Bickford, “Using selective voltage binning to maximize yield,” *Semiconductor Manufacturing, IEEE Transactions on*, vol. 26, no. 4, pp. 436–441, November 2013.

[53] R. Shen, S.-D. Tan, and X.-X. Liu, “A new voltage binning technique for yield improvement based on graph theory,” in *Quality Electronic Design (ISQED), 2012 13th International Symposium on*, March 2012, pp. 243–248.

[54] E. Yilmaz and S. Ozev, “Test application for analog/rf circuits with low computational burden,” *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 31, no. 6, pp. 968–979, June 2012.

[55] R. Voorakaranam, S. S. Akbay, S. Bhattacharya, S. Cherubal, and A. Chatterjee, “Signature testing of analog and rf circuits: Algorithms and methodology,” *IEEE Transactions on Circuits and Systems*, vol. 54, pp. 1018–1031, 2007.

[56] S. Devarakond, S. Sen, S. Bhattacharya, and A. Chatterjee, “Concurrent device/specification cause-effect monitoring for yield diagnosis using alternate diagnostic signatures,” *Design Test of Computers, IEEE*, vol. 29, no. 1, pp. 48–58, February 2012.

[57] H. Ayari, F. Azais, S. Bernard, M. Comte, V. Kerzerho, O. Potin, and M. Renovell, “Making predictive analog/rf alternate test strategy independent of training set size,” in *Test Conference (ITC), 2012 IEEE International*, November 2012, pp. 1–9.

[58] A. Gómez-Pau, L. Balado, and J. Figueras, “M-S Test Based on Specification Validation using Octrees in the Measure Space,” in *Proceedings of IEEE European Test Symposium (ETS)*, Avignon, France, May 2013, pp. 70–75.

[59] K. Huang, N. Kupp, C. Xanthopoulos, J. Carulli, and Y. Makris, “Low-cost analog/rf ic testing through combined intra- and inter-die correlation models,” *Design Test, IEEE*, vol. 32, no. 1, pp. 53–60, February 2015.

[60] A. Chatterjee and S. Cherubal, "Method for diagnosing process parameter variations from measurements in analog circuits," June 2002, uS Patent App. 09/838, 404.

[61] S. Larguech, F. Azaïs, S. Bernard, M. Comte, V. Kerzérho, and M. Renovell, "Efficiency evaluation of analog/rf alternate test: Comparative study of indirect measurement selection strategies," *Microelectronics Journal*, vol. 46, no. 11, pp. 1091–1102, 2015.

[62] M. Barragan and G. Leger, "Efficient selection of signatures for analog/rf alternate test," in *Test Symposium (ETS), 2013 18th IEEE European*, May 2013, pp. 1–6.

[63] M. Barragan and G. Leger, "A procedure for alternate test feature design and selection," *Design Test, IEEE*, vol. 32, no. 1, pp. 18–25, February 2015.

[64] H. Medellin, J. Corney, J. Davies, T. Lim, and J. Ritchie, "Octree-based production of near net shape components," *Automation Science and Engineering, IEEE Transactions on*, vol. 5, no. 3, pp. 457–466, July 2008.

[65] A. Gómez-Pau, L. Balado, and J. Figueras, "Efficient Production Binning Using Octree Tessellation in the Alternate Measurements Space," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 8, pp. 1386–1395, August 2016.

[66] T. H. Cormen, C. E. Leiserson, R. L. Rivest, and C. Stein, *Introduction to Algorithms, Third Edition*, 3rd ed. The MIT Press, 2009.

[67] A. Gómez-Pau, L. Balado, and J. Figueras, "Diagnosis of Parametric Defects in Dual Axis IC Accelerometers," *Microsystem Technologies Journal*, vol. 21, no. 9, pp. 1855–1866, September 2015.

[68] L. Balado, E. Lupon, J. Figueras, M. Roca, E. Isern, and R. Picos, "Verifying functional specifications by regression techniques on lissajous test signatures," *Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 4, pp. 754–762, April 2009.

[69] A. Gómez, R. Sanahuja, L. Balado, and J. Figueras, "Analog Circuit Test Based on a Digital Signature," in *Proceedings of IEEE Design Automation and Test in Europe Conference (DATE)*, Dresden, Germany, March 2010, pp. 1641–1644.

[70] A. M. Brosa and J. Figueras, "Digital signature proposal for mixed-signal circuits," in *Proceedings of the International Test Conference*, Atlantic City, USA, October 2000, pp. 1041–1050.

[71] A. Gómez-Pau, R. Sanahuja, L. Balado, and J. Figueras, "Identification of Component Deviations in Analog Circuits Using Digital Signatures," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Lanzarote, Spain, November 2010.

[72] A. Gómez-Pau, L. Balado, and J. Figueras, "Nondestructive Diagnosis of Mechanical Misalignments in Dual Axis Accelerometers," in *Proceedings of Design, Test, Integration & Packaging of MEMS/MOEMS (DTIP)*, Barcelona, Spain, April 2013, pp. 229–234.

[73] A. Singhee and R. Rutenbar, "Statistical blockade: A novel method for very fast monte carlo simulation of rare circuit events, and its application," in *Design, Automation Test in Europe Conference Exhibition*, April 2007.

[74] A. Singhee and R. Rutenbar, "Statistical blockade: Very fast statistical simulation and modeling of rare circuit events and its application to memory design," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 28, no. 8, pp. 1176–1189, August 2009.

[75] D. Hocevar, M. Lightner, and T. N. Trick, "A study of variance reduction techniques for estimating circuit yields," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 2, no. 3, pp. 180–192, July 1983.

[76] H. Stratigopoulos, S. Mir, and A. Bounceur, "Evaluation of analog/rf test measurements at the design stage," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 28, no. 4, pp. 582–590, April 2009.

[77] ST-Microelectronics, "Cmos065 design rule manual. 65 nm bulk cmos process," 2013, version 5.3.6.

[78] P. Mohan, *VLSI Analog Filters: Active RC, OTA-C, and SC*, ser. Modeling and Simulation in Science, Engineering and Technology. Springer, 2012.

[79] N. Nagi, A. Chatterjee, H. Yoon, and J. Abraham, "Signature analysis for analog and mixed-signal circuit test response compaction," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 17, no. 6, pp. 540–546, June 1998.

[80] H. Ayari, F. Azais, S. Bernard, M. Comte, M. Renovell, V. Kerzerho, O. Potin, and C. Kelma, "Smart selection of indirect parameters for dc-based alternate rf ic testing," in *VLSI Test Symposium (VTS), 2012 IEEE 30th*, April 2012, pp. 19–24.

[81] M. G. Kendall, "A new measure of rank correlation," *Biometrika*, vol. 30, no. 1/2, pp. 81–93, June 1938.

[82] A. Gómez-Pau, L. Balado, and J. Figueras, "Quality Metrics for Mixed-Signal Indirect Testing," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Madrid, Spain, November 2014.

[83] K. Beznia, A. Bounceur, R. Euler, and S. Mir, "A tool for analog/rf bist evaluation using statistical models of circuit parameters," *ACM Trans. Des. Autom. Electron. Syst.*, vol. 20, no. 2, pp. 31:1–31:22, March 2015.

[84] K. Lee, *Principles of Microelectromechanical Systems.* Wiley, 2011.

[85] *ADXL203 dual axis accelerometer datasheet*, Analog Devices, 2010.

[86] A. Gómez-Pau, L. Balado, and J. Figueras, “Testing Dual Axis IC Accelerometers Using Lissajous Compositions,” in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Albufeira, Portugal, November 2011.

[87] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, 3rd ed. New York, NY, USA: McGraw-Hill, Inc., 2002.

[88] A. Gómez-Pau, L. Balado, and J. Figueras, “Indirect Test of M-S Circuits Using Multiple Specification Band Guarding,” *Integration, the VLSI Journal*, vol. 55, pp. 415–424, September 2016.

[89] A. Gómez-Pau, L. Balado, and J. Figueras, “Mixed-Signal Test Band Guarding Using Digitally Coded Indirect Measurements,” in *Proceedings of International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, Istanbul, Turkey, September 2015.

[90] H. G. Dimopoulos, *Analog Electronic Filters. Theory, Design and Synthesis.* New York: Springer, 2012.

[91] G. Leger and M. J. Barragan, “Brownian distance correlation-directed search: A fast feature selection technique for alternate test,” *Integration, the VLSI Journal*, pp. –, 2016.

[92] T. W. Anderson and D. A. Darling, “Asymptotic theory of certain “goodness of fit” criteria based on stochastic processes,” *Ann. Math. Statist.*, vol. 23, no. 2, pp. 193–212, 06 1952.

[93] E. Lupon and L. Balado, “Digital/analogue converter architectures for digital asics: A performance comparison,” in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Barcelona, November 1996.