UNIVERSITAT DE BARCELONA

Wideband pulse amplifiers for the integrated cameras of the Cherenkov Telescope Array

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This thesis was submitted to the Faculty of Physics, University of Barcelona (UB), as a fulfillment of the requirements to obtain the PhD degree. The work presented was carried out in the years 2010-2015 in the Department of Electronics at UB with the help of my advisor David Gascón.

Short abstract: This thesis is focused on novel design circuitry for the channel signal path of a Cherenkov Telescope camera. The amplification is divided into gain stages in order to achieve the requirements of the design. The first stage, presents an innovative low noise wideband pre-amplifier design whereas, the second amplification stage proposes a novel gain circuitry design, being impossible with the classic schemes at the required technology. This second stage also derives and adapts the signal to the following parts of the read-out system of the Cherenkov Telescope camera.

An innovative design that achieves all the restrictions with very low power consumption fulfills the requirements for the first pre-amplification stage. The solution selected is based on a novel current mode circuit to create multiple gain paths at the very front end of the input stage of the readout electronics, simultaneously achieving high dynamic range, low noise, low input impedance, low voltage and low power performances.

The pre-amplification stage also comprises a closed loop transimpedance amplifier with a novel class AB output stage designed with a $0.35\mu m$ SiGe technology, allowing the design to drive a cable or a transmission line (typ. 50Ω load) while preserving high bandwidth with moderate power consumption.

This thesis presents an alternative method to implement fully differential wideband pulse amplifiers. The required gain can be reached, while preserving also the bandwidth. Linearity for fast pulses is at the level of solutions based on feedback OTA, limited by slew rate and other transient issues. The design exhibits a large degree of tuneability. An amplifier in a $0.35\mu m$ CMOS technology implements and validates the GBW product of 8 GHz. This design also incorporates a closed loop transimpedance amplifier with a novel class AB output stage based on the design of the first amplification stage, but designed in a $0.35\mu m$ CMOS technology which is more difficult to achieve.

Keywords: Microelectronics design, silicon technology microelectronics, integrated circuits, telescopes.

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Agraïments

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Resum

Els raig còsmics son bàsicament radiacions d'alta energia principalment originats fora del Sistema Solar. Aquestes fonts còsmiques poden causar emissions de raig γ mitjançant diferents mecanismes d'acceleració astronòmica com ara el sincrotró entre d'altres [5].

Actualment existeixen dues tècniques per observar els raig γ procedents de l'espai exterior: l'observació directa mitjançant detectors de partícules a bord dels satèl·lits, i la detecció indirecta per mitjà de detectors terrestres que utilitzen la tècnica Cherenkov.

L'atmosfera absorbeix la major part de la radiació gamma. Per tant, es fa impossible la detecció directa de raigs γ a la superfície de la terra. No obstant això, és possible detectar l'efecte dels raigs γ en l'atmosfera. Quan un raigs γ primari interactua inicialment amb una molècula de l'atmosfera, aquest genera un parell electró-positró. D'aquesta manera es crea una dutxa d'aire estès (EAS), que origina l'emissió de fotons Cherenkov.

La detecció de la llum Cherenkov corresponent a una dutxa generada per uns raigs γ a l'atmosfera no és una tasca fàcil. L'àrea que cobreix la dutxa de llum Cherenkov és molt tènue, amb imatges de no més d'uns pocs milers de fotons, i de durada molt curta entre 2,5 i diverses desenes de nano segons. Això fa necessari l'ús de fotodetectors molt sensibles i ràpids, així com electrònica de baix soroll i també ràpida, capaç de detectar i guardar les imatges rellevants. Aquestes deteccions es realitzen mitjançant l'ús de telescopis d'imatges Cherenkov atmosfèriques (IACTs).

Observar la dutxa de raigs γ amb més d'un IACT al mateix temps permet l'ús de la estereoscopia amb la finalitat de poder reconstruir la dutxa en imatges de 3 dimensions [6], [7].

El següent pas de la comunitat internacional d'astronomia de raigs γ consisteix en la construcció d'un gran conjunt amb molts IACTs, utilitzant l'última tecnologia puntera per construir els millors telescopis fins a l'actualitat, i per tant cobrir tot l'espectre dels raigs γ de totes les fonts en existent en el cel. Aquest és l'objectiu del consorci Cherenkov Telescope Array (CTA) citeCTAweb.

Els telescopis IACTs es basen típicament en una estructura mecànica amb un sistema de mirall reflector que recull els fotons de les dutxes i les reflecteix cap a la càmera.

Com que les dutxes Cherenkov duren només uns pocs nano segons, és important assegurar-se que, d'una banda, els fotons capturats en els IACTs que s'han generat al mateix temps, arriben a la càmera en el mateix intent de temps. Això requereix l'ús de reflectors parabòlics tessel·lats formant una parabòlica, de manera que la longitud dels camins que els fotons han de viatjar sigui la mateixa. D'altra banda, els fotodetectors utilitzats en les càmeres IACT han de ser molt sensibles per tal de poder detectar la major proporció possible dels

fotons que entrin mitjançant una alta eficiència de detecció de fotons (PDE). Aquests fotons detectats generalment s'anomenen electrons de fotos (PE).

Es pretén construir tres tipus de telescopis (els anomenats telescopis de mida petita (TSM), els telescopis de mida mitjana (MST) i els telescopis de mida gran (LSTs)) amb diferents mides dels seus miralls reflectors, optimitzats per cobrir els diferents règims d'espectre d'energia [8].

Un dels tipus de detectors de fotons és el tub fotomultiplicador (PMT), i correspon al més utilitzats en els IACTs. Un PMT té un càtode fotoelèctric que absorbeix la llum i emet un electró. Un PMT també conté altres elèctrodes de forma consecutiva anomenats dinodes. Cada dinode es manté a un voltatge positiu més alt que el seu predecessor. Els electrons són atrets per cada dinode successivament, i al impactar-hi es desprenen diversos electrons addicionals per a cada impacte. Com el corrent d'electrons es desplaça de dinode en dinode, es genera finalment una cascada electrons.

Els PMTs aconsegueixen sensibilitats prou bones com per a poder mesurar fotons individualment. Tenen poc soroll en la foscor, però de vegades generen fotons sense haver rebut cap tipus de llum a causa del corrent de foscor, o generen més d'un impuls per a un mateix fotó després d'una cascada d'electrons. Funcionen amb rangs de longituds d'ona sensibles en l'ultraviolat (UV) i l'infraroig (IR) que corresponen amb les dutxes de llum Cherenkov. També tenen una resposta molt ràpida al nivell de nano segons, per contra, els electrons no es generen en tots els dinodes al mateix temps, sinó que es generen amb una certa dispersió en el temps que depèn del nombre de dinodes, l'alta tensió aplicada i altres paràmetres.

Els polsos generats pels fotosensors (normalment PMTs) son molt estrets i han de poder-se mostrejar d'una forma molt ràpida per tal de ser capaços de determinar amb una alta precisió instant d'arribada, i poder integrar la seva càrrega en una finestra de temps prou estreta que permeti reduir la contribució induïda pel soroll de fons degut a la llum cel durant la nit (NSB). Una amplada típica de l'impuls d'un PMT de 2.5 ns necessita mostrejar-se a 800 MHz d'acord amb el teorema de Nyquist, obtenint una freqüència de mostreig de 1 Gs/s. Tenint en compte que una càmera IACT pot tenir al voltant de 1.000 píxels i 8 nivells de quantificació, enregistrar de forma contínua els senyals de tots els píxels d'una càmera significaria una taxa de dades d'1 TB/s, el qual resultaria immanejable. En lloc d'això, els IACTs actuals únicament enregistren de forma contínua quan es detecta un esdeveniment interessant. Per tal d'aconseguir fer això, s'utilitza un sistema d'adquisició de dades basat en memòries analògiques juntament amb un complex sistema de desencadenament.

Aquest memòries analògiques mostregen els senyals d'entrada a una alta freqüència de mostreig, però amb petits acumuladors muntats en una determinada configuració d'anell. L'opció de l'electrònica de part davantera (FE) en la col·laboració NECTAr (Nova Electrònica per al conjunt CTA) per a les càmeres de CTA (que és on està centrada aquesta tesi) està realitzat en un xip de mostreig de 16 bits d'entre 1 i 3 GS/s i que es basa en memòries

analògiques, incloent-hi la major part de les funcions de lectura [9].

El sistema de desencadenament analitza cada pols i decideix si el senyal correspon a un esdeveniment de Cherenkov vàlid per a ser emmagatzemada o no. L'estratègia bàsica del complex sistema de desencadenament és, en un primer nivell, activar inicialment un grup de píxels veïns (disparador de nivell 0 o L0) i després fer-ho a nivell de la càmera sencera (nivell 1 o L1 i possiblement nivell 2 o L2). La decisió final és pren pel sistema disparador a nivell de matriu de telescopis [10].

Com que els polsos ràpids procedents d'un PMT requereixen una sistema de lectura ràpid [11] aquests es llegeixen mitjançant un preamplificador amb un gran ample de banda (BW), un alt rang dinàmic (DR) i de baix soroll. El preamplificador ha d'estar a prop del fotosensor connectat amb un cable o una línia de transmissió a l'electrònica FE. D'acord amb simulacions de Monte Carlo [12] el BW analògic del sistema complet ha de ser d'almenys 300 MHz, per la qual cosa el BW del preamplificador ha de ser d'aproximadament 500 MHz. Es requereix un DR de 16 bits d'una banda per a poder mesurar el senyal d'un sol foto-electró (SPE) amb finalitats de calibratge, i d'altra banda per a poder mesurar polsos més alts de llum de fins a 5000 PE. Atès que el PMT ha de funcionar a un guany baix (40 K) per tal d'evitar problemes d'envelliment, aconseguir una bona resolució en la mesura del SPE imposa requisits de baix soroll. El soroll de càrrega equivalent de $(ENC) < 4Ke$ significa que la densitat espectral de potència (PSD) del soroll de corrent referenciat a l'entrada ha de ser menor de $10pA/\sqrt{Hz}$ per a una lectura en mode corrent. Per a la implementació integrada del preamplificador es necessari una impedància d'entrada baixa i un punt d'operació de voltatge baix per tal d'aconseguir un gran BW.

D'acord amb els requisits del consorci CTA, les especificacions de la càmera per als diferents telescopis necessiten circuits electrònics dedicats fora de les especificacions dels components comercials que hi ha disponibles en el mercat. Per motius d'efectivitat en el cost i la innovació tècnica en l'estat de l'art, s'han desenvolupat diversos circuits integrats d'aplicació específica (ASICs) completament personalitzats. L'objectiu d'aquesta tesi és el desenvolupament d'un canal d'amplificació complert per poder injectar els polsos ràpids procedents dels sensors de la càmera cap les memòries analògiques del circuit digitalitzador. En base a les grans restriccions del canal d'amplificació per al projecte CTA, s'han aplicat noves tecnologies per tal de cobrir per una banda, el BW requerit pel baix nivell de soroll que es necessita i d'altra banda disminuir el consum d'energia necessari tant com sigui possible.

Aquesta tesi es centra en el disseny de l'etapa amplificadora per als telescopis LST i MST en la primera etapa d'amplificació (preamplificador), i també en una segona etapa d'amplificació i condicionament de la senyal per als telescopis MST.

La primera etapa d'amplificació es basa en un preamplificador en mode corrent de banda ampla amb 16 bits de DR. En aquesta tesi es proposa un nou circuit en mode corrent per tal de superar la limitació del senyal màxim mitjançant la creació de diversos camins de guany

en la primera part de l'etapa d'entrada. El corrent d'entrada es divideix en l'etapa d'entrada en base comuna en dues (o més) corrents de sortida escalades. Després, cada corrent es llegeix en un mirall de corrent dedicat que pot ser optimitzat per a diferents situacions. El mirall de corrent de guany alt requereix circuits específics de control de saturació per tal d'assegurar que la divisió de corrent segueix sent prou precisa fins i tot si aquest mirall de corrent es satura. Finalment, el senyal de corrent es converteix en voltatge mitjançant un amplificador de transimpedància de llaç tancat.

El xip pre-amplificador per CTA (PACTA) compleix els requisits generals del projecte CTA en base a un disseny innovador que aconseguir superar totes les restriccions amb un molt baix consum d'energia. S'han dissenyats i provats versions tant de composició única com diferencials. El consum d'energia de les solucions alternatives basades en components comercials COTS que es van provar per als prototips de les càmeres dels telescopis de CTA es van descartar ja que tenien consums de com a mínim 4 vegades més gran.

La col·laboració nèctar [13] té la intenció de construir un nou circuit integrat que inclou la major part dels components discrets necessaris fins ara i correspon a una de les opcions de FE considerades per a les càmeres CTA [11]. Una millora en els costos, la fiabilitat i les prestacions de la càmera s'aconsegueix mitjançant la maximització en la integració de la electrònica de FE en un ASIC, en un sol xip de mostreig a GHz.

Una solució de llaç totalment tancat basat en amplificadors de tensió en realimentació (OTA o OpAmp) no és factible ja que es requereix un producte de guany per ample de banda (GBW) de més de 8 GHz, mentre que el producte GBW màxim que es pot aconseguir en tecnologia CMOS de 0,35 μm està molt per sota d'1 GHz ([14], [15]). En aquesta tesi s'explora un enfocament alternatiu basat en transconductors d'alta freqüència (HF) linealitzats, els quals inclouen un circuit dedicat per ajustar l'offset de DC per tal d'estar acoblat correctament en DC al ADC NECTAr0, i seguit a continuació per un convertidor de corrent a tensió de gran marge, i finalment un acumulador de bucle tancat i baixa impedància de sortida serveix per accionar les càrrega capacitives de l'entrada de les memòries analògiques.

Abstract

Two techniques are currently available to observe the γ-rays coming from outer space: the direct observation by particle detectors on board of satellites, and the indirect detection by ground-based detectors using the Cherenkov technique. The atmosphere absorbs the most of the gamma radiation so, the direct detection of γ-rays at ground level becomes impossible. However, it is possible to detect the effect of γ-rays in the atmosphere. When a primary γ-ray first interacts with a molecule of the atmosphere it generates an electron-positron pair. In this way an Extended Air Shower (EAS) is created, originating the Cherenkov photon emission. Detecting the Cherenkov light corresponding to an air shower generated by a γ-ray is not an easy task. Cherenkov light pool is very faint, having Cherenkov images at the camera with no more than a few thousand photons, and the duration is very short, between 2.5 and several tens of nanoseconds. This makes necessary the use of very sensitive and fast photo detectors, as well as fast and low noise electronics, capable to detect and save the interesting images. These detections are performed by using Imaging Atmospheric Cherenkov Telescopes (IACTs).

One type of photon detector is the photomultiplier tube (or PMT), most commonly used in IACTs. A PMT has a photoelectric cathode that absorbs light and emits an electron. A PMT also contains other electrodes in sequence called dynodes. Each dynode is kept at a higher positive voltage than the preceding one. Electrons are attracted to each successive dynode, and upon striking the dynode they knock off several additional electrons from the dynode. As the electron stream travels from dynode to dynode, more and more electrons are emitted as part of a cascade.

The pulses generated by the photo sensors (typically PMTs), being very narrow, need to be sampled very fast in order to determine with high precision its arrival time, and to integrate its charge in a narrow window which allows to reduce the noise contribution induced by night sky background (NSB). A typical 2.5 ns width pulse from a PMT needs to be sampled at 800 MHz to recover at least the first lobe according to Nyquist theorem, being 1 Gs/s a typical sampling frequency. Considering that an IACT camera can have around 1000 pixels and 8 quantization levels, a continuous recording of the signals from all the pixels in a camera would mean a data rate of 1 TB/s, which is unmanageable. Instead of that, current IACTs only records continuously when an interesting event is detected. In order to do that, they uses a complex data acquisition system based on analogue memories with a complex trigger system. This analogue memories sample the input signals at high sample rate, but with small buffers mounted in a dedicated ring configuration. The NECTAr (New Electronics for the CTA array) collaboration's front end (FE) option for the camera of the CTA (which is this thesis focused) is a 16 bits and 1 – 3 GS/s sampling chip based on analogue memories including most of the readout functions [9]. The trigger system, analyzes each pulse, and decides if the signal corresponds to a valid Cherenkov event to be stored or not [10].

The fast pulses coming from the PMT requires a fast readout option [11] with a wideband, high dynamic range and low noise pre-amplifier. The pre-amplifier is attached to the photo sensor and it is connected by a cable or transmission line to the front end electronics, which is placed in the camera. According to Monte Carlo simulations [12] the analogue bandwidth (BW) of the full system must be at least 300 MHz, and so the pre-amplifier BW about 500

MHz. A 16 bit dynamic range (DR) is required on one side by the measurement of the single photo-electron signal (SPE) for calibration purposes, and on the other side by the highest light pulse (5000 PE). Since the PMT operates at low gain (40 K) to avoid ageing problems, achieving a good SPE resolution imposes low noise requirements, Equivalent Noise Charge (ENC) $< 4Ke$ which means that the input referred current noise power spectral density (PSD) should be smaller than $10pA/\sqrt{Hz}$ for a current mode readout. Low input impedance and low voltage operation are required for integrated implementation and to achieve large BW.

According to the CTA consortium requirements, the camera specifications for the different telescopes needs dedicated electronic circuits, since these specifications can not be achieved with current commercial components in the market. Due to cost effective and state of the art innovation, some full custom ASICs have been developed. The aim of this thesis is to develop a full amplification channel path to inject the fast pulses coming from the camera sensors to the analogue memories of the digitizer circuitry. Based on the hard constrains of the amplification channel path for the CTA project, new technologies are applied to cover on one hand, the required wideband at the low noise level and, on the other hand decrease the power consumption required as much as possible.

This thesis is focused in the design of the amplifier path stage of the CTA cameras at the first amplification stage (pre-amplifier) and also, at a second amplification stage and signal conditioning. The first amplification stage is based on a wideband current mode preamplifier with 16 bits DR. We propose a novel current mode circuit to overcome the maximum signal limitation by creating multiple gain paths at the very front end of the input stage. The input current is split in the common base input stage into two (or more) output scaled currents. Then each current is readout with a dedicated current mirror. The high gain current mirror requires dedicated saturation control circuitry in order to assure that current division is still accurate even if this mirror saturates. Finally, the current signal is converted to voltage by a closed loop transimpedance amplifier. The pre-amplifier for CTA (PACTA) chip fulfills the CTA general requirements based on an innovative design that achieve all the restrictions with very low power consumption. The power consumption of the alternative solutions based on COTS components which were tested for CTA camera prototypes but discarded is at least 4 times higher.

The NECTAr collaboration [13] intends to build a new integrated circuit including most of the discrete components needed so far. It is one of the front end electronics options considered for the CTA cameras [11]. A gain in cost, reliability and camera performances can be achieved by maximizing the integration of the front-end electronics in an ASIC, a single GHz sampling chip. A fully closed loop solution based on voltage feedback amplifiers (OTA or OpAmp) is not feasible because a Gain-bandwidth (GBW) product of more than 8 GHz is required, and the maximum GBW product that can be achieved in a $0.35\mu m$ CMOS technology is well below 1 GHz ([14], [15]). An alternative approach based on linearised high frequency (HF) transconductors is explored, which includes dedicated circuitry to adjust the DC offset in order to be properly DC coupled to the NECTAr0 ADC, and is followed by a high swing current to voltage conversion, and finally a low output impedance closed loop buffer is used to drive a capacitive load.

Acronyms

AC Alternating Current

ACTA Amplifier for CTA

ADC Analog-to-digital converter

APD Avalanche Photo Diode

ASIC application-specific integrated circuit

BW Bandwidth

CM Common Mode

CMOS Complementary Metal–Oxide–Semiconductor

COTS Commercial Off-The-Shelf

CTA Cherenkov Telescope Array

DAC Digital-to-Analogue Converter

DAQ Data acquisition

DC Direct Current

DFM Design For Manufacturing

DPO Digital Phosphor Oscilloscope

DR Dynamic Range

DRC Design Rule Check

EAS Extended Air Shower

ENC Equivalent Noise Charge

ENI Equivalent Noise Current

FE Front End

FWHM Full Width at Half Maximum

GBP gain bandwidth product

HF High Frequency

HG High Gain

IACT Imaging Atmospheric Cherenkov Telescope

INL Integral Non-Linearity

IR Infra Red

LF Low Frequency

LG Low Gain

LSB Least Significant Bit

LSM Laser Scanning Microscopy

LST Large-Sized Telescope

LVDS Low-voltage Differential Signaling

LVPECL Low-Voltage Positive/pseudo Emitter-Coupled Logic

MSB Most Significant Bits

MST Medium-Sized Telescope

NECTAr New Electronics for the CTA array

NSB Night Sky Background

OPAMP Operational Amplifier

OTA Operational Transconductance Amplifier

PACTA PreAmplifier for CTA

PCB Printed Circuit Board

PM Phase Margin

PDE Photon Detection Efficiency

PMT Photo Multiplier Tube

PoR Power-on Reset

PSD Power Spectral Density

PSRR Power Supply Rejection Ratio

QFN Quad Flat No-leads

SAM Sampling Analogue Memory

SC Slow Control

SE Single Ended

SFP Small Form Factor Pluggable

SiPM Silicon Photomultiplier

SiGe Silicon Germanium

SPE Single Photo-Electron

SPI Serial Peripheral Interface

SS Slave Select

SST Small-Sized Telescope

S/R Signal-to-noise Ratio

TC Temperature Coefficient

THD Total Harmonic Distortion

TIA Transimpedance Amplifier

TIB Trigger Interface Board

UB University of Barcelona

UV Ultra Violet

VCSEL Vertical-Cavity surface-Emitting Laser

Pels qui ens agradaria que hi fóssin, preò no hi són.

1

Introduction

Cosmic rays are immensely high-energy radiation, mainly originating outside the Solar System. A significant fraction of primary cosmic rays are originated from the supernovae of massive stars, pulsars and active galactic nuclei, quasars, gamma-ray bursts and dark matter annihilation studies. These cosmic sources can cause γ-ray emissions by different astronomical accelerating mechanisms like synchrotron, curvature radiation, inverse Compton effect, neutral pion decay and other accelerating mechanisms [5].

Two techniques are currently available to observe the γ-rays coming from outer space: the direct observation by particle detectors on board of satellites, and the indirect detection by ground-based detectors using the Cherenkov technique. Direct detection by on-board satellite detectors is the most direct solution to detect cosmic γ-rays by measuring them where they have not been absorbed out of the atmosphere yet. However, this thesis is based on the ground-based detectors.

The atmosphere absorbs the most of the gamma radiation so, the direct detection of γ-rays at ground level becomes impossible. However, it is possible to detect the effect of γ-ray interacting in the atmosphere. When a primary γ-ray first interacts with a molecule of the atmosphere it generates an electron-positron pair. These two particles will further interact with other atmosphere molecules, loosing a fraction of their energy by the bremsstrahlung effect, and thus emitting a lower energy γ-ray. The new γ-rays create more electron-positron pairs that generate even lower energy γ-rays and the process repeats until the produced γ-rays have so low energy that they cannot produce new electron-positron pairs. In this way an Extended Air Shower (EAS) is created, originating the Cherenkov photon emission. The Cherenkov photons are emitted in a cone characterized by a certain angle θ, known as Cherenkov angle. Nevertheless, the higher the shower occurs, the more space the cone has to spread and, at the end, the Cherenkov photons cast on a circle of roughly 120 m radius, whatever the height at which the EAS happened (typically at 10 Km high) [2]. Figure 1.1, illustrates a detecting gamma rays schematic, with Cherenkov telescopes.

Detecting the Cherenkov light corresponding to an air shower generated by a γ-ray is not an easy task. Cherenkov light pool is very faint, having Cherenkov images at the camera with no more than a few thousand photons in the best cases, and the duration is very short, between 2.5 and several tens of nanoseconds. This makes necessary the use of very sensitive and fast photo detectors, as well as fast and low noise electronics, capable to detect, identify and save the interesting images. These detections are performed by using Imaging Atmospheric Cherenkov Telescopes (IACTs). Analysing the images obtained by the IACTs, it is possible to calculate the so-called Hillas parameters [16], which are directly related with the meaningful physical parameters of the original γ-rays which generated the showers, such as their energies and incoming directions.

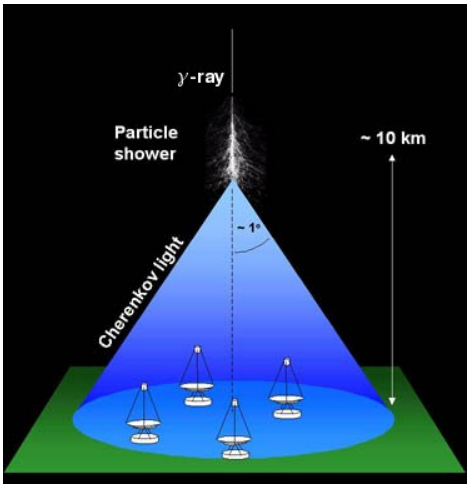
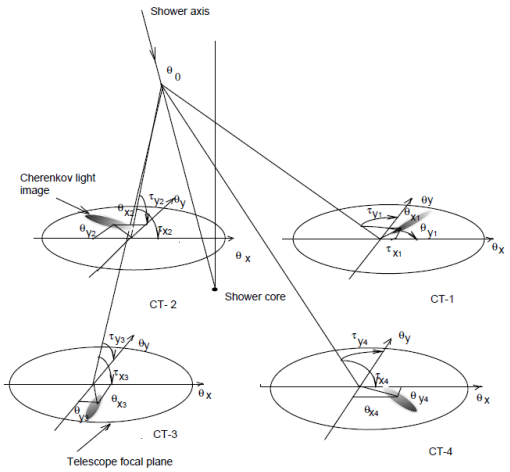
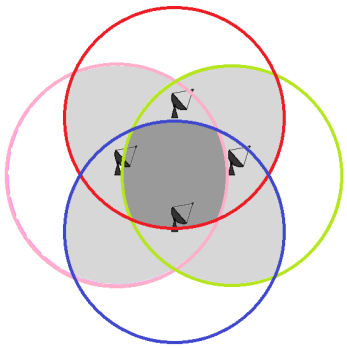


Figure 1.1.: Schematic of detecting gamma rays with Cherenkov telescopes. The Cherenkov light is beamed in the air shower and can be collected with optical detector. Referred to [1].

Observing a γ-ray shower with more than one IACT at the same time allows using stereoscopy to reconstruct the shower in 3 dimensions [6], [7]. Compared to the monoscopic observations, stereoscopic data recording allows a precise three-dimensional determination of the shower maximum position and impact parameter, an effective Hillas parameter [16] extrapolation, a better energy resolution and a more stringent rejection of muons, hadrons and Night Sky Background (NSB). Moreover, it also improves the angular resolution, making possible to distinguish sources which are very close. Figure 1.2, shows an image reconstruction scheme with a stereo array of 4 IACTs and their effective collection area.



(a) Shower image reconstruction with a stereo array of 4 IACTs.



(b) Collection areas of an array of 4 IACTs.

Figure 1.2.: Scheme of stereoscopic observation with an array of IACTs [2].

Direct detection is preferable for low energies, where the size of the Cherenkov showers is small, with not many Cherenkov photons, making these showers, difficult to distinguish from the night sky background photons. While the Cherenkov technique is more effective for high energies, that will scape undetected quite frequently in direct techniques.

The IACTs developed in the last 25 years are ground-based detectors. The first one was Whipple, which in 1989 detected a TeV emission from the Crab Nebulae for first time [18]. After Whipple, other IACTs were built like HEGRA [19], which stands for High-Energy-Gamma-Ray Astronomy. HEGRA took data between 1987 and 2002, at which point it was dismantled in order to build its successor, MAGIC, at Roque de los Muchachos Observatory on La Palma. MAGIC, Major Atmospheric Gamma Imaging Cherenkov Telescopes, was built in 2003 with a diameter of 17 meters for the reflecting surface. A second MAGIC telescope (MAGIC-II), at a distance of 85 m from the first one, started taking data in July 2009. Together they integrate the MAGIC telescope stereoscopic system [20]. Other IACTs like CANGAROO, an acronym for Collaboration of Australia and Nippon (Japan) for a GAmma Ray Observatory in the Outback located near Woomera, South Australia operates since 1992. Since 1999 CANGAROO-II, an evolution of CANGAROO was built with a bigger diameter dish (7m and expanded to 10m in the year 2000 to increase the light collection). CANGAROO-III, is not a telescope itself, but an array of four CANGAROO-II expanded telescopes. The full array operates since 2004 [21]. The largest Cherenkov telescope in the world is HESS, stands for High Energy Stereoscopic System in Namibia. HESS is a stereoscopic telescope system, where four telescopes view the same air shower and it was operational by late summer 2001. In 2012 the phase II of the HESS project was completed, obtaining an array of five telescopes were the last one (HESS-II) is a 28-meter-sized mirror [22]. The last observatory that built a Cherenkov telescope is VERITAS, Very Energetic Radiation Imaging Telescope Array System [23] in Arizona; an array of four 12m telescopes that was completed in 2007.

The next step of the the international γ ray astronomy community consists of building a large array with many IACTs, using the latest high technology to build the best telescopes ever, and thus covering all the γ ray spectrum from all the sources in all the sky. This is the target of the Cherenkov Telescope Array (CTA) consortium [17].

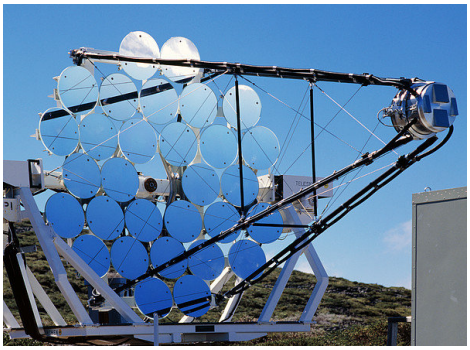
The IACTs telescopes are commonly based on a mechanical structure with a reflector mirror system to collect the photons of the showers and reflects them into the camera.
This mechanical structure should allow at the camera, to move in azimuth[i] and also elevation. The reflector is not made by a single mirror due to the price and to the complexity of developing a mirror of about 28 m diameter. Instead of that, many individual tesselated[ii] spherical mirrors which can be reoriented by individual actuators in order to compensate possible deformations of the structure due to gravity, wind or even earthquakes.
As the Cherenkov showers last only few nanoseconds, it is important to ensure that, on the one hand, the photons collected in the IACTs, which were generated at the same time, arrive to the camera at the same time. This requires the use of tesselated parabolic reflectors with overall parabolic shape, so the length of the paths that the photons have to travel is the same (figure 1.4). On the other hand, the photo detectors used in IACT cameras must be very sensitive to detect the largest possible proportion of incoming photons, requiring high

[i] An azimuth is an angular measurement in a spherical coordinate system. The vector from an observer (origin) to a point of interest is projected perpendicularly onto a reference plane; the angle between the projected vector and a reference vector on the reference plane is called the azimuth.

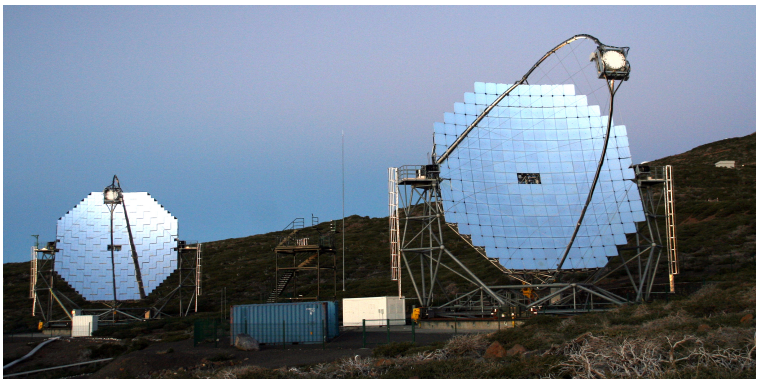
[ii] A tessellation of a flat surface is the tiling of a plane using one or more geometric shapes, called tiles, with no overlaps and no gaps.

(a) CANGAROO-I.

(b) CANGAROO-II.



(c) HEGRA.



(d) MAGIC.

(e) VERITAS.

(f) HESS.

Figure 1.3.: IACTs developed in the last 25 years.

Photon Detection Efficiency (PDE)[iii]. These detected photons are usually known as photo electrons (PE).

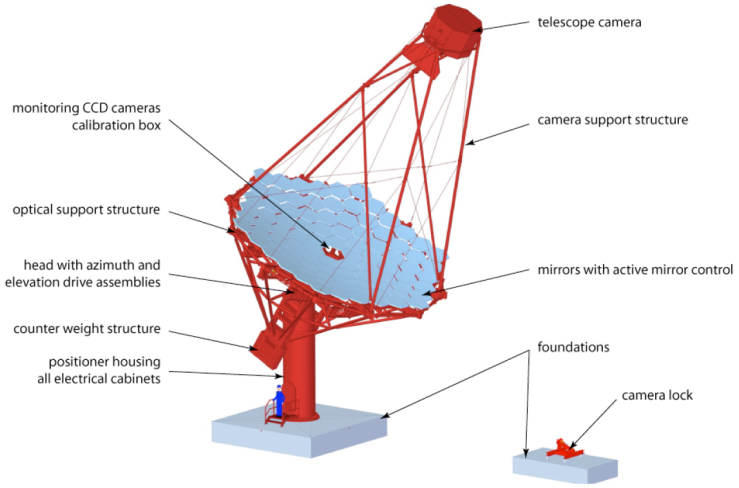
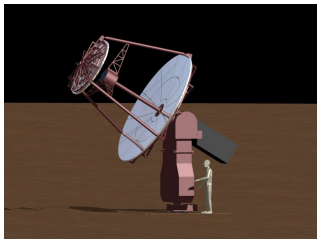
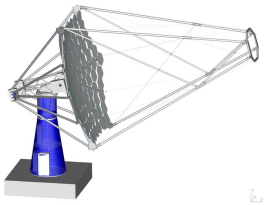


Figure 1.4.: Illustrative description of the CTA Medium-Sized Telescope (MST) design with the main assemblies and components [3].

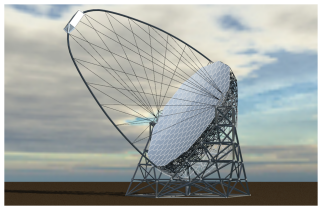
Current systems of Cherenkov telescopes use at most five telescopes, providing best stereo imaging of particle cascades over a very limited area (see figure 1.2(b)), with most cascades viewed by only two or three telescopes. An array of many tens of telescopes would allow the detection of γ-ray induced showers over a large area on the ground, increasing the number of detected γ-rays dramatically, while at the same time providing a larger number of views for each shower. This would result in both improved angular resolution and better suppression of cosmic-ray background events thanks to the coincidence requirement. With the aim of building such array of IACTs, the Cherenkov Telescope Array (CTA) Consortium was formed [17]. The CTA Consortium aims to build two observatories in both hemispheres with tens of telescopes in each one. With a budget of around 200.000.000 euros, the installation of the first telescope prototypes in the sites is scheduled at the beginning of 2016, while the installation of the majority of the telescopes will take place in 2017. There will be three types of telescopes with different reflector sizes, optimized to cover different energy regimes [8]:



(a) Small-sized telescopes (SST) of CTA.



(b) Medium-sized telescopes (MST) of CTA.



(c) Large-sized telescopes (LST) of CTA.

Figure 1.5.: CTA will consist of three types of telescopes with different mirror sizes in order to cover the full energy range. The image describes the design concept for each telescope size.

- The small-sized telescopes (SSTs) (figure 1.5(a)) will be optimized to detect showers

[iii] The Photon Detection Efficiency (PDE) is defined as the efficiency to detect an incident photon and produce a current peak at the output of the photo-detector.

generated by γ-rays of high energy range. The flux of γ-rays is severely reduced, so a large area in the ground must be covered to increment the number of detected showers. In this way, a high number of SSTs is required, covering an area of several square kilometres. Additionally, well above the SST energy threshold, the Cherenkov showers are very large and with many photons (5000 PE), so if the shower is in the field of view of the telescope, it is very easy to collect enough photons to reconstruct it. Due to these characteristics of the showers generated by γ-rays of high energy range, the SSTs will have relatively small reflectors (4-6 m diameter) and a field of view of around 10°. Moreover, as the telescopes need to be cheap (to build many of them) and a very high sensitivity is not required, the SSTs are the ideal place to use innovative designs based on double reflector optics, or different kind of photo sensors like Silicon Photo Multipliers (SiPMs)[iv] than the ones used in the other CTA telescopes.

- Medium-sized telescopes (MSTs) (figure 1.5(b)) will be optimized for the medium energy range. The coverage of this energy regime is instrumental for the CTA project, as the medium range includes a large fraction of the cosmic objects to be discovered and studied by the ground-based γ-ray astronomy in the next 20 years. This is the typical energy range covered by current instruments and, based on them, the MSTs will have a reflector of around 12 m and a field of view of 6-8 degrees. The main improvement in sensitivity of CTA in this energy range will come from the large area covered, and from the higher quality of shower reconstruction, since showers will be typically imaged by a larger number of telescopes than for current few-telescope arrays.

- The large sized telescopes (LSTs) (figure 1.5(c)) are aimed to detect γ-rays of the energy gap between the maximum energy γ-rays detectable with satellites and the minimum energy ones detectable with current IACTs. At these energies the showers are small and very faint, so telescopes with large reflectors (23 m diameter) are required. The best optical performance of the telescope is achieved with focal lengths similar to the reflector diameter. This imposes a restriction on the camera weight and size, and therefore small fields of view (around 5°) are enforced. Moreover, improving the sensitivity to low-energy γ-ray showers is a big challenge for the photo sensors, which must have a high PDE, the readout, which must be able to sample very fast adding low electronics noise.

Figure 1.6, shows an artist's impression of telescope network for the CTA observatory concept with the three telescope sizes. The telescopes array will consist on 4 LST located at the centre of the network, tens of MST located at the surroundings of the large ones, and about a hundred of SST located at the peripheral area of the telescopes network, covering an area about $\approx 4km^2$.

The photomultiplier tube (or PMT) is most commonly type of photon detector used in IACTs. A PMT has a photoelectric cathode that absorbs light and emits an electron. A PMT also contains electrodes in sequence called dynodes. Each dynode is kept at a higher positive voltage than the preceding one. Electrons are attracted to each successive

[iv] Silicon photomultipliers, are Silicon single photon sensitive devices built from an avalanche photodiode (APD) array on common Si substrate. The idea behind this device is the detection of single photon events in sequentially connected Si APDs. Every APD in SiPM operates in Geiger-mode and is coupled with the others by a polysilicon quenching resistor.

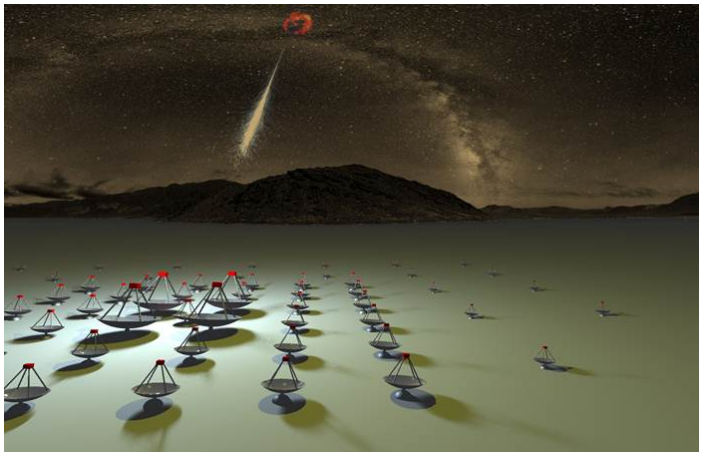


Figure 1.6.: Artist's impression of telescope network for the CTA concept [4].

dynode, and upon striking the dynode they knock off several additional electrons from the dynode. As the electron stream travels from dynode to dynode, more and more electrons are emitted as part of a cascade. At the final anode, 10^4 to 10^8 electrons may be collected for every electron emitted from the cathode. Figure 1.7, shows a cross-section of a photomultiplier tube structure and a schematic representation with its operation principle.

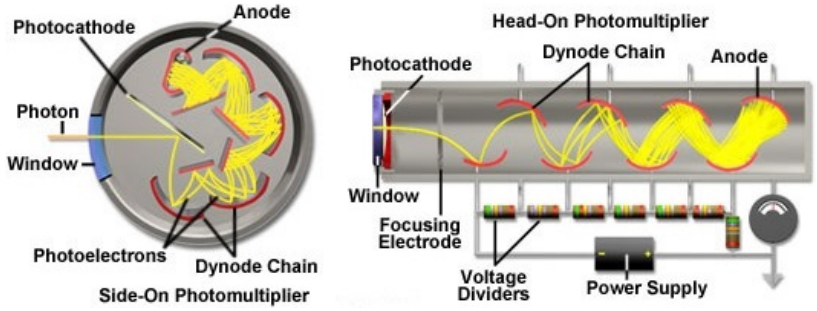


Figure 1.7.: Photomultiplier vacuum tube cross-section with the common dynode chain configuration.

The PMTs achieve sensitivities good enough for single photon measurements. They have low dark noise, pulses with no photons or more than one pulse for the same photon. These phenomena are known as dark current and after-pulsing, respectively. They are sensitive at the Ultra Violet (UV) and Infra Red (IR) wavelength range which is according to the Cherenkov light showers, also with very fast responses at the nanosecond level. Electrons are not generated in the dynodes at the same time, but with a certain time dispersion, which depends on the number of dynodes, the high voltage applied and other parameters. They are also mechanically sensitive and fragile, and need to be manufactured by hand, so, they became expensive for mass production. They are also sensitive to magnetic fields, obtaining orientation dependencies effects. This effect is usually solved by covering the PTM vacuum tube with mu-metal[v] foil. There are other photo sensors but in comparison with the PMTs, have less sensitivity. Due to the larger sensitivity area of the PMTs than the other photo

[v] Mu-metal is a nickel-iron soft magnetic alloy with very high permeability suitable for sensitive electronic equipment shielding. Mu-metal is composed of approximately 80% nickel, 5% molybdenum, small amounts of various other elements, such as silicon, and the remaining 12 to 15% iron. The high permeability makes mu-metal useful for shielding against static or low-frequency magnetic fields.

sensors as Avalanche Photodiodes (APDs) or Silicon Photomultipliers (SiPM), the PMT become cheaper than the other solution by the time of writing this thesis. Figure 1.8 shows two 8-dynode PMT models selected by the CTA consortium. On the other hand, the SiPM are not sensitive to the magnetic fields and probably will be the technology used in the future IACTs.

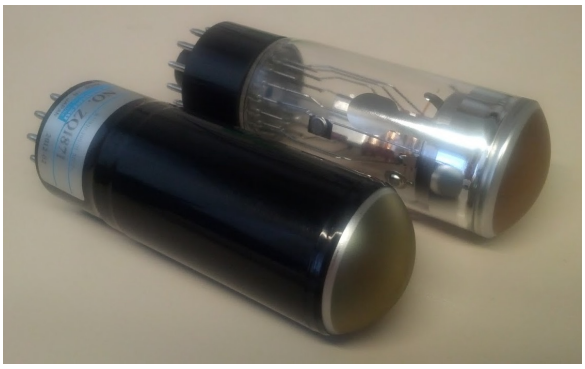


Figure 1.8.: Photomultiplier tube selectod for the CTA consortium. The right one, shows the dynodes structure and the left one is covered by mu-metal foil.

The pulses generated by the photo sensors (typically PMTs), being very narrow, need to be sampled very fast in order to determine with high precision its arrival time, and to integrate its charge in a narrow window which allows to reduce the noise contribution induced by NSB. A typical 2.5 ns width pulse from a PMT needs to be sampled at 800 MHz to recover at least the first lobe according to Nyquist theorem, being 1 Gs/s a typical sampling frequency. Considering that an IACT camera can have around 1000 pixels and 8 quantization levels, a continuous recording of the signals from all the pixels in a camera would mean a data rate of 1 TB/s, which is unmanageable.

Instead of that, current IACTs, only records continuously, when an interesting event is detected. In order to do that, they uses a complex data acquisition system based on analogue memories with a complex trigger system.
These analogue memories sample the input signals at high sample rate, but with small buffers mounted in a dedicated ring configuration. The NECTAr (New Electronics for the CTA array) collaboration's front end (FE) option for the camera of the CTA (which is the focus of this thesis) is a 16-bit and 1 – 3 GS/s sampling chip based on analogue memories including most of the readout functionality [9].

The trigger system, analyzes each pulse, and decides if the signal corresponds to a valid Cherenkov event to be stored or not. The basic strategy of the complex trigger system is to trigger first a neighbouring group of pixels (level 0 trigger or L0) and then at the level of the camera (Level 1 or L1 and possibly Level 2 or L2). The final decision is taken by the array level trigger [10]. Figure 1.8, shows the global architecture of NectarCAM, with the trigger implementation.

The fast pulses coming from the PMT, requires a fast readout option [11] with a wideband, high dynamic range and low noise pre-amplifier. The pre-amplifier is attached to the photo sensor and it is connected by a cable or transmission line to the front end electronics, which is placed in the camera. According to Monte Carlo simulations [12] the analogue bandwidth

(BW) of the full system must be at least 300 MHz, and so the pre-amplifier BW should be of about 500 MHz. A 16 bit dynamic range (DR) is required to cover on one side the measurement of the single photo-electron signal (SPE) for calibration purposes, and on the other side by the highest light pulses (5000 PE). Since the PMT operates at low gain (40 k) to avoid ageing problems, achieving a good SPE resolution imposes low noise requirements, Equivalent Noise Charge (ENC) $< 4ke$ which means that the input referred current noise power spectral density (PSD) should be smaller than $10pA/\sqrt{Hz}$ for a current mode readout. Low input impedance and low voltage operation are required for an integrated implementation and in order to achieve large BW.

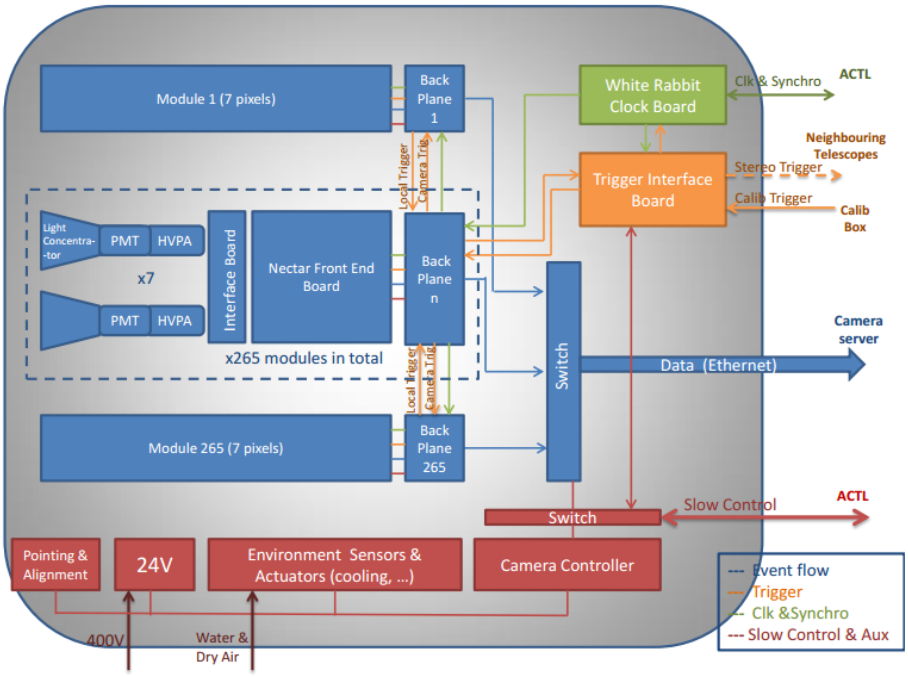


Figure 1.9.: Global architecture of NectarCAM, with the analogue trigger implementation [3].

According to the CTA consortium requirements, the camera specifications for the different telescopes need dedicated electronic circuits, out of the specifications of the commercial components. Due to cost considerations, and state of the art innovations, some full custom ASICs have been developed. The aim of this thesis is to report on the development of a full amplification channel path to inject the fast pulses coming from the camera sensors (PMTs at the writing of this thesis), to the analogue memories of the digitizer circuitry. Based on the demanding constrains of the amplification channel path for the CTA project, new solutions are applied to cover on one hand, the required bandwidth at the low noise level and, on the other hand decrease the power consumption as much as possible.

- To cover a range from the SPE measurements for calibration camera purposes to the largest amount of photons (∼5000 PE), the required DR is of about 16 bits. The PMT should be operated at low gain (∼40k) to minimize ageing so, a pre-amplification stage (located as close as possible to the PMT output pin) will be mandatory to reduce as much as possible the noise contribution. These pre-amplifier stage should be able to follow the input pulses form the PMT so, it requires a BW of at least $500MHz$. Finally, this first amplification stage must deliver output signals to the FE by a cable or

printed circuit board (PCB) tracks and connectors so, low impedance capabilities will be required. As the input signals of the analogue memories of the digitization circuits are differential signals, a differential signal at the output of the pre-amplification stage will be desirable.

- The NECTAr ASIC is a differential input analogue memory digitizer, with a capacitive input circuit, a second amplification stage will be required to adapt on the one hand the signal for the analogue memories to the desired common-voltage input levels and, on the other hand distribute the signal to the trigger system with enough gain and BW. As the trigger system will be located outside the NECTAr ASIC and, eventually, in a separated mezzanine board, low impedance capabilities will be also required. On the contrary, these second amplification stage should be located as close as possible to the NECTAr ASIC to do not disturb the signal due to the capacitive inputs.

This thesis is focused in the design of the amplifier path stage of the LSTs and MSTs at the first amplification stage (pre-ampifier) and also, at a second amplification stage and signal conditioning for the MSTs for CTA. In this way, the thesis has been organized as follows.

Chapter 2 describes the first amplification stage, which is based on a wideband current mode preamplifier with 16 bits DR to cover from the single photo electron measurements up to the large amount of photons of the LST and MST telescopes. Measurement results of an ASIC designed in Austriamicrosystems $0.35\mu m$ SiGe technology are presented and manufactured.

Chapter 3 presents the design of the input amplifier for the high gain path of the new ASIC, which has been prototyped on a dedicated die. The NECTAr collaboration [13] intends to build a new integrated circuit including most of the discrete components needed so far. It is one of the front end electronics options considered for the CTA cameras [11]. A gain in cost, reliability and camera performances can be achieved by maximizing the integration of the front-end electronics in an ASIC, a single GHz sampling chip. The first version of the chip is NECTAr0, it is based on the Sampling Analogue Memory(SAM) chip fabricated in Austria microsystems $0.35\mu m$ CMOS technology [24]. Nevertheless, the circuit could be used for low gain path as well in case that some gain is needed for this path. High gain amplifiers must have a voltage gain of 20 and a bandwidth of 400 MHz fora 3 pF load [11]. Furthermore, amplifier non-linearity must not exceed 1%. Input referred series noise (en) PSD must be smaller than $3nV/\sqrt{Hz}$ in order to perform SPE calibration at a PMT gain of $2x10^5$. Output excursion must be higher than 1.5 Vpp with a 3.3 V power supply.

Chapter 4 concludes this thesis with the summary of the different goals achieved and a list of the contributions published related to the amplification path design in scientific journals and important conferences. Future avenues of research are also mentioned in this chapter.

2

PreAmplifier for the CTA cameras (PACTA)

Some of the PMT cameras for CTA, uses front-end electronics based on an analogue memory which samples and stores the signal at 1 to 2 GS/s with 16 bit dynamic range (DR) [25], [12]. A 16 bit DR is required on the one hand by the measurement of the SPE for calibration purposes, and on the other hand by the highest light pulse (5000 PE), which corresponds to a 10-20 mA input peak current (figure 2.1).

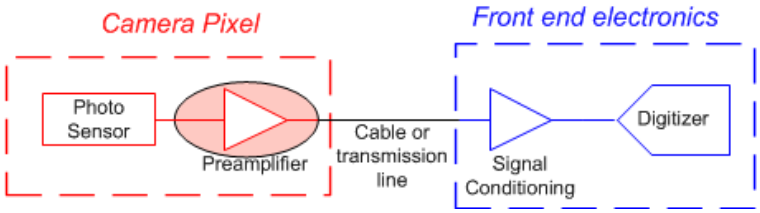


Figure 2.1.: Block diagram of the CTA camera electronics.

The preamplifier is attached to the photosensor (in order to minimize the inductance at the pre-amplifier input signal) and it is connected by a cable or transmission line to the front end electronics, which is placed in the camera. The baseline photosensor candidates are high quantum efficiency PMTs, although the camera design must be modular allowing a possible upgrade to SiPMs.

Table 2.1, summarizes the preamplifier requirements.

Table 2.1.: Preamplifier requirements.

Noise	$ENC < 5Ke$
Dynamic range	From $< 1/10$ of SPE to 5 KSPEs: 16 bits with $< 3\%$ nonlinearity
BW	500 MHz. Total BW including FE must be 300MHz
Input impedance	< 20WLow pick-up noise and high BW
Low power	About 100mW with low impedance driver (cable)
Reliability/compactness	Mass production, Integrated circuit, ASIC

Readout schemes for a large DR (approaching 10^5) require multiple gain ranges prior to analog-to-digital conversion. To achieve this DR, an input stage with sufficiently low noise is required [26]. In the aforementioned design options, the 16 bit DR is achieved using 2 gains feeding 2 analogue memory channels per PMT pixel with a ratio 1:20, each with an effective 12-bit DR.

2.1 Design of PACTA

Since PMT has to be operated at low gain (40K) to avoid ageing problems, a low noise preamplifier is required. To achieve good SPE resolution a $S/N \geq 10$ in the charge spectrum is required. In terms of Equivalent Noise Charge (ENC) it means $ENC < 4Ke$. This requirement shall be translated to series and parallel noise requirements. As the PMT capacitance is quite low, it will be assumed that parallel noise dominates the noise performance. Provided that the amplifier BW is much higher than inverse of the integration time T, it can be shown [27] that the ENC of a amplifier with an input referred noise current PSD i_n whose output is integrated (to compute the charge) for a time T is, for white noise,

$$ENC^2 \approx 1/2 \cdot i_n^2 \cdot T \tag{2.1}$$

Hence, the parallel noise requirement is,

$$i_n \leq \frac{\sqrt{2} \cdot G}{\sqrt{T} \cdot (S/N)_{MIN}} \tag{2.2}$$

where G is the PMT gain. From figure 2.2, it is clear that the input referred current noise PSD should be smaller than $10pA/\sqrt{Hz}$, since optimal integration time is between 5 and 10 ns [12].

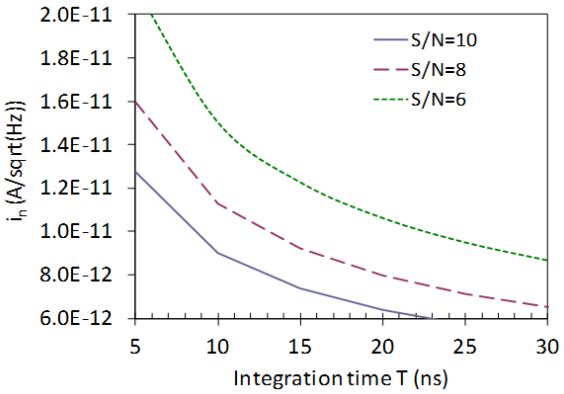


Figure 2.2.: Parallel noise requirement as function of integration time T, for different S/N in the SPE spectrum.

In order to achieve low energy threshold, NSB contribution needs to be minimized. According to Monte Carlo simulations [12] the BW of the system must be at least 300 MHz, and so the preamplifier BW about 500 MHz. Low input impedance is preferred since it enhances the frequency response and minimizes capacitive coupling. Low voltage operation is needed to minimize power consumption and because the circuit will be implemented as an ASIC.

Figure 2.3 shows the two main blocs of the desired pre-amplifier. The current mode input stage, and the low impedance output buffer in differential mode.

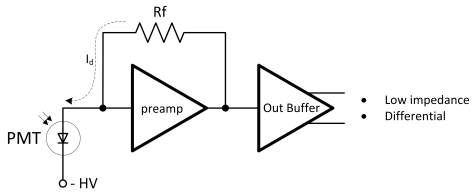


Figure 2.3.: Pre-amplifier block diagram of the current mode input stage and the low impedance output buffer in differential mode.

Current mode circuits, based on super common base or regulated cascode stage are well suited to fulfils most of previous requirements. For instance, a very low noise amplifier for calorimetry applications is described in [28], achieving a 16 bit DR. However, this design is not well suited for low voltage operation because input current is quickly converted to a voltage signal and for 16 bit DR this means large signal excursion. In current mode designs multiple gain paths are typically created using a current mirror to replicate the input signal with different scaling factors [29]. Unfortunately, large currents saturate the input branch of the mirror and DR is in practice limited to 14 bits.

We propose a novel current mode circuit[i] to overcome the maximum signal limitation by creating multiple gain paths at the very front end of the input stage; which is described in section 2.1.1. The input current is split in the common base input stage into two (or more) output scaled currents. Then each current is readout with a dedicated current mirror which can be optimized for different performances (figure 2.4). The current mirror design is described in section 2.1.2. The high gain current mirror requires dedicated saturation control circuitry in order to assure that current division is still accurate even if this mirror saturates.Finally, the current signal is converted to voltage by a closed loop transimpedance amplifier which is described in section 2.1.3. Small signal analysis of the circuit will be discussed in section , whereas noise performance will be studied in section 2.1.6.

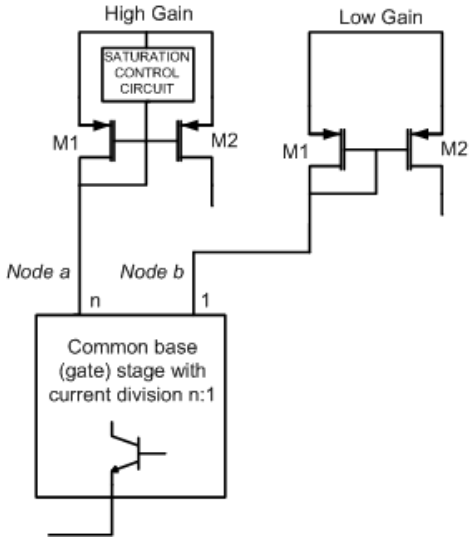


Figure 2.4.: Block diagram of the current mode circuit.

[i]This novel scheme is patented [30]. See 4.3 for a detailed information of the patent.

2.1.1 Input stage

The common base stage for the current division is shown in figure 2.5. The transistors Q_n to Q_0 are in linear active operation region and are equal and matched, they provide the input current, which is splitted into 2 output currents scaled by factor n. Those transistors are lay-out in common centroid and the emitter degeneration at R_E is used to improve matching and to linearise the input impedance. As in current mirrors, the current of the different branches must be equal because the base to emitter voltage of Q_1 to Q_0 is equal by construction. Because of the *Early effect*, the current matching depends on the voltage variation at the collectors of Q_1 and Q_0. To minimize these effects cascode transistors Q_{Cn} to Q_{C0} are added in order to increase the output impedance of the stage.

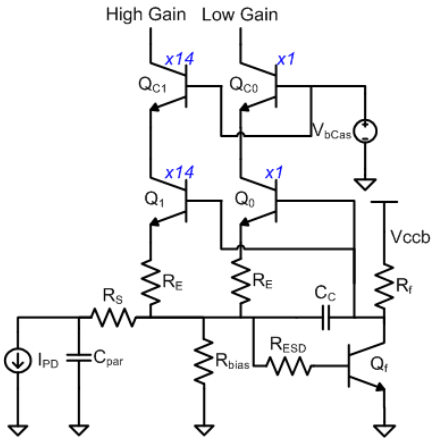


Figure 2.5.: Simplified schematic of the input stage (common base stage for current division) of the PACTA chip.

The voltage feedback is used to decrease the input impedance. Since the input impedance is very small, a series resistor R_S is used to degrade the quality factor of a possible resonance of the inductance of the bonding wire with the input capacitance. It also helps in linearising the input impedance. A larger resistor R_{ESD} is used for protection of the base of Qf transistor, it can be larger than R_S since it does not increase the input impedance.

Section 2.1.5 shows an exhaustive small signal analysis of the input stage and the closed loop input impedance calculation.

Section 2.1.6 shows a detailed noise analysis and simulations of the input referred noise current.

2.1.2 Current readout stage

The current mirrors in figure 2.4 are low voltage cascode current mirrors (see figure 2.6) with a common base transistor Q_{cb} with local feedback to the minimize input impedance as well as the voltage variation in the collectors of Q_{C1} and Q_{C0} of the input stage. These

current mirrors act as a wideband amplifier with high DR. It is possible to achieve a BW exceeding 500MHz with a current gain A_I of 2.5 (for high gain) and 12 bit dynamic range. This is crucial to achieve the GBP requirements of the ASIC, especially for the high gain path.

Current mirror of figure 2.6 makes use source degeneration (R_{SM}). For large bias currents (or for a high pulse rate) g_{mM1} increases, and so it does the GBP of the local feedback loop. Source degeneration limits the effective value of g_{mM1}.

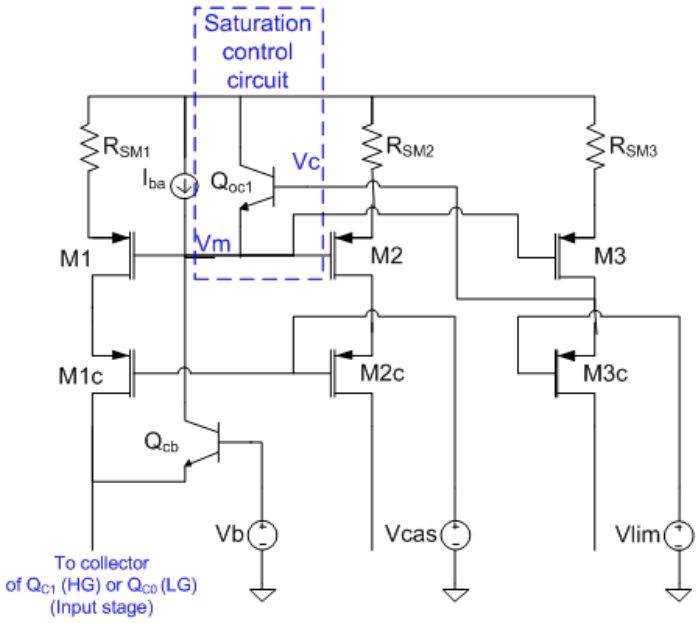


Figure 2.6.: Simplified schematic of the current mirrors of the PACTA chip. HG mirror incorporates a saturation control circuit

However, $M1/M1c$ enters the ohmic region for large signals and make a feedback and the low input impedance is lost, for this reason, the high gain (HG) current mirror comprises a saturation control circuit, see figure 2.6 on the top. High input currents may cause large variations in the voltage at the collectors of Q_{C1} and Q_{C0} of the input stage (figure 2.4) when M1 or M1c transistors of HG mirror enter the ohmic region.

The saturation control circuit quenches the excess current through Q_{oc1} (and Q_{cb}), to avoid this. The transistor Q_{oc1} is controlled by the voltage $Vc - Vm$. At the quiescent operation or for low currents the circuit is designed so that $Vc - Vm \ll V_{be\_ON}$, where V_{be_ON} is the conduction threshold voltage of Q_{oc1}. When the input current increases, the drain current of M1 to M3c increases as well. Vc increases with drain current ($Vc = Vlim + Vgs_{M3C}$), whereas Vm decreases ($Vm = Vcc - Vgs_{M1}$). When $Vc - Vm > V_{be\_ON}$ the excess current is taken by Q_{oc1}. The turn on point of Q_{oc1} can be controlled by scaling up/down M1 and M3c and by the control voltage Vlim.

2.1.3 Transimpedance stage

The closed loop transimpedance amplifiers of figure 2.16 are based on high GBP operational amplifiers, where singled ended version and the fully differential versions have been implemented. A simplified schematic of a fully differential operational amplifier is shown in figure 2.7. It is a folded cascode amplifier with a second Miller stage and then, a class AB output stage will be added (section 2.1.4). Miller compensation is used with nulling resistor. The input pair is degenerated to improve slew rate. A fast and accurate continuous time common mode feedback is provided by an error amplifier.

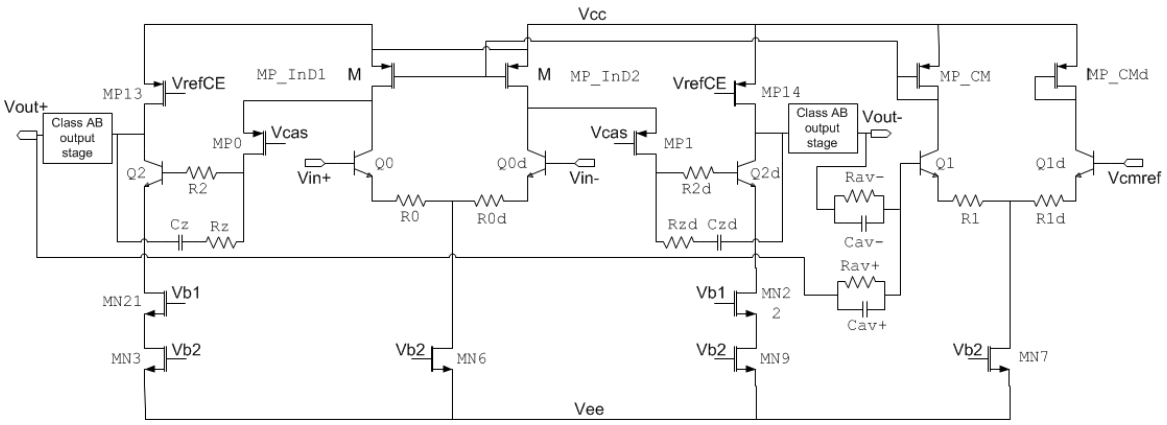


Figure 2.7.: Simplified schematic of the fully differential operational amplifier of the PACTA chip.

Main performances of the amplifier are: low frequency gain of 65 dB, GBP higher than 700MHz with a minimum Phase Margin (PM) of 70 degrees and slew rate exceeding 1 V/ns. Power consumption is between 50 and 60mW (at 3.3V power supply).

2.1.4 Class AB output stage

Figure 2.8 shows the proposed class-AB output stage. Emitter follower stage is composed by Q_2 and Q_3 parallel NPN transistors. A series resistor R_S senses Q_3 current, which in first order approximation is equal to Q_2 current. This current is controlled by a feedback loop closed by MP_1 which controls current source transistor Q_1.

It is a negative feedback loop which stabilizes Q_3 and Q_2 current. When the stage is sinking current, collector current in Q_3 decreases and V_S increases, and hence MP_1 drain current increases, since its V_{GS} increases. Then, Q_1 provides more current reacting to the initial decrease in Q_2 and Q_3 current. Therefore, the feedback mechanism not only allows increasing the sinking capability of the stage, but also stabilizes $Q_2 - Q_3$ current, thus linearizing the emitter follower stage. The sourcing capability of NPN follower is high by nature, but the feedback also stabilizes the emitter follower current in a limited range (the

quiescent current of Q_1).

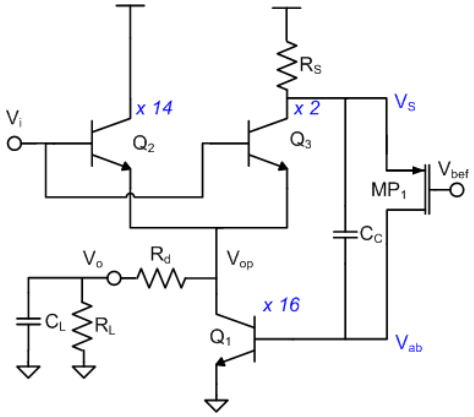


Figure 2.8.: Simplified schematic of the class AB output stage of the PACTA chip.

A series resistor R_d is used to assure stability even for large capacitive loads. This resistor can be used also to provide line termination in the emitter, which is a common practice in HF line drivers (see figure 2.9).

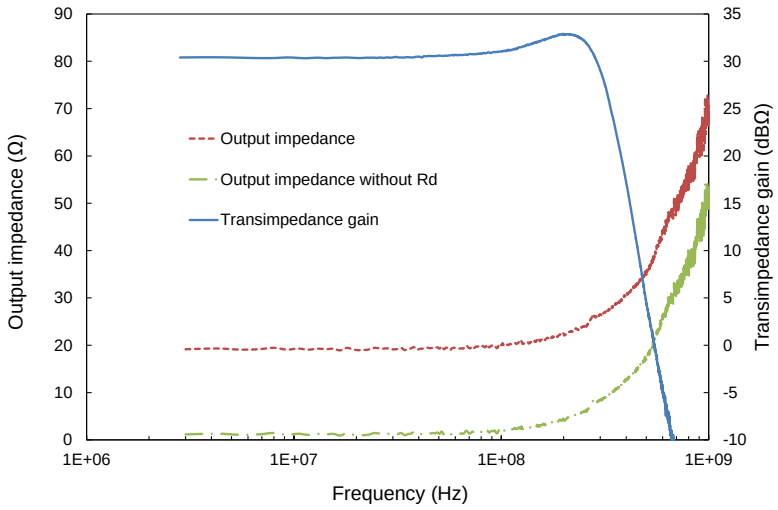


Figure 2.9.: PACTAv1.4 Measurement results of the TIA output impedance and transimpedance gain for $V_{CC} = 3.3V$, $R_L = 50\Omega$, $C_L = 10pF$, $R_d = 18\Omega$.

Load is AC coupled to minimize static power consumption. The ratio between maximum and quiescent Q_1 collector current is about 3. When this maximum current is reached $Q_2 - Q_3$ collector current becomes null and the stage is in slewing operation. Maximum ratio results from a trade-off between local feedback gain and stability. Total quiescent current (I_{QT}) is about 5 mA.

Circuit depicted in figure 2.8 is very simple, which is adequate to perform as output stage of

wideband close loop amplifiers. Nevertheless, the local feedback loop must be very fast and, hence, its stability needs to be studied.

Main drawback of this output stage is that the control of its quiescent current is not accurate. Nevertheless, an additional low frequency feedback can provide precise control of the quiescent current without degrading the HF performance.

Quiescent current can be controlled by adjusting V_{bef}. However, large fluctuations around the nominal value are caused by process or temperature variations. Bias voltage V_{bef} is generated by a closed loop control circuit. Quiescent current in the emitter follower is monitored trough V_S voltage, which is compared to the voltage drop caused by a reference current I_{Qref} in resistor R_{Sb}, a replica of R_S resistor. The loop is closed by a high gain OTA, with very low power consumption since it is a LF loop.

The quiescent current of each follower unit is set to I_{Qref}, provided quiescent current in MP_1 is negligible. Temperature coefficient is smaller than 0.07 % / C. According to Monte Carlo simulations, the standard deviation is smaller than 2 % both for process and mismatch variations.

The class AB output stage shown in figure 2.8 is a new version of all NPN push-pull stage [31]. A lower voltage operation is achieved (by 1 V_{be}), so the stage can be integrated in the operational amplifier of figure 2.7. The push-pull operation is based on fast local feedback loop which GBP exceeds 2 GHz with a PM higher than 60 deg. This stage can provide more than 20mA peak current with a quiescent current of 5 mA. This allows driving low load impedances with AC coupling, i.e. the cable or transmission line impedance connecting PACTA and FE electronics [32].

2.1.5 Small signal analysis

The stability of the high frequency feedback loop of the input stage (figure 2.5) must be carefully studied. Stability and other small signals can be studied after evaluation of the feedback loop gain $T(s)$. Using the return ratio technique, $T(s)$ is computed, yielding, for a dominant pole situation,

$$T(s) \approx \frac{g_{mQf}\left(s+\frac{g_{mQi}}{C_{\pi Qi}}\right)R_E C_i}{\left(s+\frac{1}{C_i Z^0_{i_{OL}}}\right)\left(s+\frac{1}{(c_{\pi Qi}+c_{Rf})R_f}\right)\left(s+\frac{1}{(c_{\pi Qi}\|c_{Rf})R_E}\right)} \tag{2.3}$$

where $Z^0_{i_{OL}} = 1/g_{mQi} + R_E$ is the LF open loop input impedance and $C_i \approx C_{par} + c_{\pi Qf} + (1 + g_{mQf}R_f)C_C$ is total equivalent the input capacitance, including the Miller capacitance related to C_C. C_{par} is the parasitic capacitance at the input of the ASIC, including pad capacitance, stray capacitance and detector capacitance. The parasitic capacitance at the collector of Q_f (to ground) is C_{Rf}. Other parameters correspond to elements defined in figure 2.5 and standard notation is used for small signal parameters of transistors Q_f and Q_i, being the later the parallel combination of Q_1 and Q_0.

There are two simple methods to compensate the loop. First one is Miller compensation (C_C), which performs pole splitting. It is also possible to perform dominant pole compensation by emitter degeneration R_E of Q_1 and Q_0 transistors. Emitter degeneration also helps in linearising the input impedance $Z_{i_{OL}}$ and improves matching. However, it limits the dynamic range and increases noise. The second method consists in decreasing the loop gain $T(0) \approx g_{mQf}R_f$, but as will be discussed later on, decreasing the loop gain means increasing the input impedance. Compensation will be basically performed with C_C.

As can be noticed in figure 2.10, dominant pole $p_d \approx 1/C_i Z^0_{i_{OL}}$ compensation can be performed increasing C_C. With $C_C = 750fF, p_d \approx 100MHz, GBP \approx 1GHz$ and $PM > 75deg$.

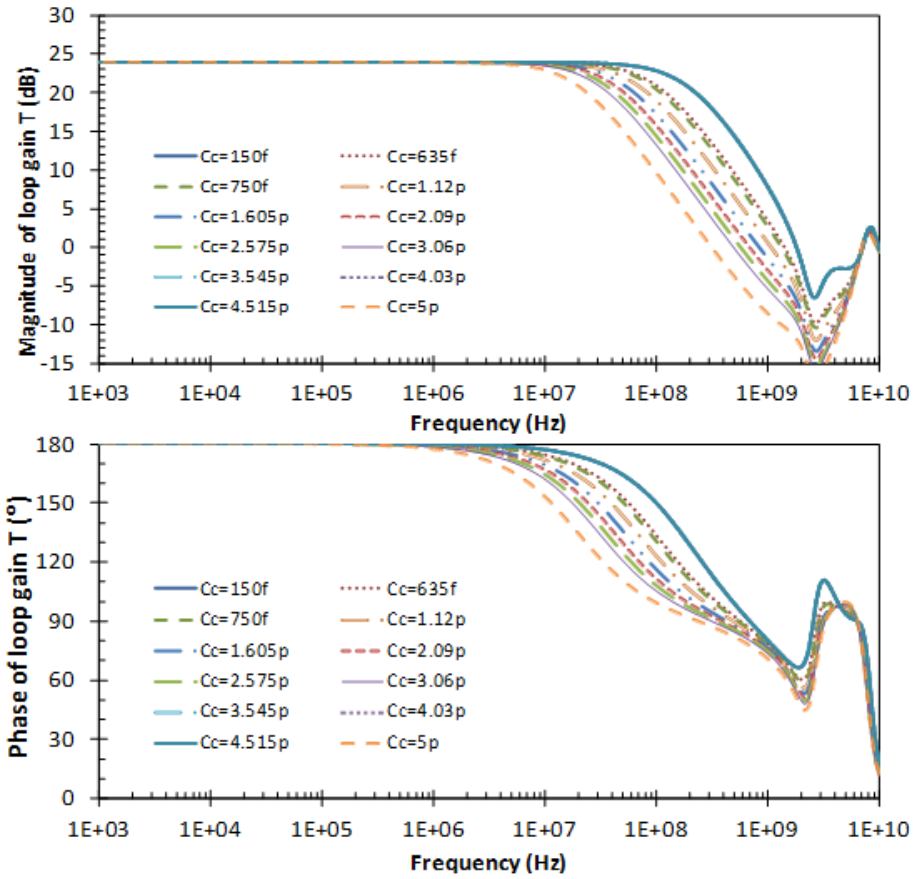


Figure 2.10.: Loop gain T(f) for different C_C: magnitude (top) and phase (bootom). Inductance of the bonding wires is considered.

As shown in figure 2.11, with dominant pole compensation, both phase margin (PM) and GBP are stable even for high loop gain. The loop gain $T(0)$ can be controlled by Vccb, setting the quiescent current of Q_f, and thus, g_{mQF}. PM is still high enough when the inductance of bonding wires are taken into account.

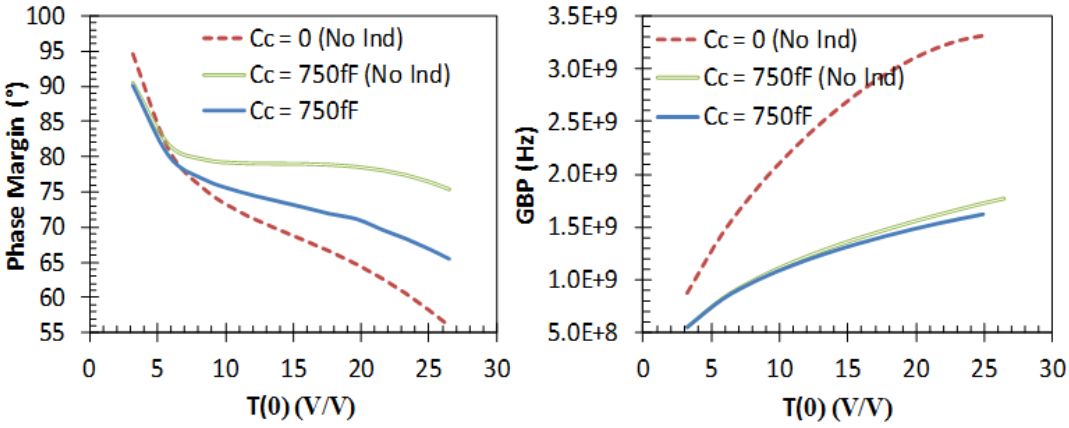


Figure 2.11.: Loop gain T(f) phase margin (left) and GBP (right) as function of loop gain, with an without C_C. The effect of the inductance of the bonding wires is studied for $C_C = 750fF$.

Even if $T(0)$ increases the GBP is quite stable since Miller compensation makes p_d smaller, because when loop gain is very high $C_i \approx g_{mQf} R_f C_C$, and therefore $GBP_{MAX} \approx (2\pi Z^0_{i_{OL}} C_C)^{-1} \approx 1.8GHz$.

Closed loop input impedance can be computed by Blackman's impedance formula,

$$Z_{i_{CL}}(s) \approx \frac{R_E + \frac{1}{g_{mQ1}}}{g_{mQf} R_f} \frac{\left(s\left(c_{\pi Q1} + C_{Rf}\left(g_{mQ1} R_E + 1\right)\right) \frac{R_f}{g_{mQ1} R_E + 1} + 1\right)}{\left(s \frac{c_{\pi Q1}}{g_{mQ1}} + 1\right)} \tag{2.4}$$

So, the close loop impedance at LF is,

$$Z_{i_{CL}}(0) \approx \frac{R_E + \frac{1}{g_{mQ1}}}{g_{mQf} R_f} = \frac{Z^0_{i_{OL}}}{T(0)} \tag{2.5}$$

If $g_{mQ1} R_E \ll 1$, from (eq. 2.4),

$$Z_{i_{CL}}(s) \approx \frac{\left(c_{\pi Q1} + C_{Rf}\right)\left(s + \frac{1}{\left(c_{\pi Q1} + C_{Rf}\right) R_f}\right)}{g_{mQ1} c_{\pi Q1}\left(s + \frac{g_{mQf}}{c_{\pi Q1}}\right)} \tag{2.6}$$

As can be noticed in figure 2.12, dominant pole p_d of $T(s)$ (eq. 2.3) has no effect in (eq. 2.6), thus inductive effect only appears at high frequency, the zero of (eq. 2.6) (second pole in (eq. 2.3)).

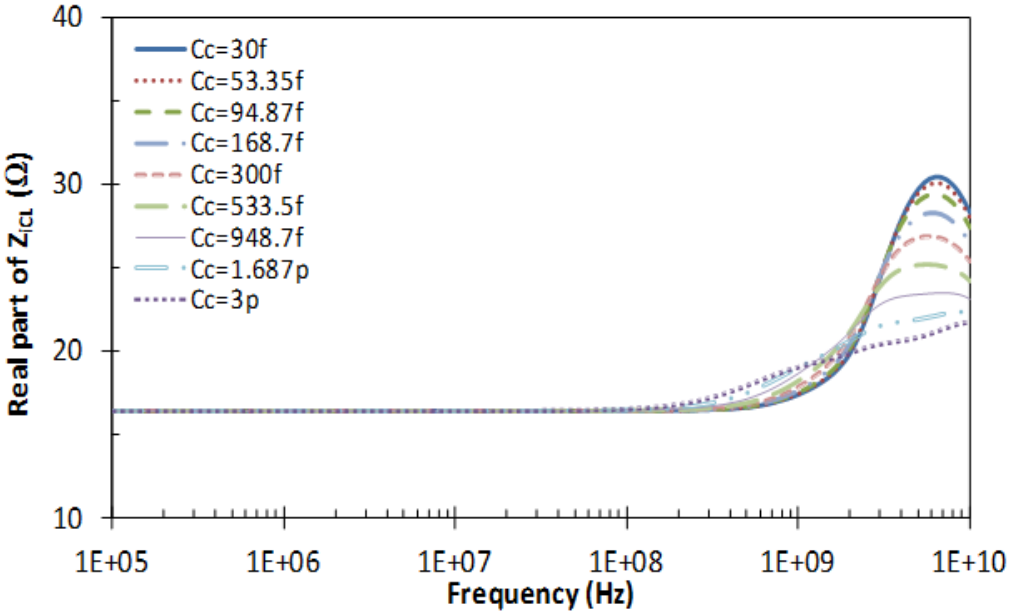


Figure 2.12.: Magnitude of the input impedance for different C_C.

The dependence of input impedance on LF loop gain $T(0)$ is depicted in figure 2.13.

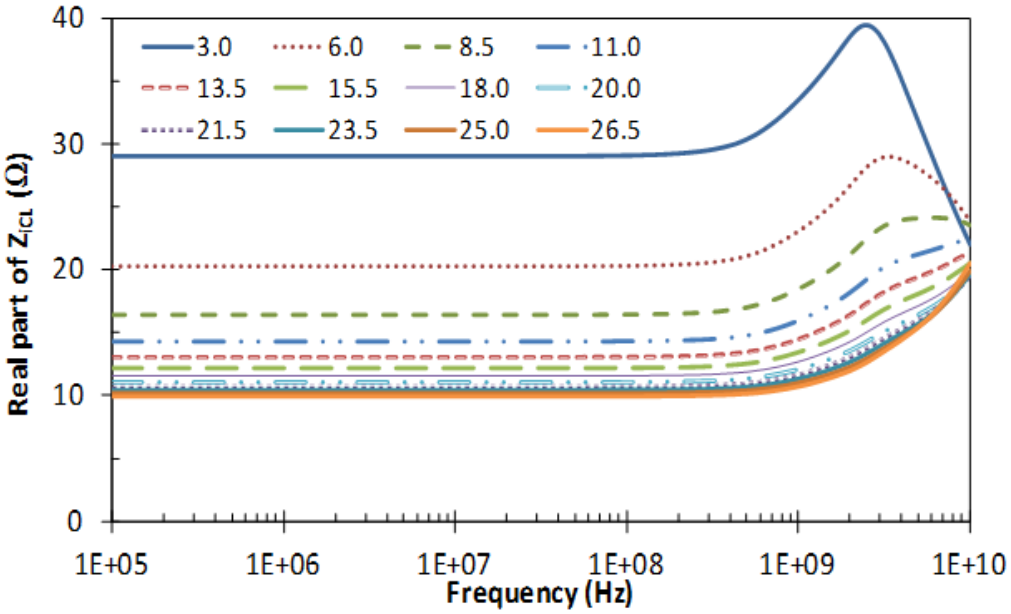


Figure 2.13.: Magnitude of the input impedance for different loop gain.

2.1.6 Noise analysis

Input referred series noise generator e_n of the input stage in figure 2.5 is,

$$e_n^2 \approx 4KT\left[\frac{1/2}{g_{mQf}} + r_{bbQf} + R_S + R_{ESD} + \frac{1/2}{g_{mQfi}T(0)} + \frac{r_{bbQf}}{T(0)} + \frac{R_E}{T(0)}\right] \tag{2.7}$$

Dominating terms in (eq. 2.7) are feedback transistor Q_f contributors (thermal noise of base resistance and collector current shot noise) and thermal noise of R_S and R_{ESD} resistors. Noise contributors related to Q_i transistors can be neglected since their contribution is divided by the LF loop gain $T(0)$. For the typical settings $e_n \approx 0.8nV/\sqrt{Hz}$, as confirmed by simulation (figure 2.14).

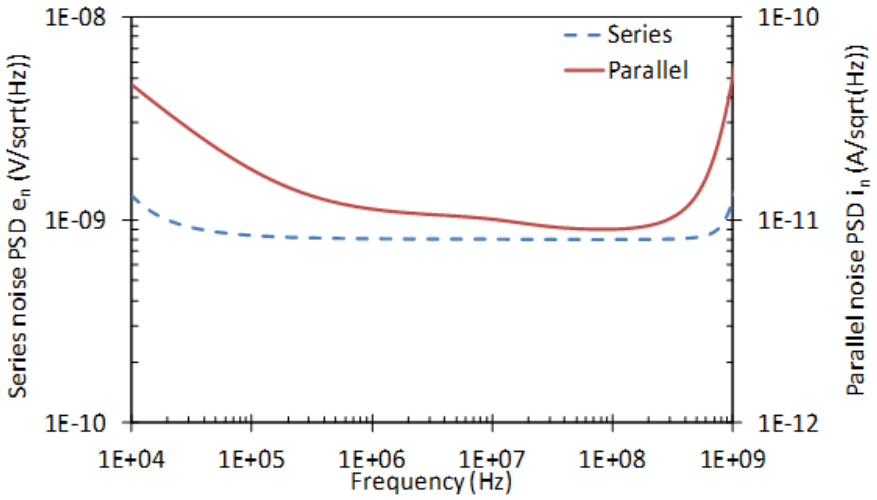


Figure 2.14.: Series and parallel noise. Spectre simulation.

The contribution of the current mirror following output stages is negligible.

Input referred parallel noise generator of the input stage is,

$$i_n^2 \approx \frac{4KT}{R_{bias}} + 2qI_{BQf} + i_{nMIR}^2 \tag{2.8}$$

where i_{nMIR} is the input referred noise current of the current mirror (figure 2.6), whose value is, approximately,

$$i_{nMIR}^2 \approx \left(1 + \frac{1}{A_I}\right)^2 \left(\frac{g_{mM1}}{g_{mM1}R_{SM1} + 1}\right)^2 4KT\left[\frac{2}{3g_{mM1}} + R_{SM1}\right] \tag{2.9}$$

for typical operation point $i_{nMIR} \approx 4.2pA/\sqrt{Hz}$ and $i_n \approx 8.4pA/\sqrt{Hz}$, fulfilling noise requirements discussed in table 2.1. Figure 2.15 shows the simulation results for the total integrated input referred noise current or Equivalent Noise Current (ENI) as function of the detector capacitance. For low detector capacitance (below 5 pF), parallel noise dominates.

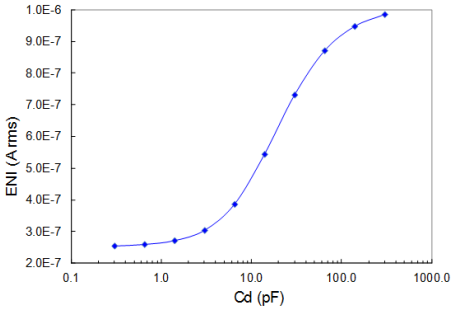


Figure 2.15.: Simulation of the ENI as function of detector capacitance (Cd).

This is the situation for PMTs. Conversely, for higher detector capacitances series noise dominates and the total equivalent noise increases as long as the BW of the system is not limited by the input node time constant. This is the typical situation for SiPMs and LAAPDs. The circuit has been optimized for PMT readout, however performance is still quite good for SiPM, since ENI is still well below single micro cell signal of SiPM. Series noise can be optimized since R_{ESD} can be decreased if necessary; it is quite easy to achieve $e_n \approx 0.6nV/\sqrt{Hz}$.

2.2 PreAmplifier for CTA (PACTA) prototypes

Based on the block diagram of the pre-amplifier for the first amplification stage (see figure 2.4), four ASIC versions has been designed at the moment of writing this thesis. So, the first pre-amplifier version includes the novel input current circuitry in order to validate the new development. It also includes the current mirrors and the saturation control for the high gain branch which are the most innovative parts of the design and it must be tested separately. After the result analysis of this first version, a second version adds a single ended output version like the first prototype, and also, a differential output version, in order to analyse the noise and power consumption effects. Then, ones the circuits is validated by the second version measurement results, a third version integrates the required biasing circuitry in order to minimise the external components required for the pre-amplifier. Finally, a fourth pre-amplifier version, focuses in the noise improvements by adding an option positive feedback that reduces the noise of about 10%, but it also implies a certain BW reduction.

Figure 2.16 shows the block diagram of the complete pre-amplifier for CTA (PACTA) ASIC used to validate the novel input stage and the saturation control circuitry of the high gain amplification branch.

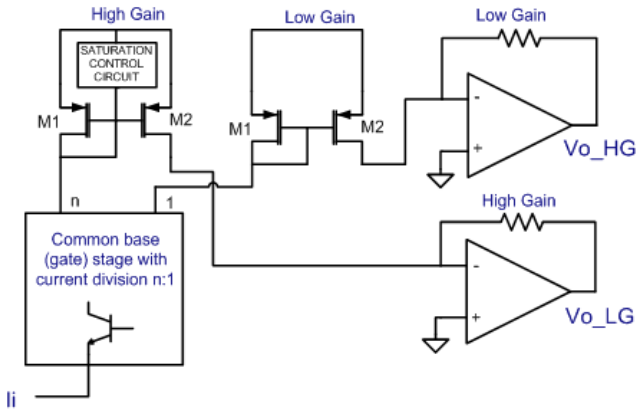


Figure 2.16.: Reduced block diagram of the PACTA chip.

A differential version of PACTA has been also designed, as outlined in figure 2.17. Two replicas of the input stage are connected to a fully differential transimpedance amplifier. PMT signal is connected to the input of one of the replicas, whereas the input of the other one should be connected to an equivalent source impedance (a small capacitance) in order to balance the circuit and achieve optimal common mode (CM) noise rejection. It is also possible to use it as test pulse input.

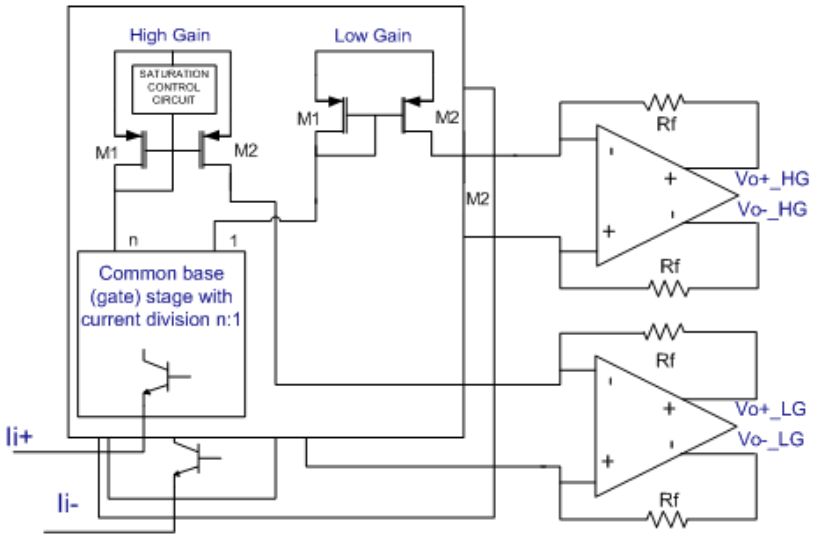


Figure 2.17.: Functional block diagram of the PACTA chip for the differential configuration

Even if the PMT signal is single ended (unless last dynode signal is used) a differential configuration has a number of advantages:

- Good common mode (CM) noise rejection. This greatly improves the power supply noise and pick up noise rejection.
- Higher dynamic range.
- Improved linearity (for the fully differential op amp).
- Robust differential signal transmission to FE electronics.

The main drawbacks of the differential configurations are: higher input equivalent noise and additional power consumption. Ideally, noise should be increased by $\sqrt{2}$ with respect to calculations and simulations summarized in previous section, since in principle both replicas of the input stage can be considered uncorrelated. However, some CM noise sources of the bias circuitry are cancelled in the differential configuration and the increment is lightly smaller. For differential configuration $i_n \approx 11.8pA\sqrt{Hz}$, and, thus, an $ENC < 4Ke$ can be achieved for an integration time slightly smaller than 10 ns. The power consumption is increased but the single ended to differential conversion should be performed anyway in the signal conditioning block of the FE shown in figure 2.16 since most digitizers are differential. Therefore, the total camera power consumption can be indeed reduced because the single to differential conversion can be performed much more efficiently in the ASIC.

Table 2.2.: PACTA prototype versions comparative.

	PACTAv1.1	**PACTAv1.2**	**PACTAv1.2b**	**PACTAv1.4**
Technology	AMS SiGe 0.35μm BiCMOS			
Submission date	June 2010	June 2011	June 2012	June 2012
Reception date	October 2010	October 2011	October 2012	October 2012
Main building blocks	1 diff. PACTA 1 input stage	1 diff. PACTA 2 SE PACTAs	1 diff. PACTA Biasing circuitry	1 diff. PACTA[ii] Biasing circuitry

PACTA prototype has been designed in Austriamicrosystems 0.35μm SiGe BiCMOS technology. The first version, PACTAv1.1, included a differential input stage and a complete PACTA, but without cable driving capability (figure 2.18(a)). The second version, PACTAv1.2, includes two single ended PACTAs and a differential PACTA (figure 2.18(b)). This version improves the linearity and compensation of the input stage and the current amplifier, it includes a new fully differential OpAmp with higher slew rate (1 V/ns) and a low output impedance stage with cable and transmission line driving capabilities. Some bias current blocs, distributes the required current to configure the two (HG & LG) blocs. The bias currents of the different configurable options (also for the bias voltages configurations), should be provided externally by using current source references circuits.

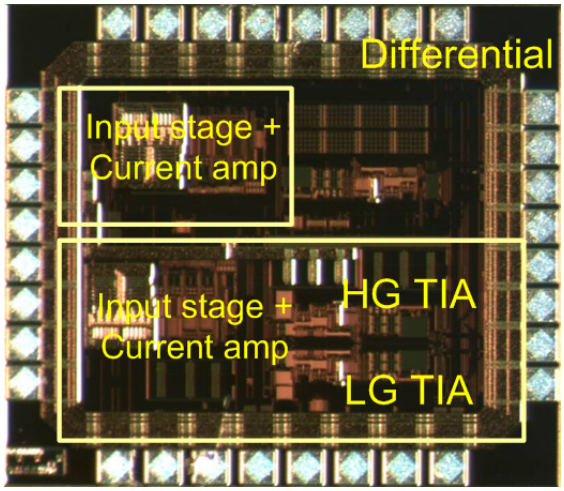
Although both single ended and differential versions have been prototyped, because of aforementioned reasons the preferred solution is the differential architecture.

PACTAv1.2b is the third version of the Pre-Amplifier for CTA (figure 2.18(c)). This third version includes one differential PACTA with a low output impedance stage (the one implemented and tested in the second version) and all the biasing currents (and voltages), are generated internally in order to minimize the required external circuits (just a resistor network to drive the bias currents). The biasing voltages are supplied by an internal Vref source, and then, just a resistor voltage divider is required to provide all the voltage biasing options. PACTAv1.4 is the fourth version of the Pre-Amplifier for CTA (figure 2.18(d)). This version includes some improvements of the previous version at the input stage in terms of parasitic noise and also introduces a noise reduction configuration ($< 10 - 20\%$), where

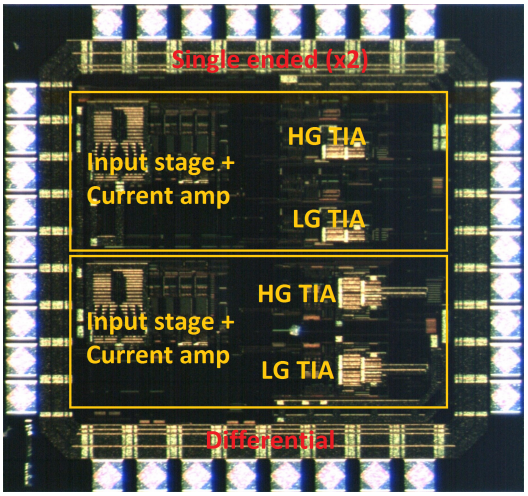
[ii] Noise optimized

the I+ is used as a feedback input to reduce even more the whole noise of the amplifier by reducing a little the bandwidth. There is a working point optimization thanks to the measurements obtained at the PACTAv1.2 version (see table 2.2).

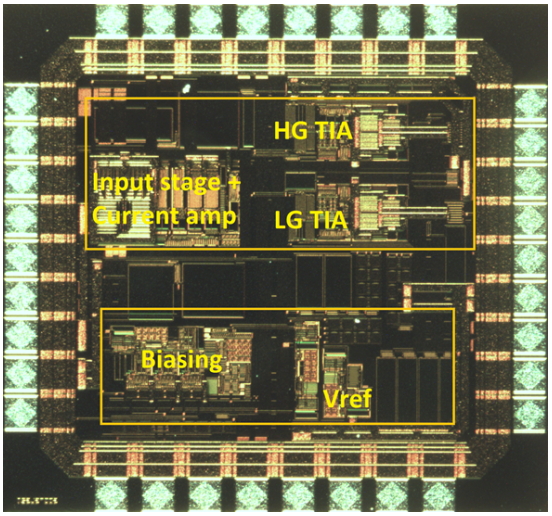
The last two PACTA version was designed and prototyped simultaneously. PACTAv1.2b was a more conservative option, just integrating the biasing at the ASIC, but the amplifier itself, is the already tested at the PACTAv1.2 in order to get a known version ready for the CTA project time schedule, and it was conceived as a back up option of the next PACTA version prototype. Whereas the PACTAv1.4 introduces some risky modifications at the input stage, which is the most critical part of the design. After the measurements of all the versions, 2500 PACTAv1.4 units has been produced and verified until year 2015, in order to equip the first LST-CTA camera and the NectarCAM demonstrators.



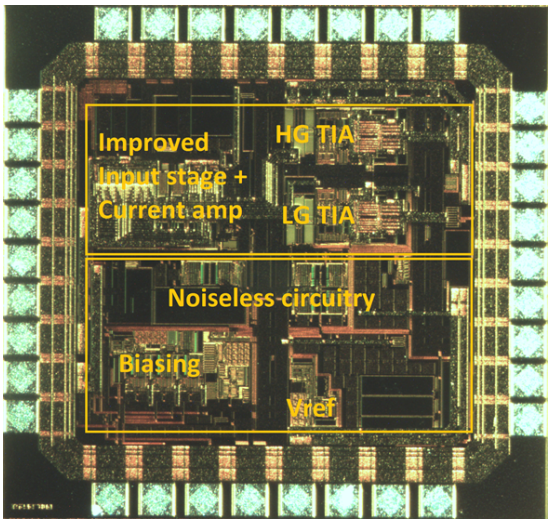
(a) PACTAv1.1 asic photography.



(b) PACTAv1.2 asic photography.



(c) PACTAv1.2b asic photography.



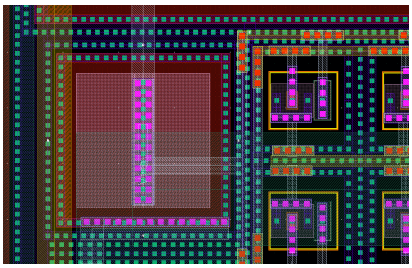
(d) PACTAv1.4 asic photography.

Figure 2.18.: Micro photography of the different PACTA ASIC prototypes developed: PACTAv1.1, PACTAv1.2, PACTAv1.2b and PACTAv1.4.

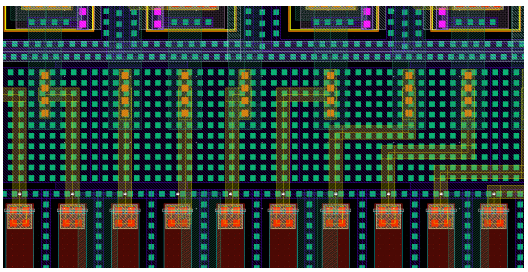
2.3 Layout details

Due to the noise and BW restrictions, the novel current division scheme at the very front end part of the circuit becomes the most critical part of the design. Special layout design techniques are applied, in order to get the best performances available in the fabrication technology [33].

One of these techniques is to minimize the ohmic influence of the vias used, by adding as much via contacts between the different layer connection as possible. Each via contact has an associated intrinsic resistor so, the more contacts in the layer transition, the less resistance associated to these via is obtained. This technique is specially important at the substrate connection, so contacts to ground are placed in the *"free"* areas in order to achieve a good ground connection to the associated substrate contact at each point. Other important effect is reduce the possibility of unconnected paths due to via obstruction at the fabrication process. Design For Manufacturing (DFM) rules option at the design rule check (DRC) process, indicates the area suggested to add more contacts between layers. DFM describes the process of designing a product in order to facilitate the manufacturing process in order to reduce its manufacturing costs. This rule guidelines are more restricted rules that assures a yield improvement in the ASIC production. Figure 2.19 shows a sample layout of the DFM guideline application by applying as much contacts as possible to interconnect different layers.



(a) Sample layout of the DFM guideline application by applying as much contacts as possible to interconnect different layers.



(b) Sample layout of the DFM guideline application by applying as much contacts as possible at the substrate connection.

Figure 2.19.: Design For Manufacturing (DFM) guideline application layout examples.

The problem of the collection of charge, by a device for converting electromagnetic fields to/from electrical currents, is known as antenna effect.The antenna effect is an effect that can potentially cause yield and reliability problems during the manufacture of MOS integrated circuits. Fabrication foundries normally supply antenna rules, which are rules that must be obeyed to avoid this problem. A violation of such rules is called an antenna violation. Antenna rules are normally expressed as an allowable ratio of metal area to gate area. There is one such ratio for each interconnect layer. The area that is counted may be more than one polygon and corresponds to the total area of all metal connected to gates without being connected to a source/drain implant. Fixes for antenna violations consist on

several techniques as change the order of the routing layers, add vias near the gates, to connect the gate to the highest layer used or add diodes to the net (see figure 2.20). A diode can be formed away from a MOSFET source/drain. The aim of place diodes is to drain the collected charge of the associated path.

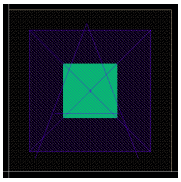
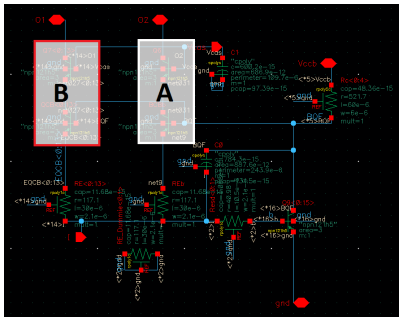
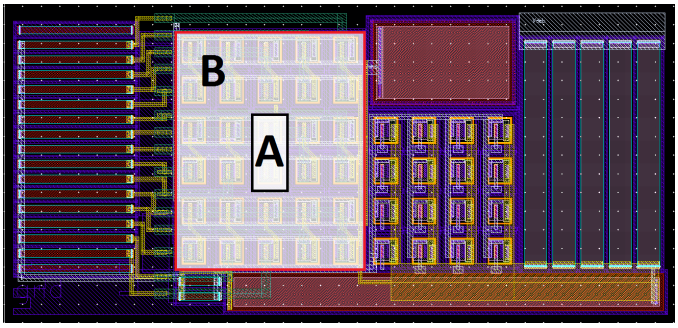


Figure 2.20.: Diode layout to solve the antenna violations.

Analogue circuits are sensitive to mismatch variations as a function of layout position, so one layout technique to combat this is called Common Centroid. Common centroid layout refers to a layout style in which a set of devices has a common center point. Another benefit of using the Common Centroid layout approach is that it minimizes the effects of mask misalignment. In order to introduce more degrees of freedom for transistor placements, splitting each transistor in half (same length and half width) and connecting the corresponding parts in parallel allow to from a common-centroid layout technique. Common centroid results in a circuit with twice as many transistors as the original one without altering the electrical functionality. Interdigitate arrayed resistors by splitting them in smaller ones connected in series, produce a common centroid layout. The minimum aspect ratio of a resistor is at least five times longer than it is wide. Figure 2.21 shows a common centroid structure sample schematic and layout of a BJT pair of transistors corresponding to the input pair of the PACTA pre-amplifier.



(a) Schematic sample of the common centroid application technique.



(b) Sample layout of the common centroid application technique.

Figure 2.21.: Common centroid application technique.

In order to minimize the subtract noise, the different devices can be designed with a guard ring and inside a well to reduce the coupling to the substrate in order to prevent the latch-up [34]. Figure 2.22 shows a guard ring sample layout of an array of PMOS transistors isolated from the N-substrate.

Polysilicon etch rates depend on how closely spaced poly lines are drawn. Areas where poly edges on the outsides of multiple devices has been etched more than on the insides of

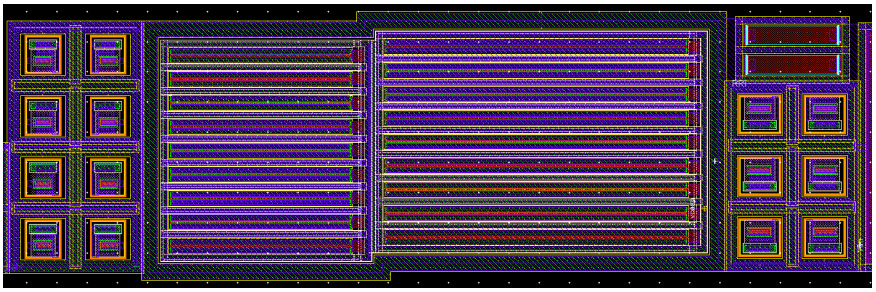


Figure 2.22.: Guard ring sample layout of an array of PMOS transistors isolated from the N-substrate.

the devices, resulting in performance mismatch. Placing dummy devices on the outside of the active devices minimizes edge effects. This technique is it valid for all the devices and becomes more relevant at the critical parts of the circuits like critical resistor values or pairs of transistors. Figure 2.23 shows a PMOS transistors array sample layout with dummy devices located at the top and bottom of the structure.

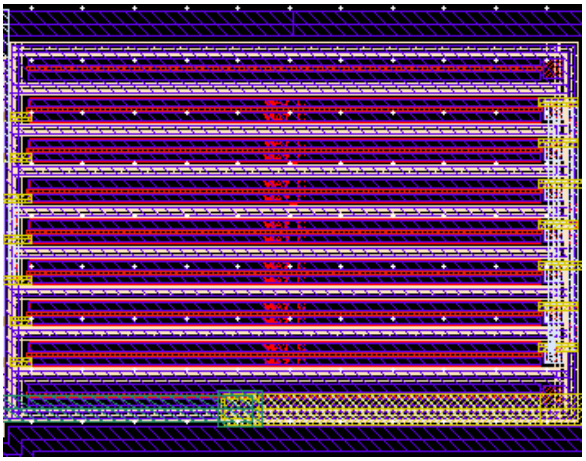


Figure 2.23.: PMOS transistors array sample layout with dummy devices located at the top and bottom of the structure.

Due to the difference in the temperature coefficients of two different materials, it is not recommended to construct matched devices from different materials. For example, match resistor a different polysilicon materials. Figure 2.24 shows a sample layout of two different resistor types in common centroid configuration but in separated structures for each resistor type.

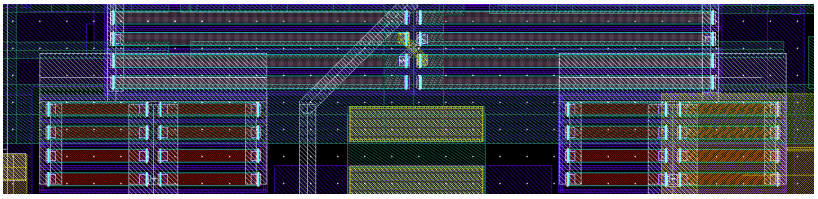
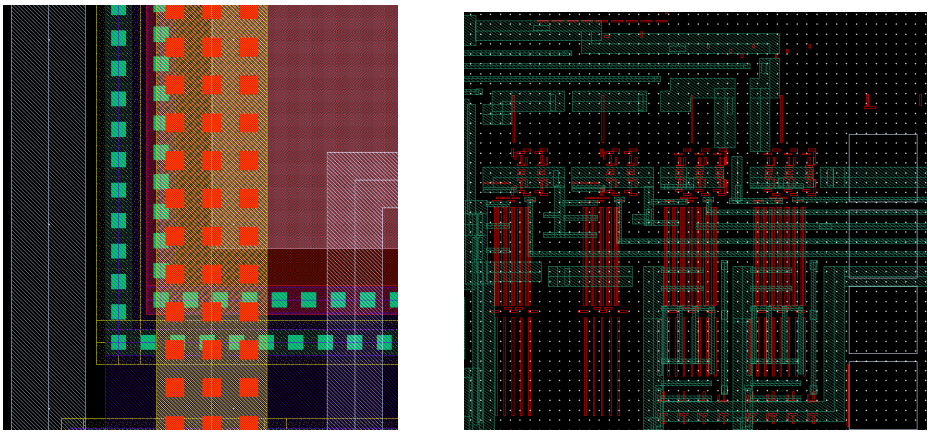


Figure 2.24.: Sample layout of two different resistor types in common centroid configuration but in separated structures for each resistor type.

Duplicate and fulfill with vias two metal layers overlapped (see figure 2.25(a) with met 2 in white and met 3 in yellow, overlapped and fulfilled with contact vias), reduces de inductance associated to a path, and increases the current density available in a minor influence than duplicate the track width with just one metal layer, because the capacitance of a path is related to its width but the thickness contribution is much less significant. On the other hand, wide metal layer has 5 times more current density than the other layers[iii] (see figure 2.25(b)).



(a) Duplicate and fulfill with vias two metal layers overlapped sample technique.

(b) Wide metal path sample layout.

Figure 2.25.: Routing path improvements technique.

Most of those techniques, requires an additional layout space so, it will be used in the critical parts of the circuits and if there is enough are to implement it.

The BiasCurrent block, generates all the required bias currents for the different parts of the PACTA pre-amplifier and it has been tacked special care at the temperature compensated current reference. See the right part of the figure 2.26. Also, the bias voltage circuit (see figure 2.27) uses the special layout techniques like the common centroid for the PMOS transistors. OpdifAB block, uses most of the aforementioned techniques, but in a special way, the wide metal track routing (see figure 2.28).

According to the layout design techniques described previously, the PACTA pre-amplifier design follows the floor-planning described in figure 2.29(a), where the amplification stage is located at the bottom of the chip with the input stage at the left (marked as 1)and the two differential low impedance output buffers (one for each gain branches) at its immediate right (marked as 2 and 3). The biasing circuitry is located at the top part of the design but close enough to do not get unwanted effects at the biasing signals (marked as 4). The different bias currents and voltages are first generated in the circuitry located a the very top of the PACTA design (marked as 5), and then distributed by the block located at the centre of the chip, near to the final gain stage, and also

[iii] Current density characteristic for the Austria Micro Systems (AMS) 0.35μm SiGe technology

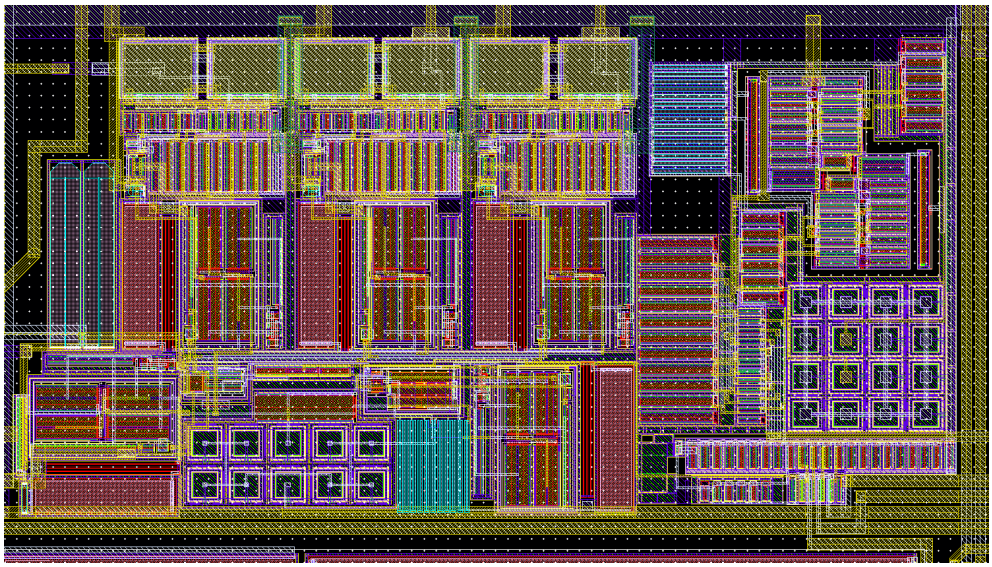


Figure 2.26.: BiasCurrents layout that generates all the required currents with the temperature compensated current reference circuit al the right.

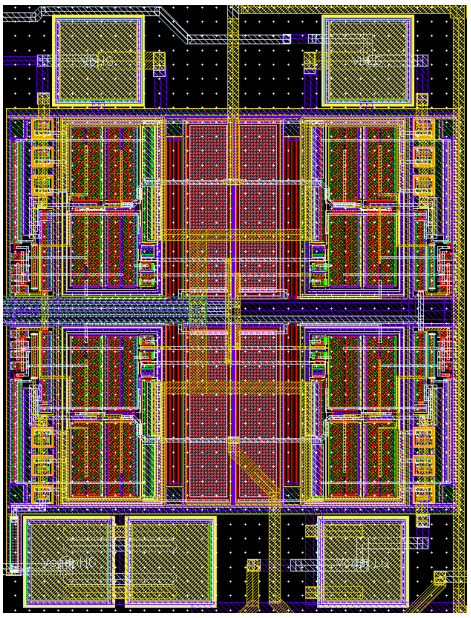


Figure 2.27.: BiasIntV layout that generates all the required bias voltages for the PACTA preamplifier.

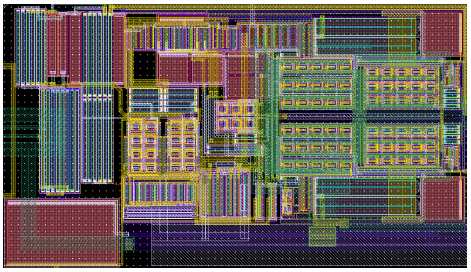
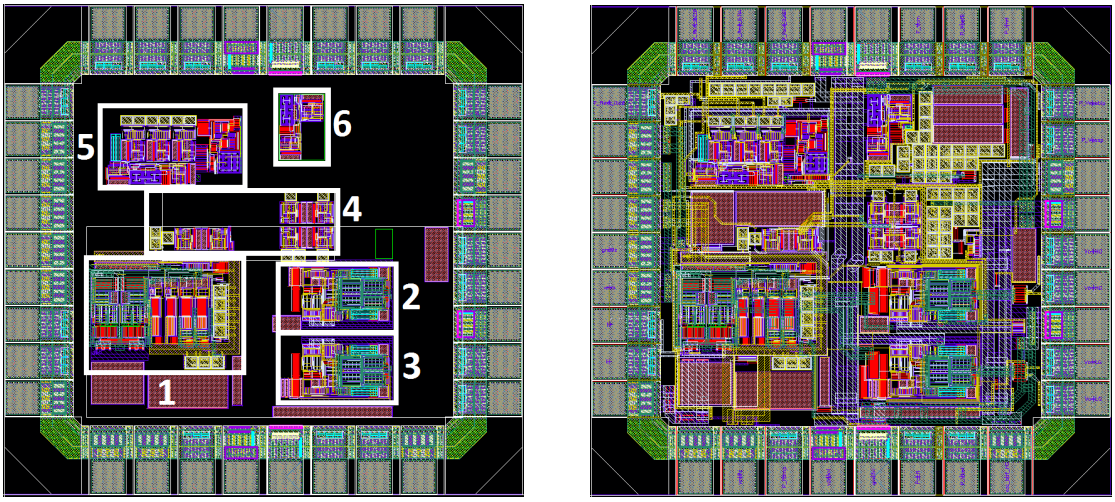


Figure 2.28.: OPdifAB layout block that corresponds to the low impedance output buffer for the PACTA preamplifier.

the temperature compensated current reference (marked as 6), in order to avoid the temperature effect of the amplification stage. Figure 2.29(b) corresponds to the complete ASIC layout, and it can be appreciated the decoupling capacitors and the different power rails.



(a) Floor-planning of the different blocks of the PACTAv1.4 ASIC design.

(b) Wide metal path sample layout.

Figure 2.29.: PACTAv1.4 Layout design on the left and the floor-planning of the different blocs at the right.

Figure 2.30 shows a detailed view of the floor-planing of the amplification stage, with the power supply rails after the input stage (left) and the two output buffers (right). All the different power supplies (one for the input stage and other one for the output buffer) are separated also at the ground level by a SUBDEF layer until the bonding level, to minimize the unwanted signal coupled by the substrate at both critical parts of the design.

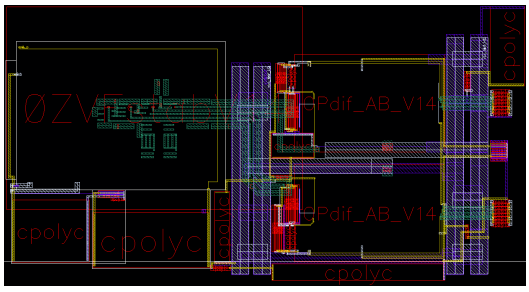


Figure 2.30.: Floor-planning of the gain stage of the PACTAv1.4 ASIC design.

So, the pad ring is mainly designed to minimize the path distances specially at the critical part which are the differential input signals[iv]. The signal pads are surrounded by ground (or power) pads in order to avoid coupling between the signal and the biasing, but also, because the power signals, presents less DC influence due to they are well decoupled by different capacitors (see figure 2.31).

[iv] The I+ input signal is not used as an input signal, but a dummy one in order to get a differential path at the very beginning

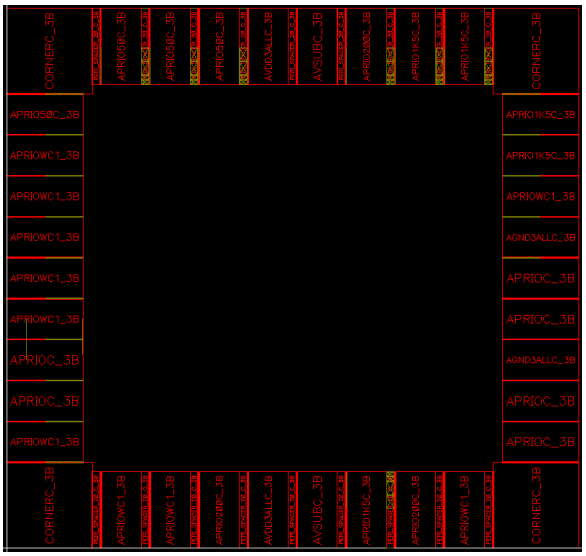


Figure 2.31.: Pad ring floor-planning of the PACTAv1.4 ASIC design.

2.4 Test results

Subsection 2.4.1 shows the typical application circuit of the pre-amplifier and the information related to the package used. If it is not expressly mentioned, all the measurements in subsection 2.4.2 are related to the last pre-amplifier version which is PACTAv1.4 and under ambient temperature conditions ($25°C$).

2.4.1 Package & usage

PACTAv1.4 has been the version selected to be used as CTA project base line for the LST and the MST telescopes, figure 2.32 shows the typical application circuit, with the required A.C. couplings at the inputs and outputs. It is also included the resistor network values, required for the biasing in order to achieve the requested operating point.

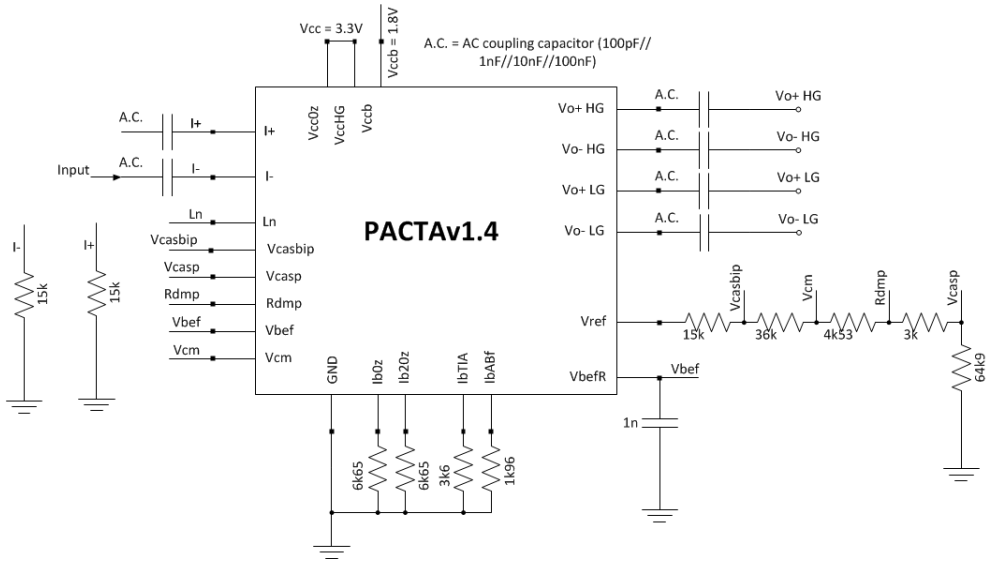
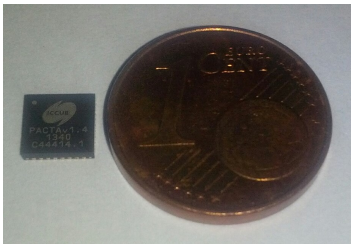
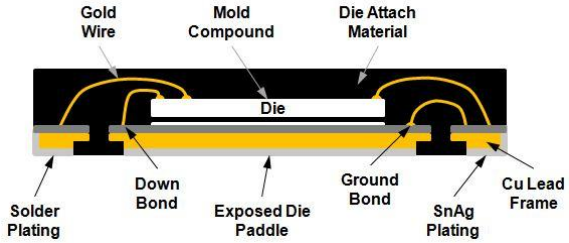


Figure 2.32.: PACTAv1.4 Typical application circuit.

In order to minimize the associated package inductance, PACTA uses a Quad Flat No-leads (QFN) package which has an associated inductance of about $\approx 0.25nH$ (QFN package of 32 pins and 5x5 mm size) [35].
Due to the thermal pad included in the bottom centre part of the QFN packages, it is also possible to minimize the wire bondings length for the ground pins by using down bonds techniques, see figure 2.33 for a QFN cut section detail. Connecting this thermal pad to the ground plane improves the thermal dissipation but also the ground connection of the ASIC.



(a) PACTAv1.4 sice detail comparation with a 1 cent coin.



(b) PACTAv1.4 QFN Bonding detail section.

Figure 2.33.: PACTAv1.4 Package details.

Figure 2.34 shows a scaled image of the die[v] with the bonging diagram used for the PACTAv1.4 asic with the ground connection at the thermal pad.

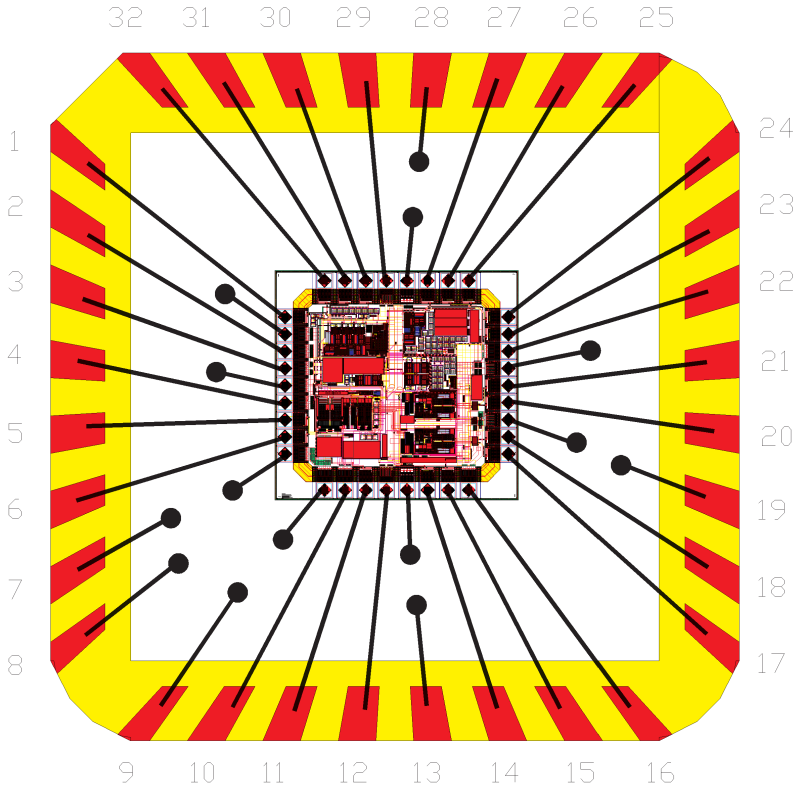


Figure 2.34.: PACTAv1.4 Bonding Diagram with the DIE ground pads connected to the central package pad.

The PACTAv1.4 generates an internal voltage reference to provide the required bias voltage sources at the V_{REF} output (typically 2,28 V). This voltage reference is a temperature dependence compensated circuit in order to avoid the possible temperature variations in

[v] A die in the context of integrated circuits is a small block of semiconducting material, on which a given functional circuit is fabricated. Typically, integrated circuits are produced in large batches on a single wafer of electronic-grade silicon (EGS) or other semiconductor (such as GaAs) through processes such as photolithography. The wafer is cut ("diced") into many pieces, each containing one copy of the circuit. Each of these pieces is called a die.

de camera and so, the unwanted modifications of the PACTA operating point due to the modification of the voltage biasing associated.
The temperature dependence is expressed by the temperature coefficient (TC). The definition of TC varies, (e.g. the slope or the box method is used). TC is expressed in $[ppm/°C]$. With the box method the TC is calculated by [36]:

$$TC = \frac{V_{out,max} - V_{out,min}}{V_{out,nom}} \cdot \frac{1}{T_{max} - T_{min}} \cdot 10^6 \tag{2.10}$$

With maximum and minimum output voltages $V_{out,max}$ and $V_{out,min}$ over the specified temperature between T_{max} and T_{min} and $V_{out,nom}$ the nominal voltage at default room temperature: $T_{nom} \approx 25°C$.

The DC voltage-temperature characteristic is obtained with DC Analysis with sweep variable temperature going from $0°C$ till $70°C$. The result is shown in figure 2.35. According to the box method of (2.10) the TC obtained is 26 $ppm/°C$.

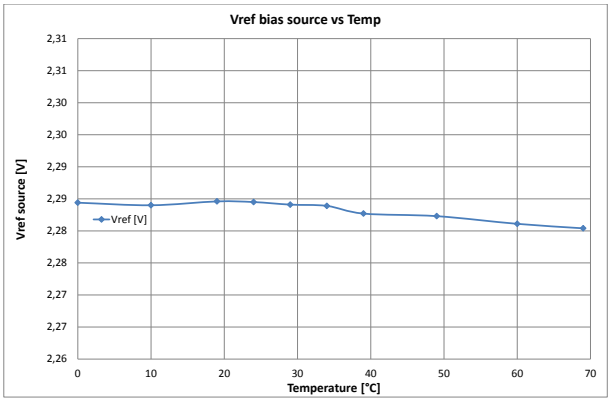


Figure 2.35.: PACTAv1.4 V_{ref} bias voltage source reference vs Temperature variation with $15k\Omega$ at R_{in} and Ln On.

Just a resistance network is needed to generate the different reference values: V_{casbip} is typically fixed to 2 V. V_{CM} provides the common voltage at the output (typ. 1,33 V). V_{Rdmp} typically 1,25 V and V_{casp} is typically fixed to 1,19 V.
A servo control loop controls the operating point of the output stage: (V_{bef}) is connected to the V_{befR} (typ. 2,2 V) and a de-coupling capacitor (1 nF) is used to stabilize the output reference.
It is recommended to use resistors with low TC (and equal between the different resistors inside the V_{REF} network) to avoid temperature variation effects. Values of $\pm 100 ppm/°C$ or bellow will be enough to avoid the temperature dependence (see table 2.3).

The PACTAv1.4 is biased by using four different current sources. I_{b0z} and I_{b20z} are the input stage bias current configuration and are typically fixed to $180\mu A$ by using a resistor of $6,65k\Omega$ respectively. I_{bcas} biases the TIA output stage and it is typically fixed to $330\mu A$

Table 2.3.: PACTAv1.4 Voltage biasing values (typ.).

V_{REF} **(V)**	V_{bef} **(V)**	V_{casbip} **(V)**	V_{CM} **(V)**	V_{Rdmp} **(V)**	V_{Casp} **(V)**
2.28	2.2	2	1.33	1.25	1.19

by using a resistor of $3,6k\Omega$. I_{bABf} configures the OPAMP output stage and it is typically fixed to $605\mu A$ by using a resistor of $1,96k\Omega$ (see table 2.4).
It is also recommended to choose resistors with low temperature coefficient like the voltage reference resistor network.

Table 2.4.: PACTAv1.4 Current biasing values (typ.).

$I_{b0z}(\mu A)$	$I_{b20z}(\mu A)$	$I_{bcas}(\mu A)$	$I_{bABf}(\mu A)$
180	180	330	600

The table 2.5 summarizes test results of PACTA prototypes.

Table 2.5.: Preamplifier requirements.

Parameter	**Results**	**Comments**
BW	500 MHz	
Noise (ENC). Diff	5 ke	10 ns integration time
Noise (ENI). Diff	400 nA rms	
SNR for SPE spectra	8 (40k / 5k e)	At nominal PM gain (40k)
Input range	20 mA	
Transimpedance HG	$1.2k\Omega$	
Transimpedance LG	75Ω	
Input impedance	$< 20\Omega$	Adjustable
Dynamic Range	15.9 bits	
Relative linearity error	< 2 %	(Charge meas). -fit/fit
Output swing over 50Ω (AC coupling)	1.4 Vpp	Differential output
	0.8 V	Single ended output
Power consumption @3.3 V operation	120 - 150 mW	2 diff. outputs (HG / LG)
	80 - 100 mW	2 S.E. outputs (HG / LG)

See the PACTAv1.4 Data Sheet at the Appendix A with more detailed indication for the implementation and usage.

2.4.2 Measurement results

Figure 2.36 shows the signal responses by applying a negative pulse at the I- PACTA input. So, the non-inverting output (Vo+) will be a negative pulse (like the input), and the inverting output (Vo-) will be positive output (opposite to the input signal). This must be taken into account in order to select the correct VoD configuration.

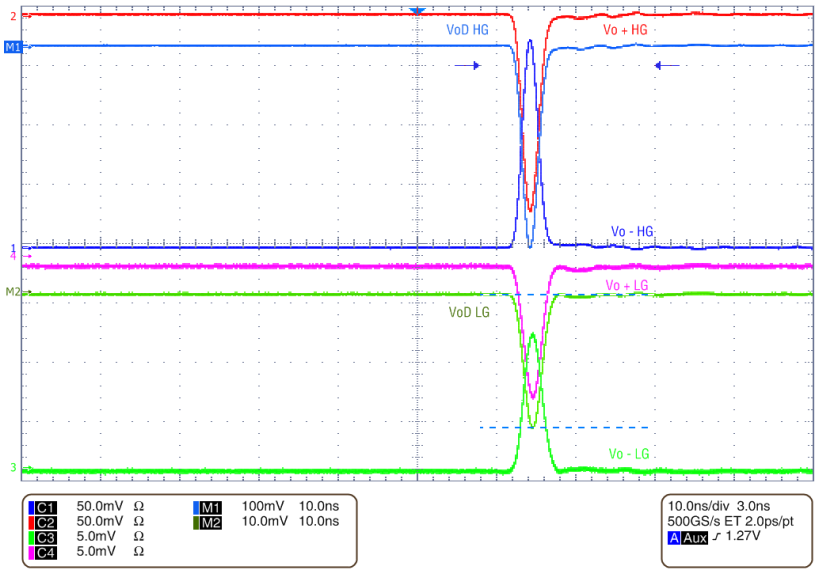


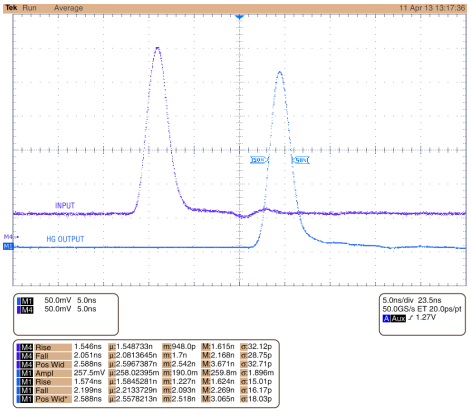
Figure 2.36.: PACTAv1.4 shape measurements with a negative pulse at the I− input. VoD is obtained by $(Vo+) - (Vo-)$.

In order to achieve fast pulse signals, PACTAv1.4 has a recovery time bellow 1.5 ns for both gain branches. Figure 2.37 shows the pulse width, amplitude, rise time and fall time by using an input signal in the linear region at the two gain branches.

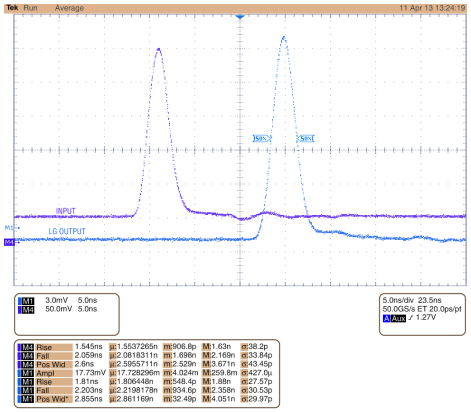
Differential HG and LG output signals are shown in figure 2.38 for input pulses of different amplitudes. The input pulse shape mimics the expected single photo electron pulse (SPE) shape. Even if the HG saturates for input peak currents exceeding 1 mA, the LG is still operating properly (thanks to the saturation control circuit at the HG branch). This can be also noticed in the transfer function of the circuit, as shown in figure 2.39.

The input signal for linearity test is the one depicted in figure 2.37, that try to mimics the signal shape from a SPE which corresponds of a $3\mu A$ of peak current. Linear region of HG and LG overlaps for more than 1 decade, allowing accurate calibration and HG is still linear bellow the single photo-electron.

The precise linearity error measurements of figure 2.40 confirm that the PACTA dynamic range is higher than 4 decades. Linearity error is given by the integral of the pulse, since the charge is the relevant information to compute the amount of light or energy deposited in the

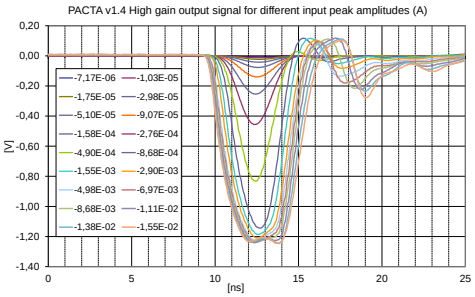


(a) PACTAv1.4 shape measurements with a negative pulse at the I- input. $V_{O_{HG}}$ is obtained by (Vo-) – (Vo+).

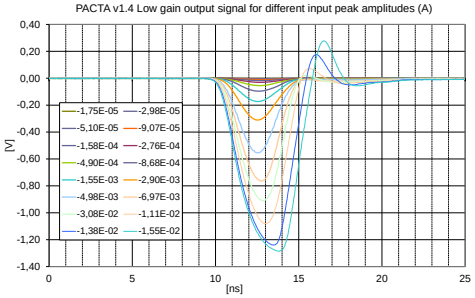


(b) PACTAv1.4 shape measurements with a negative pulse at the I- input. $V_{O_{LG}}$ is obtained by (Vo-) – (Vo+).

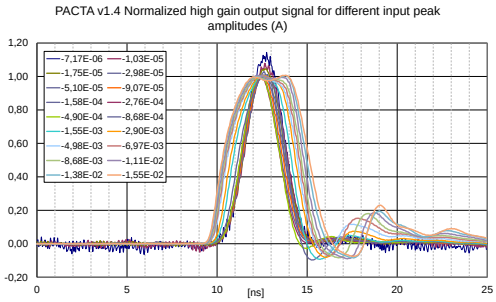
Figure 2.37.: PACTAv1.4 shape measurements with a negative pulse at the I- input. V_OD is obtained by (Vo-) – (Vo+). Input signal is depicted inverted in order to maintain the picture polarity



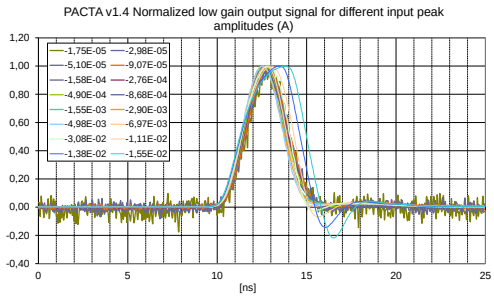
(a) HG (No Normalized).



(b) LG (No Normalized).

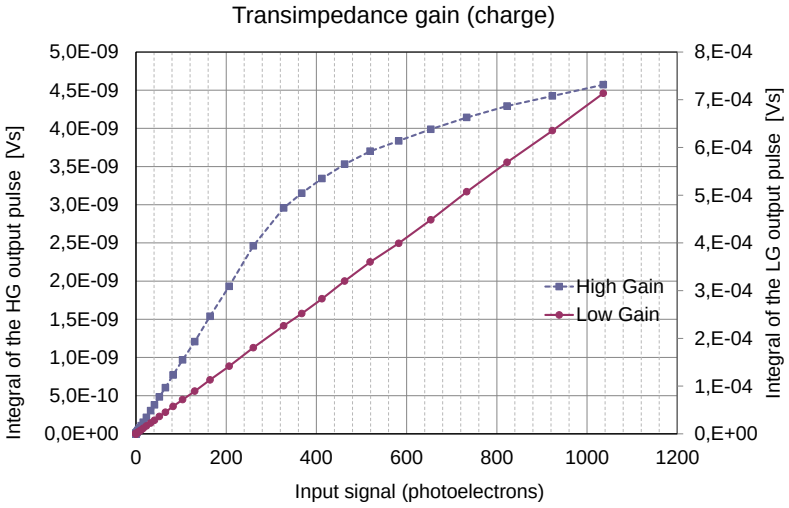


(c) HG (Normalized).

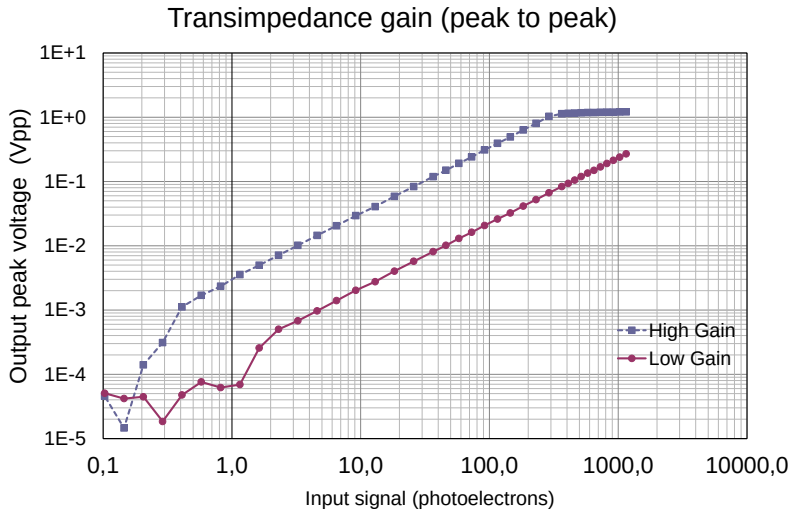


(d) LG (Normalized).

Figure 2.38.: PACTAv1.4 Differential output for different input pulse amplitudes with typical SPE pulse with $15k\Omega R_{in}$ and Ln On: HG (top left) and LG (top right). Normalized shape is shown for both at the bottom.



(a) Integral of the HG and LG differential outputs (linear).



(b) Integral of the HG and LG differential outputs (logarithmic).

Figure 2.39.: Integral of the HG and LG differential outputs as function of input peak current for typical SPE pulse shape: linear and logarithmic scale.

sensor. As previously mentioned, the pulses are typically integrated after digitization in order to compute the charge. It is also important to notice that relative linearity error given in figure 2.40 is defined as the relative residue with respect to the fit (not to the full scale), i.e. the ideal charge obtained by linear fit is subtracted from the charge measurement and then it is normalized to the fit value. The obtained linearity error is less than 2% for both gain branches.

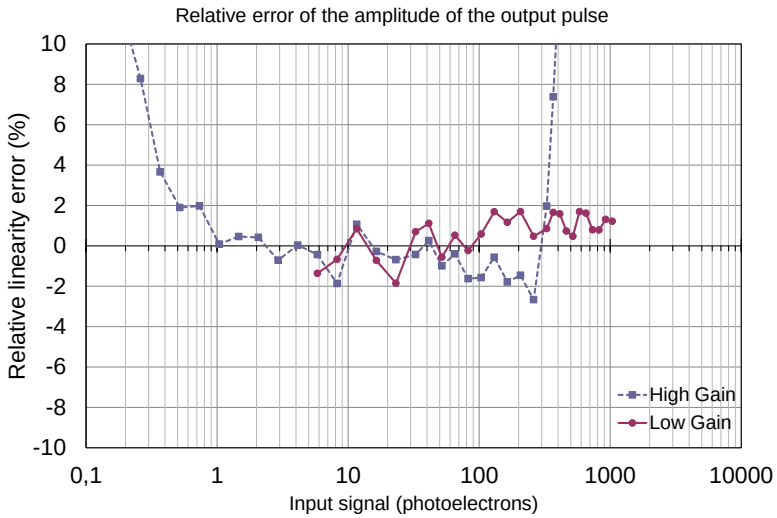


Figure 2.40.: HG and LG linearity error for charge measurement versus input peak current (typ. SPE pulse).

The dynamic characterization of the system is a measure of magnitude of the output as a function of frequency, in comparison to the input [37]. This measurement associated with a low-pass filter system, results as the difference between the upper and lower frequencies in a continuous set of frequencies (bandwidth). We used a network analyser to measure the frequency response of the system at each PACTA output, so we have required a post processed analysis to calculate the bandwidth in order to obtain a differential response of the system. The bandwidth obtained by applying a -30dBm input signal is 484 MHz. for HG path with $R_{in}15k\Omega$ and Ln On, and 361 MHZ for LG path, as can be noticed from figure 2.41. The dependence of the frequency response on the signal level is small [38].

According to the impedance measurement, the electrical impedance is the opposition that a circuit presents to a current when a voltage is applied. So, due to PACTA is a current amplifier, a series resistor (R_S) transforms the output voltage of the measurement instrumentation (network analyser) to current for the preamplifier input. Figure 2.42 shows the measured Z_{in}. Z_{out} is also measured and its $\approx 20\Omega$ are according to the ones in section 2.1.4.

The figure 2.43 on the left shows the SPE spectrum measured obtained with a PACTA and a PMT candidate for CTA. The PMT is operated at the nominal gain, which is 4x104 when it is biased at about 900 V (812V for the PMT model Hamamatsu R11920 s/n ZQ1871 calibrated by the manufacturer). The signal is digitized with 20 GS/s and 1 GHz BW DPO scope and then the charge is integrated numerically. Additional gain is obtained with commercial amplifiers; total transimpedance gain is $14.4k\Omega$. The ENC can be easily computed from the standard deviation parameter of the Gaussian function that fits the pedestal ($\sigma 1$ parameter), thus ENC $\approx \frac{11.8pVs}{q \times 14.4k\Omega} = 5.1Ke$, for 10 ns integration time. S/N is about 8. SPE spectrum has

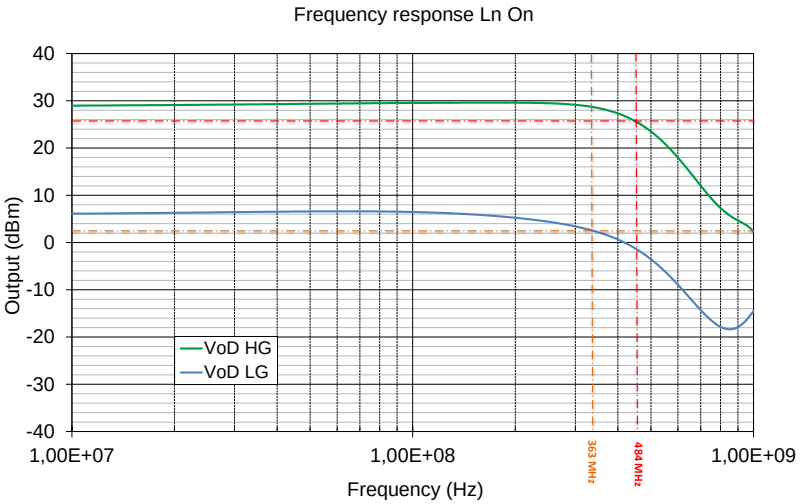


Figure 2.41.: PACTAv1.4 frequency response test with $R_{in}10k\Omega$ and Ln On.

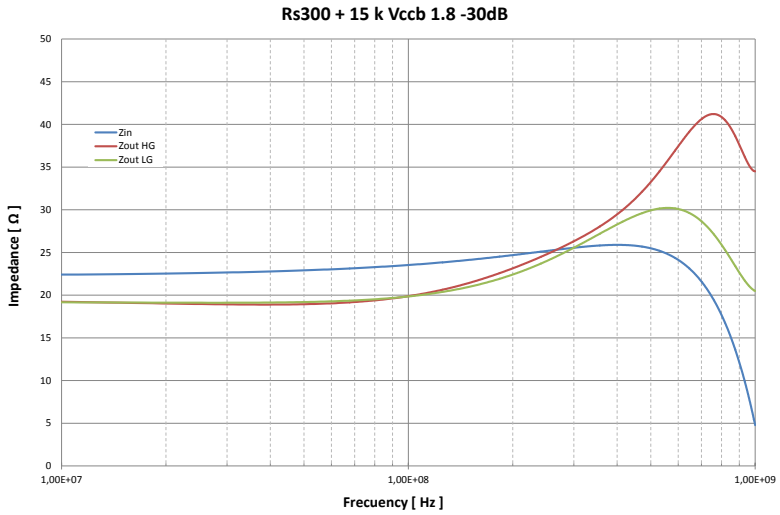
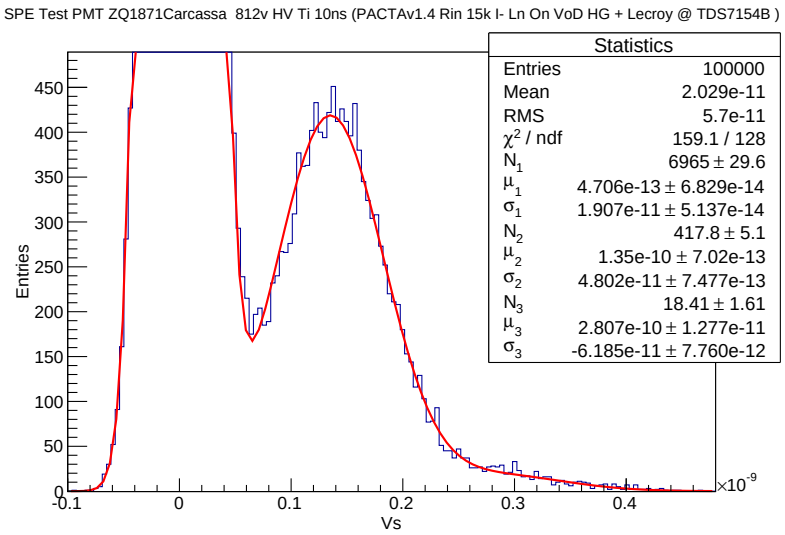
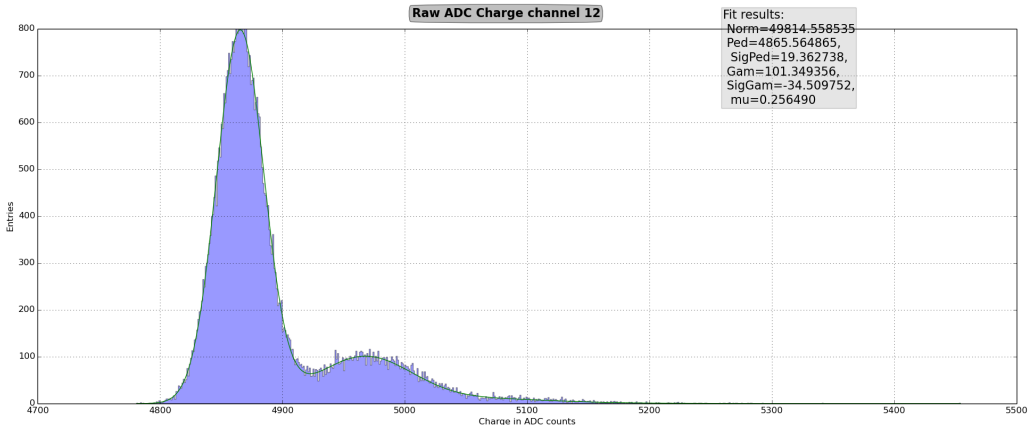


Figure 2.42.: PACTAv1.4 Impedance test with R_{in} 300 and $15k\Omega$ and Ln On.

also been measured with a prototype of a FE board designed for CTA by the NECTAr collaboration [39]. The result is shown in figure 2.43(b) using the same PMT at the same conditions.



(a) SPE spectrum with PACTA and a DPO scope (ti=10 ns).



(b) SPE spectrum with PACTA and NECTAR FE (ti=16 ns).

Figure 2.43.: SPE spectrum with PMT at nominal gain (40K) by using PACTA with a DPO scope (for 10 ns integration time) and NECTAR front end electronics (for 16 ns integration time).

The measured and theoretical ENC as function of the integration time are compared in figure 2.44 for both differential PACTAs. The required ENC of 4Ke is achieved for an integration time smaller than 8 ns.

Theoretical ENC is computed for 2 scenarios. In the first one ENC is calculated from expression (2.1), so it is only related to the total input referred parallel white noise generator (computed in section 2.1.6). In the second one PACTA series noise and noise of the off-

chip amplifiers is also taken into account. Theoretical calculations and measurements are compatible, especially when ENC is measured without PMT. The difference is not due to the additional capacitance, which is very low for this PMT, but by the interference or pick up noise. The discrepancies are more significant for short integration times, indicating the presence of HF pick up noise.

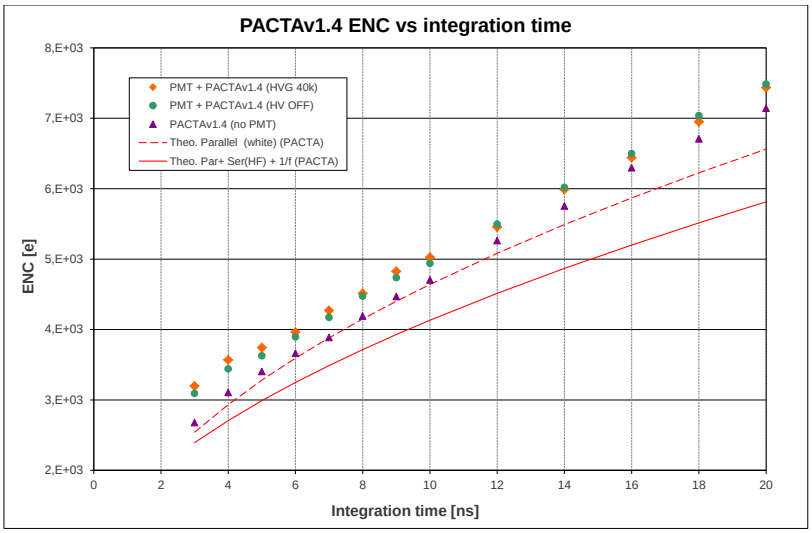


Figure 2.44.: ENC vs integration time, for calculations at different measurement conditions.

Average ENI for 12 chips is 400 nA rms (differential PACTA), in good agreement with noise analysis of section 2.1.6. According to figure 2.15, for moderate detector capacitances ENI is about 275 nA rms. Since uncorrelated noise sources add in quadrature, 275 nA rms $\times\sqrt{2} \approx 400$ nA rms should be expected for a differential PACTA.

Signal-to-noise ratio (S/R) is a measure that compares the level of a desired signal to the level of background noise (unwanted signal) and is used as a physical measure of the sensitivity of a system (2.11).

$$S/N = \frac{\mu_{sig}}{\sigma_{noise}} \tag{2.11}$$

where μ is the signal mean or expected value and σ is the standard deviation of the noise.

Figure 2.45 shows the S/N ratio measured in an anechoic chamber (-90 dB from outside) of PACTAv1.4 for different integration times in order to avoid unwanted contributions of the environment.

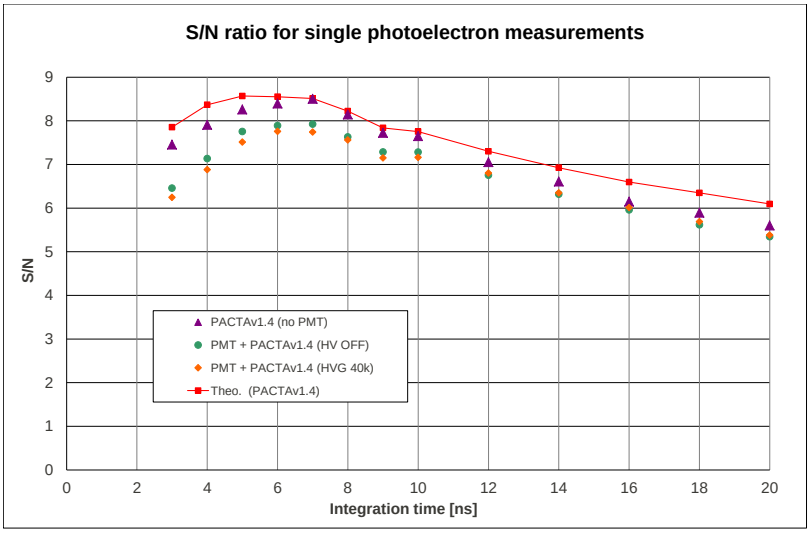


Figure 2.45.: PSCTAv1.4 S/N ratio for SPE measurements with $R_{in}15k\Omega$ and Ln On.

Given a sine wave generator of very low inherent distortion, it can be used as input to amplification equipment, whose distortion at different frequencies and signal levels can be measured by examining the output waveform (figure 2.46).

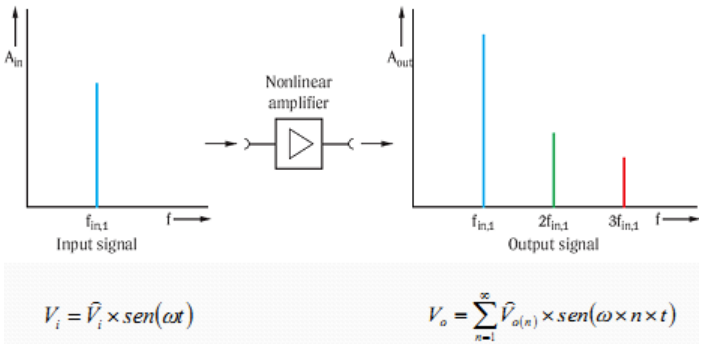


Figure 2.46.: Total Harmonic Distorsion (THD) definition for a Nonlinear amplifier [40].

The total harmonic distortion, or THD, of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. THD is used to characterize the linearity and the quality of the systems [41]. Lower THD means pure signal emission without causing interferences to other electronic devices. The THD is usually expressed in percent or in dB relative to the fundamental as distortion attenuation.

$$THD(dB) = \frac{P_1 + P_2 + P_3 + \cdots + P_\infty}{P_0} = \frac{\sum_{i=1}^{\infty} P_i}{P_0} \tag{2.12}$$

So, measuring different output amplitudes at each fundamental input frequency, the THD obtained is depicted in figure 2.47.

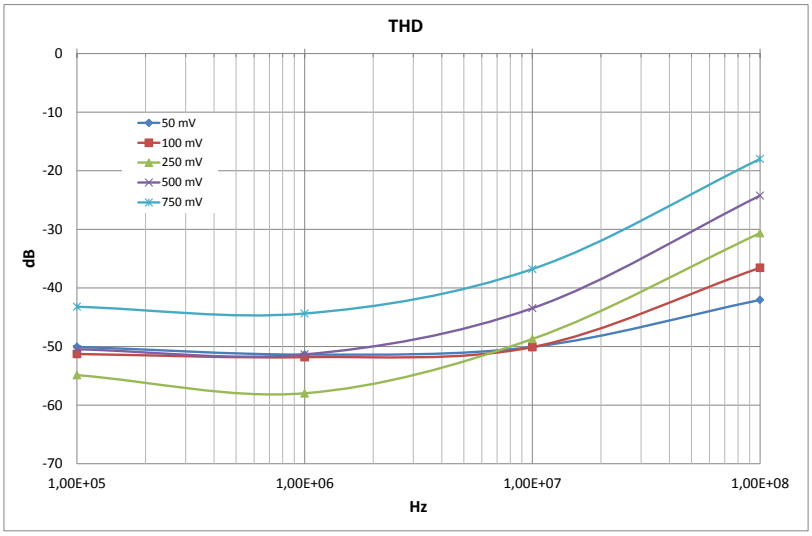


Figure 2.47.: PACTAv1.4 Total Harmonic Distorsion (THD) test with R_{in} 3k3 at different output signal amplitudes.

The frequency domain response of the differential output signal (HG) with a 500mV amplitude for a 1MHz input signal, shows a THD of -50 dB (see figure 2.48).

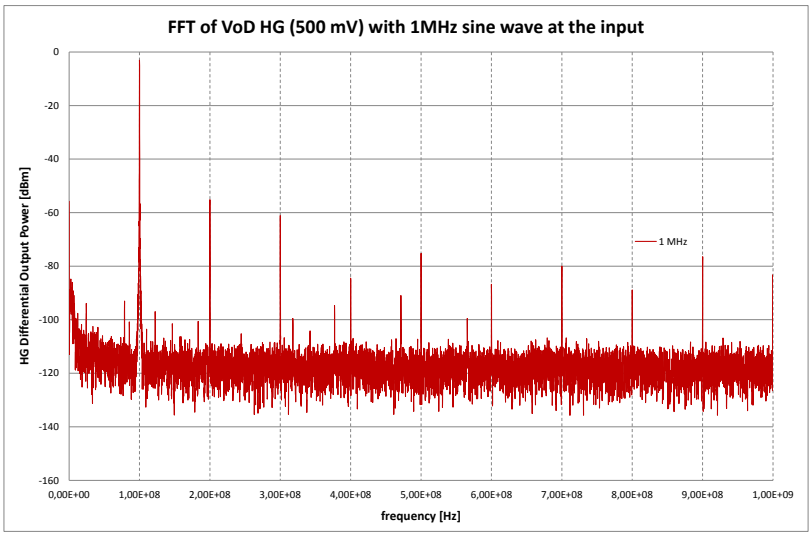


Figure 2.48.: PACTAv1.4 Frequency domain response of the differential output signal (HG) with a 500mV amplitude for a 1MHz input signal with R_{in} 3k3.

Power supply variation could affect to the amplifier gain, and so, the response obtained could be affected by the power supply variations. PACTAv1.4 has been designed to minimize this

effect and gain variations below 2% are observed (see figure 2.49). This effect, can also be noted in the PSRR characterization.

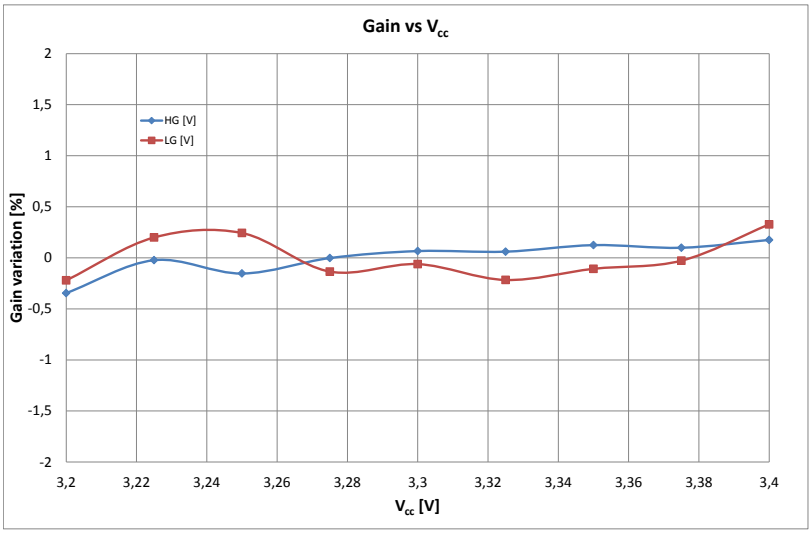


Figure 2.49.: PACTAv1.4 Gain variation as a function of Power supply (V_{CC} with 15k R_{in} and L_n On at HG.

Power Supply Rejection Ratio (PSRR) is the ability of an amplifier to maintain its output voltage as its DC power-supply voltage is varied and quantifies the amplifier's sensitivity to power supply changes [42]. Varying the supply voltage with a sine wave at several frequencies will result in a measured rejection ratio.

$$PSRR(dB) = 20log\left(\frac{\Delta V_{SUPPLY}}{\Delta V_{out}} \cdot A_v\right) dB \tag{2.13}$$

According to (2.13), a measurement by using a network analyser is performed. Figure 2.50 shows the results obtained by applying a -18dB to the V_{CC} power source. A bias tee[vi] is required to introduce the power supply changes to the DC level. So, PACTAv1.4 obtains a -60 dB with a -18dB at the V_{CC} power supply up to 100 MHz.

Common mode operating point could affect to the amplifier gain, and so, the response obtained could be affected by the power supply variations. PACTAv1.4 has been designed to minimize this effect and gain variations below 2% are observed (see figure 2.51).

[vi] A bias tee is a three port network used for setting the DC bias point of some electronic components without disturbing other components. The bias tee is a diplexer. The low frequency port is used to set the bias; the high frequency port passes the radio frequency signals but blocks the biasing levels; the combined port connects to the device, which sees both the bias and RF. It is called a tee because the 3 ports are often arranged in the shape of a T.

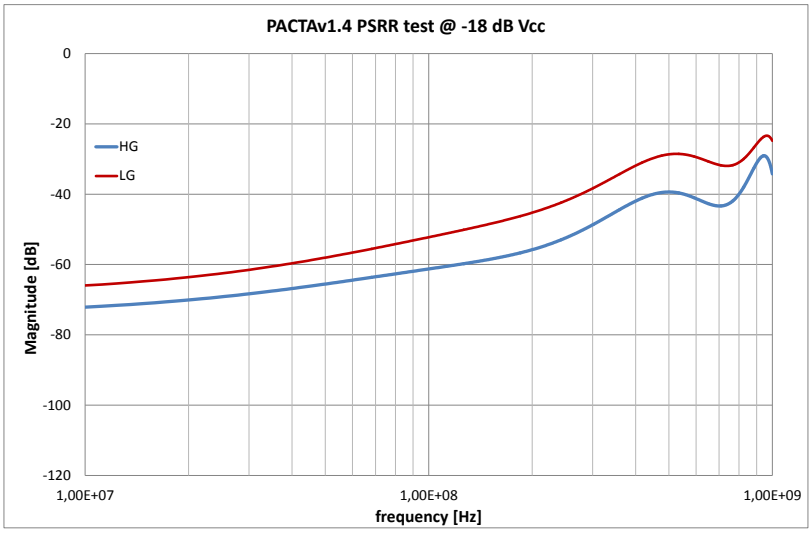


Figure 2.50.: PACTAv1.4 PACTAv1.4 PSRR measurements with 15k R_{in} and L_n On at Vcc of -18 dB.

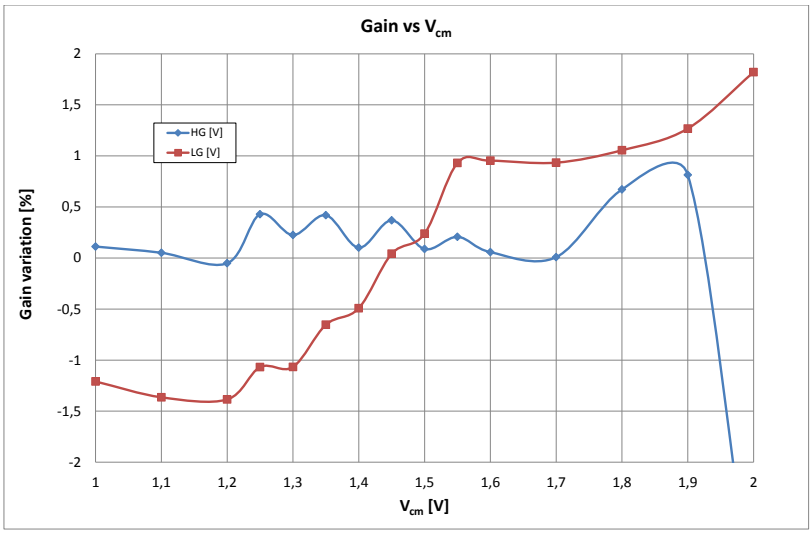


Figure 2.51.: PACTAv1.4 Common Mode variation vs Gain with 15k R_{in} and L_n On at HG.

On the other hand, the common mode operation point is directly related to the output range of the amplifier. So, adjusting this operating point, the effective phe range can be configured (see figure 2.52).

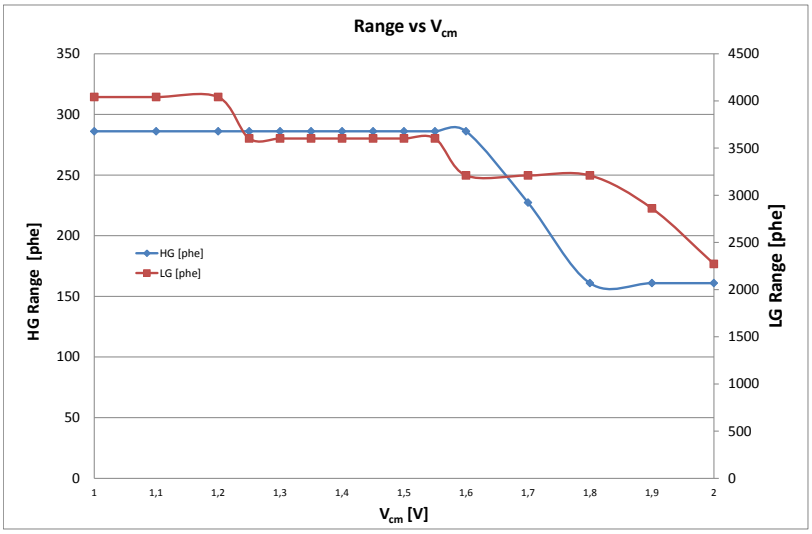


Figure 2.52.: PACTAv1.4 Common Mode variation vs Range with 15k R_{in} and L_n On at HG.

The power consumption variation as a function of the temperature dependence is $\approx 2\%$ (see figure 2.53).

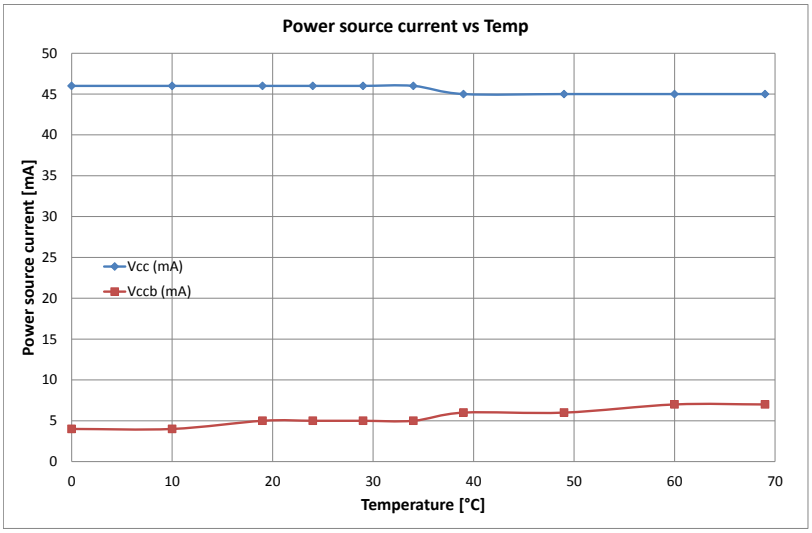


Figure 2.53.: PACTAv1.4 Power source current required as a function of the ambient temperature.

As a consequence of the power source variation, a gain variation is obtained. But thanks to the temperature compensated voltage reference source (see figure 2.35), the gain variation

is about ±0.5% for both gain branches (HG & LG). Figure 2.53, shows the charge gain variation as a function of the temperature.

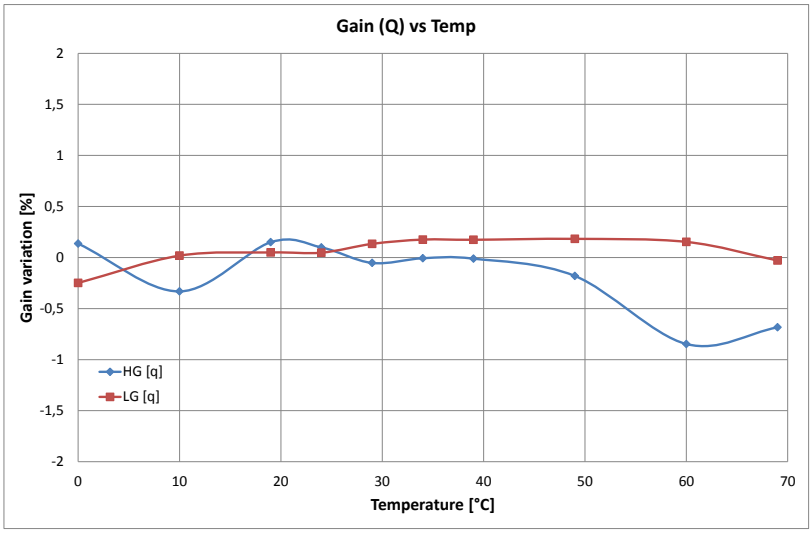


Figure 2.54.: PACTAv1.4 Charge Gain variation as a function of the ambient temperature.

2.5 Other applications

As it is mentioned in the Introduction Chapter, the SiPM sensors, will probably be the selected sensors for the future IACTs. There are a lot of performance improvements according to the main manufacturer announcements [43]. So, the CTA consortium are considering also an upgrade of their cameras to that new kind of photo sensors. Due to that, and as a future woks plans of this thesis, the PACTA pre-amplifier, is also tested to being operated with SiPM by using a very preliminary schematic like the represented at the figure 2.55.

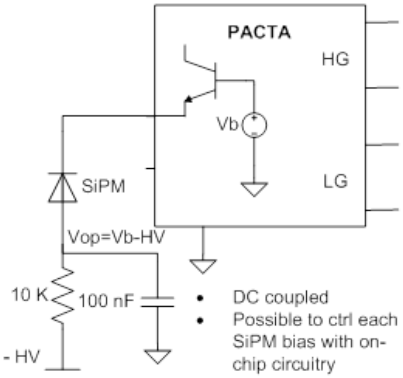
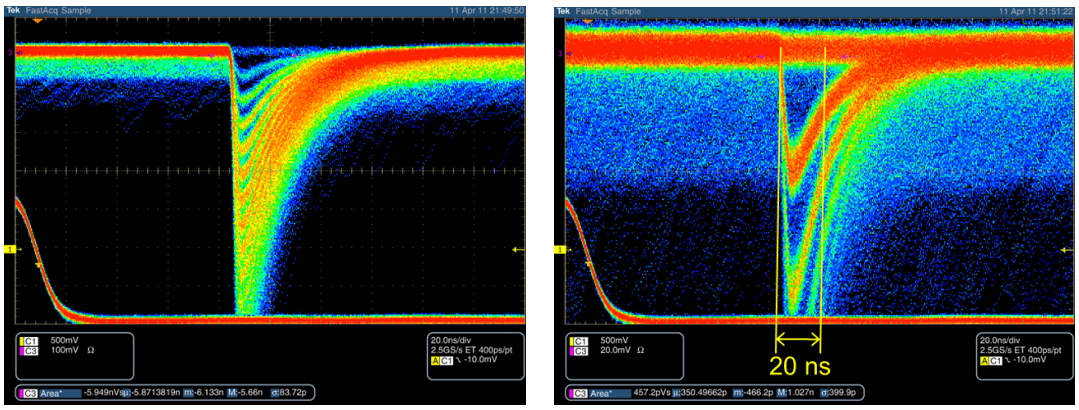


Figure 2.55.: Schematic diagram to use the PACTA pre-amplifier with SiPM sensors.

The figure 2.56(a) on the left shows the SPE spectrum measured obtained with a PACTA and a SiPM (model Hamamatsu MPPC S10931-050P). The SiPM is operated at 1V of over voltage above its breakdown voltage. The signal is digitized with 20 GS/s and 1 GHz BW DPO scope by a fast acquisition option to shows multiple waves at the same screen. A detailed view of the first photo-electron is shown in figure 2.56(b) using the same SiPM at the same conditions.



(a) SPE spectrum with PACTA and a SiPM.

(b) SPE spectrum detail at the first photo electron with SiPM.

Figure 2.56.: SPE spectrum with SiPM by using PACTA with a fast acquisition option of a DPO scope.

The low current mode circuit are well suited for SiPM readout and just a DC coupling is required to read the input signal (plus the polarization circuit for the SiPM, but less complex that the PMT polarization circuitry). The measured signal, shows that the recovery time seems to be dominated by the internal SiPM time constant.

The charge spectrum of a SPE for the PACTA output by using a SiPM sensor, shows the different photo-electrons detected much more clear than the SPE by using a PMT (see figure 2.57).

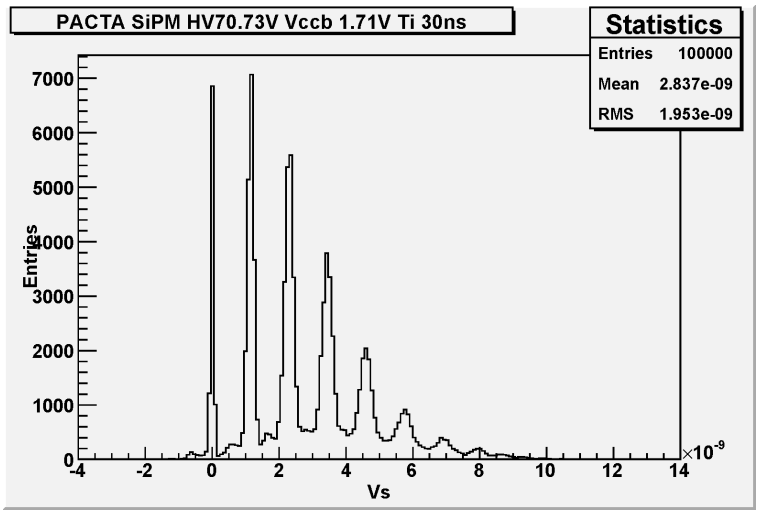
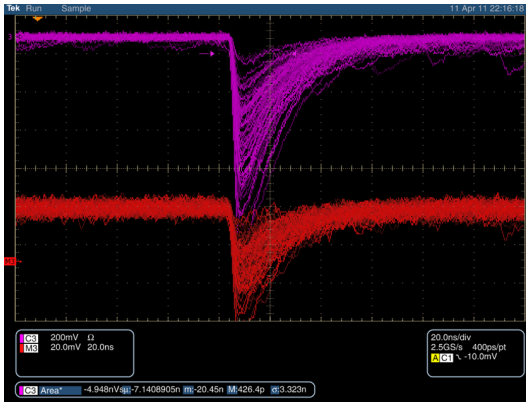
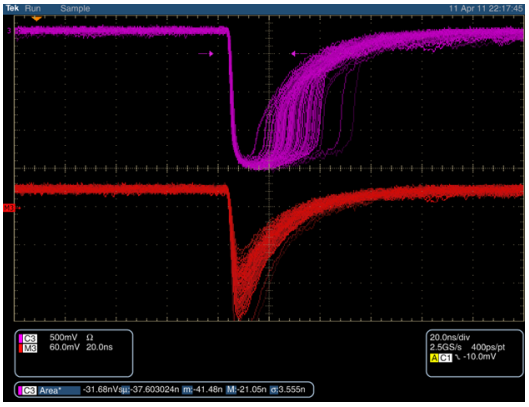


Figure 2.57.: SPE charge spectrum of the PACTA output with a SiPM input signal.

Also, the relusts shows that the Bi-gain configuration of the PACTA pre-amplifier is still working as it is shown at figure 2.58(a) where the violet waveform represents the differential high gain PACTA ouput and the red one, represents the differential low gain PACTA output with an output signal at the a linear range at both PACTA gain branches. Whereas, figure 2.58(a) shows the HG PACTA output branch saturated, but the LG is still working.



(a) Bi-Gain PACTA output signal at linear range with SiPM signal input.



(b) Bi-Gain PACTA output signal at the HG branch saturated with SiPM signal input.

Figure 2.58.: Bi-Gain PACTA output signal with SiPM signal input.

As it is shown in figure 1.9, the Trigger Interface Board (TIB) must comply with several requirements in order to work together with the readout electronics. First, the trigger decision must be taken in a cluster level and distributed to all camera clusters through the central backplane and from here to the TIB. This TIB board gathers different trigger origins and produces the final trigger command which is send to the central backplane again to be distributed to all the clusters in order to actually start their readout. In the case of LSTs, the trigger interface board of each camera is also connected to the TIBs of the neighbour LSTs sharing their trigger information in order to implement stereo trigger schemes.

When there are several IACTs working in coincidence in an array, it is possible to improve the NSB rejection by imposing that only the events which caused trigger in two or more telescopes in a given time window are digitized. The system which checks this condition is generally known as array-level trigger or "Stereo trigger" and is usually implemented as an electronic module in a central position of the array. Every time that the camera trigger of one telescope is generated, it sends a trigger signal to the central unit, typically through an optical fiber (see figure 2.59) [2].

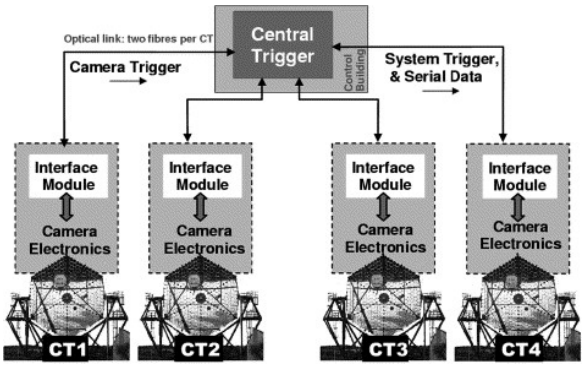


Figure 2.59.: Scheme of the HESS array trigger [44].

Some essential hardware elements of the Trigger Interface Board are the optical links. Even in the case of MSTs triggering in mono, where no communication with neighbours would be required, some optical links are needed for the communication with the calibration box (calibration and pedestal triggers), or as an alternative possibility to implement fixed delays with optical fibers.

The optical links were implemented in the first prototype with standard Small Form Factor Pluggable (SFP) transceivers, like the ones used in optical Gigabit Ethernet networks. These transceivers are easy to control, and very adequate for data transmission through cheap OM3 optical fibers in distances of up to 550 m length. However the tests showed that the SFP transceivers were not a suitable option for sending trigger pulses.

When testing an optical link, it was observed a high level of noise in the received signal. This was caused because, in the transmitter, the differential low-voltage positive/pseudo emitter-coupled logic (LVPECL) inputs are AC coupled as shown in figure 2.60. If the signal is changing very fast, like it is the case in the Ethernet signals[vii], it works properly but,

[vii] Optical Gigabit Ethernet uses 8b/10b encoding, which achieves DC balance by mapping 8 bit symbols in 10 bit symbols, where there are never more than 5 consecutive zeros or ones [45].

this is not the case of the digital trigger pulses. These trigger pulses sent by the camera telescopes consists of pulses of a few nanoseconds width (around 10 ns), which are sent at a maximum rate of some hundreds of kHz. This means that the baseline is set to "0" during most of the time. Looking at the scheme of figure 2.60, it is easy to understand that the DC levels of such a differential signal are removed by the capacitors, so the DC voltage is the same in the positive and negative inputs of the receiver (points marked as TD+ and TD- in the figure). In this situation, the slightest noise fluctuations are recognized by the transmitter as "0s" or "1s", sending noisy pulses. Real pulses are effectively sent, but together with thousands of noise pulses.

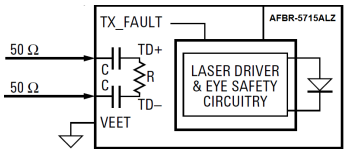


Figure 2.60.: Emitter part of an SFP, transceiver, AC coupled.

The solution to this problem will consist of replacing the SFP transceivers of the first TIB prototype by analogue optical links implemented with discrete vertical-cavity surface-emitting laser (VCSELs) and PIN photo-diodes[viii]. Designing the optical transmitter and receiver with discrete VCSELs and PiN photo-diodes is an option which provides with great flexibility to optimize the bandwidth, the cost or the power consumption. The drawback is that some analogue processing stages need to be designed in order to feed the VCSEL with a signal inside its input range, and to recover an low-voltage differential signaling (LVDS) signal from the analogue output of the photo-diode. The most critical characteristic is the bandwidth, which must be as large as possible in order to have pulses with very sharp edges, thus maintaining the timing information.

The receiver, first introduces the current signal from the photo-diode into a PACTA transimpedance amplifier. The output of the PACTA is a differential voltage signal, which is converted into single-ended. Then the single-ended output is compared with a threshold, which generates the LVDS output.

Figure 2.61 shows the signal at different parts of the receiver scheme. The blue line is the PIN photo-diode output (measured in voltage), the ping line corresponds to the differential putput of the PACTA pre-amplifier and the yellow line is the output of the single-ended to differential stage (this stage introduces certain gain to increase the range of the comparator stage).

The transceivers have been implemented in test boards and tested with two optical fibers of 2 and 500 m. Figure 2.62(a) shows the measured signals corresponding to the 2 m link. The purple line was measured with a probe[ix] with the aim to show that this kind of links can handle pulsed signals properly. On the other hand, figure 2.62(b) shows the input and output with a 500 m optical fiber, demonstrating that the optical power

[viii] A PIN diode is a diode with a wide, undoped intrinsic semiconductor region between a p-type semiconductor and an n-type semiconductor region. The p-type and n-type regions are typically heavily doped because they are used for ohmic contacts.

[ix] The length of the probe cable is longer than the one of the cable which connects the LVDS output to the oscilloscope. This is why the LVDS output appears before the analogue pulse.

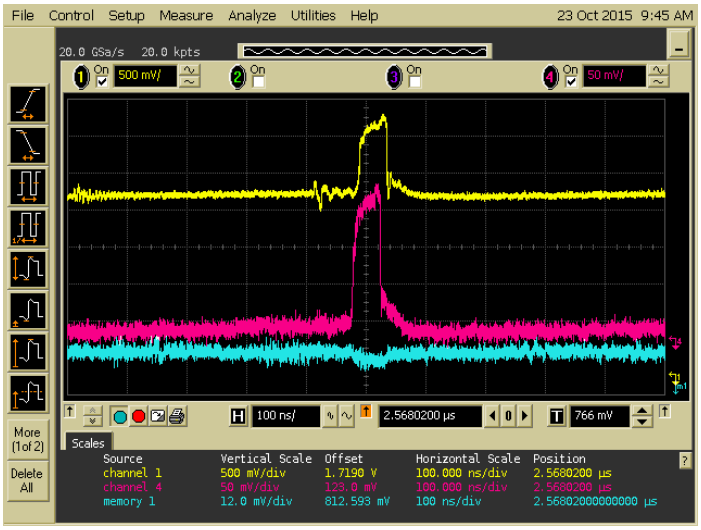
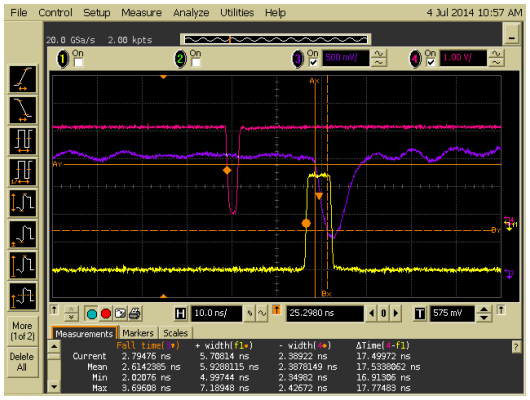
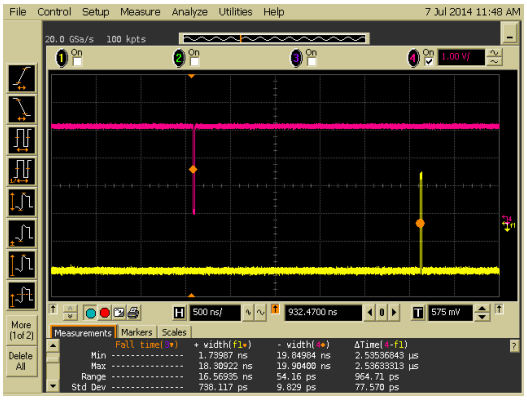


Figure 2.61.: Emitter part of an SFP, transceiver, AC coupled.

and the sensibility of the receptor are adequate. The bandwidth is large enough to allow sharp edges and, as a result, the jitter is very low: only 77 ps with the 500 m optical fiber.



(a) Inverted copy of the input signal (magenta), received analog signal at the input of the comparator (purple) and LVDS output (yellow) of the analog optical link, with a 2 m optical fiber.



(b) Inverted copy of the input signal (magenta) and received LVDS output (yellow) of the analog optical link, with a 500 m optical fiber.

Figure 2.62.: Two optical fibers of 2 and 500 m length by using the PACTA pre-amplifier at the receiver link stage.

The PACTA pre-amplifier represents at the moment of writing this thesis, a transimpedance amplifier with better performances in terms of bandwidth, transimpedance gain and low noise than the most of the commercial transimpedance amplifier in the market and it can be used in any optical communication link to amplify the current output of the receiver photo-diode. In the TIB case, the special characteristics of the trigger signal (short pulses with the most of the time to "0"), had required a dedicated ad hoc design with enough bandwidth to maintain the timing accuracy at the rising edge of the trigger pulse, which the PACTA pre-amplifier can provide without introduce significant noise level signals to the system, as it is demonstrated previously.

Confocal Laser Scanning Microscopy (LSM) is based on a conventional optical microscope in which instead of a lamp, a laser beam is focused onto the sample and an image is built up pixel-by-pixel by collecting the emitted photons, usually with a PMT. Thus, LSM combines point-by-point illumination with simultaneous point-by-point detection. The images of a mouse intestine section in figure 2.63, noticeably illustrate the gain in resolution in confocal LSM imaging over conventional wide field imaging [46].

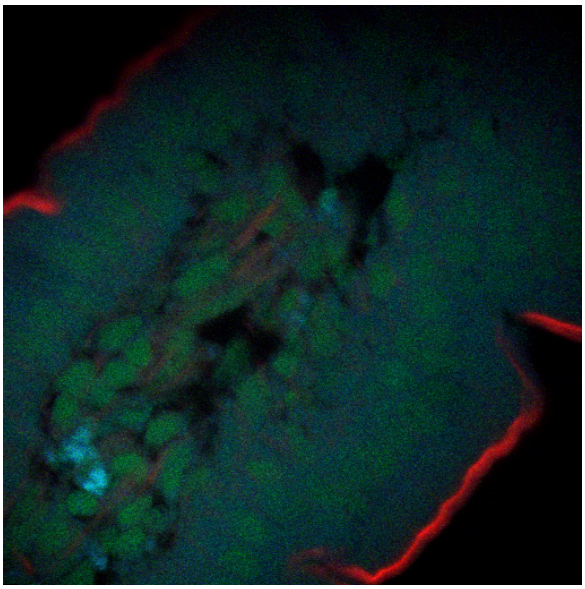


Figure 2.63.: Mouse intestine section image ($100\mu m \times 100\mu m$ observation area) with Alexia Fluor 350 WGA, Alexa Fluor 568 phalloidin SYTOX Green observed with a confocal LSM with pulses of 150 fs FWHM[x]at 76MHz in a Ti-sapphire laser at 810 nm wavelength of about 30 mW of average light power.

Two-photon excitation LSM can be a superior alternative to confocal microscopy due to its deeper tissue penetration, efficient light detection, and reduced photo-toxicity. The high flux of excitation photons typically required is usually obtained using a femtosecond laser. One of the most common ultra-short pulse lasers is the Ti-sapphire laser that has typical pulse widths of approximately 150 femtoseconds and a repetition rate of about 80 MHz [48].
In order to get good resolution at the images reconstructed at the LSM observations, the size of these images becomes an important factor. The typical image size in a LSM observation is at least of 512 x 512 pixels so, several hundred thousand laser shots impact to the specimen to observe. In order to avoid undesired effects like photo-bleaching or photo-toxicity, it is crucial to minimize as much as possible the laser power and pixel dwell time. In the other hand, demands on recordings of fast biological processes require fast acquisition speeds thus very high readout speeds. One of the limits in the readout is the bandwidth of the electronic circuitry, and especially when there is some averaging applied at each pixel samples, in order to reduce the photonic fluorescence noise.
Most of the current electronic circuits used in the readout systems of fluorescence microscopy are low bandwidth systems (below 100 MHz). This could seems enough according to the common data acquisition (DAQ) systems used to store the pixel-by-pixel images that can

[x]Full width at half maximum (FWHM) is the width of a spectrum curve measured between the two extreme values on the y-axis which are half the maximum amplitude [47].

operate up to 10 MS/s. Some techniques are used to "collect" multiple fluorescence pulses in order to do not loose information due to the DAQ sampling rate as integration circuits, that their output is proportional to the amount of the input signal during a period of time [49].

In that sense, the use of the PACTA pre-amplifier as a low-noise wideband pre-amplifier to improve the collection speed while maintaining the dynamic range of the acquisition (see figure 2.64 for the block diagram of the system used), shows a considerable improvement as a comparison of the image observed with a typical commercial pre-amplifier (see figure 2.65).

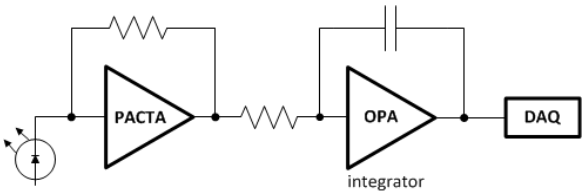
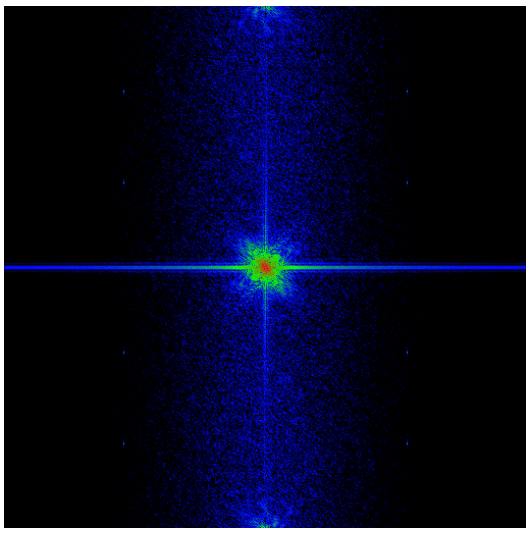


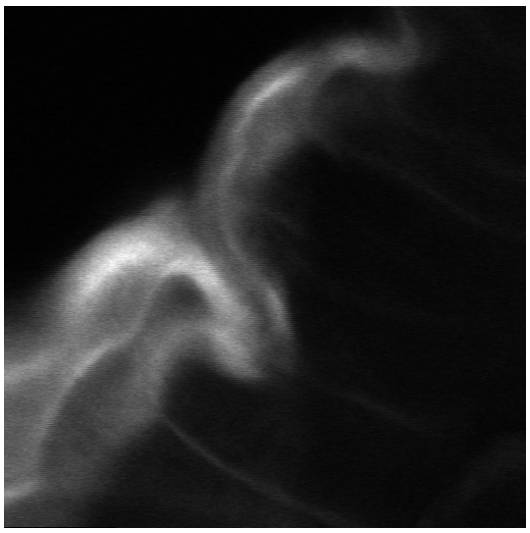
Figure 2.64.: Simplified block diagram of the schematic used to send the data coming form the PMT of the confocal LSM to the DAQ by using the PACTA pre-amplifier.

Using the integration circuitry, the PMT of the fluorescence microscopes, can be read with low bandwidth pre-amplifiers. But, analysing the images obtained, it can be appreciated a loose in the high frequencies at the FFT spectrum. Figure 2.65(a) shows an FFT spectrum of 2.65(b) where each point represents a particular frequency contained in the spatial domain image. Notice that all the data is concentrated at the centre of the image, whereas the same specimen illuminated at the same conditions by using the PACTA pre-amplifier as a low-noise wideband amplifier of 500 MHz, with a dedicated integrator scheme, there is no loose at the FFT spectrum (see figure 2.65(c) and 2.65(d)).

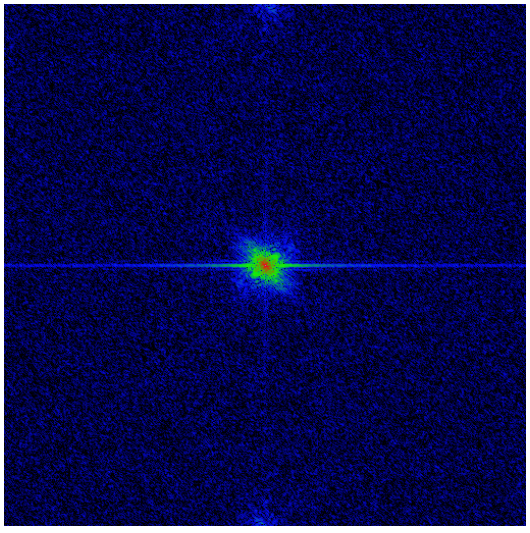
These image analysis, means that the use of low bandwidth pre-amplifiers for confocal LSM high speed observations presents a mixing data information between the consecutive scanned pixels whereas the observations with high bandwidth pre-amplifiers, all the data is processed at each own pixel obtaining more realistic images of the fluorescence data coming from the specimen observed.



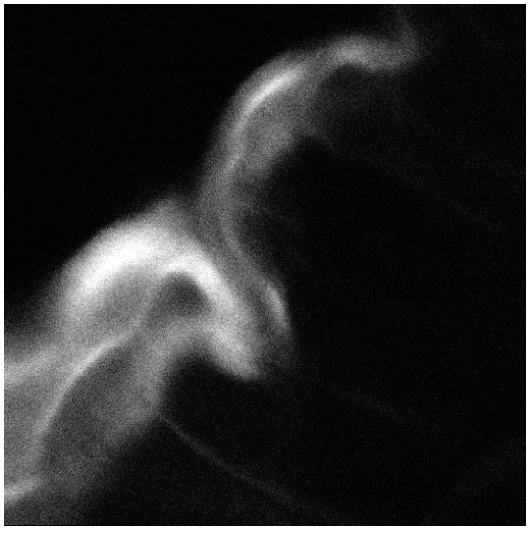
(a) FFT spectrum of the image.



(b) Image zoom of the mouse intestine wall with 200kHz bandwidth readout system.



(c) FFT spectrum of the image.



(d) Image zoom of the mouse intestine wall with PACTA pre-amplifier.

Figure 2.65.: Images analysis comparison with a commercial pre-amplifier (Hamamatsu C-7319) and PACTA.

2.6 PACTA Conclusions

The PACTA chip fulfils the CTA general requirements based on an innovative design that achieve all the restrictions with a very low power consumption. Single ended and differential versions have been designed and tested. The chip is based in a novel current mode circuit to create multiple gain paths at the very front end of the input stage of the readout electronics, allowing to achieve simultaneously high dynamic range, low noise, low input impedance, low voltage and low power performances. The power consumption of the input stage is below 10mW with a BW of 500 MHz.

- High dynamic range (16 bits).
- High bandwidth (500 MHz).
- Low noise ($i_n < 10pA/\sqrt{Hz}$ or $ENC < 5Ke$).
- Low input impedance ($< 20\Omega$).
- Low voltage/low power. Input stage can be operated at 3.3 V, with low power consumption ($< 10mW$).

The PACTA chip also comprises a closed loop transimpedance amplifier with a novel class AB output stage allowing PACTA to drive a cable or a transmission line (typ. 50Ω load) while preserving high BW (500 MHz) with moderate power consumption; less than 150mW for a dual (HG and LG) differential output. The power consumption of the alternative solutions based on COTS components which were tested for CTA camera prototypes but discarded is at least 4 times higher.

3

Amplifier for the CTA cameras (ACTA)

The front-end electronics (FE) of the CTA cameras is based on an analogue memory which samples and stores the signal at more than 1 GHz [12]. The CTA observatory will have about 50 to 100 telescopes of various sizes, each of them with 1000 to 4000 channels (depending on the telescope size). These number of channels (form 50.000 to 400.000) requires an special care at the electronics design to make it as cheaper but with the maximum performances as possible. An integrated circuit solution is the best option to adjust the performance to the requirements at low prices due to the number of channels needed. The dynamic range (DR) required for the FE is on the one hand by the measurement of the single photo-electron signal (SPE) for calibration purposes, and on the other hand by the highest light pulse (5000 PE). As depicted in figure 3.1, this DR will be achieved using two gains feeding two analogue memory channels per PMT pixel with a ratio 1:20, each with an effective 12-bit DR.

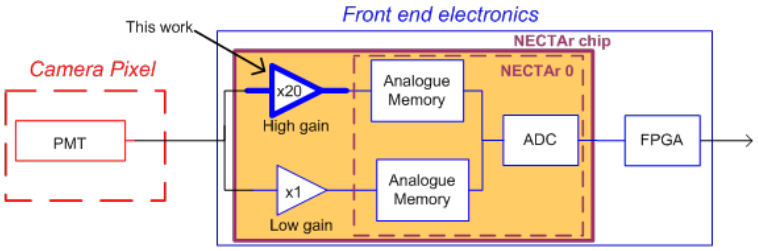


Figure 3.1.: Block diagram of the front end electronics proposed by NECTAr project.

The NECTAr (New Electronics for the CTA array) collaboration [13] intends to build a new integrated circuit including most of the discrete components needed so far. It is one of the front end electronics options considered for the CTA cameras [25]. A gain in cost, reliability and camera performances can be achieved by maximizing the integration of the front-end electronics in an ASIC, a single GHz sampling chip. The first version of the chip is NECTAr0, it is based on the Sampling Analog Memory (SAM) chip [24] fabricated in Austriamicrosystems $0.35\mu m$ CMOS technology. This chapter, present the design of the input amplifier for the two gain paths of the new stand alone ASIC. High gain amplifiers must have a voltage gain of 20 and a bandwidth of 400 MHz for a 3 pF load [25]. Furthermore, amplifier non-linearity must not exceed 1%. Input referred series noise (e_n) power spectral density (PSD) must be smaller than $3nV/\sqrt{Hz}$ in order to perform SPE calibration at a PMT gain of 2×10^5. Output excursion must be higher than 1.5 Vpp with a 3.3 V power supply.

3.1 Design ACTA

A fully closed loop solution based on voltage feedback amplifiers (OTA or OpAmp) is not feasible because a Gain-bandwidth (GBW) product of more than 8 GHz is required, and the maximum GBW product that can be achieved in a $0.35\mu m$ CMOS technology is well below 1 GHz ([14], [15]). An alternative approach based on linearised high frequency (HF) transconductors is explored. As depicted in figure 3.2, the transconductor, which includes dedicated circuitry to adjust the DC offset in order to be properly DC coupled to the NECTAr0 ADC, is followed by a high swing current to voltage conversion, and finally a low output impedance closed loop buffer is used to drive a capacitive load.

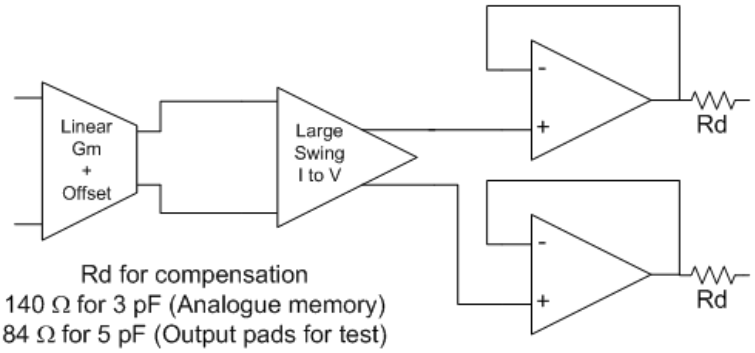


Figure 3.2.: Block diagram of the proposed amplifier.

3.1.1 Linearized HF Transconductor

Linearized transconductors are the basic building block for G_mC filters (continuous-time filters implemented with transconductance amplifiers and capacitors), which are often used in HF applications [50]. After analyzing and simulating several topologies, the bias offset cross coupled differential ([51] and [52]) has been selected, since it fulfills linearity, noise and bandwidth requirements. It can be readily shown that a perfectly linear transfer function can be obtained by means of two cross coupled differential transistor pairs operating in saturation [50].

First, Wang and Guggenbuhl [51] used voltage shifters from the inputs to the gates of the transistors of the differential pairs to create the offset voltage. However, those voltage shifters introduce additional poles; thus limiting the bandwidth. Szczepanski et al. [52] presented an alternative technique to overcome this limitation; the circuit is shown in figure 3.3.

Both differential pairs are biased by a direct current I_{bias} in combination with an adjustable floating voltage source V_b. Using the standard square-law of the MOS devices in saturation it

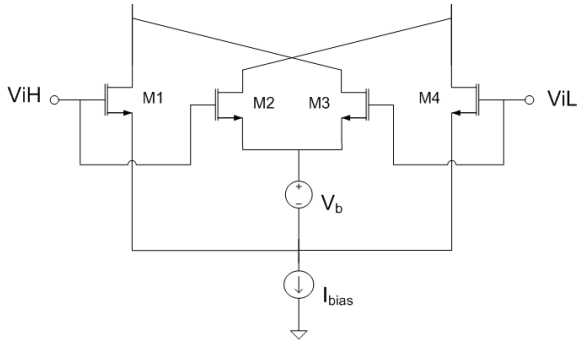


Figure 3.3.: Cross coupled transistor pairs with bias offset.

can be shown, that the differential output current is $I_{oD} = KV_bV_{iD}$, where $K = 1/2\mu C_{ox}W/L$. μ is the charge-carrier effective mobility. C_{ox} corresponds the capacitance of the oxide layer per unit area. W corresponds to the channel width and L to the channel length. Thus, the block exhibits a perfectly linear transconductance of value $G_m = KV_b$ which is tunable by varying the floating DC voltage source, provided that the output impedance of the source is low enough; otherwise G_m depends also on I_{bias} [52].

The floating low impedance voltage source is shown in figure 3.4. The voltage is controlled by the offset in the V_{gs} of two matched PMOS transistors (M5/M6), drain current of M5 is fixed to I_s whereas drain current of M6 is connected to a the controlled current source I_{cf}, allowing to tune V_b. Low output impedance is achieved thanks to the high-gain negative feedback including offset transistors M5/M6, differential amplifier M1/M2 and output transistor M4, which has a large W/L ratio in order to be able to cope with large I_{bias} currents (up to 8 mA).

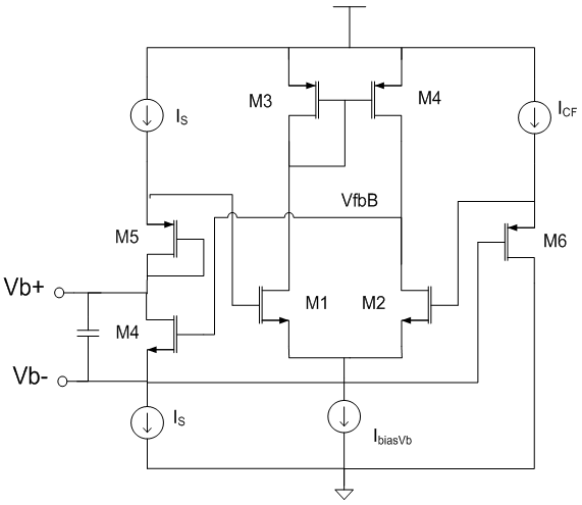


Figure 3.4.: Floating voltage source V_b.

The transistor of the cross coupled differential pair must operate in saturation; the condition $|Vin| \leq \sqrt{\frac{I_{bias}}{K} - \frac{3}{4}V_b^2} - \frac{V_b}{2}$ sets the limit of the dynamic range of the circuit. Since both V_b and K are proportional to G_m, it means that there is a trade-off between power consumption, linearity and transconductance, which is linked to the noise and GBW performances. The former is dominated by the channel thermal noise of M1–M4 (figure 3.3); to achieve the

required input referred noise, G_m has to be larger than 5 mS. It has to be pointed out that cross-coupling degrades noise performance via G_m subtraction. Concerning GBW product, having a gain of 20 V/V means that G_m has to be as large as 15 mS; because, as discussed in next subsection, the current to voltage conversion is limited to $< 1.5k\Omega$ to preserve a minimal BW of 400 MHz. In order to achieve such a large G_m, the W/L ratio of the transistor of the crosscoupled pairs has to be large, thus minimal length ($0.35\mu m$) and a large width ($150\mu m$) are used. Moreover, use of NMOS is mandatory, despite of its worse linearity because of body effect, with respect to PMOS in a NWELL technology, were NMOS and PMOS, means n and p channel MOSFET transistor, respectively. NWELL means n substrate type.

Second order effects like channel length modulation, mismatch, mobility reduction and body effect degrade the linearity performance of the circuit. Since minimal channel length is used, the only way to minimize channel length modulation is through control of drain voltage, this is discussed in next subsection. Regarding mismatch, the input transistors are relatively large area devices with common centroid layout. Body effect will be present since no PWELL is available in this technology; however both the body effect and the mobility reduction effects can be partially compensated via properly scaling of the W/L ratios of both crosscoupled pairs [52] were PWELL means p substrate type.

3.1.2 Large Swing Current-to-Voltage Conversion

As depicted in figure 3.5, the output of the transconductor is sensed by the transimpedance amplifier composed by the regulated common gate transistor M5 (M7) and the resistor R_C. The input impedance of the common gate stage is decreased by the feedback provided by the wideband common source amplifier composed by M8 (M6) and R_F.

The motivation to achieve low input impedance at the source of M5 (M7) is twofold. On the one hand, the bandwidth is not limited by the time constant related to this node, despite of the large capacitance (large transistors are required). On the other hand, it avoids linearity degradation via channel length modulation, since the drain voltage of the transistors of the cross-coupled differential pairs is kept nearly constant for the full dynamic range.

The folded structure maximizes the voltage swing in the output nodes, the only headroom is given by the minimal saturation V_{ds} voltage for common gate transistors M5 (M7) and current sources ($2/3I_{bias}$). The dominant pole of the amplifier is given by the only internal high impedance node, i.e. the output node. Taking into account the input capacitance of the output buffer, for a BW exceeding 400 MHz maximum R_C should be $1.5k\Omega$.

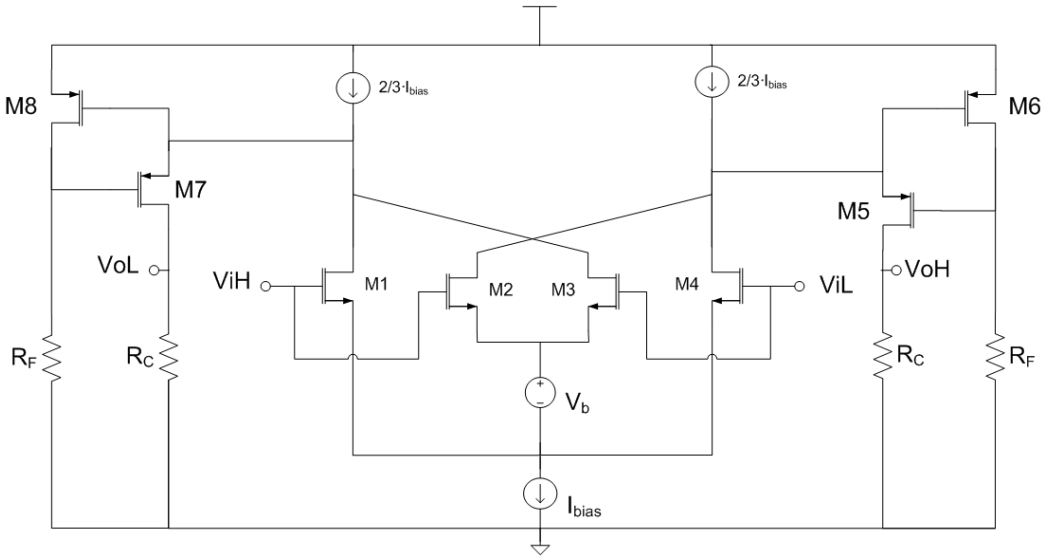


Figure 3.5.: Simplified schematic of the amplifier, without output buffers.

3.1.3 Output Buffer

The final version of the output buffer is a closed loop buffer (for unity gain a GBW product of 400 MHz is sufficient) based on a low power class A/AB OpAmp (figure 3.6). It is a Miller OpAmp with a NMOST as output transistor (M8), therefore it possesses good capability to sink current to the load but the sourcing capability is limited by the PMOS current source that bias the output NMOS. Two additional mechanisms to boost the current sourcing capability for large signals have been added. A linear class AB boost increases the current that can be sourced to the load by a factor 2. Furthermore, a class B circuit provides a second boost of an additional factor 6 through M7b. When $Vi+$ increases very fast, due to a non linear transient effect, Hz node decreases. A source follower (Mfb) copies small signal variations in node Hz to the gate of M7b, which is the node Hzf. When the voltage at the Hz node decrease's, the current in M7b increases, speeding up the charge of C_L load capacitor. Therefore, the voltage at nodes $Vi-$ and Hz increases, and the steady state is reached faster.

The biasing circuit that controls Mfb is a non-linear circuit. The bias voltage (V_{biasB}) is such that M7b is off at quiescent state. When $Vi-$ is much lower than $Vi+$, the transistor of the input stage M1, takes the differential pair current. Thus, current increases in both current mirror's of the respective boost mechanisms, M3 and M5b for the Class B, and M3 and M5a for the Class AB one. The increase of current in M5b is subtracted from the M5bc bias current and the gate-source voltage (V_{gs}) of Mfb decreases. Therefore the voltage variation at node Hzf is boosted, i.e. this is a second signal path controlling M7b transistor which ensures that this transistor drives no current in quiescent or small signal operation. The output driver can provide up to 4 mA of peak current with a total amplifier quiescent current Iq of 1 mA.

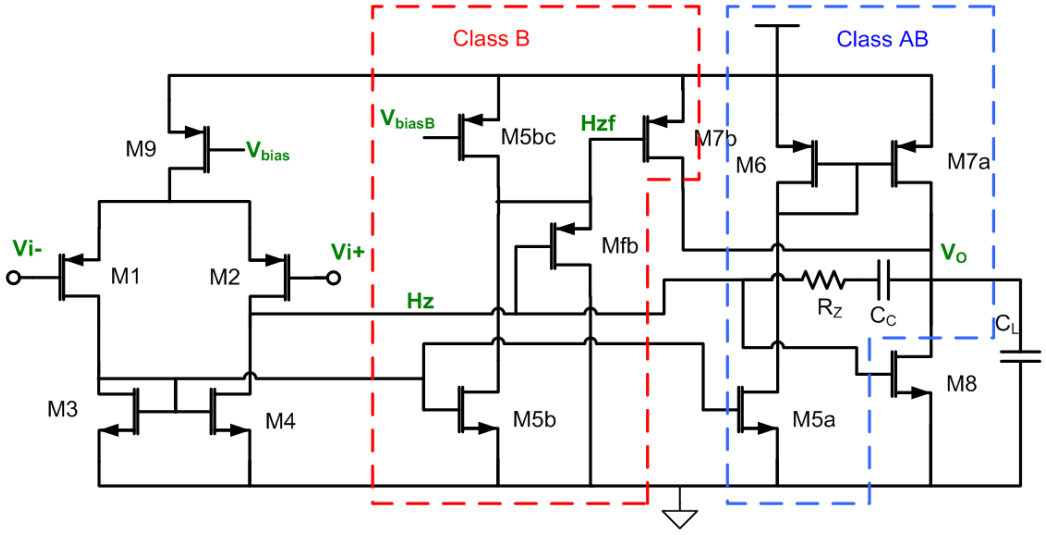


Figure 3.6.: Output buffer scheme.

The GBW product of the OpAmp exceeds 400 MHz, with a Phase Margin (PM) higher than 60 degrees. Thanks to the current boost, the slew rate ranges from 1 to 1.5 V/ns for a 5 pF load, depending on the power consumption of the circuit, which can be adjusted from 1.5 to 3 mW. A shown in figure 3.2, a series resistor at the output (R_d) helps to improve the phase margin, thanks to the compensation of the pole linked to the load capacitance C_L. However, this limits the BW; thus, Rd must be carefully tuned according to C_L. On the final chip, the output buffer must drive a 1.5 pF capacitance. In the prototype tested here, however, the outputs of the amplifier are just connected to output pads for test, and the load capacitance exceeds 5 pF.

3.2 Amplifier for CTA (ACTA) prototypes

An standalone ASIC solution has been designed in order to validate the amplification stage (see figure 3.7). This amplifier would be part of a new ASIC, developed by the NECTAr collaboration, performing the digitization at 1 GS/s with a dynamic range of 16 bits.

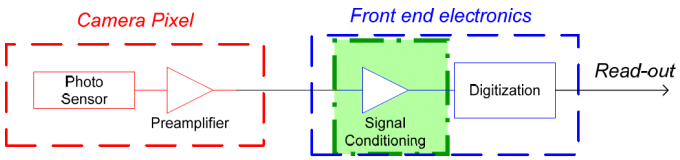


Figure 3.7.: Full path block diagram of the NECTAr camera proposal.

According to the blocs diagram proposed in the figure 3.2 to fulfil the strong requirements of this amplification stage, the design as the input amplifier development for the NECTAr digitizer should be placed as close as possible to the digitizer ASIC, in order to maximize the capacitive input performance of the dedicated digitizer ASIC.

ACTA prototype has been designed in Austriamicrosystems 0.35μm CMOS technology which is the same than the used for the NECTAr digitizer, in order to be integrated in a single chip. The first version, ACTAv1, includes two possible schemes to cover the required DR. One with a double gain configuration circuit and other one, with a Non-linear compressor configuration circuit which. The Non-linear configuration was rejected due to the complexity it adds at the digitizer stage and the accurate calibration procedure requirement in spite of avoids the duplication of the digitizer channel required. The double gain solution is based in the circuit described in section 3.1.1 which is based on a differential cross coupled transistor pair circuit with degeneration. Figure 3.14(a) shows a real photography of the ASIC developed with the different included blocks.

The second version, ACTAv2, includes four different fully differential amplifier configurations (see figure 3.14(b)). This configurations are based on an improvement in the follower PMOS transistors at the bias point configuration. But the main difference consist on use a closed-loop buffer to replace the source followers which obtains better linearity results and gets low power consumption with a class AB amplifier. This closed loop buffer is also used as the input buffer for the digitizer ASIC in collaboration with the Irfu/Saclay team. Figure 3.8 shows the layout designed for the SAM digitizer in the Nectar collaboration [39].

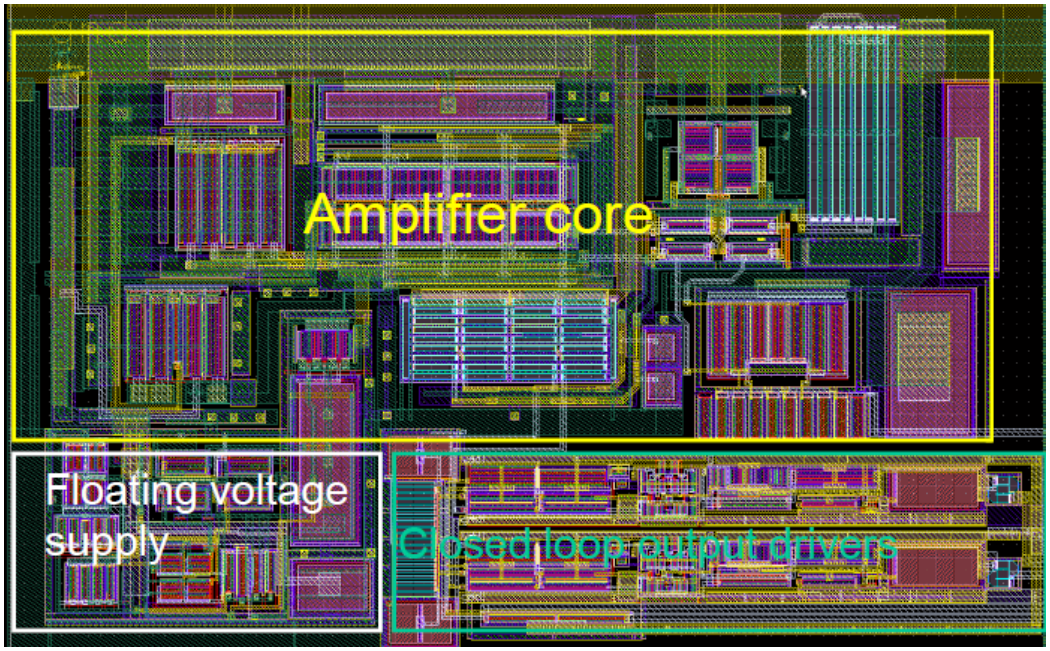
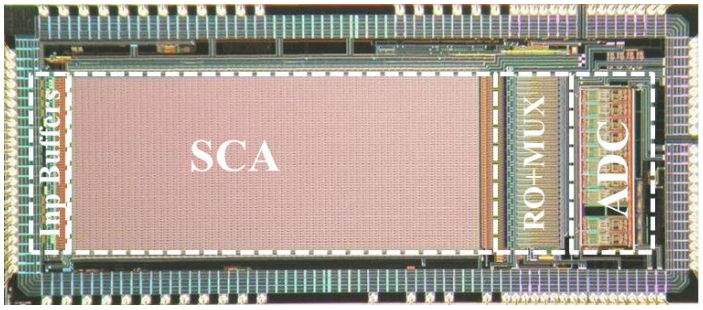
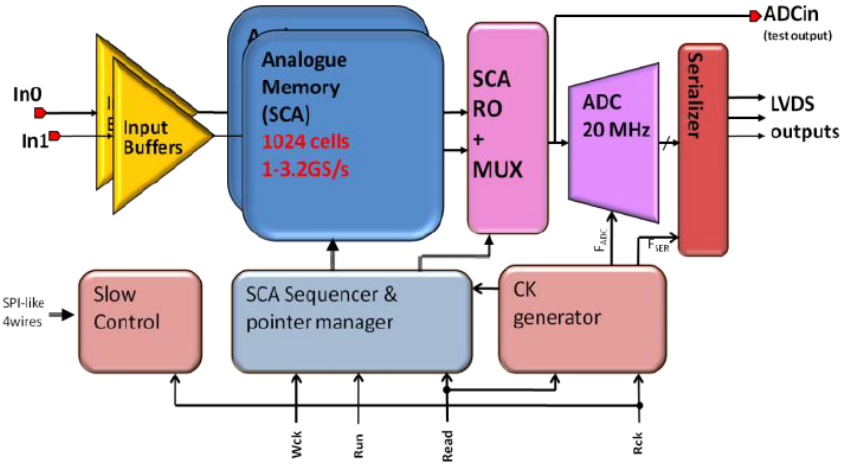


Figure 3.8.: Layout of the clossed-loop buffer for the digitizer ASIC of the NECTAr camera.

NECTAr chip is similar to the SAM, despite its longer memory depth and additional functionalities, while at the same time reducing its power consumption. In particular, the chip's input buffers are using a new high slew-rate power efficient class AB structure. As shown in the block diagram of figure 3.9(b), it includes two analogue memories – one for each input channel – similar to those of the SAM, but with a depth extended to 1024 cells to be compatible with longer trigger latencies (up to about 1μs for 1GHz sampling). Figure 3.9(a) shows the NECTAr0 layout with the the dedicated input buffers.



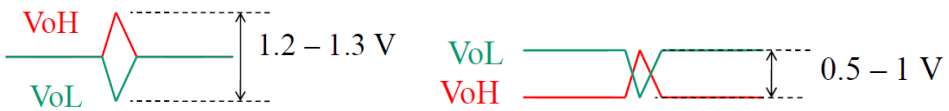
(a) Photo of the NECTAr0 chip showing its subdivisions.



(b) Block diagram of the NECTAr0 chip.

Figure 3.9.: NECTAr0 chip with the dedicated input buffers with a new high slew-rate power efficient class AB structure.

This second ACTA version includes a DC offset output voltage control circuit to accommodate the analogue memory input range. On the other hand, the analogue memory of the digitizer ASIC, requires a no input signal values between a -0.5V to -1V range and so, the requirement for the ACTA amplifier output ($Vo_D = Vo_H - Vo_L$), instead of the typical $Vo_D = 0V$. By introducing an offset at the ACTA inputs, the required offset at the outputs is obtained, and resulting a $> 2V$ at the linearity range output.



(a) $Vo_D = Vo_H - Vo_L = 0V$. (b) $Vo_D = Vo_H - Vo_L = -0.5Vto - 1V$.

Figure 3.10.: Analogue memory DC input voltage levels of the digitizer ASIC.

ACTAv2 also includes a temperature controlled biasing circuitry that obtains a final TC bellow $0.05\%/C$. This bias circuit will be used to compensate the transconductor

temperature dependence in order to stabilize the gain variations due to the temperature variations. This bias current reference with temperature compensation will be used in the next ACTA version (and also in the PACTA pre-amplifier) where the different bias current will be also integrated, in order to minimize the required external circuitry.

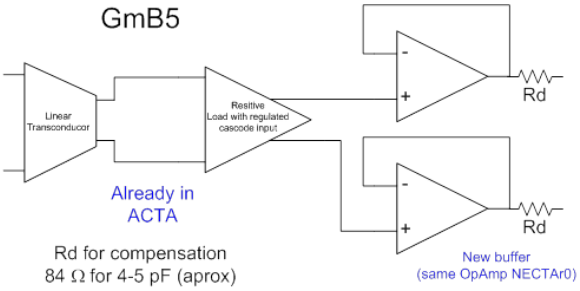
The four fully differential amplifier configurations implemented in this ACTA2 version are:

- B5: Same gain block as in ACTAv1 version. Just for debug proposals (see figure 3.11(a)).
- BO5: Same gain block as in ACTAv1 version (B5), but gain stage is modified to generate the DC offset required by the digitizer ASIC (see figure 3.11(b)).
- BO1: Same gain block as the previous configuration (BO5), but the amplifier is adjusted (by tuning the output series resistor R_{d1}) to drive smaller load capacitances according to the analogue memory input loads (see figure 3.11(c)). It also includes the digitizers input buffer in order to emulate the real capacitance load.
- BOs1: Same gain block as the previous configuration (BO1), but the buffer at the output is replaced by a differential amplifier stage (see figure 3.11(d)). It also includes the digitizers input buffer in order to emulate the real capacitance load.

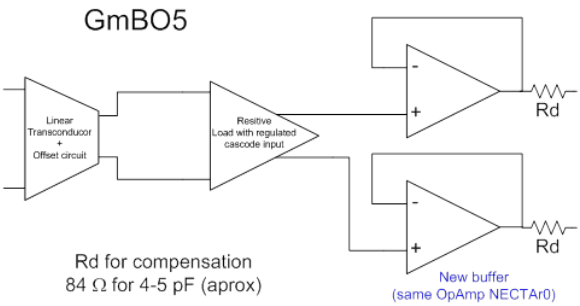
The different bias currents required should be provided externally by using current reference circuitry. The results of this second ACTA version shows that the configuration BO1 presents better frequency responses than the BO5 configuration and BOs1 configuration obtains similar results in the bias offset tuning in spite of the differential buffer modification with a sooner subtraction of the common mode signals, but with an increment of the time response (but still in the expected range). The next step is determine the optimal fully differential configuration for the HG & LH paths for the analogue memories of the digitization at the NECTAr collaboration, and also be able to provide the input signal for the trigger system of the camera.

ACTAf is the third version of the Amplifier for CTA (see figure 3.12). This third version includes three independent fully differential amplification blocs, one of them with a low output impedance stage (the one implemented to provide the input signal for the camera trigger system). All the biasing currents (and voltages), are generated internally in order to minimize the required external circuits. The slow control (SC) is based on a dedicated serial bus interface implemented with a serial peripheral interface (SPI) bus[i] (see figure 3.14(c)). This serial link permits to control and configure the ACTAf chip, including the bias current configuration. For theses purposes, the link can access in write or not destructive read to up to 15 registers (with address codes of 7 bits) of various depth. These registers generates the digital codification for the digital to analogue converters (DACs) that generates the required bias currents.

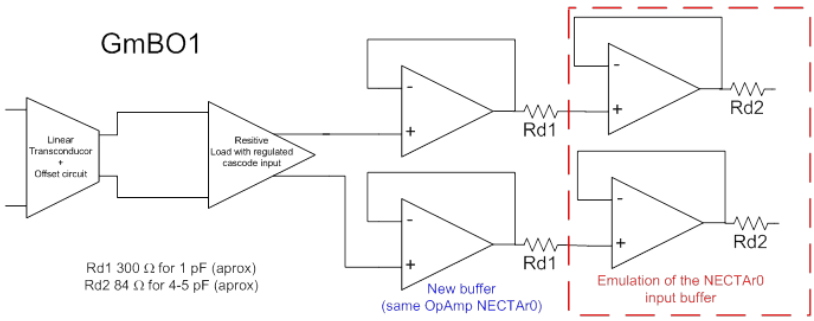
[i]The Serial Peripheral Interface (SPI) bus is a synchronous serial communication interface specification used for short distance communication, primarily in embedded systems. SPI devices communicate in full duplex mode using a master-slave architecture with a single master. The master device originates the frame for reading and writing. Multiple slave devices are supported through selection with individual slave select (SS) lines.



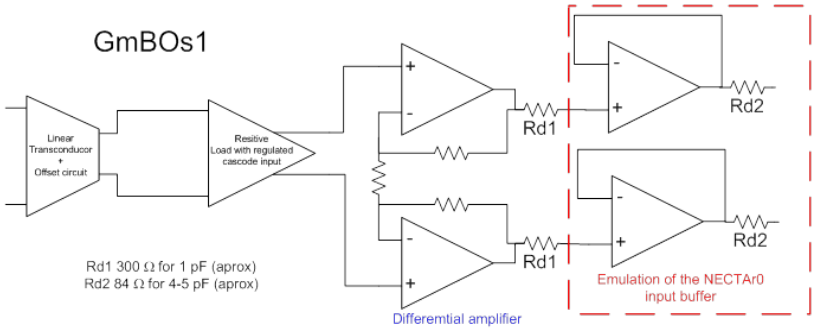
(a) ACTAv2 asic B5 block diagram configuration.



(b) ACTAv2 asic BO5 block diagram configuration.



(c) ACTAv2 asic BO1 block diagram configuration.



(d) ACTAv2 asic BOs1 block diagram configuration.

Figure 3.11.: Block diagram differences of the different ACTA ASIC configuration developed: B5, BO5, BO1 and BOs1.

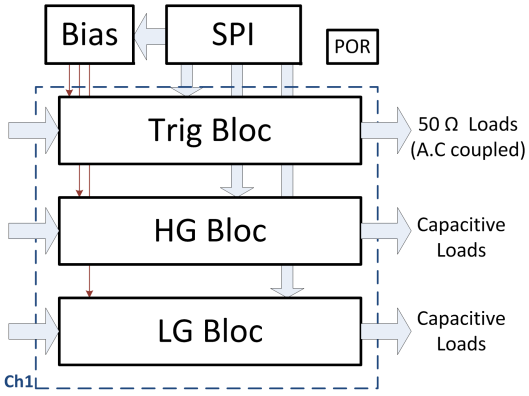


Figure 3.12.: Functional block diagram of the ACTAf 1Ch chip with the three amplification stages and the slow control by using a dedicated SPI interface.

In order to improve the performance to the FE used at the NECTAr collaboration, a Die-Up and Die-Bottom package option has been adopted to implement the digitization system at the both sides of the FE board. This packaging technique allows to implement better routed signal tracks configurations. Due to the limited board width[ii], there is not enough space to place 7 digitizer ASICs in parallel, so, half of them will be located at the opposite side of the board. In order to avoid crossing signals due to have digitizer ASICs at both board sides, a Die-Up and Die-Bottom packaging technique has been adopted, and as a consequence, all the channels implemented in the FE can be routed without crossing its inputs and output signals.

As a consequence, a forth version of the Amplifier for CTA implements two channels gain branches (ACTAf 2Ch), so. each channel includes HG & LG & Trig amplification branches. The SC capabilities are shared between all the amplification branches (see figure 3.13).

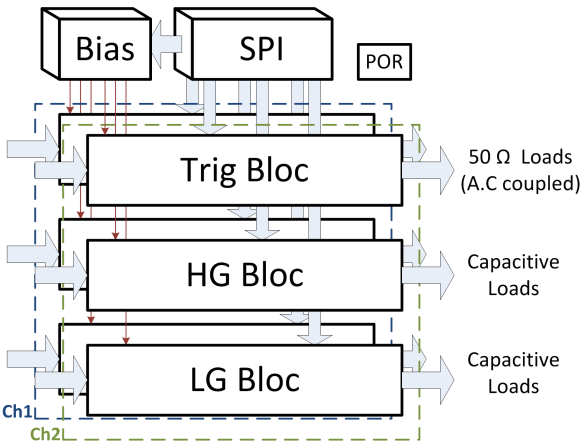
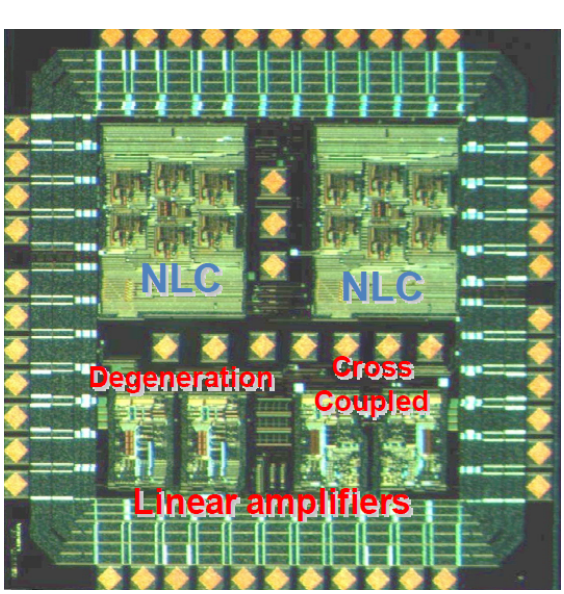
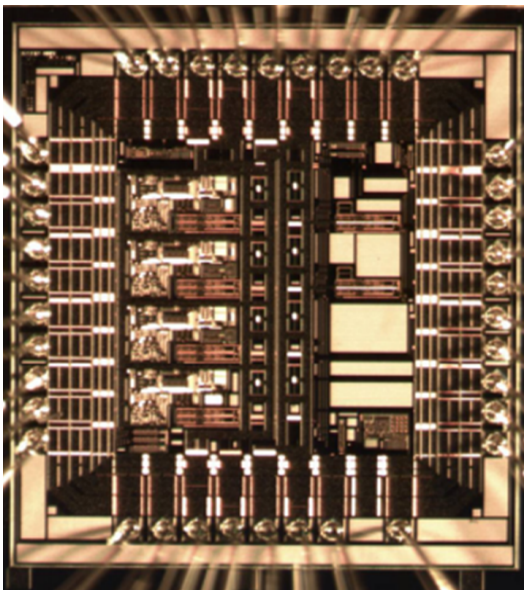


Figure 3.13.: Functional block diagram of the ACTAf 2Ch chip with the three amplification stages at each channel branch and the shared slow control by using a dedicated SPI interface.

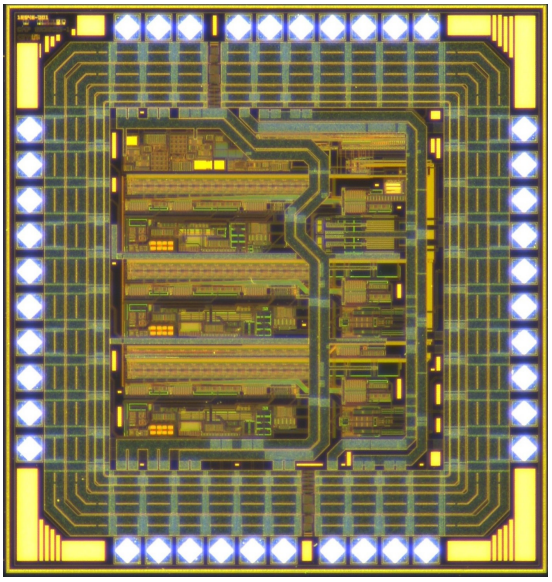
[ii]The FE board width is defined by the cluster size, which corresponds in a 7 pixel units grouped in a cluster, forming an hexagonal with a central pixel, so, the FE board width should be less than three times the diameter of the PMT entrance window



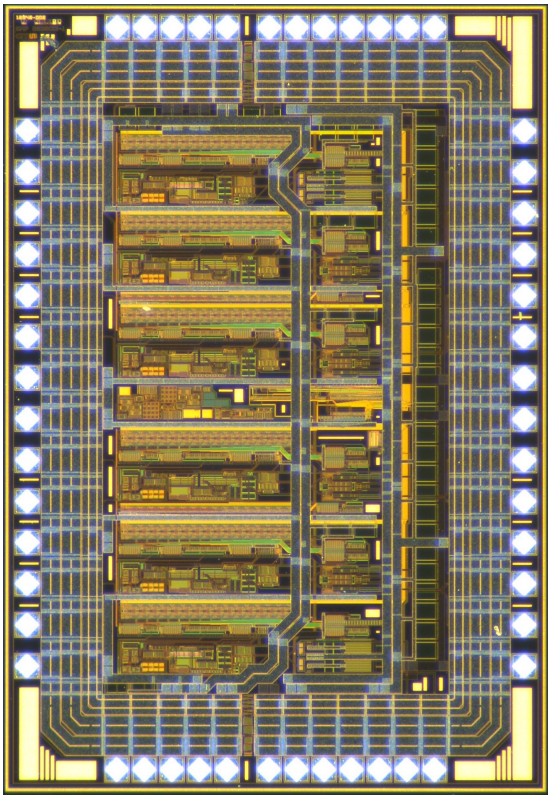
(a) ACTAv1 asic photography.



(b) ACTAv2 asic photography.



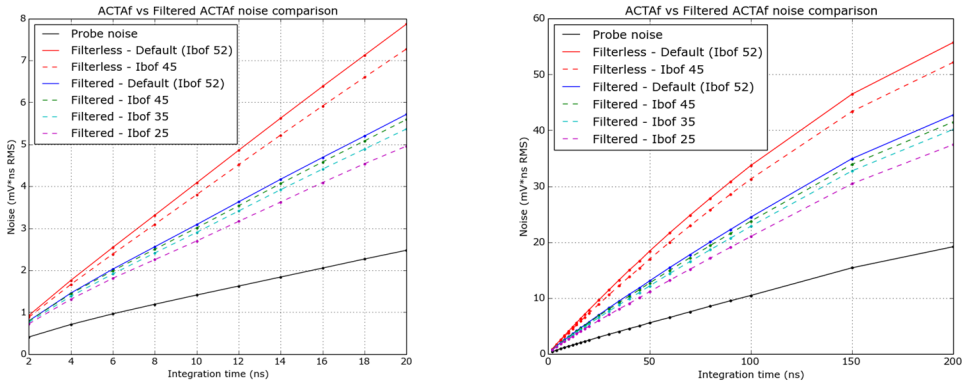
(c) ACTAf 1Ch asic photography.



(d) ACTAf 2Ch asic photography.

Figure 3.14.: Micro photography of the different ACTA ASIC prototypes developed: ACTAv1, ACTAv2, ACTAf 1Ch and ACTAf 2Ch.

Table 3.1 shows a comparative of the different ACTA versions designed and their main characteristics. Notice that the ACTAf version was submitted to the foundry on February of 2013, but due to some problems at the foundry, it was delivered on July 2014. In order to solve these problems during the fabrication process, some metal masks have to be modified and it give us the opportunity to make some improvements in terms of noise at the design, according the results obtained in the ACTAf 1Ch version (see figure 3.15). One of the main noise contributions are related to a voltage biasing source so, we decided to replace the Reset pin functionality that forces a power on reset signal (PoR), already tested and validated at the ACTAf 1Ch version, for an input pin, directly connected to that voltage biasing source, in order to plug a capacitor to decoupling and filter the related noise.



(a) ACTAf Noise comparison.

(b) ACTAf Noise comparison Zoom.

Figure 3.15.: ACTAf Noise comparision with different charge integration time.

First of all, we measure the noise of the measurement system set-up (Probe Noise curve), and then, the ACTAf noise with different biasing configurations for both ACTAf versions. As a result, the Filtered one, shows a 10% of noise reduction in comparison than the filter-less version.

Table 3.1.: ACTA prototype versions comparative.

	ACTAv1	**ACTAv2**	**ACTAf 1Ch**	**ACTAf 2Ch**
Technology	AMS 0.35μm CMOS			
Submission date	July 2009	April 2010	Feb 2013	Feb 2013
Reception date	October 2009	July 2010	July 2014	July 2014
Main building blocks	2 NLC 2 Bi-Gain	4 fully diff. Dig. Input buff.	1 Ch + SPI 1x (HG + LG + Tg)	2 Ch + SPI 2x (HG + LG + Tg)

3.3 Layout details

Most of the techniques described in section 2.3 are also applied to the ACTA amplifier design.

The BiasCurrent block, generates all the global required bias currents for the different parts of the ACTA amplifier (see figure 3.16). This bloc is located at the centre part of the ACTAf 2Ch layout design as it is shown in figure 3.17 in order to equalize the distance from each gain branch. Dedicated SPI registers collect and fix the parameters for the biasing DACs and switch selectors configuration.

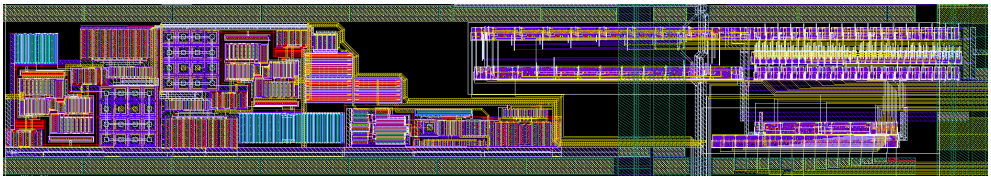


Figure 3.16.: Bias Circuits layout that generates all the required currents.

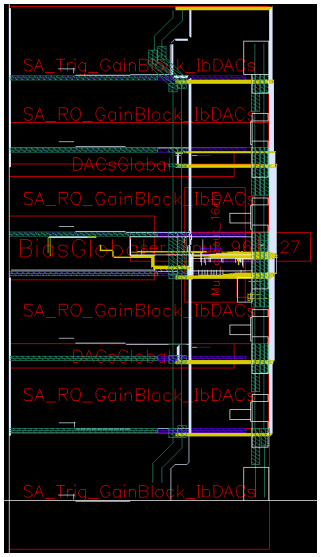
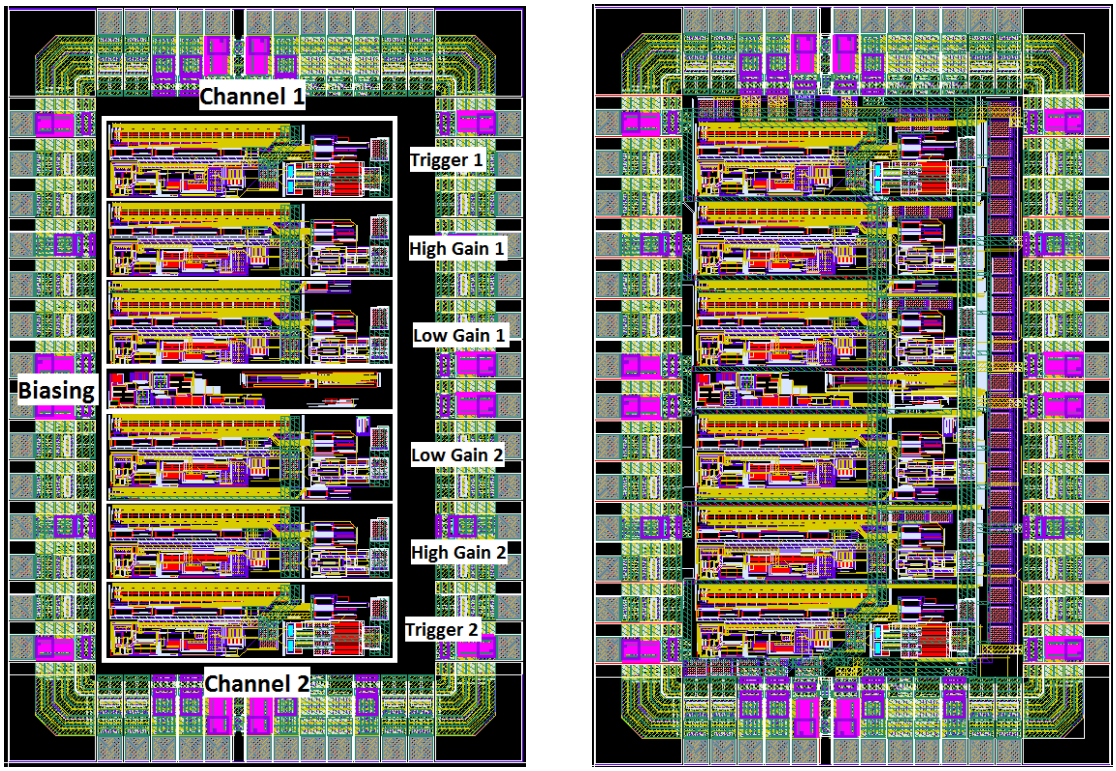


Figure 3.17.: Floor-planning of the gain branches and the biasing circuits for the ACTA amplifier.

According to the layout design techniques described in section 2.3, the ACTA amplifier design follows the floor-planning described in figure 3.18(a), where each half of the design corresponds to each channels so, the three gain branches of one channel are the three blocs located at the top of the design, and the other three gain branches of the second channel, are located at the bottom part of the layout design. The global biasing circuitry is located in the centre of the ASIC design. Figure 3.18(b) corresponds to the complete ASIC layout, and it can be appreciated the decoupling capacitors and the dedicated power rail for the output buffers at the right part.



(a) Floor-planning of the main blocks of the ACTAf 2Ch ASIC design.

(b) Layout design of the ACTAf 2Ch ASIC design.

Figure 3.18.: ACTAf 2Ch Layout design on the left and the floor-planning of the different blocs at the right.

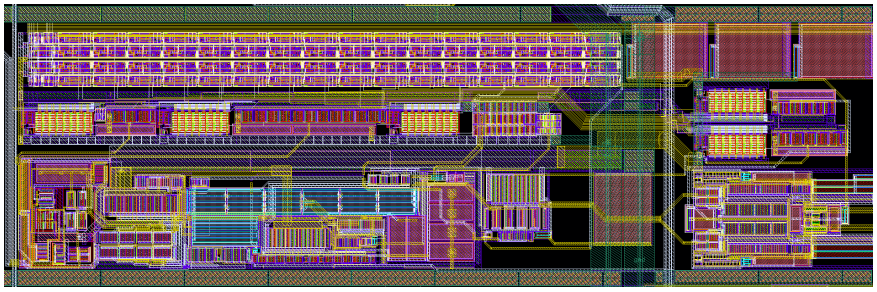
Figure 3.19 shows a detailed view of the floor-planing of the two different amplification stage branches, which are on the one hand, the trigger gain branch able to drive low output impedance loads and on the other hand, the high and low gain amplification branches, able to drive capacitive loads which are based on the same block design.

Below the register blocks located at the top part of each gain branch block, are placed the dedicated DACs to configure the local biasing circuitry (see figure 3.20).

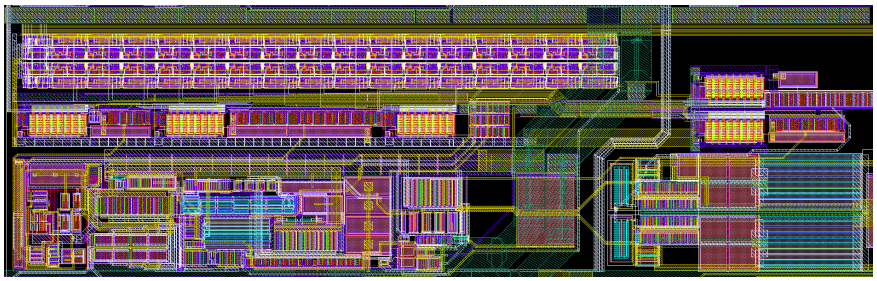
Under the DACs blocks are located the input stages with taking special care at the place and routing of the output series resistor of the differential amplifier (see figure 3.21).

After the input stages are located the output buffers (see figure 3.22) where the HG and LG gain branches are specially designed to drive capacitive loads and the trigger gain branches are specially designed to drive low impedance loads.

So, the pad ring is mainly designed to minimize the path distances specially at the critical part which are the differential input signals. The the channels are separated by ground (or power) pads in order to avoid coupling between the signals (see figure 3.23).



(a) Layout design of the ACTAf 2Ch ASIC design for the HG and LG gain branches.



(b) Layout design of the ACTAf 2Ch ASIC design for the Trigger gain branches.

Figure 3.19.: ACTAf 2Ch Layout design on the two different kind of gain branches.

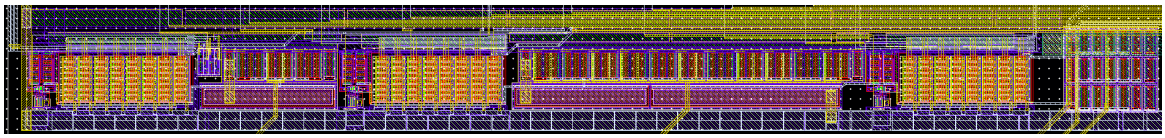
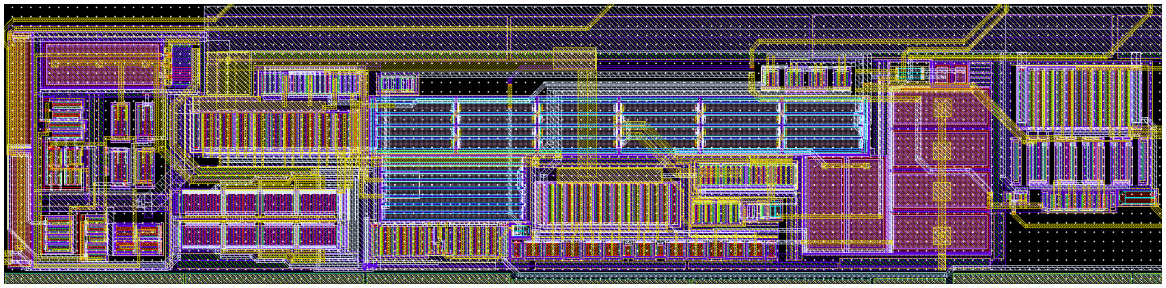
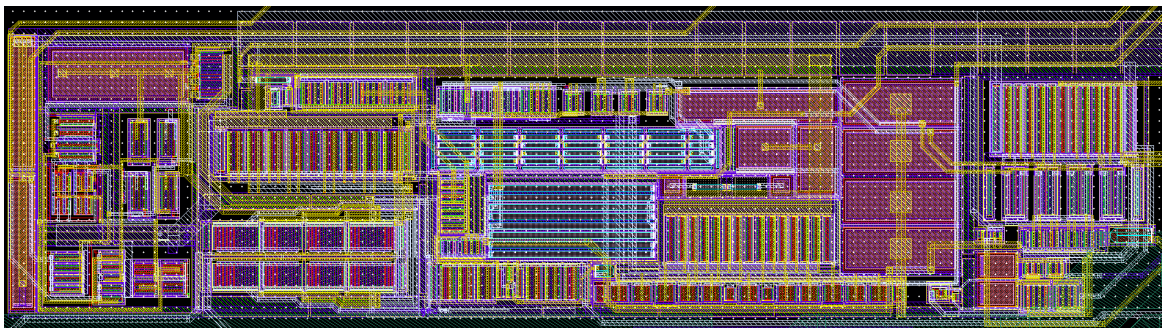


Figure 3.20.: Digital to Analog Converters local biasing blocks of the ACTAf 2Ch ASIC design.

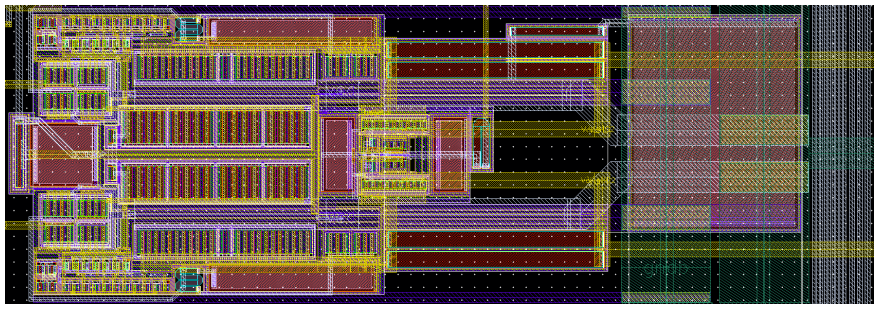


(a) Input stage layout design of the ACTAf 2Ch ASIC design for the HG and LG gain branches.

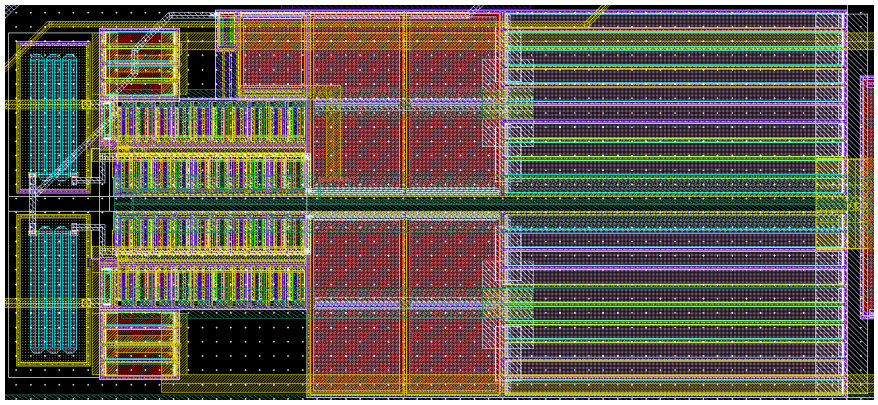


(b) Input stage layout design of the ACTAf 2Ch ASIC design for the Trigger gain branches.

Figure 3.21.: ACTAf 2Ch Layout design on the two different kind of gain branches with a detailed view at the input stage part.



(a) Output buffer layout design of the ACTAf 2Ch ASIC design for the HG and LG gain branches.



(b) Output buffer layout design of the ACTAf 2Ch ASIC design for the Trigger gain branches.

Figure 3.22.: ACTAf 2Ch Output buffer layout design on the two different kind of gain branches.

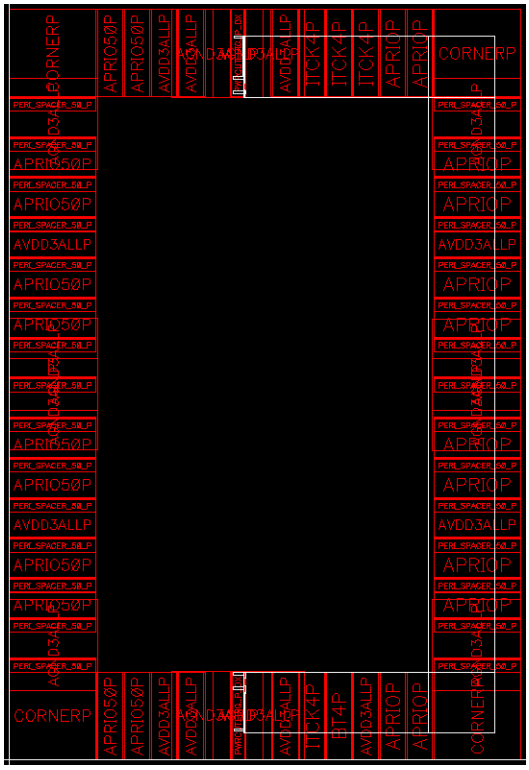


Figure 3.23.: Pad ring floor-planning of the ACTAf 2Ch ASIC design.

3.4 Results ACTA

Subsection 3.4.1 shows the typical application circuit of the amplifier and the information related to the package used. If it is not expressly mentioned, all the measurements in subsection 3.4.2 are related to the last amplifier version which is ACTAf 2Ch and under ambient temperature conditions ($25°C$).

3.4.1 Package & usage

ACTAf has been the version selected to be used as CTA project base line for the NectarCAM MST telescopes, figure 3.24 shows the typical application circuit, with the required A.C. couplings at the inputs and outputs. It is also included the resistor voltage divider, required to achieve the requested DC offset operating point.

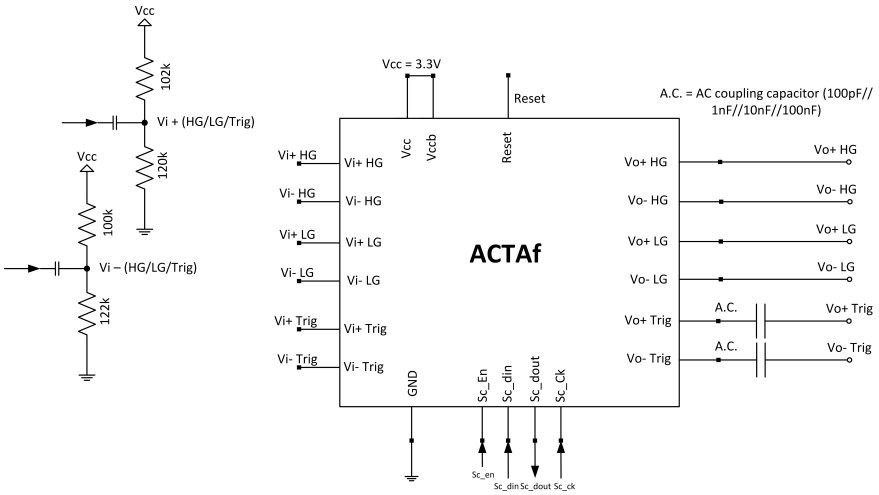
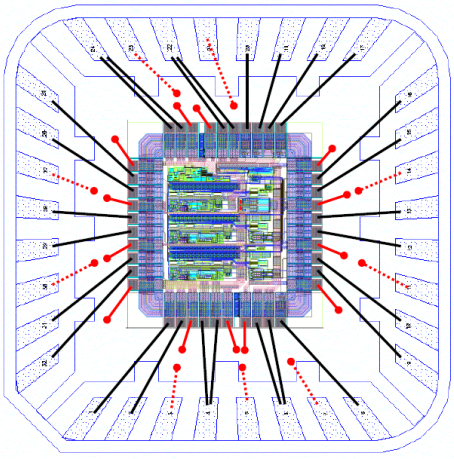


Figure 3.24.: ACTAf Typical application circuit.

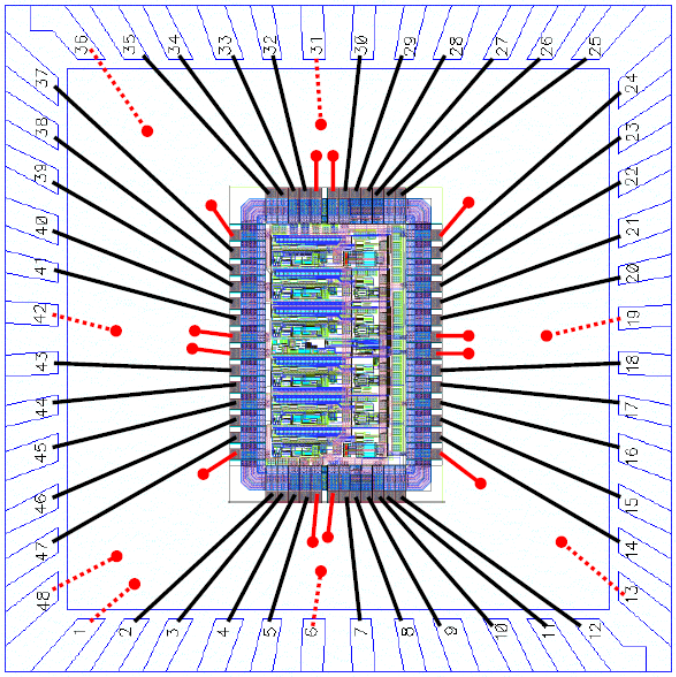
In order to minimize the associated package inductance, ACTA uses a Quad Flat No-leads (QFN) package which has an associated inductance of about $\approx 0.25nH$. QFN package of 32 pins and 5x5 mm size for the 1Ch version, and QFN package of 48 pins and 7x7 mm size [35].

Due to the thermal pad included in the bottom centre part of the QFN packages, it is also possible to minimize the wire bondings length for the ground pins by using down bonds techniques, see figure 2.33 for a QFN cut section detail of the PACTA chapter. Connecting this thermal pad to the ground plane improves the thermal dissipation but also the ground connection of the ASIC.

Figure 3.25 shows a scaled image of the die[iii] with the bonging diagram used for the ACTAf asic with the ground connection at the thermal pad of the two ACTAf chip versions.



(a) ACTAf 1Ch QFN Bonding Diagram detail.



(b) ACTAf 2Ch QFN Bonding Diagram detail.

Figure 3.25.: ACTAf Bonding Diagram with the DIE ground pads connected to the central package pad.

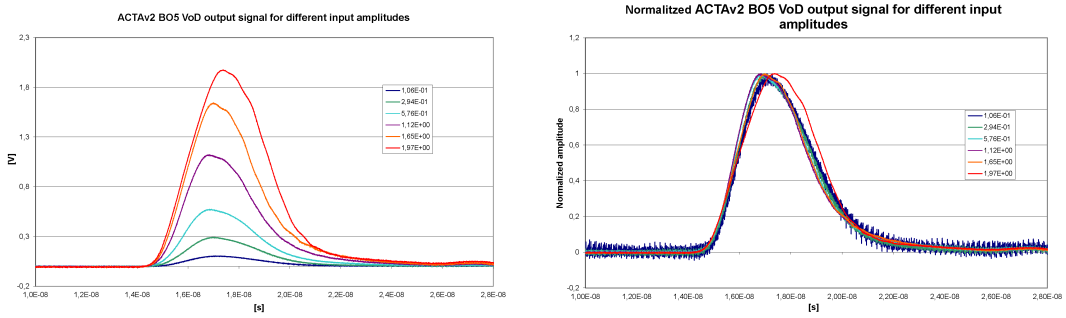
See the ACTAf 2Ch Data Sheet at the Appendix B with more detailed indication for the implementation and usage.

[iii] A die in the context of integrated circuits is a small block of semiconducting material, on which a given functional circuit is fabricated. Typically, integrated circuits are produced in large batches on a single wafer of electronic-grade silicon (EGS) or other semiconductor (such as GaAs) through processes such as photolithography. The wafer is cut ("diced") into many pieces, each containing one copy of the circuit. Each of these pieces is called a die.

3.4.2 Measurement results

In order to achieve fast pulse signals, ACTAf has a recovery time about 1.5 ns for the three gain branches. Figure 3.28 shows the pulse width, amplitude, rise time and fall time by using an input signal in the linear region at the three gain branches.

The normalized response of the amplifier for different pulse amplitudes is shown in figure 3.26. Pulse shape at the output of the amplifier is preserved even for large pulses. The relative integral non-linearity (INL) error on the charge measurement for these pulses is shown in figure 3.27. As discussed in Section 3.1.1, linearity depends on I_{bias}, which indeed dominates the power consumption. Thus, a trade-off between linearity and power consumption exists. Similar results are obtained for linearity measurements of the peak voltage.



(a) BO5 (No Normalized). (b) BO5 (Normalized).

Figure 3.26.: ACTAv2 BO5 Differential output for different input pulse amplitudes with typical focal plane instrumentation signals (top). Normalized shape is shown at the bottom.

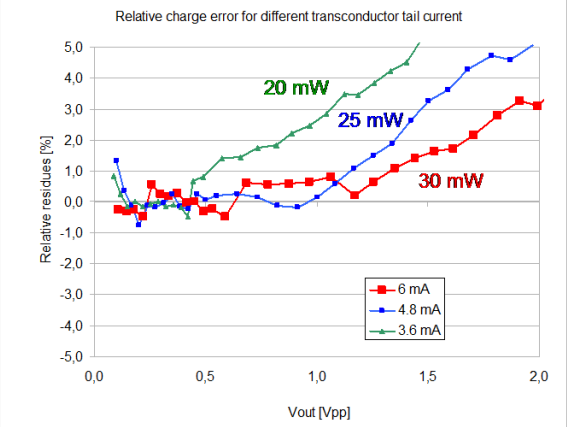
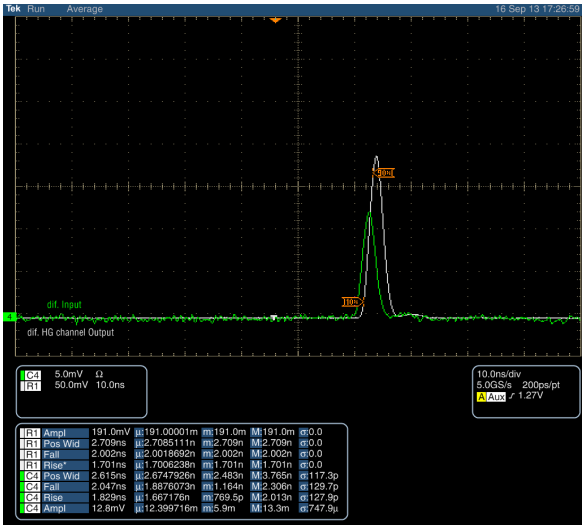
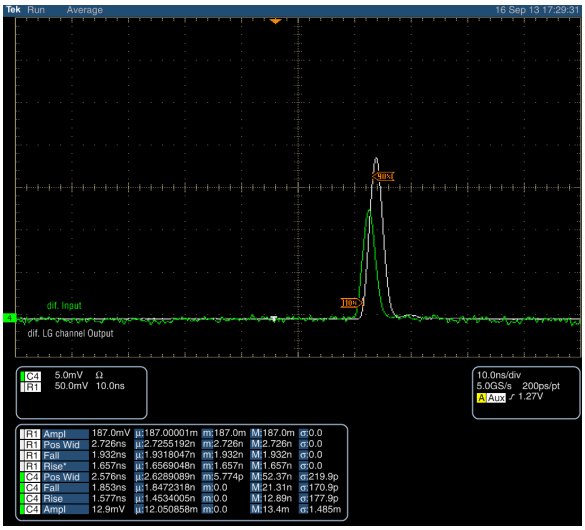


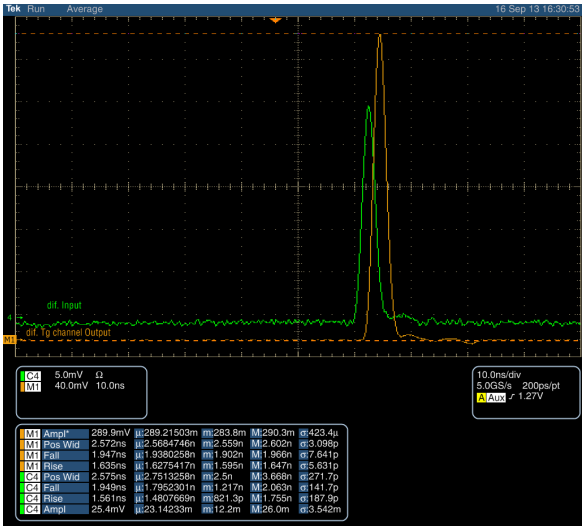
Figure 3.27.: Relative linearity (INL) error for different values of the transconductor tail current Ibias.



(a) ACTAf shape measurements at the HG gain branch.



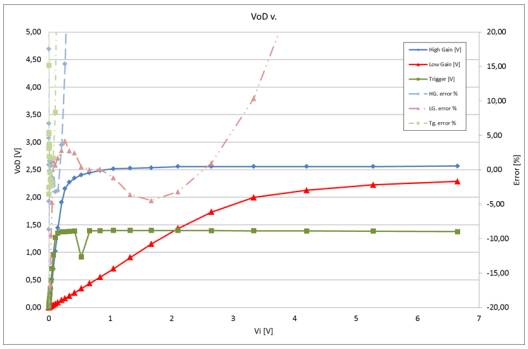
(b) ACTAf shape measurements at the LG gain branch.



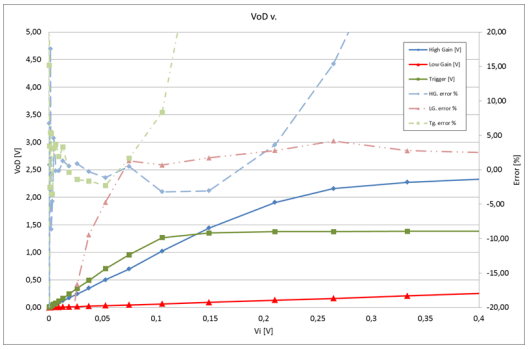
(c) ACTAf shape measurements at the Tg gain branch.

Figure 3.28.: ACTAf shape measurements with an input pulse in the linear region at the different gain branches.

The precise linearity error measurements of figure 3.29 confirm that the ACTA dynamic range is higher enough to cover all the required input signals coming form the focal plane instrumentation. Linearity error is given by the integral of the pulse, since the charge is the relevant information to compute the amount of light or energy deposited in the sensor. The obtained linearity error is less than 5% for the three gain branches.



(a) HG, LG and Tg linearity error of the different ACTAf gain branches



(b) Amplified view of the HG and Tg linearity error range.

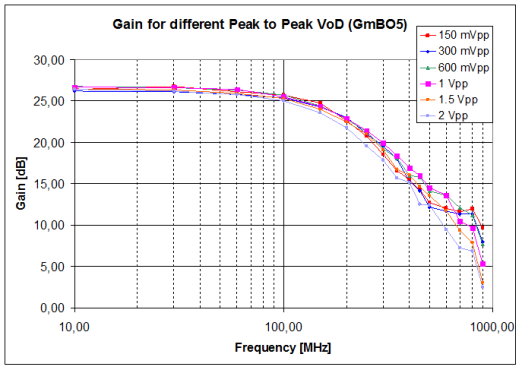
Figure 3.29.: ACTAf measurement results of the integral for the HG, LG and Tg differential outputs as function of input peak current for typical SPE pulse shape and the linearity error. Detailed view of the HG and Tg linear range.

The frequency response of the amplifier for different signal levels is shown in figure 3.30(a). The response does not show non-linearity for output below 2 Vpp. For test purposes, R_d was sized to achieve a minimal BW of 300 MHz, for a load capacitance of 5 pF, however the measured 3 dB cut-off frequency of the circuit is about 200 MHz. This is due either to an underestimation of C_L or to process variations effects on R_d, which is also sensitive to parasitic resistance because of its low value. This is not related to a limitation of the amplifier itself, as shown in figure 3.30(b), the BW is even slightly larger when an additional identical output buffer is added. This means that the measured cut-off frequency is given by the time constant $R_d \times C_L$ and that the intrinsic BW of the amplifier is much higher than 200 MHz, thus consistent with the 400 MHz expected from simulation.

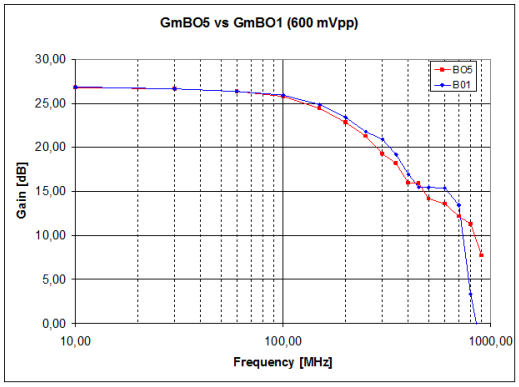
Bandwidth measurements of the ACTAf version could not be performed by using a network analyser due to the expensiveness of a four channel instrumentation option. Instead of that, two different sets of measures have been performed in order to estimate the bandwidth of the full chain and its different stages:

- Step function method
- Sine waves method

Step function method is based on the measurement of the rise time of an electrical signal looking like a step function as it is propagated through the amplification chain. With this method, one estimates the bandwidth of a system by injecting a sharp edge signal into the system and measuring the rise time of the (slightly deformed) signal at the output of the



(a) Frequency response of the amplifier for different output levels.



(b) Frequency response of the different amplifier configurations.

Figure 3.30.: Frequency response of the amplifier for different output levels with different amplifier configurations.

system. This method is only valid for a 1st order system, therefore it can't be applied to PACTA, only to ACTA. The bandwidth (BW) is calculated as the following:

$$Bandwidth[MHz] = \frac{0.35 \times 1000}{\sqrt{RiseTime_{out}^2 - RiseTime_{in}^2}} \tag{3.1}$$

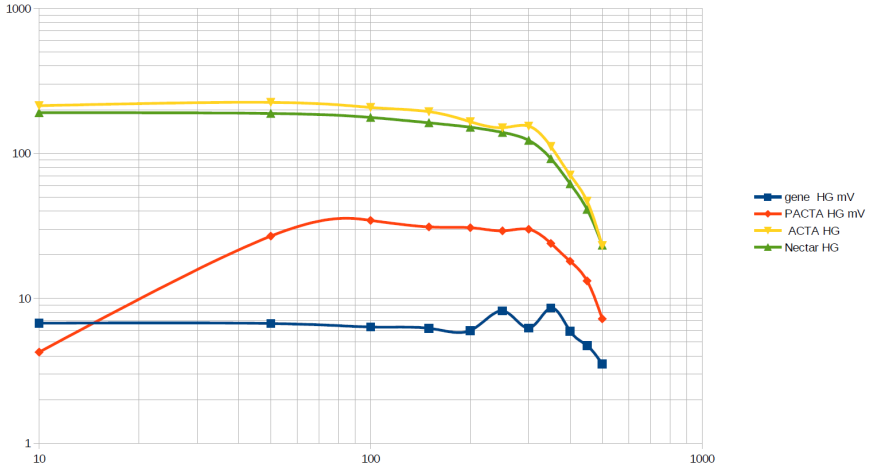
The bandwidth of the ACTA, as it is on the FE board, is similar but not exactly equivalent to the one measured on ACTA test bench. Several parameters of the ACTA allow for optimizing its bandwidth, ranging from 280 MHz in the worse case up to 820 MHz at best. Since those parameters also influence some other performances, one needs to perform a cross parameters study to choose them optimally.

Table 3.2.: Step function method to calculate the full channel bandwidth with the ACTAf amplifier.

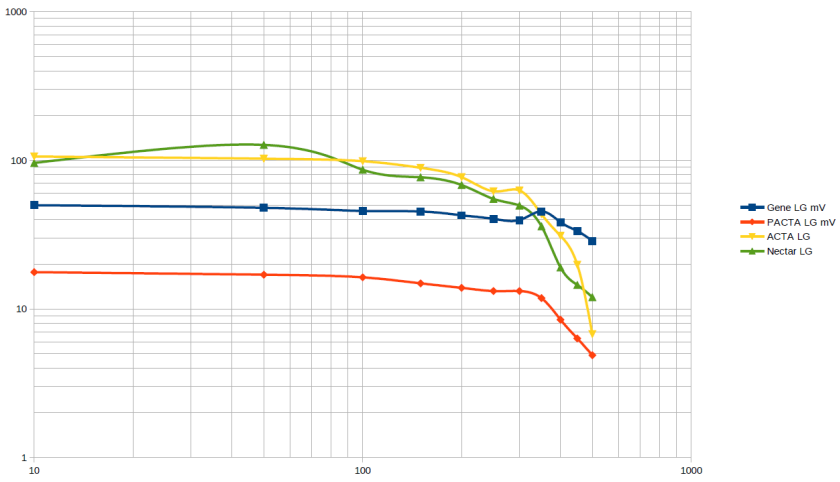
Rise time [ns]	ACTA LG in (20 dB)	ACTA HG in (40 dB)	ACTA LG out (20 dB)	ACTA HG out (40 dB)	BW [MHz] high amp	BW [MHz] low amp
default ACTA sett.	1.25	1.03	1.58	1.62	362.174	279.910
best BW ACTA sett.	1.26	1.03	1.33	1.37	821.995	387.457

Sine waves method measures the amplitude of a sine wave of various frequencies as it is propagated through the amplification chain. Figure 3.31 shows the amplitude in mV of the injected sine wave as a function of its frequency, for high gain (figure 3.31(a)) and low gain (figure 3.31(b)). The bandwidth can be estimated from these plots by calculating the frequency for which the amplitude decreases of a given factor (usually the bandwidth at -3 dB). The blues curves shows that the generator itself has an non-flat response and therefore an effective bandwidth lower than the one expected for the FE board (and than expected

from the manufacturer specifications). The overall trend of the curves looks as expected, with a flat start and a cut off in the 300-500MHz region, however some data points seem to be the result of corrupted data. This doesn't allow for a reliable computation of the bandwidth. The curves show a cut off around the expected frequency (>300MHz). However, these measures did not allow for a precise measure of the bandwidth as too many uncertainties have been acknowledged regarding those measures. A better sine wave generator and a repetition of the set of measures are required to provide a reliable measure of the bandwidth.



(a) The bandwidth of the ACTA HG channel.



(b) The bandwidth of the ACTA LG channel.

Figure 3.31.: Amplitude in mV of the injected sine wave as a function of its frequency, for high gain (top) and low gain (bottom).

The standard deviation of the noise voltage at the output is about 1 mV rms, with a slight dependence on the gain of the circuit, thus on I_{bias} and I_{cf}. It corresponds to an e_n of about $3nV/\sqrt{Hz}$, which allows to perform single photo electron calibration with a PMT gain of 2×10^5 which is not the nominal gain, it is 5 times larger, but it was required to measure the SPE without the pre-amplification stage (see figure 3.32).

Table 3.3 summarizes the key performances parameters of the circuit.

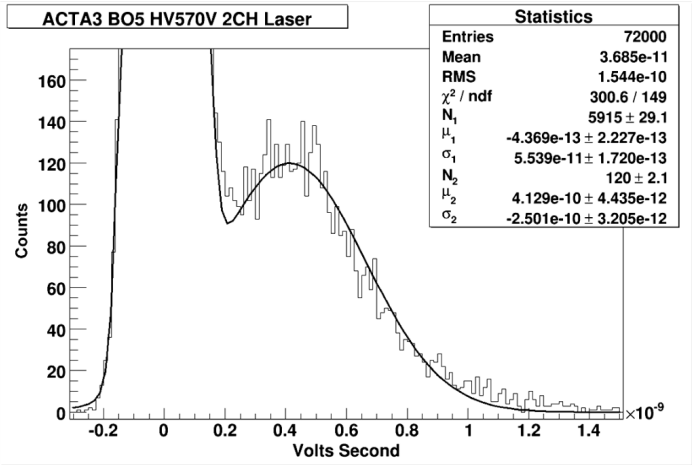


Figure 3.32.: Single photoelectron spectra at the nominal PMT gain (integration time is 10 ns).

A typical 1 s.p.e. spectrum is shown in figure 3.33 with the full channel electronics included (PMT + PACTA + ACTA + Nectar digitizer). A function including the expected distribution of events (Gaussian distribution with a Poisson law normalization) at 0, 1, 2 and up to 9 s.p.e. is fitted on the charge distribution.

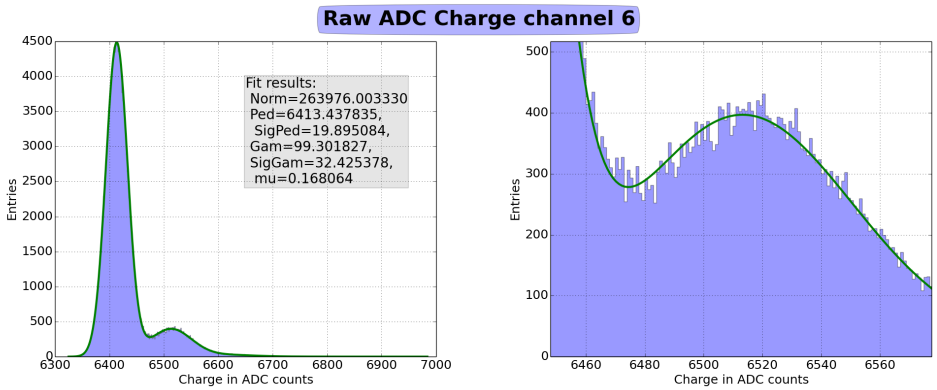


Figure 3.33.: Typical s.p.e. spectrum fitted with a function including 0 to 9 s.p.e contributions..

The typical s.p.e. spectrum can be obtained on this test bench. Using a PMT of a known gain, the position of peak of the 1 s.p.e. relative to the position of the 0 s.p.e. (pedestal) is a measure of the gain of the full readout chain on the high gain channel. Several measures will then use this conversion factor :

$$Q_{1s.p.e.} = G \times Q_{ADCcounts} \tag{3.2}$$

The different bias current sources are generated by temperature compensated current references and configurated by DACs in order to select the desired value. Each of them are managed as follows:

Table 3.3.: Main measured performances of the amplifier.

Parameter	Value	Units	Coments
Gain	5 to 20	V/V	Tuneable (through I_{cf} and I_{bias})
BW	500	MHz	$C_L = 3 - 4$ pF. Extrapolated from Bo1
Slew Rate	1 to 1.5	V/ns	For $3 - 4$ pFload (tuneable OpAmp bias)
Linearity (VoD<1 Vpp	< 1	%	Depends in I_{cf} and I_{bias}
Linearity (VoD<2 Vpp	< 3	%	Depends in I_{cf} and I_{bias}
Input ref. noise (e_n)	< 3	$nV/\sqrt{Hz}$	For gain > 5
DC offset (output)	0 to 1.5	V	Tuneable by control current (I_{bof})
Gain Temp. Coef. (TC)	0.06	% C	After temp. compensation via TC of I_{cf}
Power consumption	20-30	mW	

- I_{bgm} is a global bias current source for all the three gain branches at each channel. It is configured with a 6 bits DAC from a temperature compensated current reference.
- I_s is a global bias current source for all the three gain branches at each channel. It is configured with a 6 bits DAC from a temperature compensated current reference. Only the 3 most significant bits (MSB) are set, the 3 least significant bits (LSB) are hard-wired to 101 so, Is can be configured in steps of 5 DAC counts. Is controls the V_{bias} of $Float_V$, but V_{bias} is the difference between $I_{cf} - I_s$. I_{cf}, is already controlled, don't need to control I_s. It is better to have it locally in each gain branch and have a current link due to get better HF noise performances.
- I_{cf} is a local bias current source for each three gain branches at each channel. It is configured with a 6 bits DAC from a temperature compensated current reference.
- I_{bof} is a local bias current source for each three gain branches at each channel. It is configured with a 6 bits DAC from a temperature compensated current reference. The maximum current for the trigger gain branches is limited by smaller resistor width to achieve better BW that it can be controlled setting an smaller R_f in the transconductor by setting one local control bit by slow control. The linearity is still in the acceptance range and is not limited by VoDGm. The range should be selected by an additional control bit "OFC" of the scaling mirror after the DAC. These range selection is not applicable for the trigger gain branch because the width of resistor is smaller in order to achieve good BW performances.
- I_{bSF} is a local bias current source for each three gain branches at each channel. It is configured with a 6 bits DAC from a temperature compensated current reference.
- $I_{b_{AOP}}$ is a global bias current source for the HG and LG gain branches at each channel. It is configured with a 6 bits DAC from a temperature compensated current reference.
- $I_{b_{ABF}}$ is a global bias current source for the trigger gain branches at each channel. It is configured with a 6 bits DAC from a temperature compensated current reference.

Some parameters managed by different control bits for each gain branch at each channel configures the operating point of the amplifier. Each of them are managed as follows:

- PD is a power down bit, that disables the associated gain branch.
- BC is a bias control of the transconductor that increases the bias current in cases of large external input offset settings requirements.
- LC is a control bit that limits the resistor width to achieve better BW by setting an smaller R_f in the transconductor.
- OFC sets the full scale of the I_{bof} DAC.
- LRd sets lower damping resistor at the HG and LG gain branches buffer output. It is used for large load capacitances (if BW is too small).
- LB limits the BW at the output of gain block of the trigger gain branch. It is used in case of get BW too large, to prevent linearity problems.

I_{bgm} corresponds to the biasing configuration current of the transconductance differential pair stage. It is a global biasing current for the three gain branches at each channel level of the chip. The output voltages in common mode and differential mode variations as a function of the I_{bgm} bias current source (see figure 3.34) are about $\pm 2\%$.

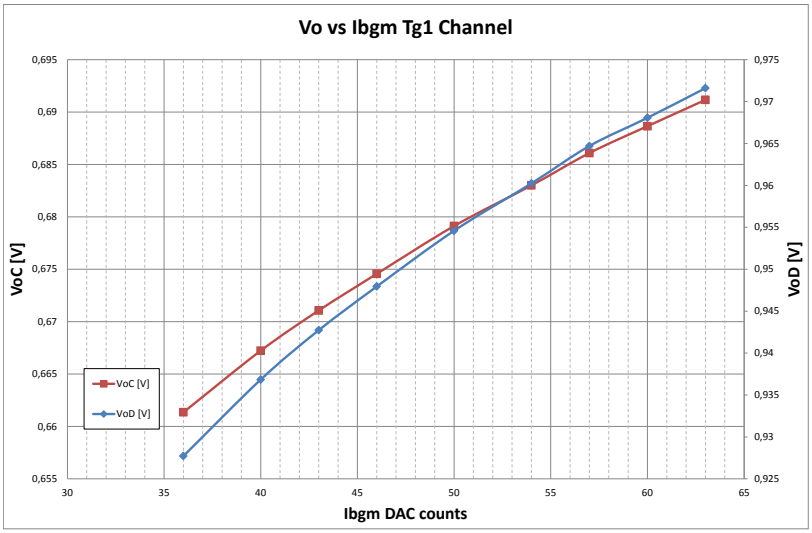


Figure 3.34.: ACTAf 2Ch output voltages in common mode and differential mode variations as a function of the I_{bgm} bias current source.

The gain variations measured at the differential voltage output and integrated charge variations as a function of the I_{bgm} bias current source (see figure 3.35), allows a fine tuning of the gain at a channel level.

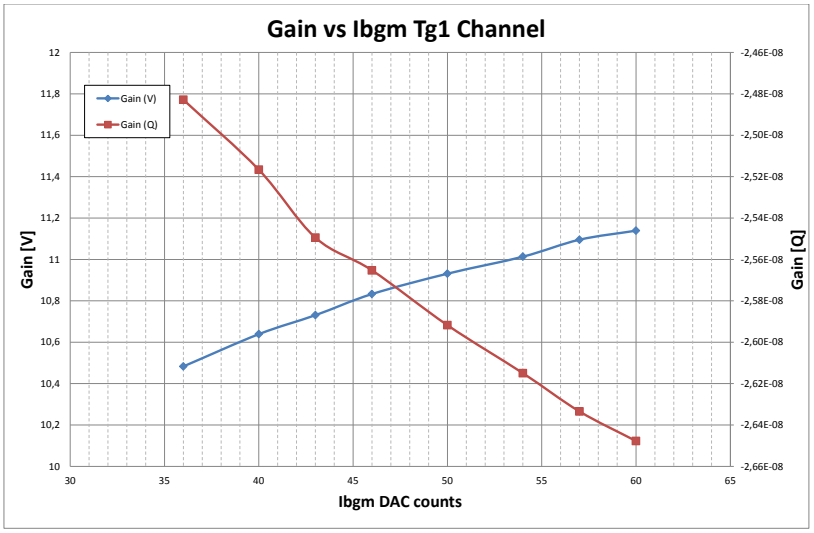


Figure 3.35.: ACTAf 2Ch gain variations measured at the differential voltage output and integrated charge variations as a function of the I_{bgm} bias current source.

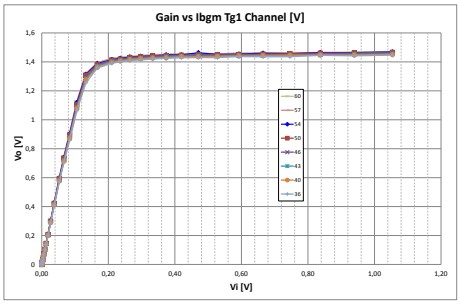
The differential output voltage as a function of the differential input voltage of different I_{bgm} bias current source values do not affect at the linearity range. Figure 3.36 shows the linearity range and the related error of the differential output voltage (and the charge). The different I_{bgm} values shows a small effect in the linearity range up to 1.1V of the differential output voltage according to the analogue memories input range (see figure 3.10) with errors below 5%.

I_{bSF} corresponds to the biasing configuration current of the source follower stage. It is a local biasing current for each of the three gain branches at each channel of the chip. The output voltages in common mode and differential mode variations as a function of the I_{bSF} bias current source (see figure 3.37) shows a variation of the common mode voltage about $\pm 3.5\%$ whereas the differential mode do not change significantly.

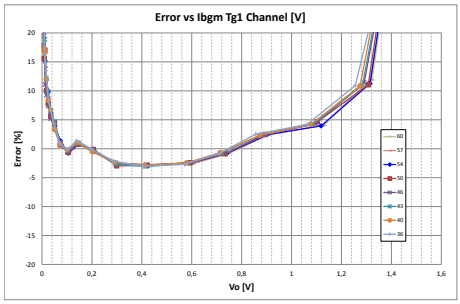
The gain variations measured at the differential voltage output and integrated charge variations as a function of the I_{bSF} bias current source (see figure 3.38), do not affect at the gain branch.

The differential output voltage as a function of the differential input voltage of different I_{bSF} bias current source values do not affect at the linearity range. Figure 3.39 shows the linearity range and the related error of the differential output voltage (and the charge). The different I_{bSF} values shows a small effect in the linearity range up to 1.1V of the differential output voltage according to the analogue memories input range (see figure 3.10) with errors below 5%.

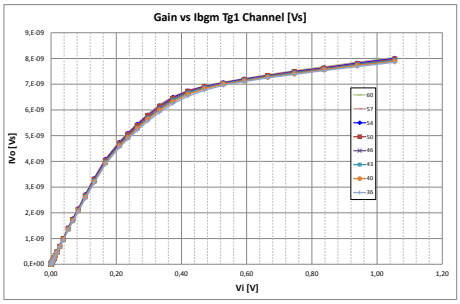
I_{bof} is configured to adjust the DC voltage level at the output of each gain branches. HG and LG branches are more or less at the same DC level requirement because both are



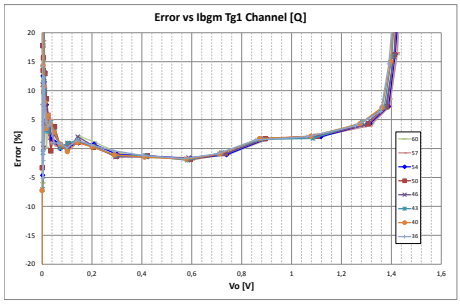
(a) Linearity range of the differential output voltage of the ACTAf 2 Ch.



(b) Related error of the differential output voltage of the ACTAf 2 Ch.



(c) Linearity range of the output charge of the ACTAf 2 Ch.



(d) Related error of the output charge of the ACTAf 2 Ch.

Figure 3.36.: Linearity range and the relative error, for differential output voltage (top) and charge (bottom) as a influence of the I_{bgm} bias current source.

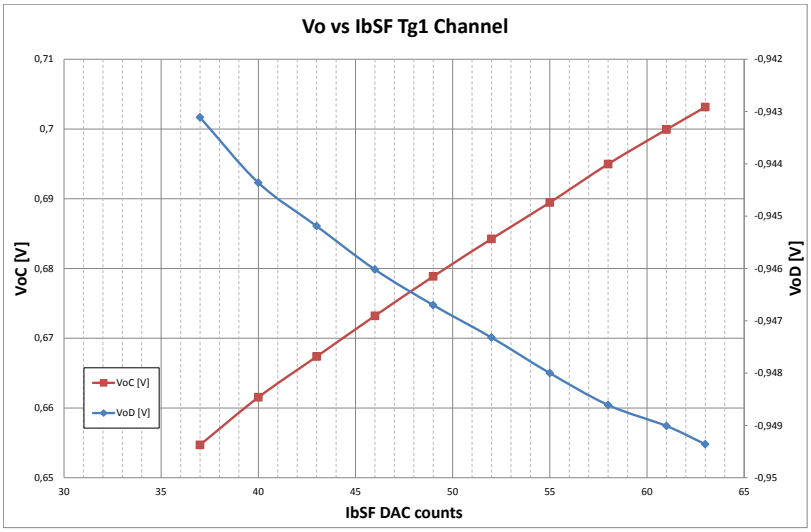


Figure 3.37.: ACTAf 2Ch output voltages in common mode and differential mode variations as a function of the I_{bSF} bias current source.

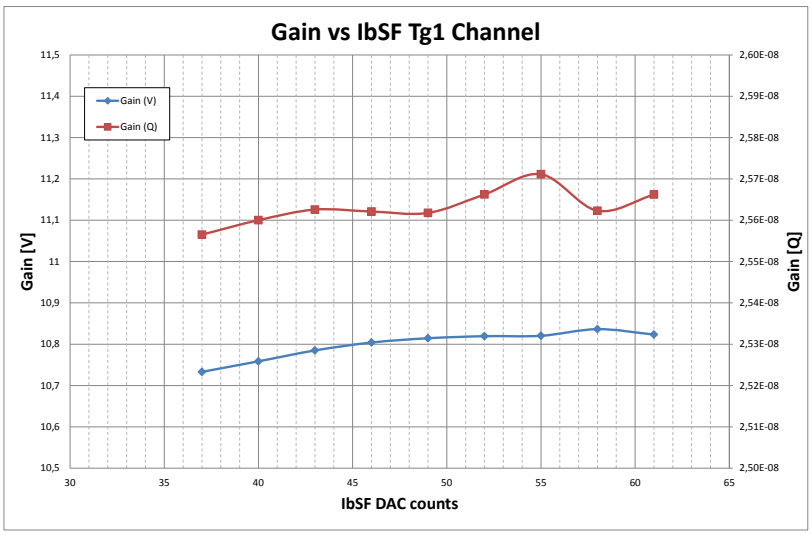
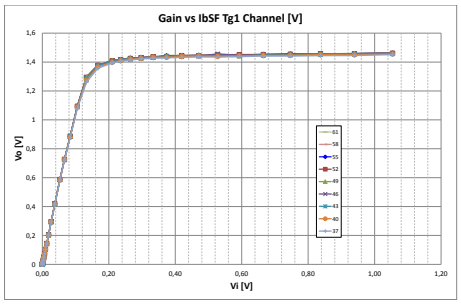
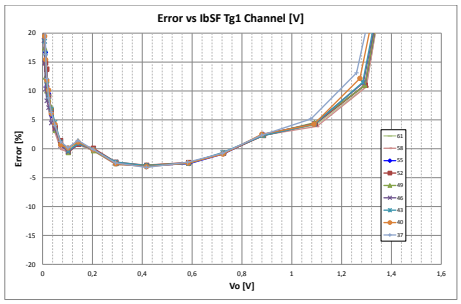


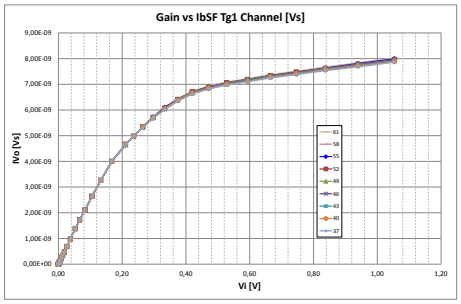
Figure 3.38.: ACTAf 2Ch gain variations measured at the differential voltage output and integrated charge variations as a function of the I_{bSF} bias current source.



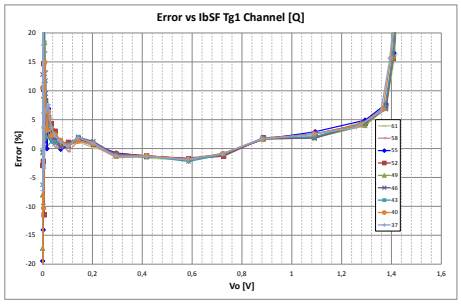
(a) Linearity range of the differential output voltage of the ACTAf 2 Ch.



(b) Related error of the differential output voltage of the ACTAf 2 Ch.



(c) Linearity range of the output charge of the ACTAf 2 Ch.



(d) Related error of the output charge of the ACTAf 2 Ch.

Figure 3.39.: Linearity range and the relative error, for differential output voltage (top) and charge (bottom) as a influence of the I_{bSF} bias current source.

connected to the analogue memories of the digitizer system, but the trigger branch has to be configured to match with the input DC level of the trigger system which is from 0 to 1.5V.

The output voltages in common mode and differential mode variations as a function of the I_{bof} bias current source (see figure 3.40) shows a variation of the common mode voltage about ±9% to ±15% whereas the differential mode variations about ±12% to ±27%. The DC offset level for the trigger channels can be adjusted from 0.6V to 0.8V, whereas the HG and LG channels can go from 1.3V to 1.7V. The differential output is directly related to the output voltage swing of the amplifier, but due to the offset introduced at the amplifier inputs, the differential output is about 1V (see figure 3.10) increasing the linearity range. So, as the "positive" output DC voltage is less than the "negative" one, the differential mode will obtain negative values varying from -0.7V to -1.2V for the HG and LG gain branches and from -0.8V to -1.1V for the trigger gain branch.

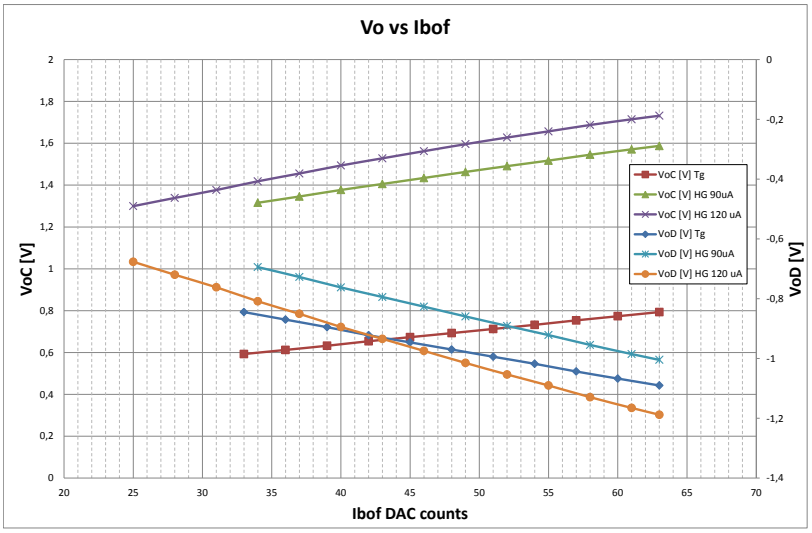


Figure 3.40.: ACTAf 2Ch output voltages in common mode and differential mode variations as a function of the I_{bof} bias current source.

The gain variations measured at the differential voltage output and integrated charge variations as a function of the I_{bof} bias current source (see figure 3.41), do not affect at the gain branch significantly (about ±2%).

The differential output voltage as a function of the differential input voltage of different I_{bof} bias current source values changes the saturation point of the differential output voltage. Figure 3.42 shows the linearity range (left plots) and the related linearity error (right plots) of the differential output voltage (and the charge at the bottom) for the trigger gain branches as an example. The different I_{bof} values shows variations of the linearity range from 1.2V to 1.4V for the Trigger gain channels and from 1.6V to 2V for the HG and LG gain branches below 5% of the relative linearity error.

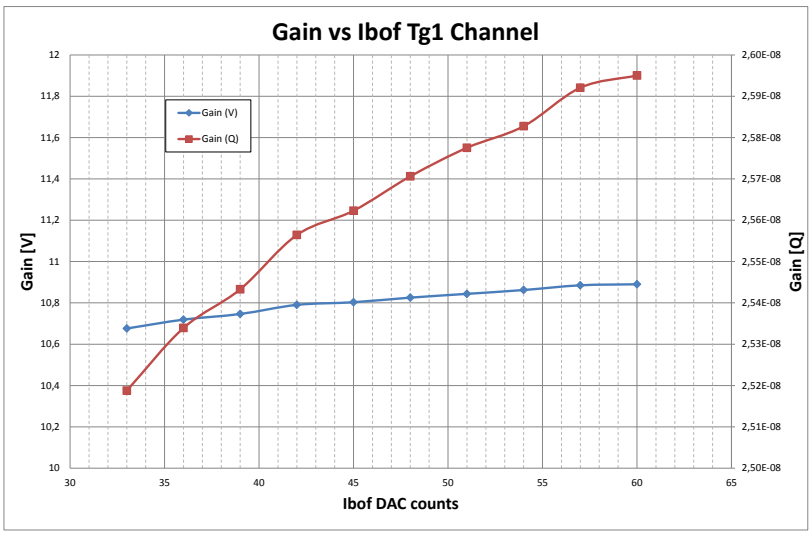
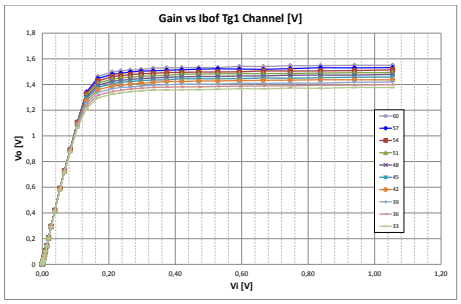
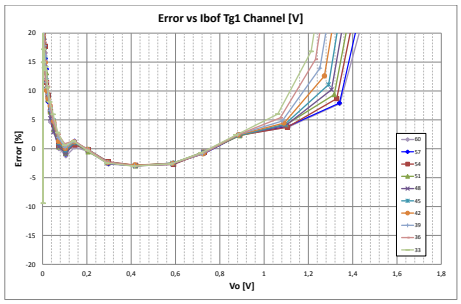


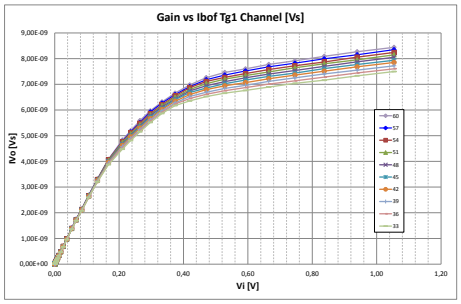
Figure 3.41.: ACTAf 2Ch gain variations measured at the differential voltage output and integrated charge variations as a function of the I_{bof} bias current source.



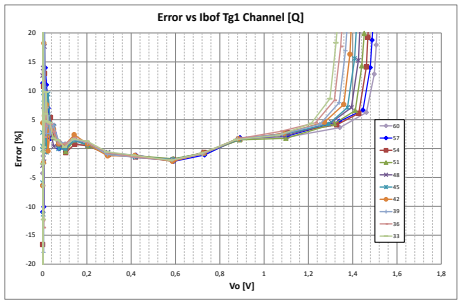
(a) Linearity range of the differential output voltage of the ACTAf 2 Ch.



(b) Related error of the differential output voltage of the ACTAf 2 Ch.



(c) Linearity range of the output charge of the ACTAf 2 Ch.



(d) Related error of the output charge of the ACTAf 2 Ch.

Figure 3.42.: Linearity range and the relative error, for differential output voltage (top) and charge (bottom) as a influence of the I_{bof} bias current source.

$I_{b_{AOP}}$ corresponds to the biasing current of the output stage for the HG and LG gain branches. It is a local biasing current for each of the two gain branches at each channel of the chip. The output voltages in common mode and differential mode variations as a function of the $I_{b_{AOP}}$ bias current source (see figure 3.43) are below ±0.2%.

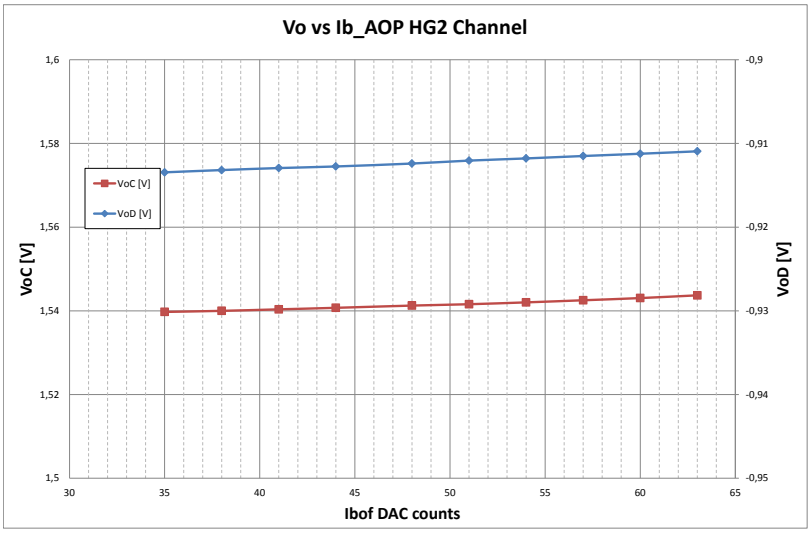


Figure 3.43.: ACTAf 2Ch output voltages in common mode and differential mode variations as a function of the $I_{b_{AOP}}$ bias current source.

The gain variations measured at the differential voltage output and integrated charge variations as a function of the $I_{b_{AOP}}$ bias current source (see figure 3.44), do not affect at the channel gain branch significantly (about ±2.2%).

The differential output voltage as a function of the differential input voltage of different $I_{b_{AOP}}$ bias current source values changes the saturation point of the differential output voltage. Figure 3.45 shows the linearity range (left plots) and the related linearity error (right plots) of the differential output voltage (and the charge at the bottom).

The different $I_{b_{AOP}}$ values shows variations of the linearity range from 1.2V to 1.8V for the HG and LG gain branches below 5% of the relative linearity error.

$I_{b_{ABF}}$ corresponds to the biasing current of the output stage for the Trigger gain branch. It is a local biasing current for the trigger gain branch at each channel of the chip. The output voltages in common mode and differential mode variations as a function of the $I_{b_{ABF}}$ bias current source (see figure 3.46) shows a variation of the common mode voltage about ±4.2% whereas the differential mode do not change significantly.

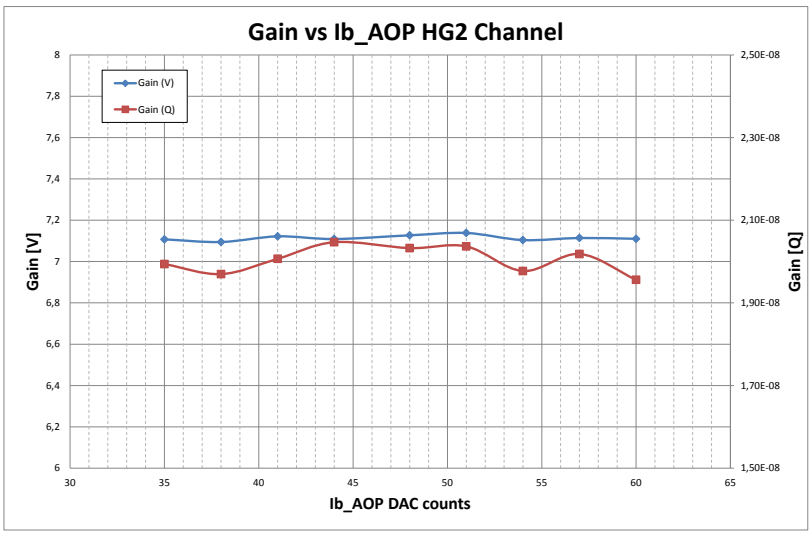
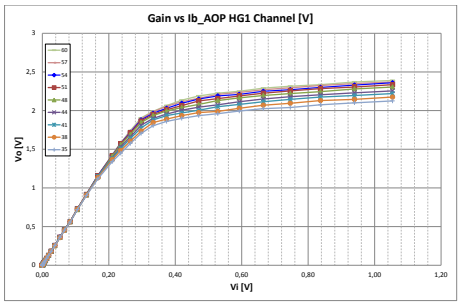
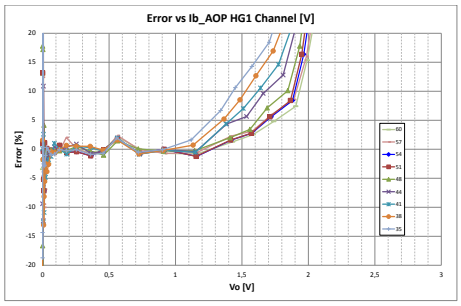


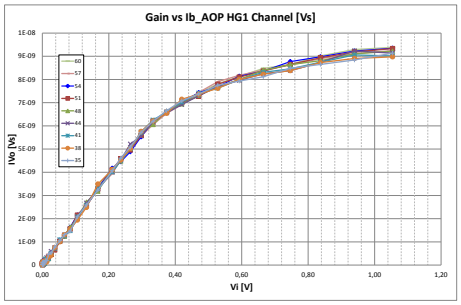
Figure 3.44.: ACTAf 2Ch gain variations measured at the differential voltage output and integrated charge variations as a function of the $I_{b_{AOP}}$ bias current source.



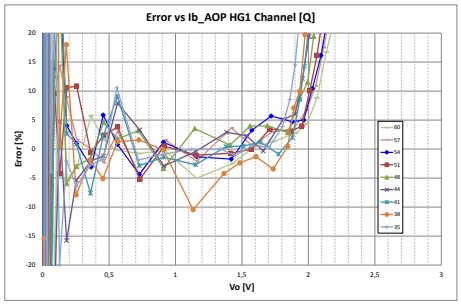
(a) Linearity range of the differential output voltage of the ACTAf 2 Ch.



(b) Related error of the differential output voltage of the ACTAf 2 Ch.



(c) Linearity range of the output charge of the ACTAf 2 Ch.



(d) Related error of the output charge of the ACTAf 2 Ch.

Figure 3.45.: Linearity range and the relative error, for differential output voltage (top) and charge (bottom) as a influence of the $I_{b_{AOP}}$ bias current source.

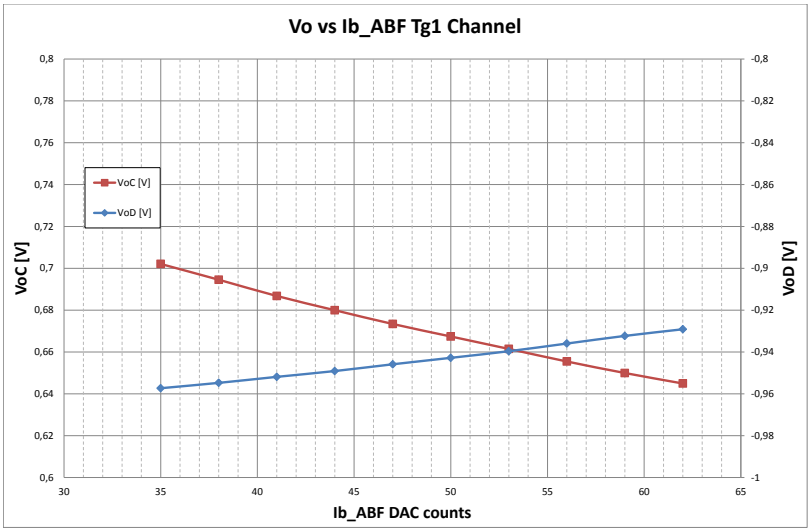


Figure 3.46.: ACTAf 2Ch output voltages in common mode and differential mode variations as a function of the $I_{b_{ABF}}$ bias current source.

The gain variations measured at the differential voltage output and integrated charge variations as a function of the $I_{b_{ABF}}$ bias current source (see figure 3.47), do not affect at the channel gain branch significantly (about $\pm 2.5\%$).

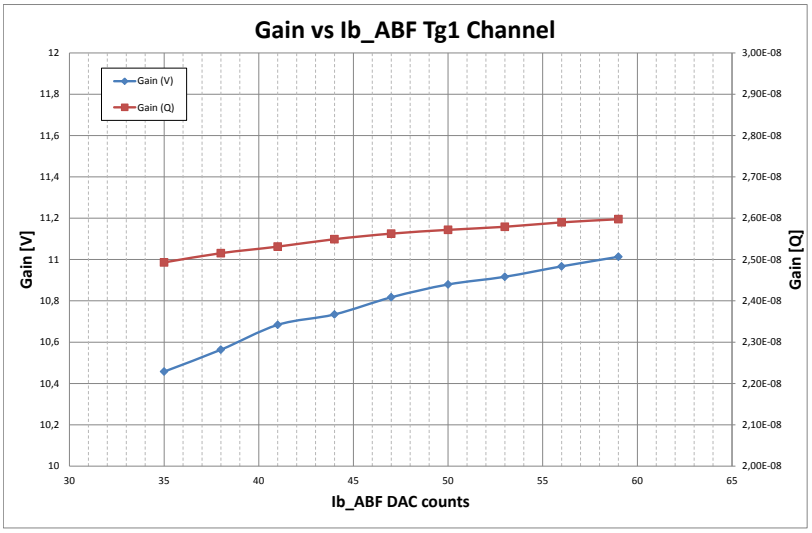
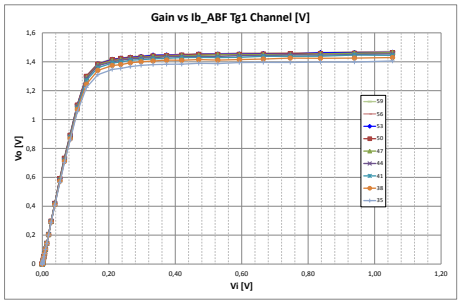


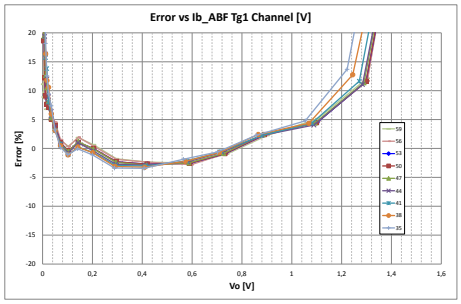
Figure 3.47.: ACTAf 2Ch gain variations measured at the differential voltage output and integrated charge variations as a function of the $I_{b_{ABF}}$ bias current source.

The differential output voltage as a function of the differential input voltage of different $I_{b_{ABF}}$ bias current source values changes the saturation point of the differential output voltage. Figure 3.48 shows the linearity range (left plots) and the related linearity error (right plots) of the differential output voltage (and the charge at the bottom).

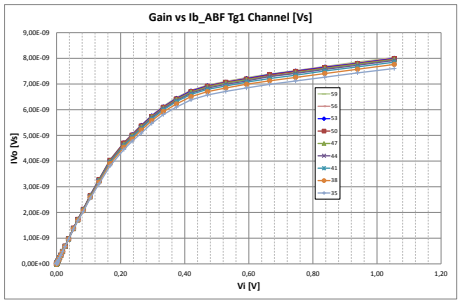
The different $I_{b_{ABF}}$ values shows variations of the linearity range from 1.15V to 1.3V for the Trigger gain branches below 5% of the relative linearity error.



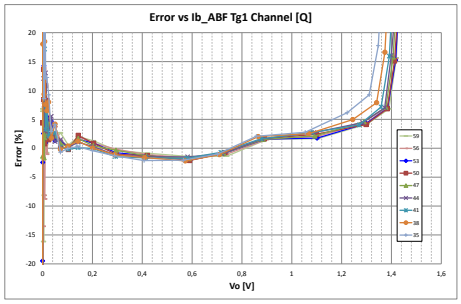
(a) Linearity range of the differential output voltage of the ACTAf 2 Ch.



(b) Related error of the differential output voltage of the ACTAf 2 Ch.



(c) Linearity range of the output charge of the ACTAf 2 Ch.



(d) Related error of the output charge of the ACTAf 2 Ch.

Figure 3.48.: Linearity range and the relative error, for differential output voltage (top) and charge (bottom) as a influence of the $I_{b_{ABF}}$ bias current source.

I_{bcf} corresponds to the biasing configuration current that determines the gain of each of the three gain branches at each channel of the chip. The gain variations measured at the differential voltage output and integrated charge variations as a function of the I_{bcf} bias current source (see figure 3.49), changes at the channel gain branch significantly (about $\pm 15\%$).

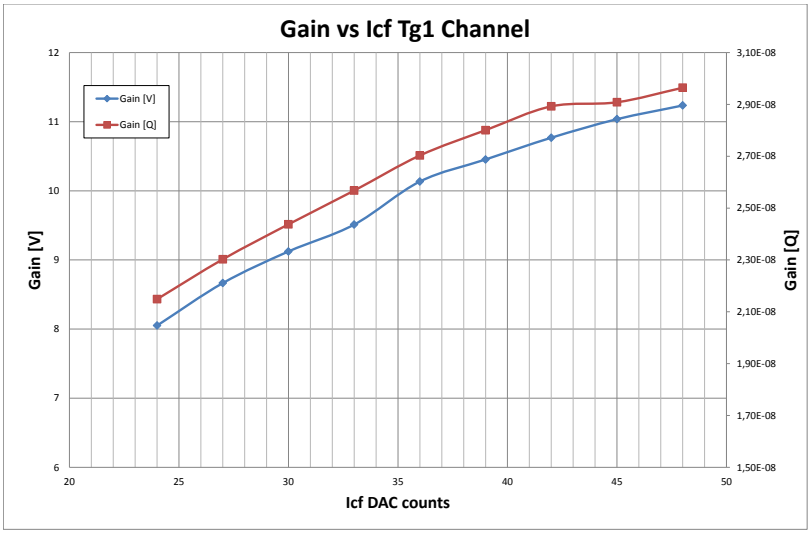
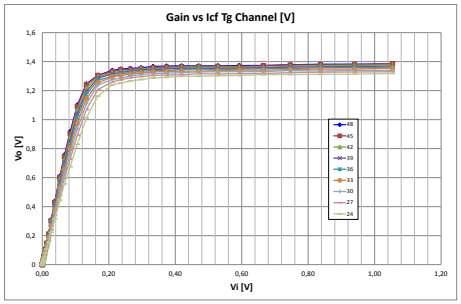


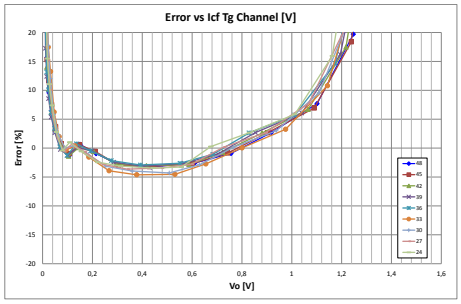
Figure 3.49.: ACTAf 2Ch gain variations measured at the differential voltage output and integrated charge variations as a function of the I_{bcf} bias current source.

The differential output voltage as a function of the differential input voltage of different I_{bcf} bias current source values changes the saturation point of the differential output voltage. Figure 3.50 shows the linearity range (left plots) and the related linearity error (right plots) of the differential output voltage (and the charge at the bottom).

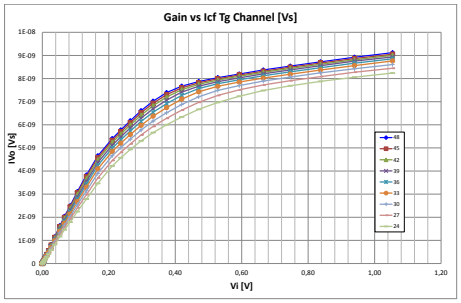
The different I_{bcf} values shows variations of the linearity range from 1.15V to 1.3V for the Trigger gain branches below 5% of the relative linearity error.



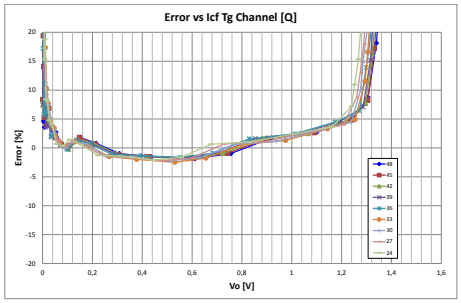
(a) Linearity range of the differential output voltage of the ACTAf 2 Ch.



(b) Related error of the differential output voltage of the ACTAf 2 Ch.



(c) Linearity range of the output charge of the ACTAf 2 Ch.



(d) Related error of the output charge of the ACTAf 2 Ch.

Figure 3.50.: Linearity range and the relative error, for differential output voltage (top) and charge (bottom) as a influence of the I_{bcf} bias current source.

3.5 ACTA Conclusions

An alternative method to implement fully differential wideband pulse amplifiers has been presented. A gain of 20 V/V (25 dB) can be reached, while preserving a BW of 400 MHz. Measurements show that linearity for fast pulses is at the few % level, thus comparable to solutions based on feedback OTA which are often limited by slew rate and other transient issues. The design exhibits a large degree of tuneability, as can be noticed from table 3.3. An amplifier with a GBW product of 8 GHz has been implemented and validated in a $0.35\mu m$ CMOS technology; it can be integrated with the analogue memory in a final chip.

The class AB circuit presented in Section 3.1.3 has been also used as unity gain input buffer of the NECTAr0 chip. Thanks to the non linear class B current boost, a switch capacitor array of 1024 cells can be driven with $>$ 400 MHz BW and less than 1mW power consumption.

The proposed architecture is inherently low voltage (headroom is just 2 saturation voltages as described in section 3.1.3), thus to achieve an output excursion of 1.5 Vpp, a 1.8 V supply voltage may be enough.

4

Conclusions

This thesis was focused on novel design circuitry for the channel signal path of a Cherenkov Telescope camera. Where, the amplification is divided into gain stages in order to achieve the requirements of the design. The fist stage, presented a innovative low noise wideband pre-amplifier design whereas, the second amplification stage presented a novel gain circuitry design, being impossible with the classic schemes at the required technology. This second stage, also derived and adapted the signal to the following parts of the read-out system of the Cherenkov Telescope camera. This section summarizes the main contributions of these designs, outlines the publications and conference participations derived from this thesis and concludes providing some interesting future avenues of research.

4.1 Conclusions

An innovative design that achieve all the restrictions with a very low power consumption fulfils the requirements for the first pre-amplification stage. Different versions have been designed and tested. The solution selected is based in a novel current mode circuit to create multiple gain paths at the very front end of the input stage of the readout electronics, allowing to achieve simultaneously high dynamic range, low noise, low input impedance, low voltage and low power performances.

The pre-amplification stage also comprises a closed loop transimpedance amplifier with a novel class AB output stage designed with a $0.35\mu m$ SiGe technology, allowing the design to drive a cable or a transmission line (typ. 50Ω load) while preserving high bandwidth with moderate power consumption.

An alternative method to implement fully differential wideband pulse amplifiers has been presented. The required gain can be reached, while preserving also the bandwidth. Linearity for fast pulses is at the level of solutions based on feedback OTA, limited by slew rate and other transient issues. The design exhibits a large degree of tuneability. An amplifier with a GBW product of 8 GHz has been implemented and validated in a $0.35\mu m$ CMOS technology. This design also incorporates a closed loop transimpedance amplifier with a novel class AB output stage based on the design of the first amplification stage, but designed in a $0.35\mu m$ CMOS technology which is more difficult to achieve.

The class AB circuit designed for the second amplification stage has been also used as unity gain input buffer of the NECTAr0 chip. Thanks to the non linear class B current boost, a switch capacitor array of 1024 cells can be driven with $>$ 400 MHz BW and less than 1mW power consumption.

4.2 Future avenues of research

A future avenue of research derived from this dissertation, might be the design of the first amplification stage to be used with the next photo-sensor CTA candidates which will be the silicon photo-multipliers (SiPM).

These other kind of photo-sensors should be considered as an array of photo-sensors itself, in order to cover a similar area that the actual PMTs. The input capacitance of this first amplification stage could be very different depending on the SiPM selected, and so, the requirements of the new pre-amplifier are directly related to that parameter. Design a circuit able to cover all the SiPM considered as a possible candidates until now will be an interesting topic of research. The number of SiPMs selected to form an array equivalent to one PMT, will determine the number of channels that should integrate the new design, where, the output, should represent an addition of all the channels in the design.

The CTA consortium is still in the design phase for the upgrading to that new sensors at the moment of writing this thesis. On the other hand, the aim of the upgrade, will be try to maintain the front-end read-out as much as possible, by only replace the focal plane instrumentation with the one equipped with the new photo-sensors so, the outputs of the new electronics should keep the differential path and also the dual gain per channel structure.

Finally, an extrapolation of the design to a nano meter CMOS technology [14] (below 180 nm) of the second amplification stage, would lead to an overall bandwidth exceeding 1 GHz (GBW product of 20 GHz), which may be interesting for the next generation of analogue sampling memories, among other applications. Nevertheless, worst matching and lower supply voltage of these technologies may arise some concerns. Regarding the former, the DC offset circuitry can manage additional offset. Main uncertainty would be the impact of the mismatch on the linearity of the transconductor.

4.3 Patent, Publications and Conferences

The list of a patent, publications and conference papers related to this dissertation are outlined in this section.

4.3.1 Patent

There is a Patent to protect the design of the novel design of the firts amplification stage.

1. *Patent:* D. Gascón, A. Sanuy and Ll. Garrido, “First front stage current-mode circuit for reading sensors and integrated circuit”, Patent, ES, ES20110030565 20110411, ES2390305 (B1), WO2012140299 (A1), November 08, 2012 [30].

4.3.2 Journal papers

The list of journal papers is detailed next.

1. *Article in Refereed Journal:* D. Gascón, A. Sanuy, E. Delagnes, X. Sieiro, F. Feinstein, J-F. Glicenstein, P. Nayman, M. Ribo, F. Toussenel, J-P. Tavernet, P. Vincent and S. Vorobiov, "Wideband pulse amplifier with 8 GHz GBW product in a 0.35 μm CMOS technology for the integrated camera of the Cherenkov Telescope Array", Journal of Instrumentation, Vol. 5, C12034, 2010.

2. *Article in Refereed Journal:* S. Vorobiov, J. Bolmont, P. Corona, E. Delagnes, F. Feinstein, D. Gascón, J.-F. Glicenstein, C.L. Naumann, P. Nayman, A. Sanuy, F. Toussenel, P. Vincent, "NECTAr: New electronics for the Cherenkov Telescope Array", Nuclear Instruments and Methods in Physics Research A, Vol. 639, Issue 1, Pag. 62-64, 2011.

3. *Article in Refereed Journal:* D. Gascón, A. Sanuy, J. M. Paredes, L. Garrido, M. Ribó and J. Sieiro, "Wideband (500 MHz) 16 bit dynamic range current mode input stage for photodetector readout", Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Pag. 750-757, 2011 IEEE.

4. *Article in Refereed Journal:* E. Delagnes, J. Bolmont, P. Corona, D. Dzahini, F. Feinstein, D. Gascón, J.-F. Glicenstein, F. Guilloux, C. L. Naumann, P. Nayman, F. Rarbi, A. Sanuy, J.P. Tavemet, F. Toussenel, P. Vincent, S. Vorobiov, "NECTAr0, a new high speed digitizer ASIC for the Cherenkov Telescope Array", Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Pag. 1457-1462, 2011 IEEE.

5. *Article in Refereed Journal:* C.L. Naumann, E. Delagnes, J. Bolmont, P. Corona, D. Dzahini, F. Feinstein, D. Gascón, J.-F. Glicenstein, F. Guilloux, P. Nayman, F. Rarbi, A. Sanuy, J.-P. Tavernet, F. Toussenel, P. Vincent, S. Vorobiov, "New electronics for the Cherenkov Telescope Array (NECTAr)", Nuclear Instruments and Methods in Physics Research A, Vol. 695, Pag. 44-51, 2012.

6. *Article in Refereed Journal:* A. Sanuy, E. Delagnes, D. Gascón, X. Sieiro, J. Bolmont, P. Corona, F. Feinstein, J-F. Glicenstein, C.L. Naumann, P. Nayman, M.Ribó, J-P. Tavernet, F. Toussenel, P. Vincent, S. Vorobiov, "Wideband pulse amplifiers for the NECTAr chip", Nuclear Instruments and Methods in Physics Research A, Vol. 695, Pag. 385-389, 2012.

7. *Article in Refereed Journal:* S. Vorobiov , F. Feinstein, J. Bolmont, P. Corona, E. Delagnes, A. Falvard, D. Gascón, J.-F. Glicenstein, C.L. Naumann, P. Nayman, M. Ribo, A. Sanuy, J.-P. Tavernet, F. Toussenel, P. Vincent, "Optimizing read-out of the NECTAr front-end electronics", Nuclear Instruments and Methods in Physics Research A, Vol. 695, Pag. 394-397, 2012.

8. *Article in Refereed Journal:* A. Sanuy, D. Gascón, J. M. Paredes, L. Garrido, M. Ribó and J. Sieiro, "Wideband (500 MHz) 16 bit dynamic range current mode PreAmplifier for the CTA cameras (PACTA)", Journal of Instrumentation, Vol. 7, C01100, 2012.

4.3.3 Conference papers

The list of conference papers is provided next.

1. *Article in Refereed Journal:* D. Gascón, A. Sanuy, and J. Sieiro, "Compact Class-AB Follower for Wideband Closed Loop Line Drivers", 19th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2012, Pag. 101-104, Seville, Spain.

2. *Article in Refereed Journal:* J-F. Glicenstein, M. Barcelo, J-A. Barrio, O. Blanch, J. Boix, J. Bolmont, C. Boutonnet, S. Cazaux, E. Chabanne, C. Champion, F. Chateau, S. Colonges, P. Corona, S. Couturier, B. Courty, E. Delagnes, C. Delgado, J-P. Ernenwein, S. Fegan, O. Ferreira, M. Fesquet, G. Fontaine, N. Fouque, F. Henault, D. Gascón, D. Herranz, R. Hermel, D. Hoffmann, J. Houles, S.Karkar, B. Khelifi, J. Knöldseder, G. Martinez, K. Lacombe, G. Lamanna, T. Leflour, R. Lopezcoto, F. Louis, A. Mathieu, E. Moulin, P. Nayman, F. Nunio, J-F. Olive, J-L. Panazol, P-O. Petrucci, M. Punch, J. Prast, P. Ramon, M. Riallot, M. Ribó, S. Rosier-Lees, A. Sanuy, J. Sieiro, J-P. Tavernet, L.A. Tejedor, F. Toussenel, G. Vasileiadis, V. Voisin, V. Waegebert, C. Zurbach, for the CTA consortium., "The NectarCAM camera project", In Proceedings of the 33rd International Cosmic Ray Conference (ICRC2013), Rio de Janeiro (Brazil). 2013.

3. *Article in Refereed Journal:* H. Kubo, R. Paoletti, Y. Awane, A. Bamba, M. Barcelo, J.A. Barrio, O. Blanch, J. Boix, C. Delgado, D. Fink, D. Gascón, S. Gunji, R. Hagiwara, Y. Hanabata, K. Hatanaka, M. Hayashida, M. Ikeno, S. Kabuki, H. Katagiri, J. Kataoka, Y. Konno, S. Koyama, T. Kishimoto, J. Kushida, G. Martinez, S. Masuda, J.M. Miranda, R. Mirzoyan, T. Mizuno, T. Nagayoshi, D. Nakajima, T. Nakamori, H. Ohoka, A. Okumura, R. Orito, T. Saito, A. Sanuy, H. Sasaki, M. Sawada, T. Schweizer, R. Sugawara, K.-H. Sulanke, H. Tajima, M. Tanaka, S. Tanaka, L.A. Tejedor, Y. Terada, M. Teshima, F. Tokanai, Y. Tsuchiya, T. Uchida, H. Ueno, K. Umehara, T. Yamamoto, for the CTA consortium., "Development of the Photomultiplier-Tube Readout System for the CTA Large Size Telescope", In Proceedings of the 33rd International Cosmic Ray Conference (ICRC2013), Rio de Janeiro (Brazil). 2013.

4. *Article in Refereed Journal:* J-F. Glicenstein, O. Abril, J-A. Barrio, O. Blanch, J. Bolmont, F. Bouyjou, P. Brun, E. Chabanne, C. Champion, S. Colonges, P. Corona, E. Delagnes, C. Delgado, C. Diaz, D. Durand, J-P. Ernenwein, S. Fegan, O. Ferreira, M. Fesquet, A. Fiasson, G. Fontaine, N. Fouque, D. Gascón, B. Giebels, F. Henault, R. Hermel, D. Hoffmann, D. Horan, J. Houles, P. Jean, L. Jocou, S. Karkar, J. Knoedlseder, R. Kossakowski, G. Lamanna, T. LeFlour, J-P. Lenain, A. Leveque, F. Louis, G. Martinez, Y. Moudden, E. Moulin, P. Nayman, F. Nunio, J-F. Olive, J-L. Panazol, S. Pavy, P-O. Petrucci, E. Pierre, J. Prast, M. Punch, P. Ramon, S. Rateau, T. Ravel, S. Rosier-Lees, A. Sanuy, M. Shayduk, P-Y. Sizun, K-H. Sulanke, J-P. Tavernet, L-A. Tejedor, F. Toussenel, G. Vasileiadis, V. Voisin, V. Waegebert, R. Wischnewski, for the CTA consortium., "NectarCAM : a camera for the medium size telescopes of the Cherenkov Telescope Array", In Proceedings of the 34th International Cosmic Ray Conference (ICRC2015), The Hague, The Netherlands. 2015.

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A

Appendix PACTA Datasheet

Institut de Ciències del Cosmos

16 bits dynamic range and 450 MHz bandwidth differential pre-amplifier for photodetector readout

Data Sheet **PACTAv1.4**

FEATURES

Dual gain path with a saturation control circuit at the HG branch
Double transimpedance gain: 1.2kΩ (HG) and 80 Ω (LG)
Dynamic range: 15.9 bits
-3 dB bandwidth of 450 MHz
Low input referred noise: 10 pA/√Hz
Noise (ENC): 4700 electrons (at 10 ns of integration time)
Relative linearity error: < 2%
Input range: 20 mAp
High Slew Rate: 1V/ns
Low output impedance stage with cable and transmission line driving capabilities
Single-ended input to differential output
Low power consumption, 132 mW at 3.3 V supply

APPLICATIONS

Photodetectors readout

GENERAL DESCRIPTION

The PACTAv1.4 is a fully differential, dual output, pre-amplifier based on current-mode architecture

The PACTAv1.4 is developed by using the Austria Micro Systems (AMS) 0.35 µm HBT BiCMOS technology and operates over the −40°C to +125°C junction temperature range. The PACTAv1.4 is available in a 32-QFN package.

TYPICAL APPLICATION CIRCUIT

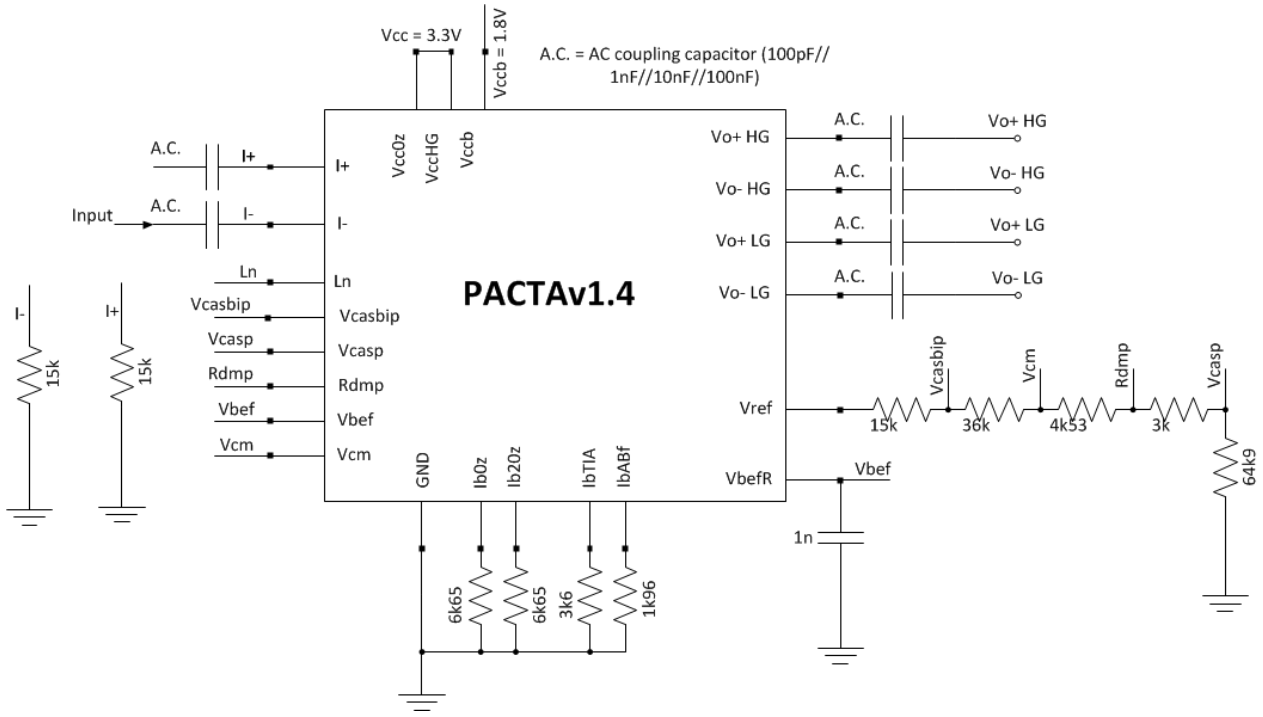

Figure 1. PACTAv1.4 Typical application circuit

Rev. 3

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Tel: 93.40.21588
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12/12—Revision 0: Initial Version

[1] Coaxial cable connection between the PMT output and the preamplifier input.

FUNCTIONAL BLOCK DIAGRAM

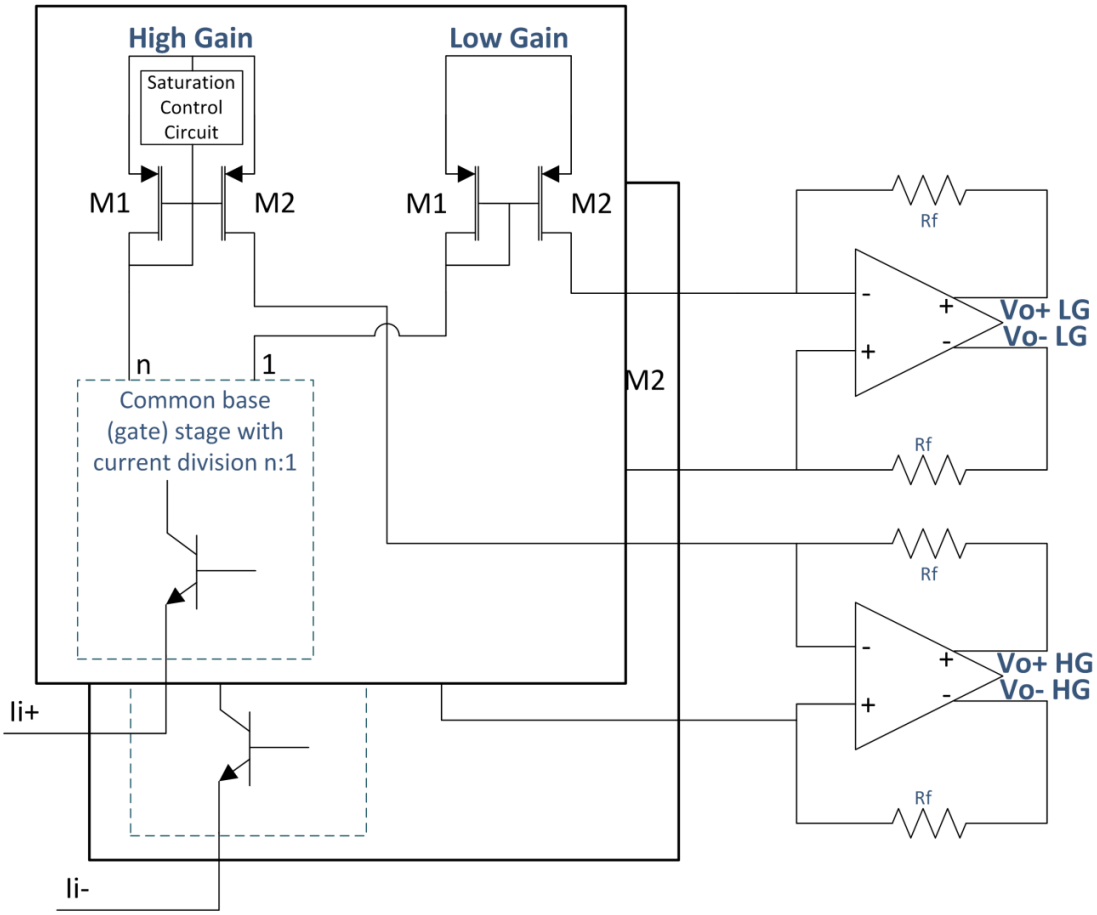


Figure 2. PACTA Functional Block Diagram

SPECIFICATIONS

T_A = +25°C, V_{cc} = 3.3 V and V_{ccb} = 1.8 V, Ln On and Rin 15 kΩ unless otherwise noted.

Table 1.

Parameters	Conditions [1]	Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
Bandwidth (-3 dB)	HG Branch (Rin 15 kΩ)		484		MHz
	HG Branch (no Rin)		417		MHz
	LG Branch		361		MHz
Dynamic Range			15.9		Bits
Total Harmonic Distortion	HG Branch, f = 1 MHz, VoD = 500 mV		-50		dB
INPUT					
Relative Linearity Error (charge)	Nonlinearity		< ± 2%		
Max Input Current Range [1]	HG Saturation		290		phe
			860		µA
	LG Saturation		> 7200		phe
			> 21.5		mA
NOISE					
Input Referred Noise [2]	f = 100MHz				
Ln On			10.5		pA/√Hz
Ln Off			12.5		pA/√Hz
Total Output RMS Noise [3]	DC to 500 MHz				
Ln On	HG		632		µV rms
	LG		414		µV rms
Ln Off	HG		742		µV rms
	LG		401		µV rms
TRANSFER CHARACTERISTICS					
Transresistance	HG	1140	1200	1260	Ω
	LG	74	78.61	82	Ω
Power Supply Rejection Ratio (PSRR)	-18dB @ Vcc ➔ Up to 100MHz		-60		dB
Gain Temperature Dependence (0 ºC to 70 ºC)	HG		< 0.05		%/ºC
	LG		< 0.05		%/ºC
OUTPUT					
Differential Offset	HG	-25	0	25	mV
	LG	-20	5	30	mV
Output Common-Mode Voltage	HG	1.1	1.37	1.6	V
	LG	1.1	1.37	1.6	V
Voltage Swing (Differential)	Rl = ∞		1.68		V_{p-p}
	Rl = 50 Ω		1.2		V_{p-p}
Output Impedance	DC to 100 MHz		20		Ω
Recovery Time	HG		< 1.5		ns
	LG		< 1.5		ns
POWER SUPPLY					
Input Voltage	V_{cc}	3.2	3.3	3.4	V
	V_{ccb}		1.8	2	V
Current	V_{cc}	46	45	44	mA
	V_{ccb}		5		mA
Power Dissipation [4]	V_{cc} = 3.3 V	145	149	152	mW

[1] At PMT gain of 40k.

[2] With an input resistor of 15kΩ.

[3] With an input resistor of 15kΩ.

[4] With an input resistor of 15kΩ.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{cc}	3.2 V to 3.4 V
V_{ccb} 1	1.8 V to 2 V
Temperature Range	
Operating (Junction)	−40°C to +125°C
Storage	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

1 A voltage regulator needs to be added to provide the V_{ccb} voltage. The baseline for the regulator chip is ADP161.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Boundary Condition

θ_{JA} is measured using natural convection on a JEDEC 4-layer board, and the exposed pad is soldered to the printed circuit board (PCB) with thermal vias.

Table 3. Thermal Resistance

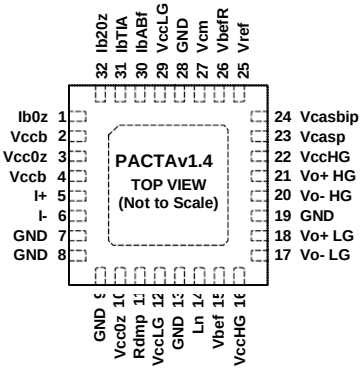
Package Type	θ_{JA}	Unit
32-Lead QFN	TBC [1]	°C/W

[1] To be confirmed.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES 1. THE EXPOSED PAD SHOULD BE SOLDERED TO AN EXTERNAL GND PLANE.

Figure 3. Pin Configuration (Top View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	I_{b0z}	Input stage Bias current.
2, 4	V_{ccb}	Positive 1,8 V power supply.
5	I+	Noninverting differential Input. Typically ac-coupled. Used as a dummy input.
6	I-	Inverting differential Input. Typically ac-coupled.
11	V_{Rdmp}	Bias voltage.
14	L_n	Low noise mode selection. When this pin is connected to V_{cc}, the low noise mode is enabled and the amplifier reduces the intrinsic noise up to 20%, but also the bandwidth on the dummy input, but not affect on the signal input (I-). When this pin is connected to ground, the amplifier operates as PACTAv1.2b amplifier version.
15	V_{bef}	Bias voltage. Servo control of the operating point at the output stage.
17	$V_{o- LG}$	Differential Output. Typically ac-coupled. This pin is biased to the V_{cm} input voltage.
18	$V_{o+ LG}$	Differential Output. Typically ac-coupled. This pin is biased to the V_{cm} input voltage.
20	$V_{o- HG}$	Differential Output. Typically ac-coupled. This pin is biased to the V_{cm} input voltage.
21	$V_{o+ HG}$	Differential Output. Typically ac-coupled. This pin is biased to the V_{cm} input voltage.
23	V_{casp}	Bias voltage.
24	V_{casbip}	Bias voltage.
25	V_{ref}	Bias voltage.
26	V_{befR}	Bias voltage.
27	V_{cm}	Common-Mode Voltage. A voltage applied to this pin sets the common-mode voltage of the output.
3, 10, 12, 16, 22, 29	V_{cc}	Positive 3,3 V power supply.
30	I_{bABf}	Output stage OPAMP Bias current.
31	I_{bTIA}	OPAMP TIA Bias current.
32	I_{b20z}	Input stage Bias current.
7, 8, 9, 13, 19, 28, Exposed Pad	GND	Ground. Exposed Pad in internally connected to GND and must be soldered to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

Operating conditions: T_A = 25°C, unless otherwise noted.

Input pulse shape and timing response measurement. See accurate pulse injector of section Applications Information.

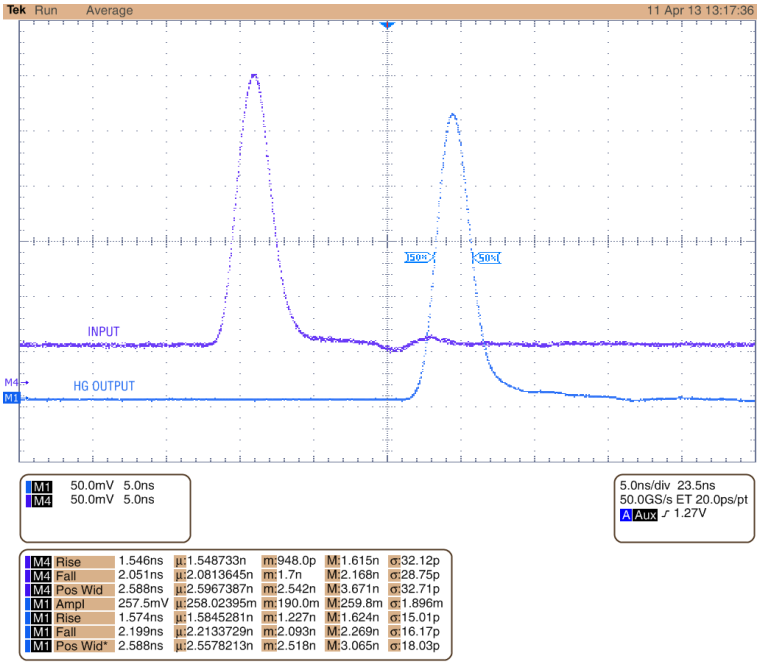


*Figure 4. PACTAv1.4 shape measurements with a **negative** pluse at the I- input. V_oHG is optained by $(V_{o-}) - (V_{o+})$*

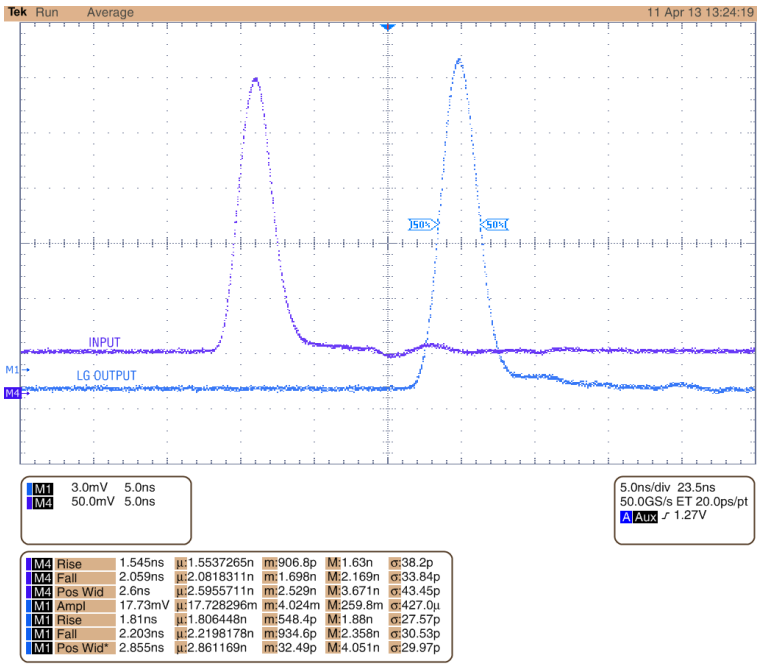


*Figure 5. PACTAv1.4 shape measurements with a **negative** pluse at the I- input. V_oLG is optained by $(V_{o-}) - (V_{o+})$*

* **Note:** Input signal is depicted inverted in order to maintain the picture polarity

One photoelectron is the equivalent pulse of a triangular signal of 3µA of peak current.
BUT the input signal for linearity test is the one depicted in Fig 4 and 5.

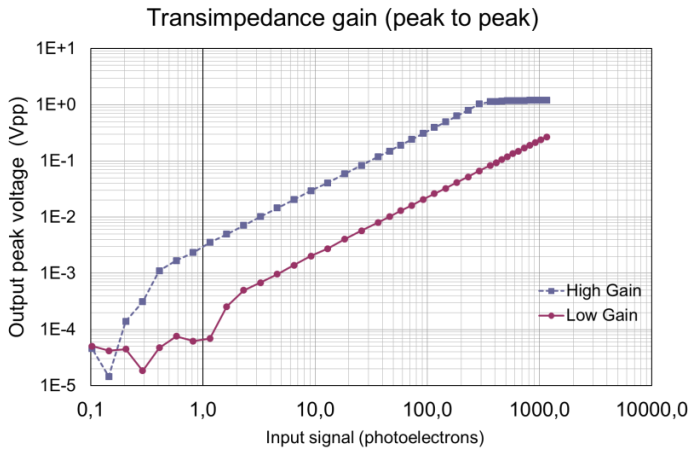


Figure 6. PACTAv1.4 Linearity test with R_{in} 15k and LN On (log scale)

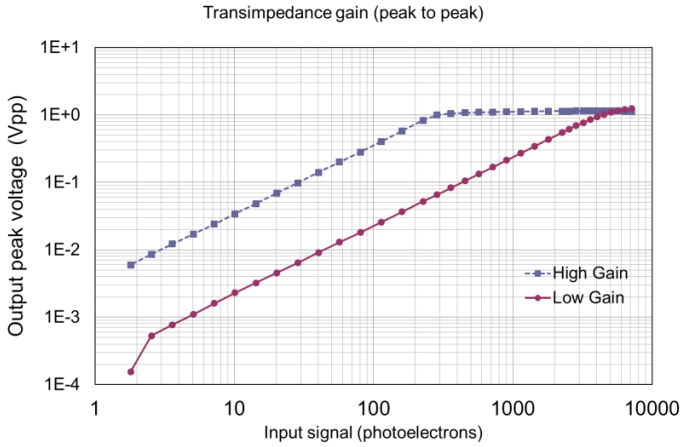


Figure 7. PACTAv1.4 Linearity test with R_{in} 10k and LN On (log scale)

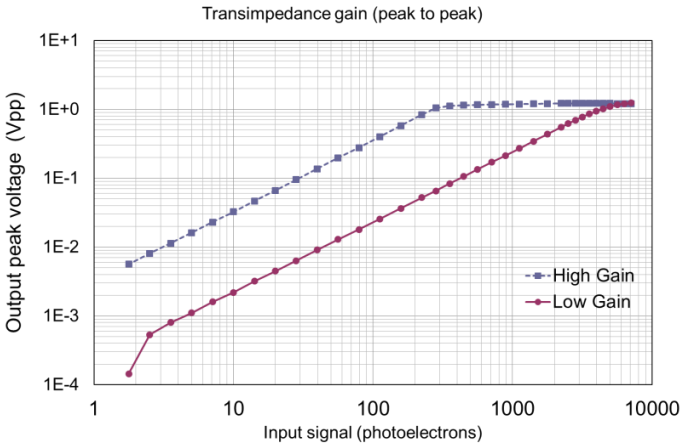


Figure 8. PACTAv1.4 Linearity test with no R_{in} and LN On (log scale)

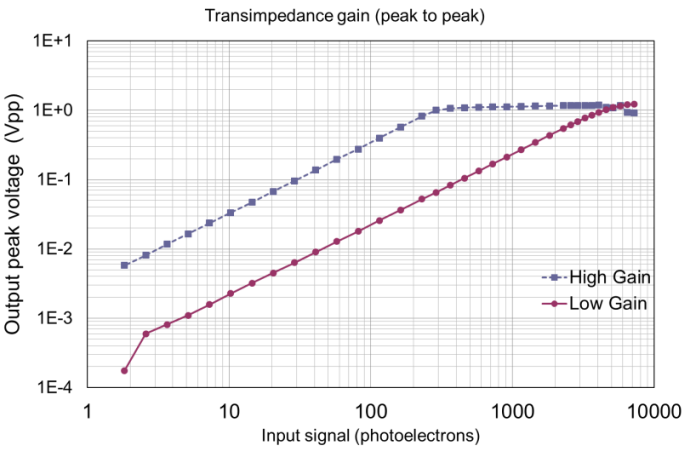


Figure 9. PACTAv1.4 Linearity test with R_{in} 15k and LN Off (log scale)

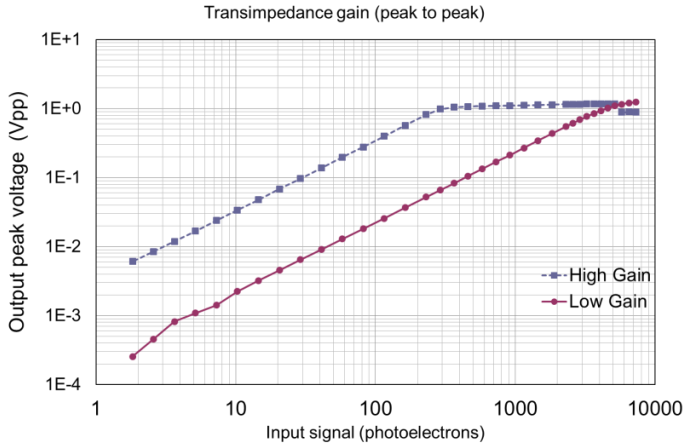


Figure 10. PACTAv1.4 Linearity test with R_{in} 10k and LN Off (log scale)

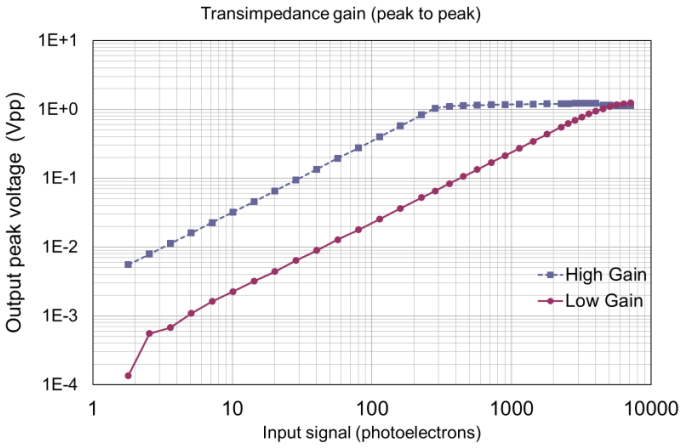


Figure 11. PACTAv1.4 Linearity test with no R_{in} and LN Off (log scale)

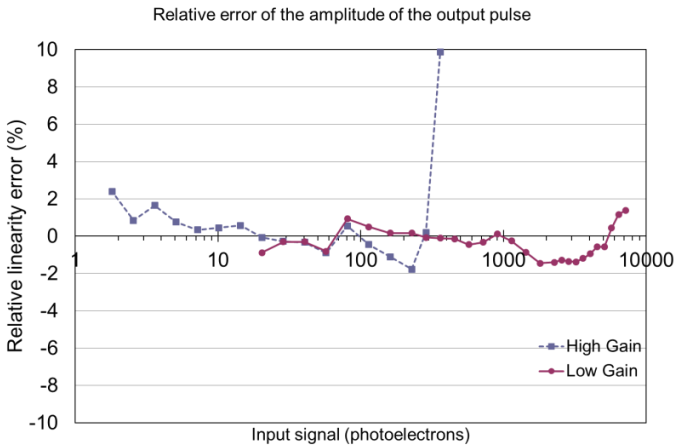


Figure 12. PACTAv1.4 Linearity relative error test with R_{in} 15k and LN On

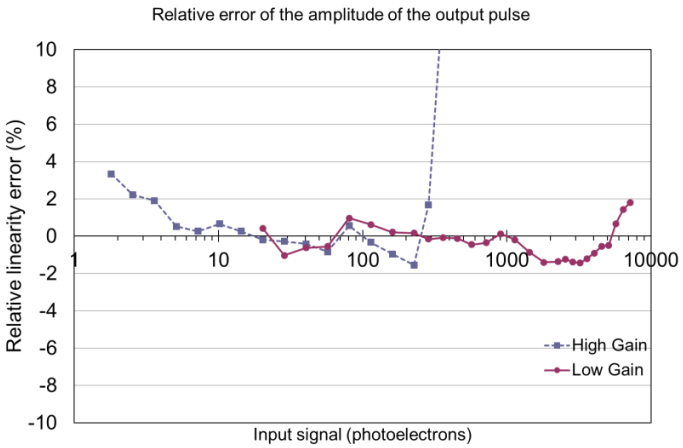


Figure 13. PACTAv1.4 Linearity relative error test with R_{in} 10k and LN On

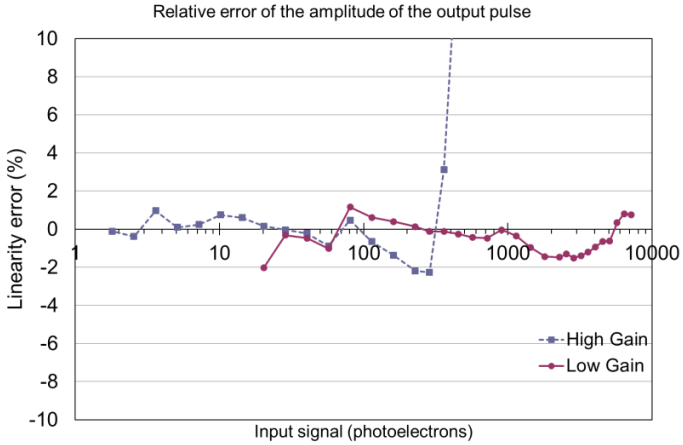


Figure 14. PACTAv1.4 Linearity relative error test with no R_{in} and LN On

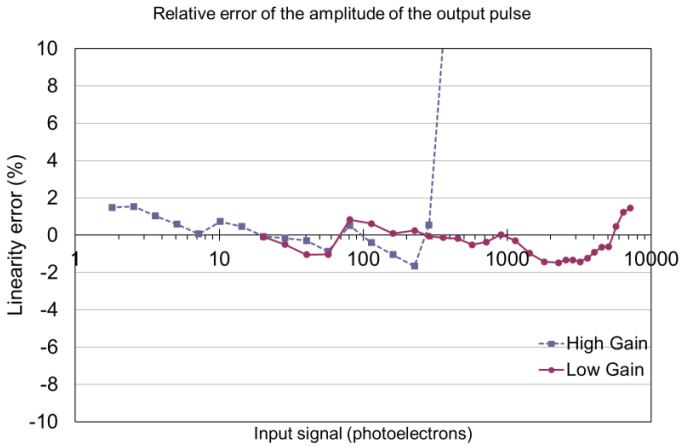


Figure 15. PACTAv1.4 Linearity test with R_{in} 15k and LN Off (log scale)

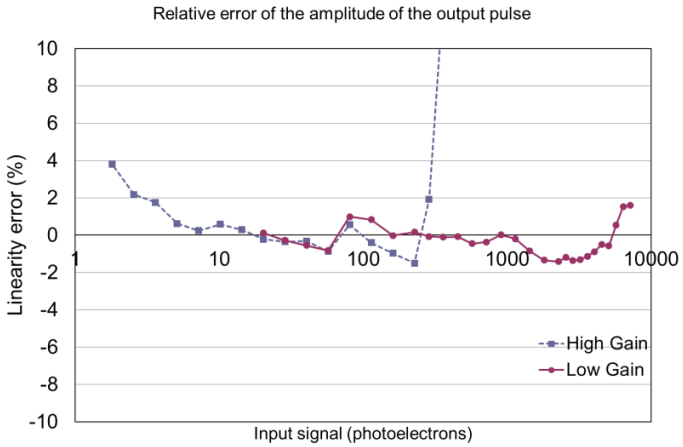


Figure 16. PACTAv1.4 Linearity relative error test with R_{in} 10k and LN Off

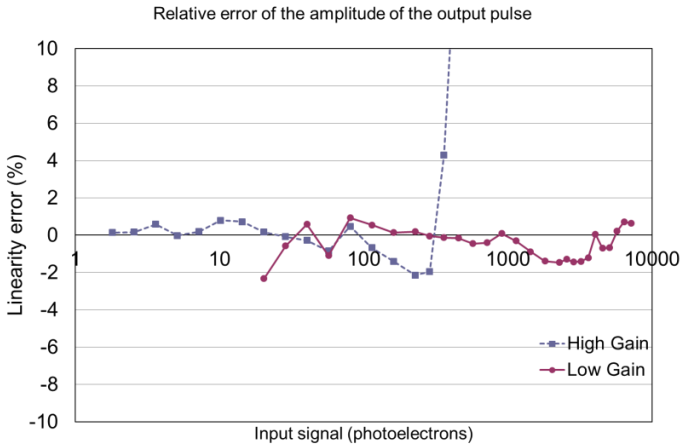


Figure 17. PACTAv1.4 Linearity relative error test with no R_{in} and LN Off

Note: Measured charge with 10 ns of integration time.

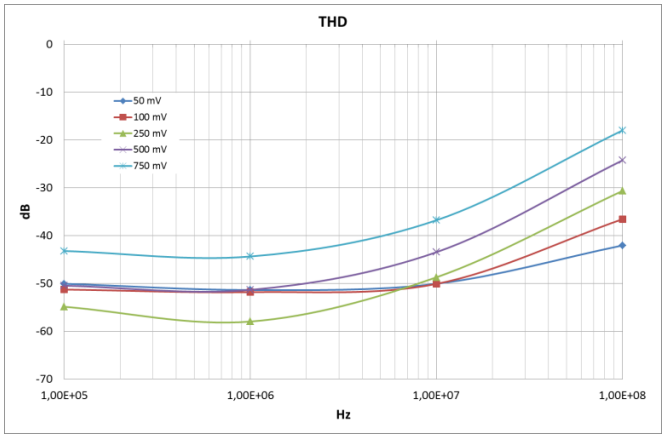


Figure 18. PACTAv1.4 Total harmonic distorsion (THD) test with R_{in} 3k3 at different output signal amplitudes

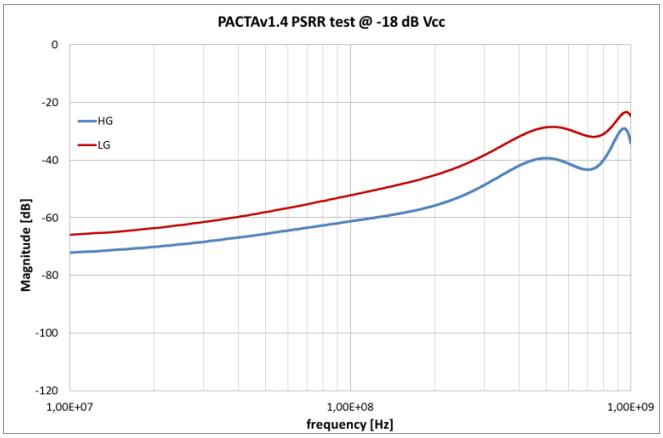


Figure 19. PACTAv1.4 PSRR measurements with R_{in} 15k and Ln On at V_{cc} of -18 dB

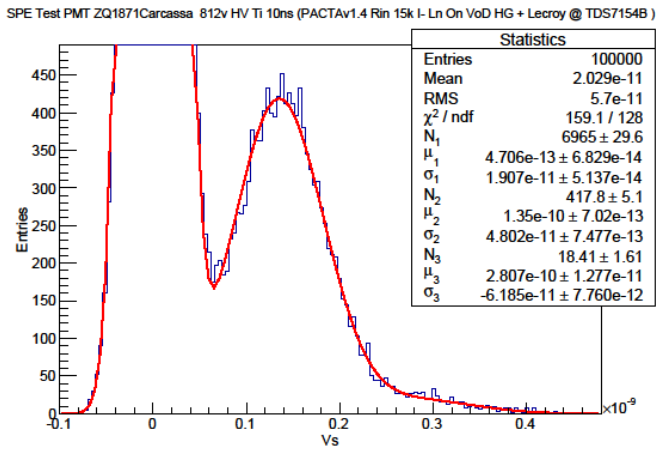


Figure 20. PACTAv1.4 spe test at 10ns of integration time with R_{in} 15k and Ln On

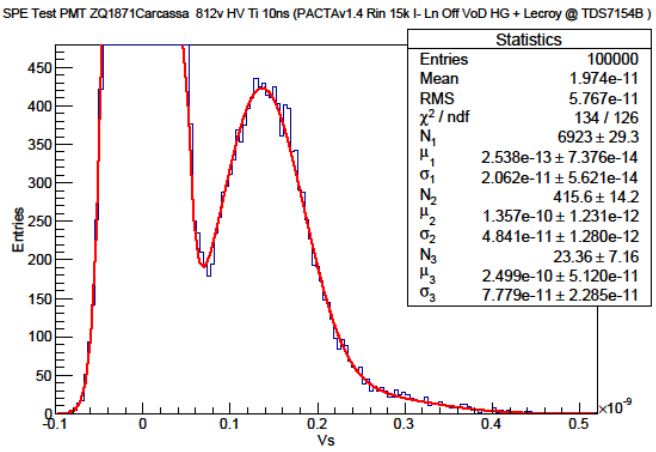


Figure 21. PACTAv1.4 spe test at 10ns of integration time with R_{in} 15k and Ln Off

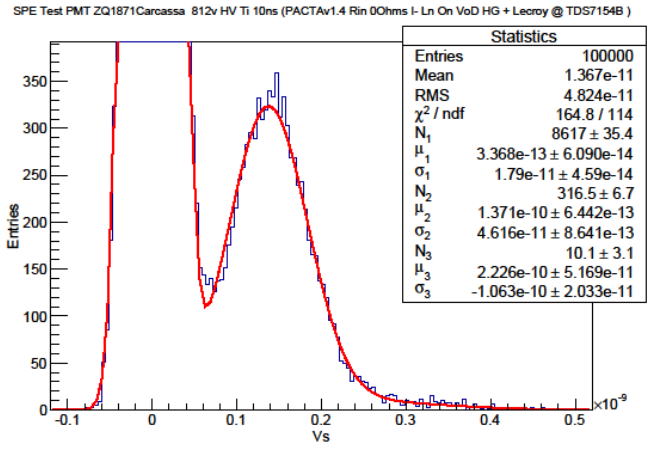


Figure 22. PACTAv1.4 spe test at 10ns of integration time with no R_{in} and Ln On

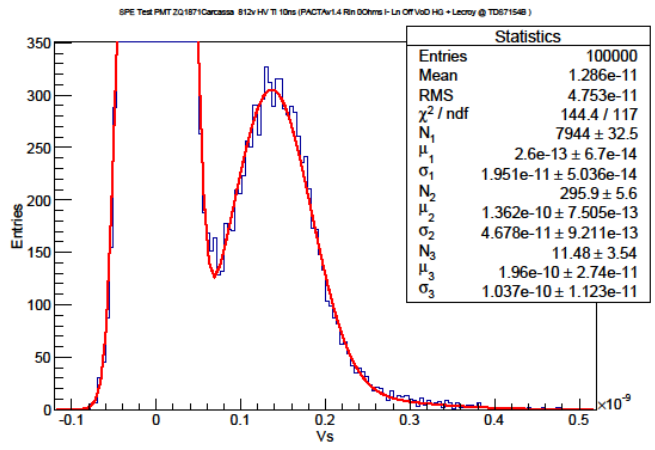


Figure 23. PACTAv1.4 spe test at 10ns of integration time with no R_{in} and Ln Off

Note: Measured with PMT R11920 (serial number ZQ1871) from Hamamatsu at 40k gain (812V).

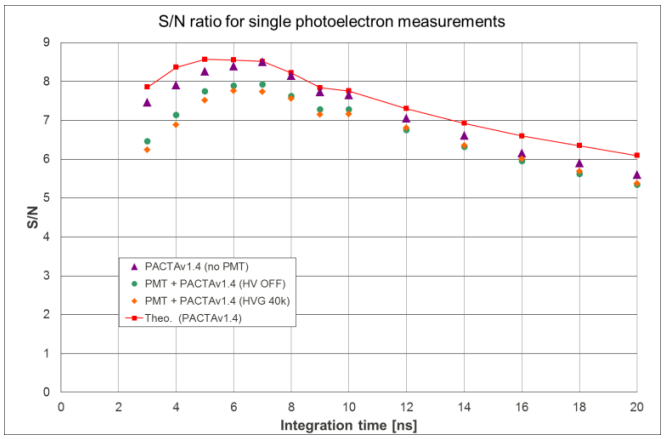


Figure 24. PACTAv1.4 S/N ratio for spe measurements with R_{in} 15k and Ln On

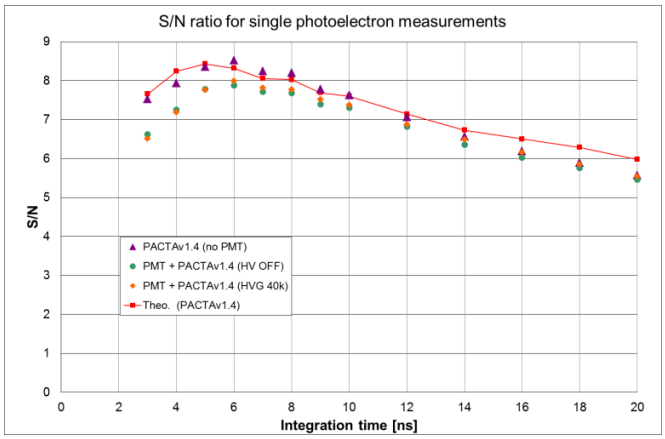


Figure 25. PACTAv1.4 S/N ratio for spe measurements with R_{in} 10k and Ln On

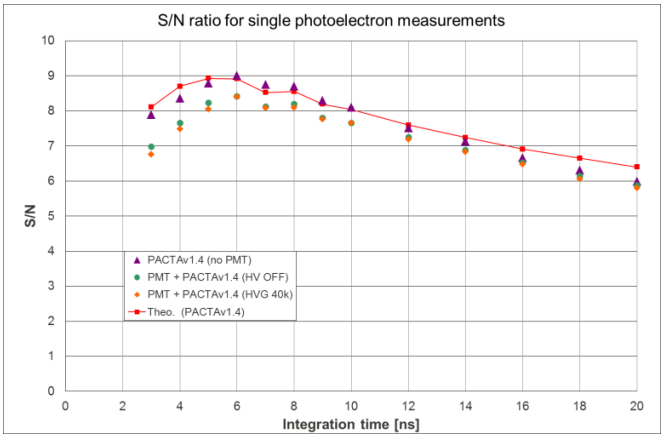


Figure 26. PACTAv1.4 S/N ratio for spe measurements with no R_{in} and Ln On

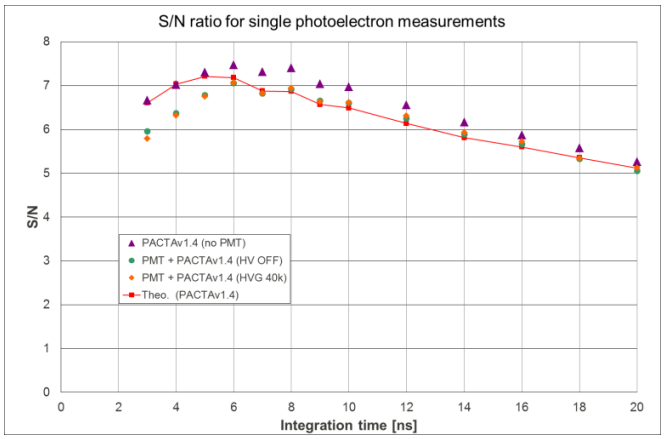


Figure 27. PACTAv1.4 S/N ratio for spe measurements with R_{in} 15k and Ln Off

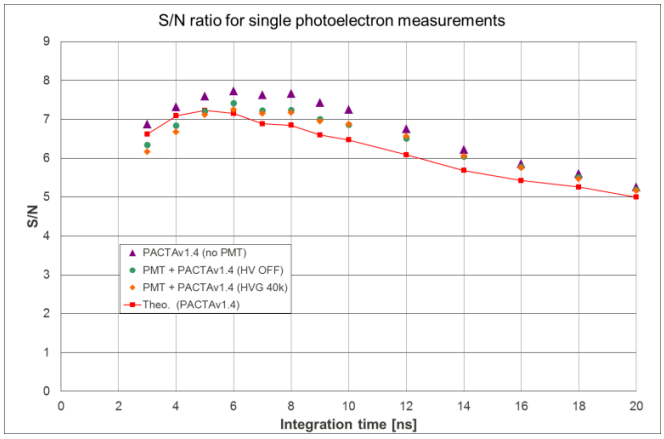


Figure 28. PACTAv1.4 S/N ratio for spe measurements with R_{in} 10k and Ln Off

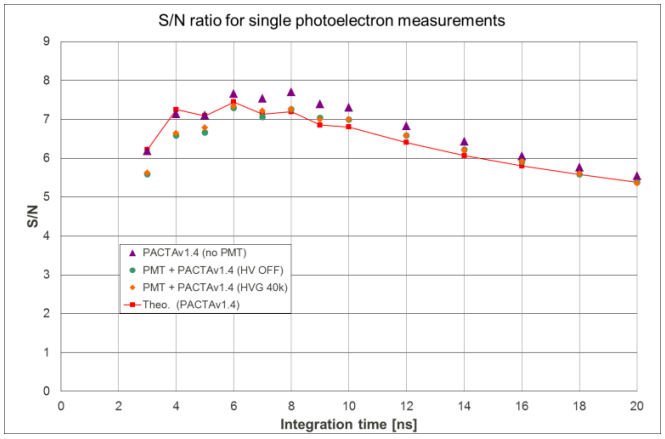


Figure 29. PACTAv1.4 S/N ratio for spe measurements with no R_{in} and Ln Off

Note: Measured with PMT R11920 (serial number ZQ1871) from Hamamatsu at 40k gain (812V).

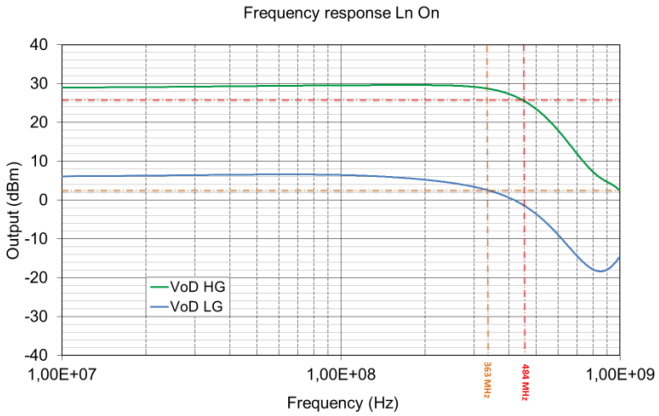


Figure 30. PACTAv1.4 frequency response test with R_{in} 15k and Ln On

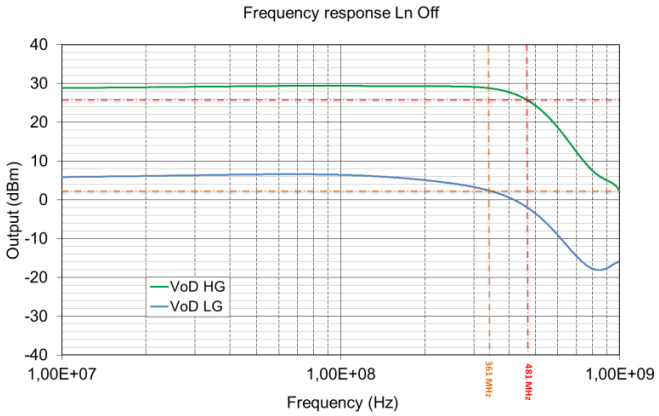


Figure 31. PACTAv1.4 frequency response test with R_{in} 15k and Ln Off

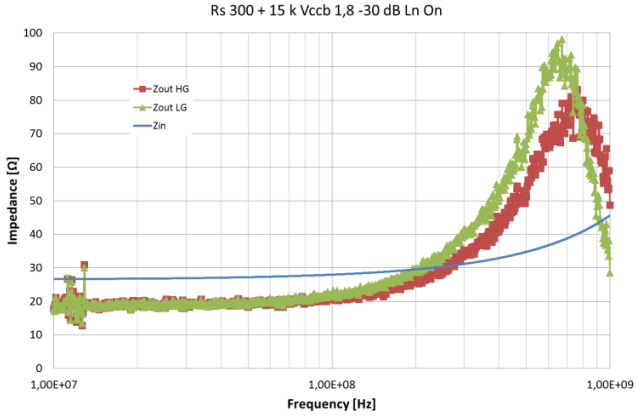


Figure 32. PACTAv1.4 Impedance test with R_{in} 300 + 15k and Ln On

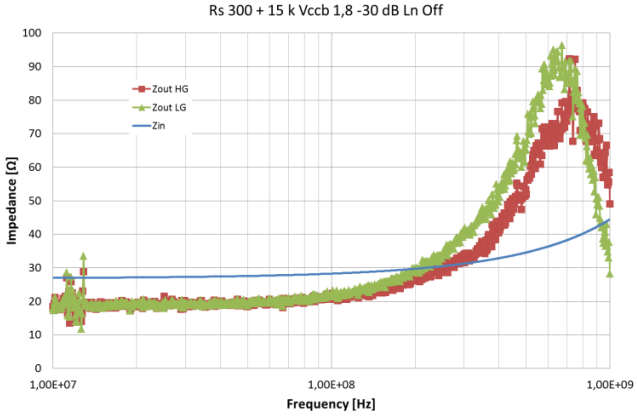


Figure 33. PACTAv1.4 Impedance test with R_{in} 300 + 15k and Ln Off

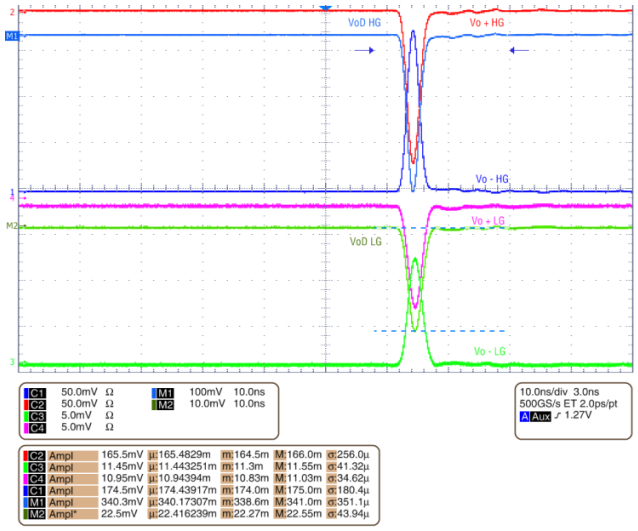


Figure 34. PACTAv1.4 shape measurements with a negative pluse at the I- input. V_oD is optained by $(V_o+) – (V_o-)$

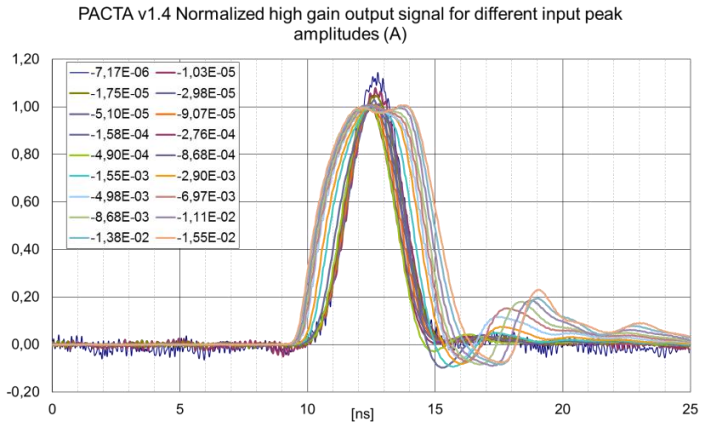


Figure 35. PACTAv1.4 shape measurements with 15k R_{in} and Ln On at HG (Normalized)

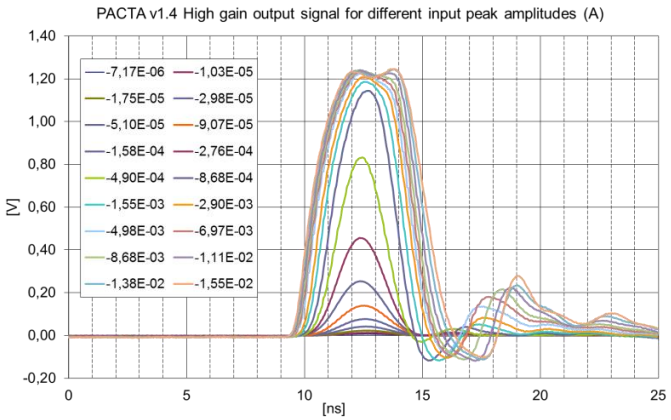


Figure 36. PACTAv1.4 shape measurements with 15k R_{in} and Ln On at HG (No Normalized)

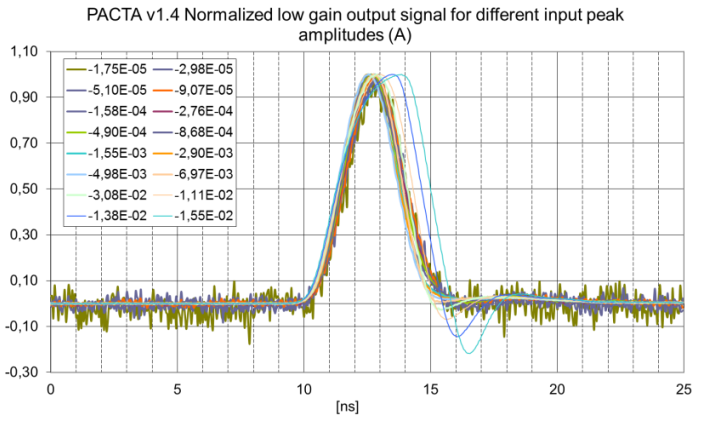


Figure 37 PACTAv1.4 shape measurements with 15k R_{in} and Ln On at LG (Normalized)

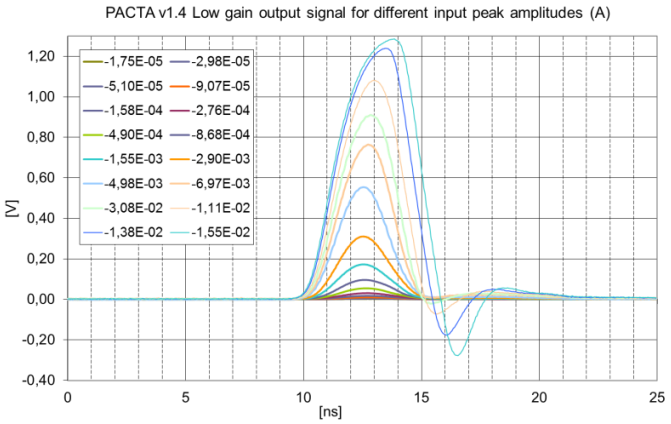


Figure 38. PACTAv1.4 shape measurements with 15k R_{in} and Ln On at HG (No Normalized)

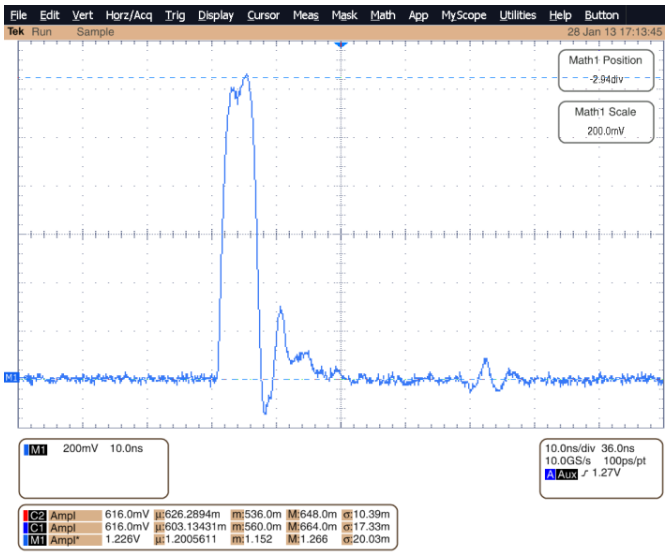


Figure 39. PACTAv1.4 Saturation recovery measurements (16 mA peak input pulse) with 15k R_{in} and Ln On at HG (No Normalized)

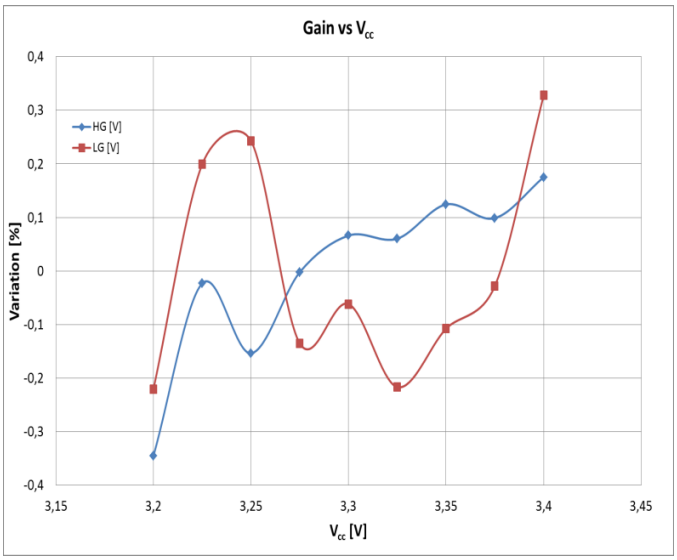


Figure 40. PACTAv1.4 Gain variation as a function of Power supply with 15k R_{in} and Ln On at HG

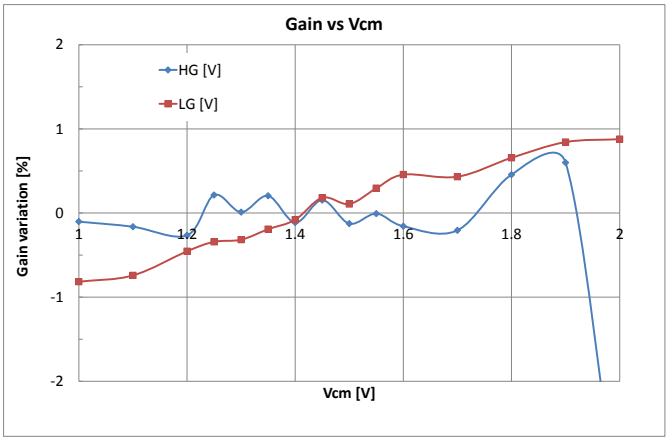


Figure 41. PACTAv1.4 Common Mode variation vs Gain with 15k R_{in} and Ln On at HG

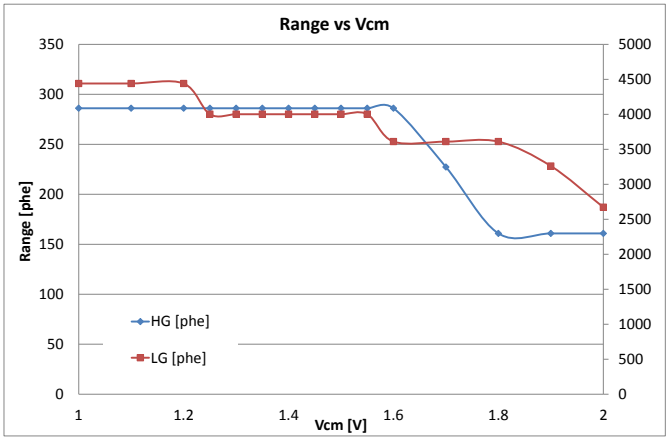


Figure 42. PACTAv1.4 Common Mode variation vs Range with 15k R_{in} and Ln On at HG

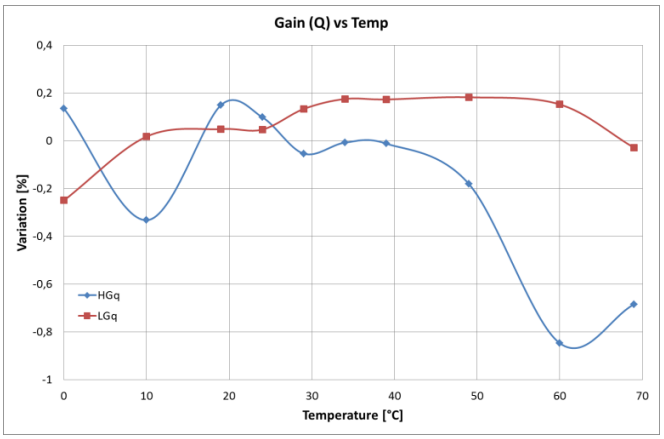


Figure 43. PACTAv1.4 Gain (Q) vs Temperature variation with 15k R_{in} and Ln On

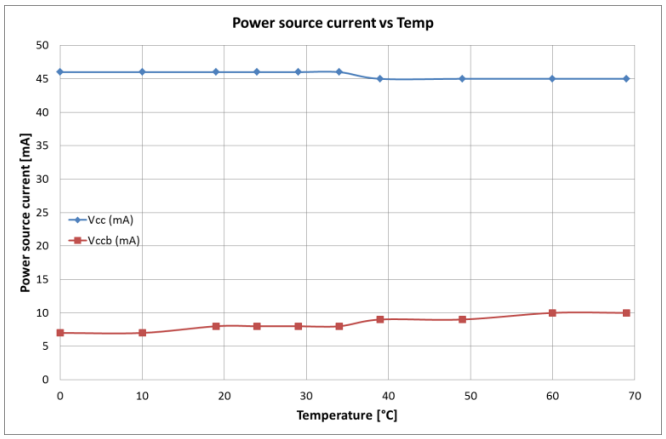


Figure 44. PACTAv1.4 Power source current vs Temperature variation with 15k R_{in} and Ln On

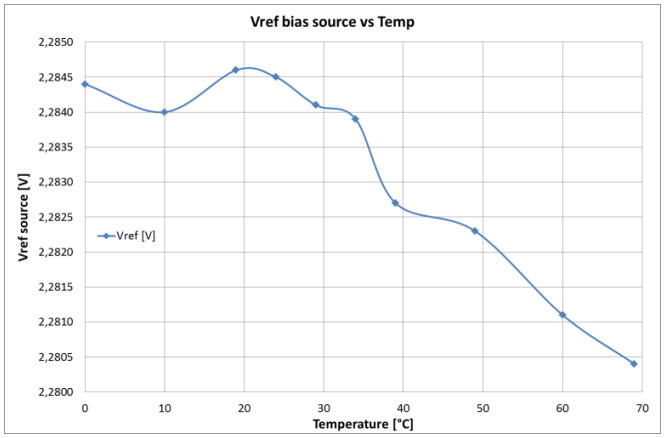


Figure 45. PACTAv1.4 V_{ref} bias voltage source reference vs Temperature variation with 15k R_{in} and Ln On

APPLICATIONS INFORMATION

Voltage Reference

The PACTAv1.4 generates an internal voltage reference to provide the required bias voltage sources at the V_{ref} output (typically 2,27V). Just a resistance network is needed to generate the different reference values: V_{casbip} is typically fixed to 2V. V_{cm} provides the common voltage at the output (typ. 1,33V). V_{Rdmp} typically 1,25V and V_{casp} is typically fixed to 1,19V.

A servo control loop controls the operating point of the output stage: (V_{bef}) is connected to the V_{befR} (typ. 2,2V) and a de-coupling capacitor (1nF) is used to stabilize the output reference.

It is recommended to use resistors with low temperature coefficient (and equal between the different resistors inside the V_{ref} network) to avoid temperature variation effects. Values of ±100ppm/ºC or bellow will be enough to avoid the temperature dependence.

V_{bef}(V)	V_{Casp}(V)	V_{Rdmp}(V)	V_{cm} (V)	V_{casbip}(V)	V_{ref}(V)
2,2	1,19	1,25	1,33	2	2.27

Bias Current Reference

The PACTAv1.4 is biased by using four different current sources. I_{b0z} and I_{b20z} are the input stage bias current configuration and are typically fixed to 180 µA by using a resistor of 6,65kΩ respectively. I_{bTIA} biases the TIA output stage and it is typically fixed to 330 µA by using a resistor of 3,6kΩ. I_{bABf} configures the OPAMP output stage and it is typically fixed to 605 µA by using a resistor of 1,96kΩ.

It is also recommended to choose resistors with low temperature coefficient like the voltage reference resistor network.

$I_{b\ 0z}$ (µA)	$I_{b\ 20z}$ (µA)	$I_{b\ cas}$ (µA)	$I_{b\ ABf}$ (µA)
180	180	330	600

Low Noise Mode Selector

An intrinsic noise reduction of 10% can be obtained by connecting the Ln pin to V_{cc}. This noise reduction also implies a bandwidth reduction only at the unused input. In certain scenarios with high pick-up noise, better results might be obtained with LN Off.

Power Supply Distribution

The power distribution is based on a V_{cc} (+3.3V) and V_{ccb} (+1.8V). A decoupling capacitor network is used to filter the noise at the power supply. Place the lower values (1nF at each V_{cc} and V_{ccb} pin) as close as possible to the amplifier in order to minimize the inductance of the path from ground to the power supply. Intermediate capacitor values (10nF and 100nF) are mounted between the device and the power source connector. Using the same package (0603 case) for all of these capacitors reduces the inductive performance of the decoupling circuit. Add tantalum capacitor (10µF) close to the power connector to minimize and filter the low frequency variations. A solid power plane reduces the resonances in the needed frequency range. The QFN32 package uses a central pad as a thermal pad, but in the PACTAv1.4 case, it is also used to ground the ASIC by using down bonds wires in order to minimize the bonding wire inductance. Place vias in the thermal pad to obtain a direct connection to the ground plane.

In order to obtain the V_{ccb} (1.8 V) power supply from the V_{cc} (3.3 V) power source, it is recommended to use a low cost (and small package) linear regulator ADP161 as it is depicted in figure 59.

It is highly recommended to limit the current of the power supply following the next table.

	V_{cc}	V_{ccb}
Voltage (V)	3.3	1.8
Current limit (mA)	50	10
Typical Current (mA)	40	4.9

Input

Each PACTAv1.4 input requires an AC coupling. Use four optionally capacitors in parallel (100pF, 1nF, 10nF and 100nF) to get a wide bandwidth frequency range at each input signal pin for high precision performances. The differential PACTA have a double input signal (I+ and I-), but it is only used the I- one and **the input signal must be a negative pulse**. It can be optionally mounted a resistor (typ. 15 kΩ) to ground at each input pin to fine tuning adjusts the tradeoff bandwidth versus noise. The bandwidth and the noise is inversely proportional to the resistor values. The minimum resistor recommended value is 15 k Ω, lower values does not produce further bandwidth increases.

Rin [Ω]	HG BW [MHz]	Noise [phe]
∞	417	4393
15 k	484	4704
10 k	476	4716

Output

The differential outputs (HG and LG) are a low impedance output. Each one requires also AC coupling (like the AC coupling circuit for the input signals). If there is any unused output, this must be terminated by a 50 Ω termination. This amplifier configuration is a Non-Inverted configuration, so a negative pulse at the I- input generates a negative pulse at the V_o + HG (also at the V_o + LG) output signal. And also it generates a positive pulse at the V_o - HG (also at the V_o - LG) output signal. This must be taken into account in order to select the correct V_oD configuration.

Input Selector Circuit

If it is required a test pulse, it implies to add an input selector circuit to choose between the test pulse (for calibration purposes) and the signal pulse (PMT). It is recommended to use a SPDT as an input selector (AS169). The typical circuit schematic for a SPDT is described in figure 55 and figure 56.

Test Pulse Circuit

Typical circuit is shown in Figure 57.

Accurate Pulse Injector

For accurate measurements (and characterization), a high output impedance source is used (figure 58).

Wire Length input effect

In figure 54 (b), it is showed a possible connection configuration where the PMT and the preamplifier are mounted in separated boards and the connection between them is performed by using a coaxial cable. In this configuration, it is recommended to not exceed a length of 8cm.

In order to provide a line termination, it is recommended to add a series resistor of 27 Ω. Some small reflection can be noticed as it is showed in figure 46 and figure 47; however linearity (figure 48, 49, 50 and 51) and frequency response (figure 52) are still within the specifications both with and without the series resistor. If the signal is integrated for < 10 ns the difference with and without this series resistor is small. If more complex digital signal processing is performed there could be some differences.

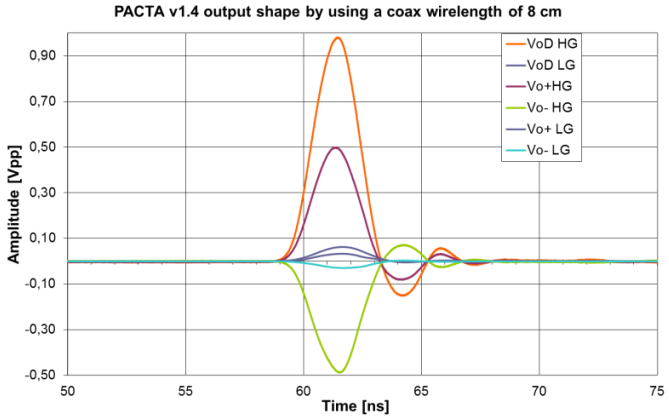


Figure 46. PACTAv1.4 pulse shape by using a coax wire of 8 cm at the input with 15k R_{in} and Ln On

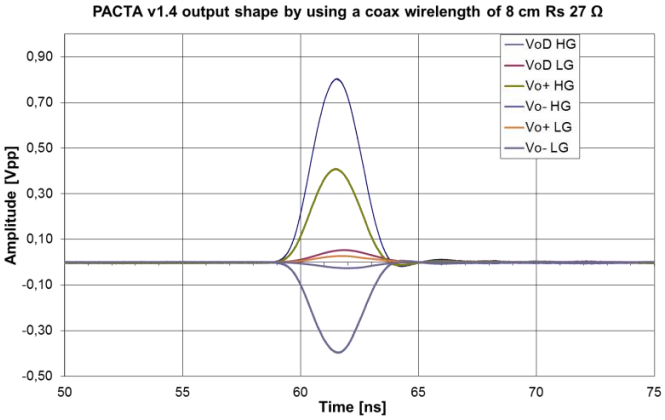


Figure 47. PACTAv1.4 pulse shape by using a coax wire of 8 cm at the input and a series resistor of 27 Ω with 15k R_{in} and Ln On

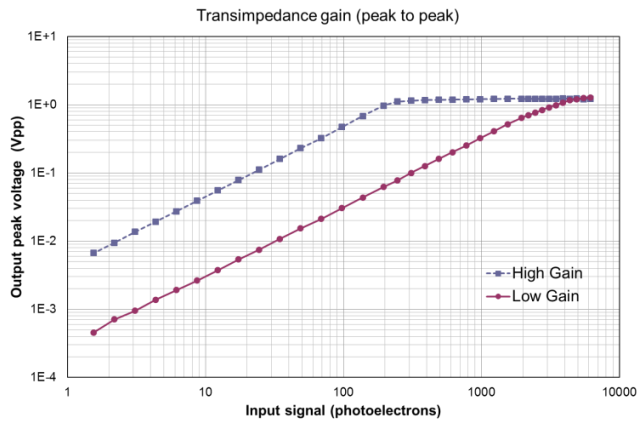


Figure 48. PACTAv1.4 Linearity test by using a coax wire of 8 cm at the input with 15k R_{in} and Ln On

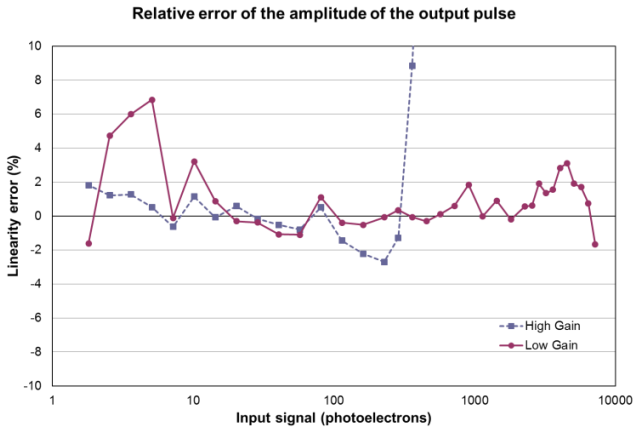


Figure 49. PACTAv1.4 Linearity relative error by using a coax wire of 8 cm at the input with 15k R_{in} and Ln On

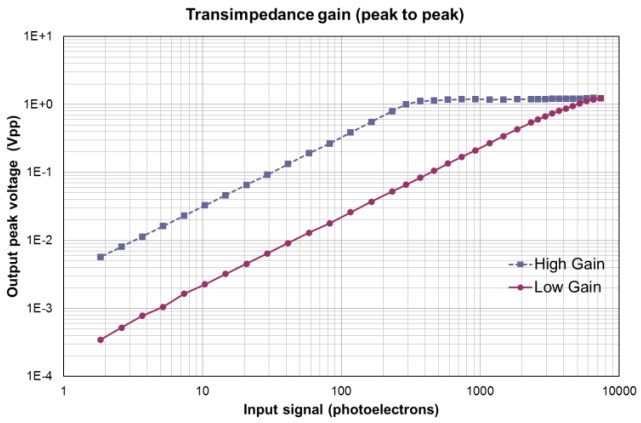


Figure 50. PACTAv1.4 Linearity relative error by using a coax wire of 8 cm at the input and a series resistor of 27 Ω with 15k R_{in} and Ln On

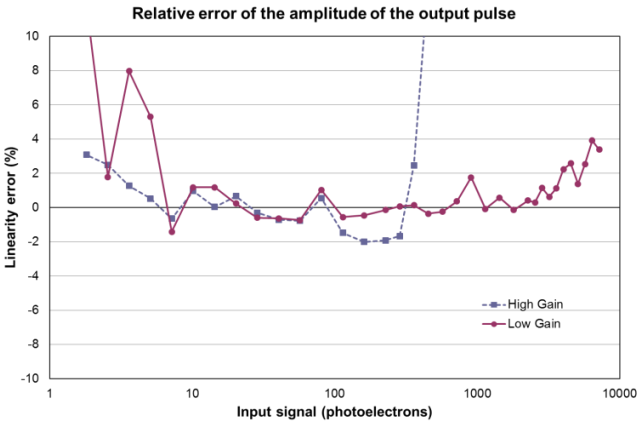


Figure 51. PACTAv1.4 Linearity relative error by using a coax wire of 8 cm at the input and a series resistor of 27 Ω with 15k R_{in} and Ln On

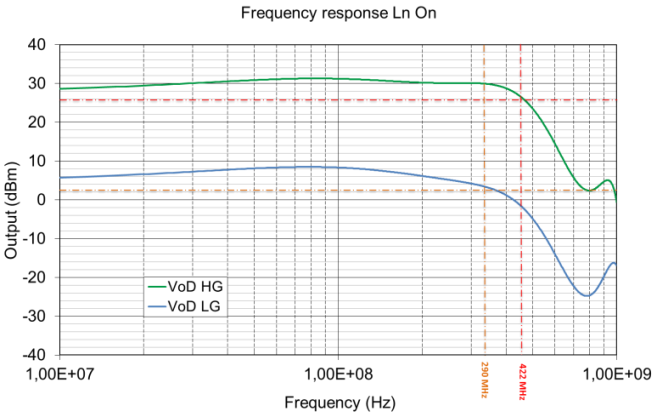


Figure 52. PACTAv1.4 Frequency response test by using a coax wire of 8 cm at the input with 15k R_{in} and Ln On

TYPICAL APPLICATION CIRCUITS

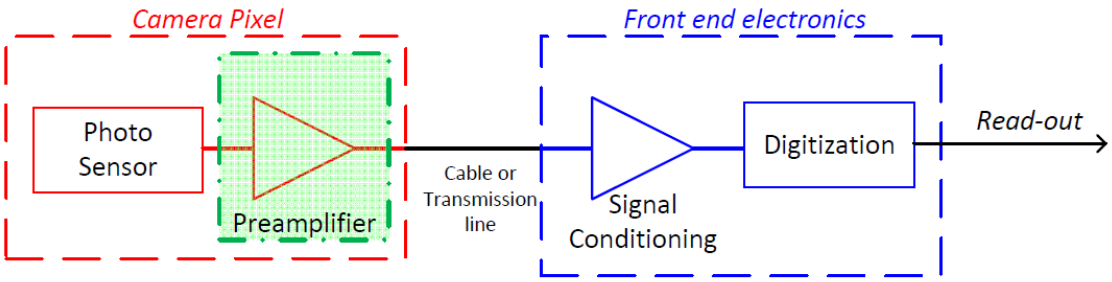


Figure 53. PACTAv1.4 typical application circuit diagram

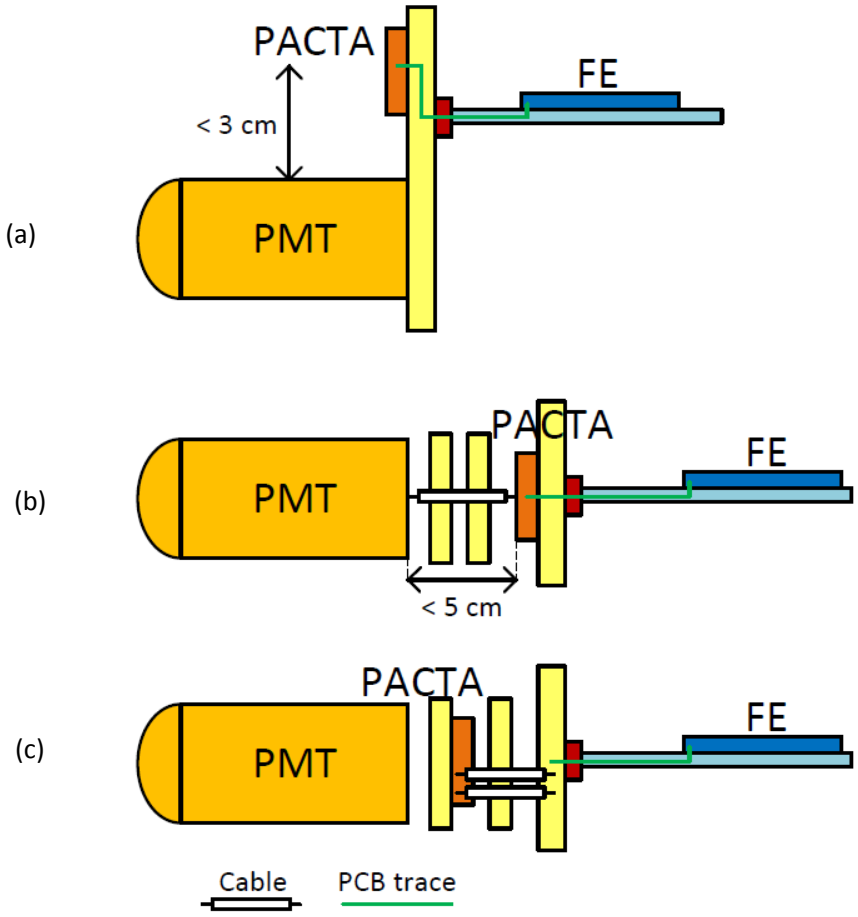


Figure 54. PACTAv1.4 typical connection possibilities for the PMT and the frontend electronics (FE)

Note:

Figure 52 (a) corresponds to a connection possibility where the PMT and the amplifier is placed at the same pcb (by using pcb track shorter than 3 cm). The output of the amplifier is connected to the FE part by using pcb tracks and connectors.

Figure 52 (b) corresponds to a connection possibility where the PMT and the amplifier is connected by using a coax wire shorter than 5 cm. The output of the amplifier is connected to the FE part by using pcb tracks and connectors.

Figure 52 (c) corresponds to a connection possibility where the PMT and the amplifier is placed at the same pcb. The output of the amplifier is connected to the FE part by using pcb tracks and connectors and 50Ω coax wires. Used configuration for the characterization results in this document

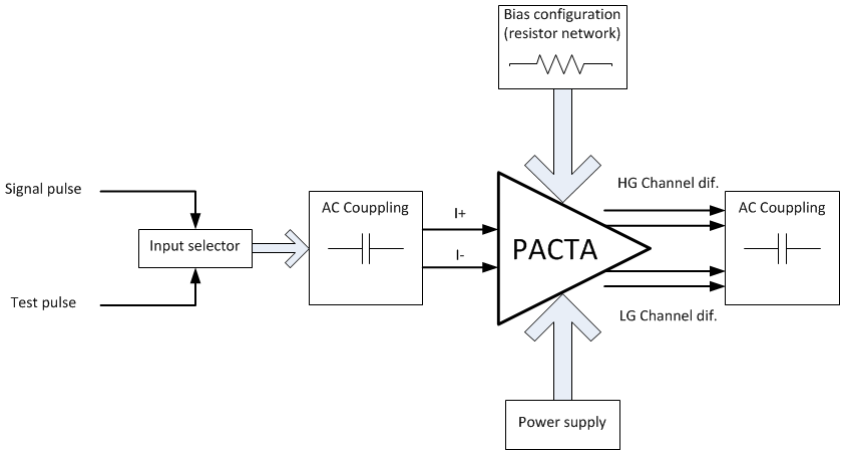


Figure 55. Input selector circuit recommendation. Use a SPDT as an input switch (AS169)

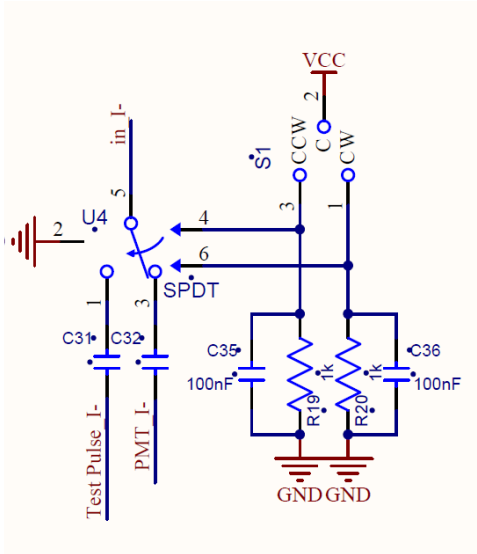


Figure 56. AS169 SPDT schematic as an input selector (input SPDT coupling capacitors of 100nF)

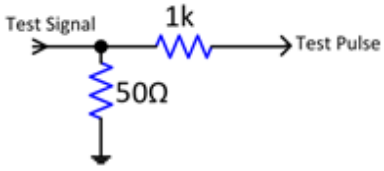


Figure 57. Test pulse schematic

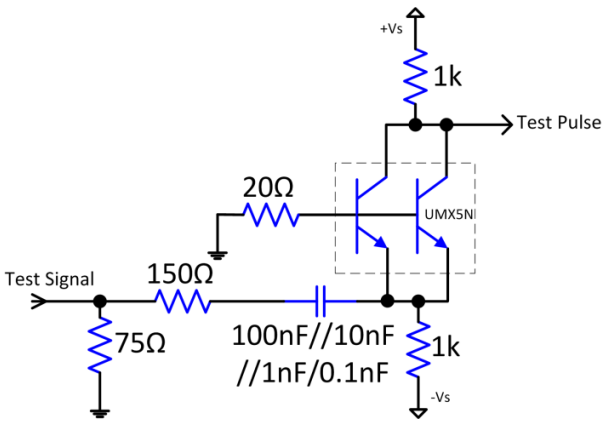


Figure 58. Accurate pulse injector (±Vs = ±6.5 V)

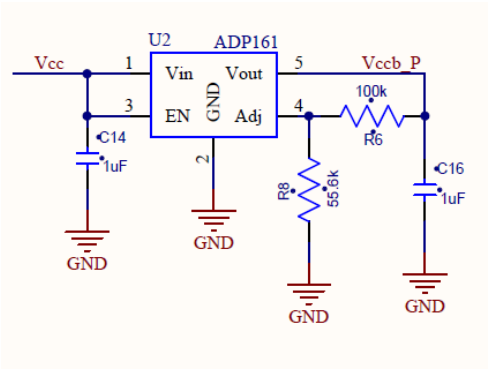


Figure 59. V_{ccb} power source generation

LAYOUT

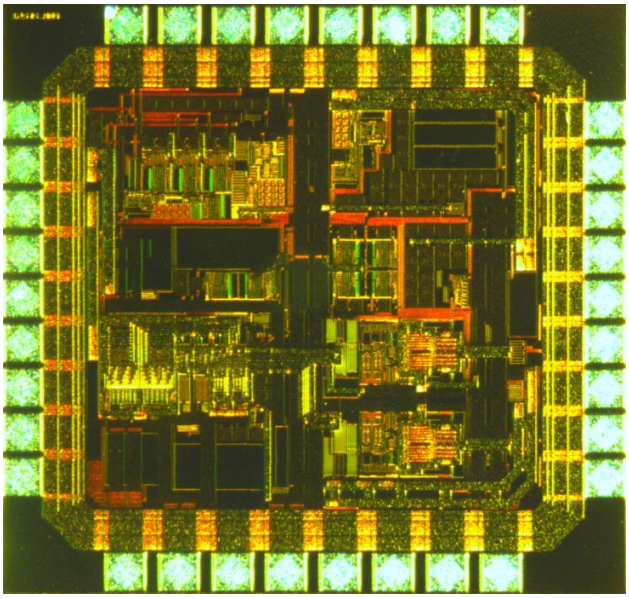


Figure 60. PACTAv1.4 Layout picture

BONDING DIAGRAM

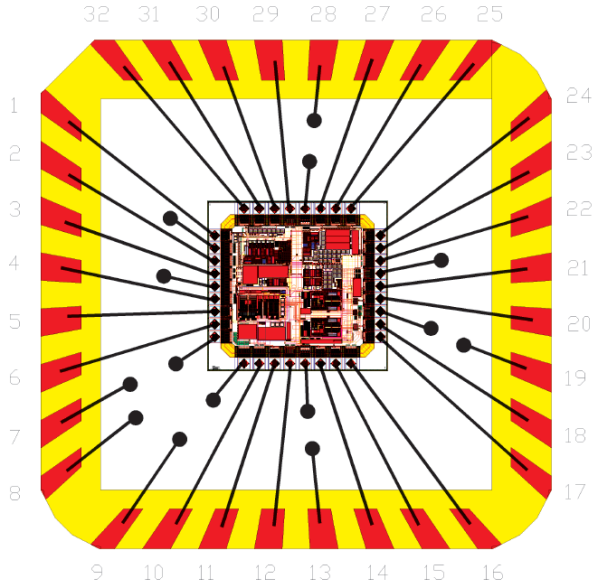


Figure 61. PACTAv1.4 Bonding Diagram with the DIE ground pads connected to the central package pad.

OUTLINE DIMENSIONS

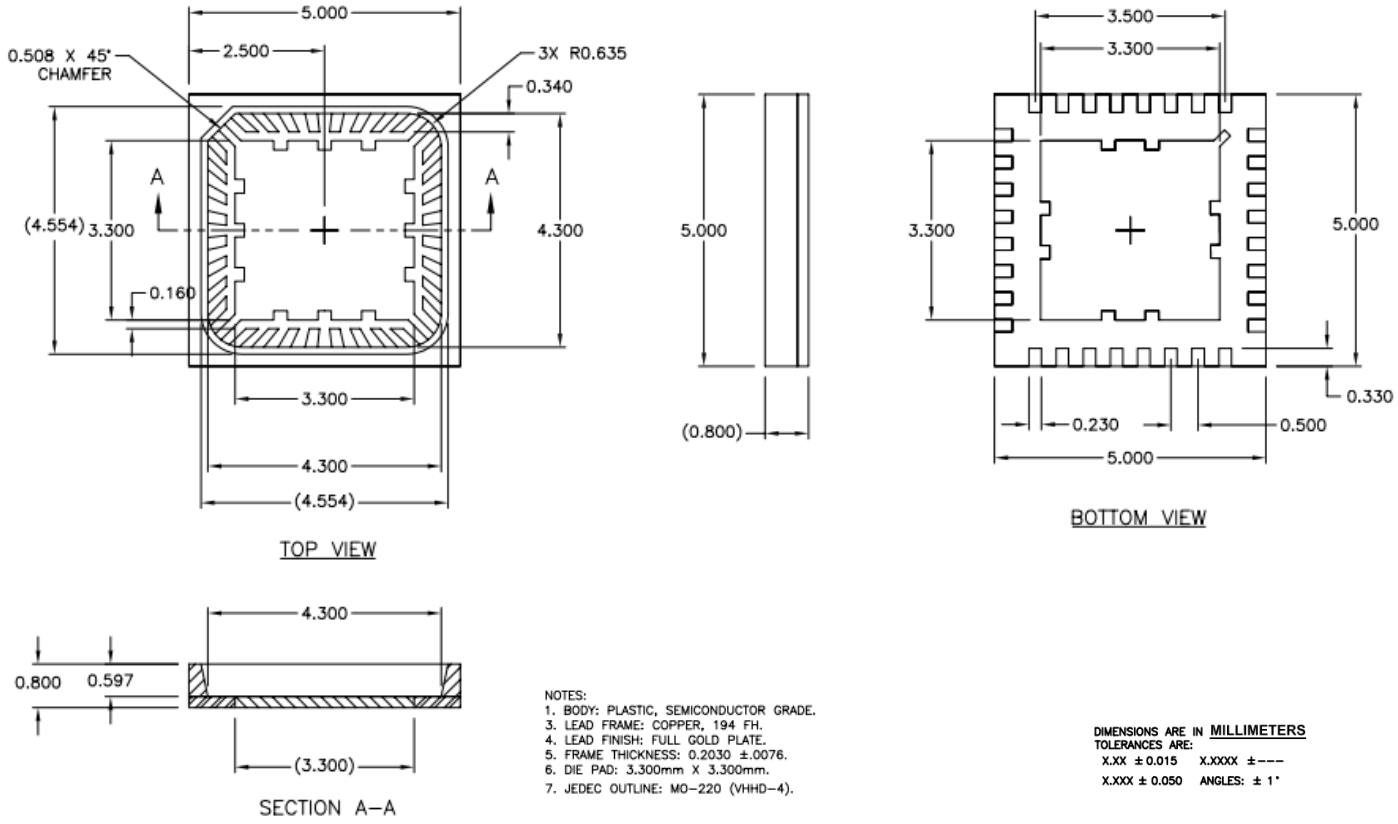


Figure 62. 32-Lead Lead Frame Chip Scale Package [QFN]
5 mm × 5 mm Body, Very Thin Quad (CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range[1]	Package Description[2]	Package Option
PACTAv1.4	−40°C to +125°C	32-Lead QFN	CP-32-7

[1] Temperature range for the ASIC technology used. To be tested at the next document revisions.
[2] Package dimensions without Lid (5 x 5 mm and 0.800 mm thickness).
[3] Lid dimensions (5 x 5 mm and 0.200 mm thickness).

NOTES

B

Appendix ACTA Datasheet

Institut de Ciències del Cosmos

Triple gain path per channel with two channels, controlled by slow control interfaces (SPI) amplifier for photodetector readout

Data Sheet **ACTAf 2Ch**

FEATURES

Triple gain path per channel
Low output impedance stage with cable and transmission line driving capabilities (only for the trigger branch)
Fully differential input/output
Low power consumption, 462 mW at 3,3V supply

APPLICATIONS

Photodetectors readout

GENERAL DESCRIPTION

The ACTAf 2Ch is a fully differential, triple branch amplifier.

The ACTAf 2Ch is developed by using the Austria Micro Systems (AMS) 0.35 µm CMOS technology and operates over the -40ºC to +125ºC junction temperature range.

The ACTAf 2Ch is available in a 48-QFN package.

TYPICAL APPLICATION CIRCUIT

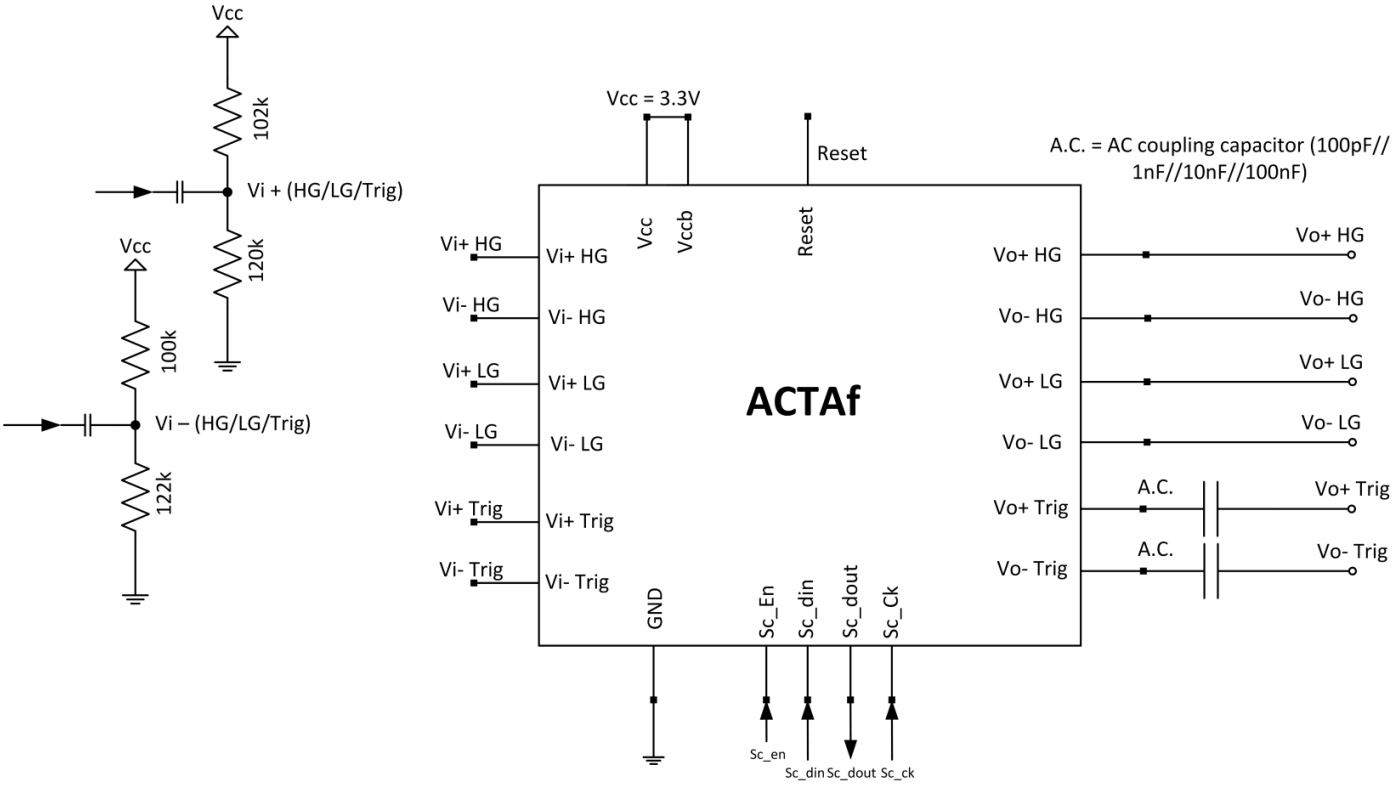


Figure 1. ACTAf 2Ch Typical application circuit

Rev. 1

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Tel: 93.40.21588
Fax: 93.40.21241
icc.ub.edu

TABLE OF CONTENTS

REVISION HISTORY

11/15—Revision 1: Small Corrections
12/13—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

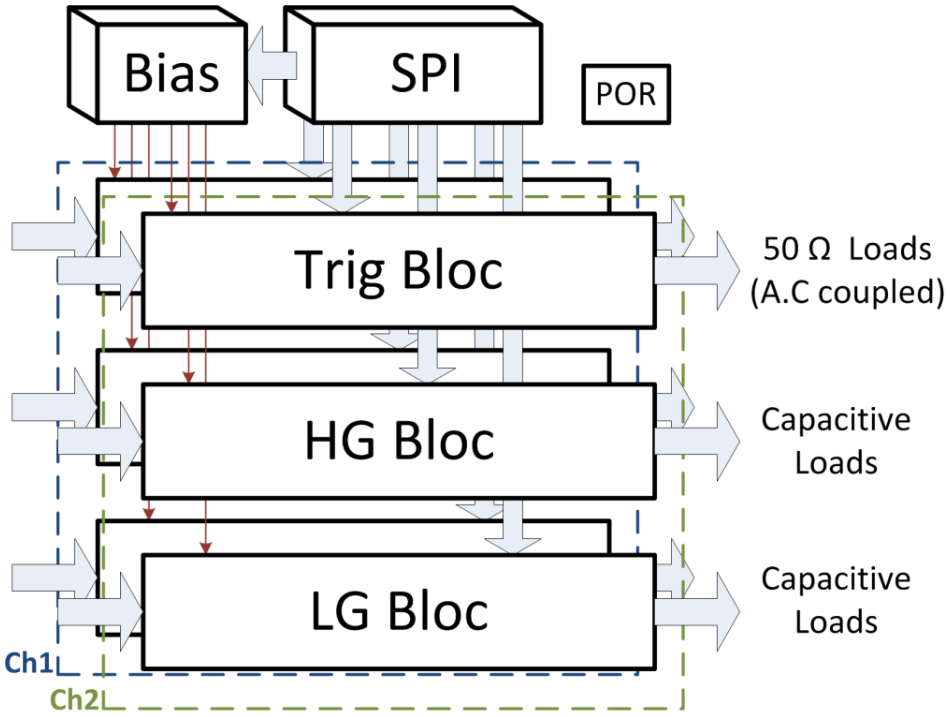


Figure 2. ACTAf (2 Ch) Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Table 1.

Parameter	Rating
V_{CC}	3.2 V to 3.4 V
Temperature Range	
Operating (Junction)	−40°C to +125°C
Storage	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Boundary Condition

θ_{JA} is measured using natural convection on a JEDEC 4-layer board, and the exposed pad is soldered to the printed circuit board (PCB) with thermal vias.

Table 2. Thermal Resistance

Package Type	θ_{JA}	Unit
48-Lead QFN (2 Ch version)	TBC [1]	°C/W

[1] To be confirmed.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

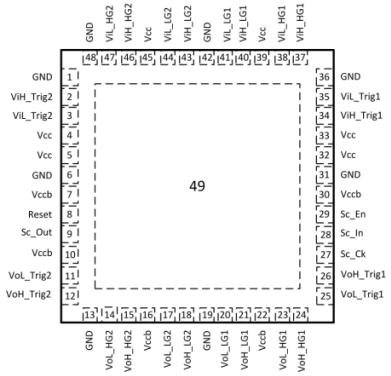
SPECIFICATIONS

T_A = +25°C, V_{cc} = 3.3 V unless otherwise noted.

Table 3.

Parameters	Conditions [1]	Min	Typ	Max	Units
DYNAMIC PERFORMANCE	HG Branch		484		MHz
Bandwidth (-3 dB)	LG Branch		417		MHz
	Tg Branch		361		MHz

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



48-LEAD (7mm x 7mm) PLASTIC QFN

NOTES 1. THE EXPOSED PAD (PIN 49) IS GND, SHOULD BE SOLDERED TO AN EXTERNAL GND PLANE.

Figure 3. ACTAf (2 Ch) Pin Configuration (Top View)

Table 4. ACTAf (2 Ch) Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6, 13, 19, 31, 36, 42, 48, Exposed Pad	GND	Ground. Exposed Pad in internally connected to GND and must be soldered to a low impedance ground plane.
2	$V_{IH\ Tg\ 2}$	Differential Input.
3	$V_{IL\ Tg\ 2}$	Differential Input.
4, 5, 7, 10, 16, 22, 30, 32, 33, 39, 45	V_{cc}	Positive 3,3 V power supply. $V_{cc} = V_{ccb}$
8	Reset	Active High.
9	Sc_{Out}	SPI SDO
11	$V_{OL\ Tg\ 2}$	Differential Output. Typically ac-coupled.
12	$V_{OH\ Tg\ 2}$	Differential Output. Typically ac-coupled.
14	$V_{OL\ HG\ 2}$	Differential Output.
15	$V_{OH\ HG\ 2}$	Differential Output.
17	$V_{OL\ LG\ 2}$	Differential Output.
18	$V_{OH\ LG\ 2}$	Differential Output.
20	$V_{OL\ LG\ 1}$	Differential Output.
21	$V_{OH\ LG\ 1}$	Differential Output.
23	$V_{OL\ HG\ 1}$	Differential Output.
24	$V_{OH\ HG\ 1}$	Differential Output.
25	$V_{OL\ Tg\ 1}$	Differential Output. Typically ac-coupled.
26	$V_{OH\ Tg\ 1}$	Differential Output. Typically ac-coupled.
27	Sc_{Clk}	SPI Clok
28	Sc_{In}	SPI SDI
29	Sc_{En}	SPI CS. Active High.
34	$V_{IH\ Tg\ 1}$	Differential Input.
35	$V_{IL\ Tg\ 1}$	Differential Input.
37	$V_{IH\ HG\ 1}$	Differential Input.
38	$V_{IL\ HG\ 1}$	Differential Input.
40	$V_{IH\ LG\ 1}$	Differential Input.
41	$V_{IL\ LG\ 1}$	Differential Input.
43	$V_{IH\ LG\ 2}$	Differential Input.
44	$V_{IL\ LG\ 2}$	Differential Input.
46	$V_{IH\ HG\ 2}$	Differential Input.
47	$V_{IL\ HG\ 2}$	Differential Input.

SLOW CONTROL SERIAL LINK

Generalities

The serial link permits to control and configure the ACTAf 2Ch chip including:

- The bias current configuration.

For these purposes, the link can access in write or not destructive read to up to 15 registers (with address codes on 7 bits) of various depth.

Initialization

With the powering, an internal device delivers a reset pulse (about 1 ms of duration) to all the registers.

Serial Link Description

The link uses 4 signals with a CMOS level [0V; 3.3V]:

- Sc_din [pin Nº 28]: input data of the serial link.
- Sc_ck [pin Nº 27]: clock of the serial link.
- Sc_en [pin Nº 29]: enable of the serial link.
- Sc_dout [pin Nº 9]: output data of the serial link.

The **Sc_din**, **Sc_ck** and **Sc_dout** may be shared between several ACTAf chips.

Sc_en should be provided individually for each ACTAf chip.

The serial link is sequenced on the **FALLING EDGE** of **Sc_ck**: input data are sampled and read/write operations are made on this edge.

For safe operation, the **Sc_din** and **Sc_en** should change at least 10ns before the falling edge of **Sc_ck** (*Setup Time*) and remain stable (*Hold Time*) 15ns after this edge.

The general data packet is defined as following:

$$[r/w\ b][Ad_6 \ldots Ad_0][D_{NBD-1} \ldots D_0]$$

Where the first bit defines the type of operation:

- r/w b = 1 : slow control read.
- r/w b = 0 : slow control write.

$[Ad_6 \ldots Ad_0]$ is the address (defined on 7 bits) of the register the user wants to access.

$[D_{NBD-1} \ldots D_0]$ are the **NBD** data bits of the frame.

The most significant bit (MSB) of address or data is always sent (or read) first.

- The **Sc_en** signal defines the slow control frame sent on **Sc_din**. It rises to high level simultaneously with the [r/w b] on **Sc_din** and returns to 0 one cycle of **Sc_ck** after the last D_0 data bit has been sent on **Sc_din**. The frame includes 8+**NBD** falling edges of **Sc_ck**.
- At the end of the frame, at least 4 negative edges of **Sc_ck** are absolutely necessary after the falling edge of **Sc_en**.

Outside the frames:

- The **Sc_dout** output is a high impedance (idle state)
- The **Sc_ck** signal is ignored by the slow control link and can be take any level.

Synchronization of the output data

By default, the data sent on the **Sc_dout** pin are synchronized locally (by the block generating them) on the falling edge of **Sc_ck**. Due to the time skews on the chip, this synchronization is not perfect and can be a limit for very high rate slow control operations. It is possible to resynchronize the data just at the **Sc_dout** level by setting *SynchroOut* to 1, this means the bit 9 of register 1 (regiter address 97 for the channel 1 and register 104 for channel 2). As it is an extra synchronization, it adds some extra delay to the data signal. The **Sc_ck** edge used for this synchronization can be selected using *OutsynchroCkb*, this means the bit 10 of the register 1 (regiter address 97 for the channel 1 and register 104 for channel 2). If it is set to 1, the synchronization is permormed on the falling edge of **Sc_ck** otherwise the rising edge of **Sc_ck** is used.

All the following chronograms are corresponding to the SynchroOut = 0 case.

Slow Control Write Operation

This operation is initiated if **r/w b**, the first bit of the frame is equal to 0.

The write operation is divided in two phases; the first one is the transmission of the target register address coded on 7 bits (fixed duration). And the second one is the data writing in the target register (variable duration according to the register depth).

At the falling edge of **Sc_en**, the **NBD** last bits sent on **Sc_din** are written in the target register defined by the address (bit 1 to 8 of the frame).

Eight **Sc_ck** falling edges after the start of the frame, the **Sc_dout** output leaves the idle state *(HiZ)*. Then during the **NBD** clock cycles, it takes the state $Y_{<NBD:1>}$ depending of the history of the link. After it reproduces the data on **Sc_din** with a latency of **NBD Sc_ck** cycles ($A_{<0>}$, $D_{<NBD-1>}$, $D_{<NBD-2>}$). **Sc_dout** enters in *HiZ* state 3 **Sc_ck** rising edges after the **Sc_en** falling edge. After this, one extra clock cycle is necessary to finish the operation.

Special case of register 0

The register with address 96 (Register 0) does not physically exist. But when it is addressed, the **Sc_dout** becomes a direct copy (without any latency) of the **Sc_din** input. The rules for the end of frame are the same as for a standard write operation. This can be used for debugging or chaining chips.

Slow Control Read Operation

The read operation is initiated if the first bit of the data frame (**r/w b)** is set to 1.

The read operation is divided in two phases; the first one is the transmission of the target register address coded on 7 bits (fixed duration). And the second one is the data reading of the target register (variable duration according to the register depth).

The bits following the address sent on **Sc_din** are dummies and can take any value.

Eight **Sc_ck** falling edges after the start of the frame, **Sc_dout** leaves the *HiZ* state to take a dummy value (depending on the history of the link). On the next **Sc_ck** falling edges the data read from the register starts to appear (MSB first) on **Sc_dout** and this during **NBD Sc_ck** edges. After this, the data on **Sc_dout** should be ignored. At the end of the frame, the **Sc_en** falling edge must be followed by a minimum of 4 **Sc_ck** falling edges; **Sc_dout** goes to *HiZ* after the 3rd one.

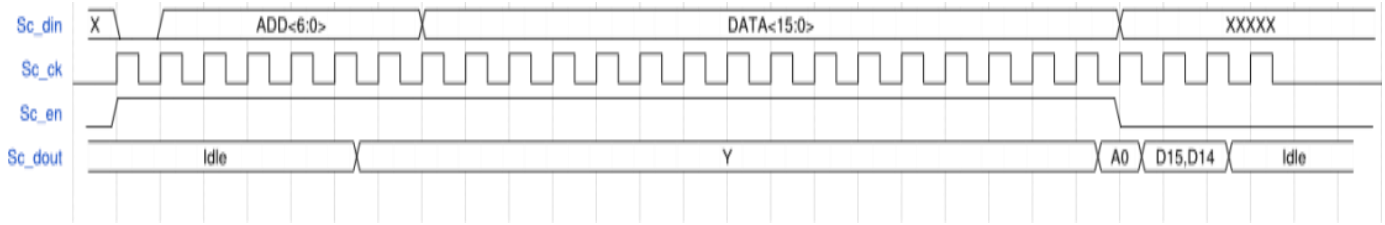


Figure 4. ACTAf v1.23 Slow Control Write frame

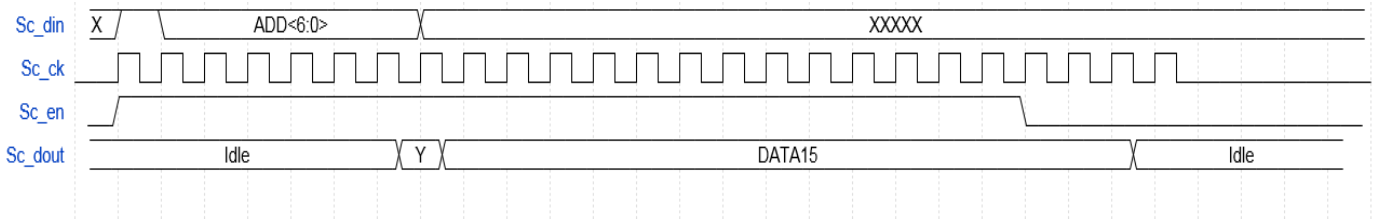


Figure 5. ACTAf v1.23 Slow Control Read frame

Configuration of bias currents

Next current values are extracted from simulation of blocks without DACs (with ideal current sources or cccs based on reference current (NTC, PTC, etc)).

Range (max value) is computed with 30% margin for process variations.

Table 5. Bias currents values and ranges

Current	Ch / Glb ?	SA RO (µA)	SA Trig (µA)	Current Master	Range (µA)	Res. (bits)	Comments
Ibgm	Global	436.6	436.6	TC0	621	6	Ref is 1 TC0 output (11 µA). vcc, gnd Voltage link. ****
Is	Global	48.5	48.5	TC0	(69)	-	Ref is 1 TC0 output (11 µA). vcc, gnd Current link. **** Only 3 MSB are set: control Vbias of FloatV, but Vbias is difference Icf-Is. Icf, already controlled, don't need to control Is. It is better to have locally in Ch and have a current link (HF noise).
Icf	Ch	139.2	139.2	PTAT	196	6	Ref is 1 PTAT output (160 µA). vcc, gnd Current link. ****
Ibof	Ch	74/100 *	21 **	NTC	RO: 90 / 120 *** Trig: 30 $_{NOOFC}$	6	Ref is 4 NTC shorted (140 µA). vcc, gnd Current link. **** Maximum current for trigger is limited by smaller resistor width to achieve BW. Linearity still ok, not limited by VoDGm.
IbSF	Ch	120	120	PTAT	165	6	Ref is 1 PTAT output (160 µA). vcc, gnd Current link. ****
Ib_AOP	Global	27.75	-	TC0	39.73	6	Ref is 1 TC0 output (11 µA). vcc, gnd Current link (local master vccb and gndb). ****
Ib_ABF	Global	-	420	PTAT	561	6	Ref is 1 PTAT output (160 µA). vcc, gnd Current link (local master vccb and gndb). ****

* Ibof = 68 µA for LG = 1 and with external offset (input resistor Rof). If there is no input resistor Rof, Ibof = 100 µA.

** Those values for Ibof are for LG = 0. Worst case in terms of resolution. If $Ibof_{max}$ is set to 68 x 1.30 = 88 µA, resolution is 1.4 µA (6 bits DAC). For SA_RO is good: 1.4 / 68 = 2 % (17 mV for offset of 850 mV). For SA_Trig is not good (1.4 / 21 = 6.6 %), but it will be AC coupled so, no problem.

*** The range should be selected by additional control bit "OFC" of the scaling mirror after DAC in each channel. Not for trigger, because width of resistor is smaller in order to achieve BW: current must be limited.

**** Scaling mirrors translate reference current to required range.

Registers table

After initialization, all the Slow Control registers are reset to their default value.

Table 6. ACTAf (2 Ch) Description of the registers

Register #	Width (bits)	Name	Default value (hex)	Access
96		Value used to test the serial link (Register 0)		W
97	16	Control / Debug register GLOBAL configurations (Register 1) CH 1	196D	¿?
98	16	Low Gain Register 1 (SA RO) CH 1	0D2D	¿?
99	16	Low Gain Register 2 (SA RO) CH 1	0B2E	¿?
100	16	High Gain Register 1 (SA RO) CH 1	0D2D	¿?
101	16	High Gain Register 2 (SA RO) CH 1	0B2E	¿?
102	16	Trigger Register 1 (SA Trig) CH 1	0B6D	¿?
103	16	Trigger Register 2 (SA Trig) CH 1	0BEE	¿?
104	16	Control / Debug register GLOBAL configurations (Register 1) CH 2	196D	¿?
105	16	Low Gain Register 1 (SA RO) CH 2	0D2D	¿?
106	16	Low Gain Register 2 (SA RO) CH 2	0B2E	¿?
107	16	High Gain Register 1 (SA RO) CH 2	0D2D	¿?
108	16	High Gain Register 2 (SA RO) CH 2	0B2E	¿?
109	16	Trigger Register 1 (SA Trig) CH 2	0B6D	¿?
110	16	Trigger Register 2 (SA Trig) CH 2	0BEE	¿?

Control bits

Control bits. NP means not present.

Table 7. Control bits

Ctrl bit	Ch / Glb ?	SA RO default	SA Trig default	Comments
PD	Ch	0	0	Power down
BP	Ch	NP	NP	Bypass
BC	Ch	0	0	Bias control of transconductor. Increases bis current in case large external input offset.
LG	Ch	1*	0	Low Gain: sets smaller *Rf* in transconductor (high BW)
OFC	Ch	0	0	Sets full scale of **Ibof** DAC. 0 => 90 µA / 1 => 120 µA
LRd	Ch	0	NP	Sets lower damping resistor at SA_RO buffer output. Used for large capacitances (if BW is too small).
LB	Ch	NP	0	Limits BW at the output of gain block of SA_Tirg (SFs output). In case BW is too large, to prevent linearity problems.

***** Should be inverted (nLG) in SA_RO to have 0 as default value for everything.

Description of the Registers

Current DAC is based on pMOS switches, so, current switch conduces for 0V.

Input codes must be inverted, that means, the inverted output of configuration registers is used.

Also, the input codes must be inverted for "hardwired" bits (Is<2:0>) on Is DAC.

Table 8. Control / Debug register GLOBAL configurations (Register 1)

Register address 97 (default value 196D hex 0001100101101101 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15:11	5	-	-	00011	Chip version
10	1	OutsynchroCkb	-	0	Resynchronize output data of slow control serial link
9	1	SynchrOut	-	0	Resynchronize output data of slow control serial link
8:6	3	Is	5	101 (101)	Bias current: only 3 MSB are set (Is<5:3>). 3 LSBs are hardwired (Is<2:0> = 101)
5:0	6	Ibgm	45	101101	Bias current: 6 bits

Table 9. Low Gain register 1 (SA RO)

Register address 98 (default value 0D2D hex 0000110100101101 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15	1	-	-	0	Unused
14	1	OFC	-	0	Control bit
13	1	BP	-	0	Control bit
12	1	PD	-	0	Control bit
11:6	6	Ibof	52	110100	Bias current: 6 bits
5:0	6	Icf	45	101101	Bias current: 6 bits

Table 10. Low Gain register 2 (SA RO)

Register address 99 (default value 0B2E hex 0000101100101110 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15	1	-	-	0	Unused
14	1	BC	-	0	Control bit
13	1	LRd	-	0	Control bit
12	1	nLG	-	0	Control bit
11:6	6	Ib_AOP	44	101100	Bias current: 6 bits
5:0	6	IbSF	46	101110	Bias current: 6 bits

Table 11. High Gain register 1 (SA RO)

Register address 100 (default value 0D2D hex 0000110100101101 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15	1	-	-	0	Unused
14	1	OFC	-	0	Control bit
13	1	BP	-	0	Control bit
12	1	PD	-	0	Control bit
11:6	6	Ibof	52	110100	Bias current: 6 bits
5:0	6	Icf	45	101101	Bias current: 6 bits

Table 12. High Gain register 2 (SA RO)

Register address 101 (default value 0B2E hex 0000101100101110 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15	1	-	-	0	Unused
14	1	BC	-	0	Control bit
13	1	LRd	-	0	Control bit
12	1	nLG	-	0	Control bit
11:6	6	Ib_AOP	44	101100	Bias current: 6 bits
5:0	6	IbSF	46	101110	Bias current: 6 bits

Table 13. Trigger register 1 (SA Trig)

Register address 102 (default value 0B6D hex 0000101101101101 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15	1	-	-	0	Unused
14	1	-	-	0	Unused
13	1	BP	-	0	Control bit
12	1	PD	-	0	Control bit
11:6	6	Ibof	45	101101	Bias current: 6 bits
5:0	6	Icf	45	101101	Bias current: 6 bits

Table 14. Trigger register 2 (SA Trig)

Register address 103 (default value 0BEE hex 0000101111101110 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15	1	-	-	0	Unused
14	1	BC	-	0	Control bit
13	1	LB	-	0	Control bit
12	1	LG	-	0	Control bit
11:6	6	Ib_ABF	47	101111	Bias current: 6 bits
5:0	6	IbSF	46	101110	Bias current: 6 bits

Table 15. Control / Debug register GLOBAL configurations (Register 1) CH 2

Register address 104 (default value 196D hex 0001100101101101 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15:11	5	-	-	00011	Chip version
10	1	OutsynchroCkb	-	0	Resynchronize output data of slow control serial link
9	1	SynchrOut	-	0	Resynchronize output data of slow control serial link
8:6	3	Is	05	000 (101)	Bias current: only 3 MSB are set (Is<5:3>). 3 LSBs are hardwired (Is<2:0> = 101)
5:0	6	Ibgm	45	101101	Bias current: 6 bits

Table 16. Low Gain register 1 (SA RO) CH 2

Register address 105 (default value 0D2D hex 0000110100101101 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15	1	-	-	0	Unused
14	1	OFC	-	0	Control bit
13	1	BP	-	0	Control bit
12	1	PD	-	0	Control bit
11:6	6	Ibof	52	110100	Bias current: 6 bits
5:0	6	Icf	45	101101	Bias current: 6 bits

Table 17. Low Gain register 2 (SA RO) CH 2

Register address 106 (default value 0B2E hex 0000101100101110 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15	1	-	-	0	Unused
14	1	BC	-	0	Control bit
13	1	LRd	-	0	Control bit
12	1	nLG	-	0	Control bit
11:6	6	Ib_AOP	44	101100	Bias current: 6 bits
5:0	6	IbSF	46	101110	Bias current: 6 bits

Table 18. High Gain register 1 (SA RO) CH 2

Register address 107 (default value 0D2D hex 0000110100101101 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15	1	-	-	0	Unused
14	1	OFC	-	0	Control bit
13	1	BP	-	0	Control bit
12	1	PD	-	0	Control bit
11:6	6	Ibof	52	110100	Bias current: 6 bits
5:0	6	Icf	45	101101	Bias current: 6 bits

Table 19. High Gain register 2 (SA RO) CH 2

Register address 108 (default value 0B2E hex 0000101100101110 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15	1	-	-	0	Unused
14	1	BC	-	0	Control bit
13	1	LRd	-	0	Control bit
12	1	nLG	-	0	Control bit
11:6	6	Ib_AOP	44	101100	Bias current: 6 bits
5:0	6	IbSF	46	101110	Bias current: 6 bits

Table 20. Trigger register 1 (SA Trig) CH 2

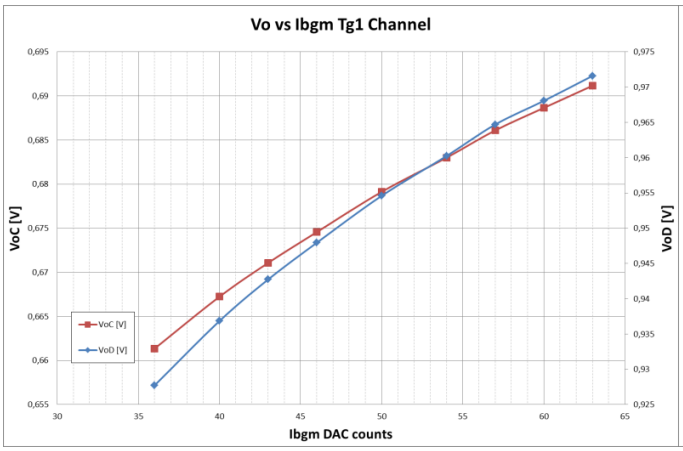
Register address 109 (default value 0B6D hex 0000101101101101 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15	1	-	-	0	Unused
14	1	-	-	0	Unused
13	1	BP	-	0	Control bit
12	1	PD	-	0	Control bit
11:6	6	Ibof	45	101101	Bias current: 6 bits
5:0	6	Icf	45	101101	Bias current: 6 bits

Table 21. Trigger register 2 (SA Trig) CH 2

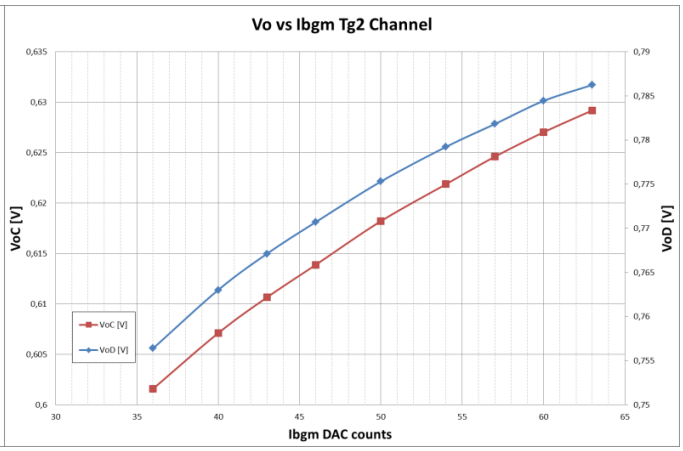
Register address 110 (default value 0BEE hex 0000101111101110 binary)					
bits	**bit #**	**Description**	**Default (dec)**	**Default (binary)**	**Coments**
15	1	-	-	0	Unused
14	1	BC	-	0	Control bit
13	1	LB	-	0	Control bit
12	1	LG	-	0	Control bit
11:6	6	Ib_ABF	47	101111	Bias current: 6 bits
5:0	6	IbSF	46	101110	Bias current: 6 bits

TYPICAL PERFORMANCE CHARACTERISTICS

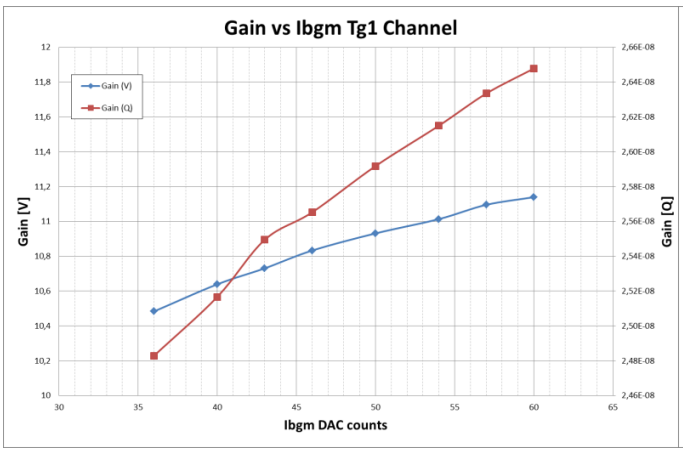
Operating conditions: T_A = 25°C, unless otherwise noted.



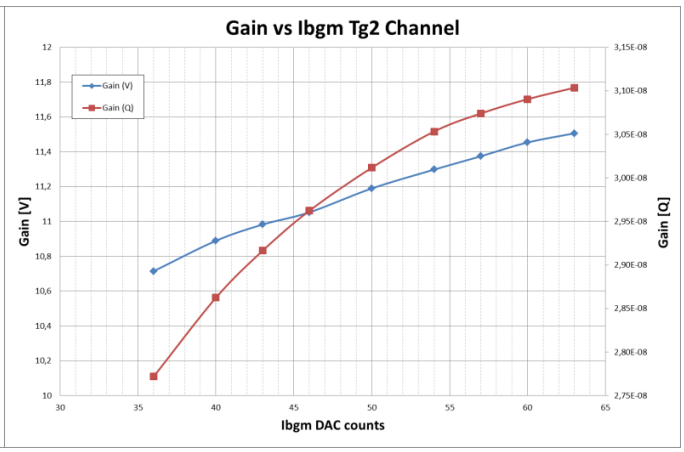
ACTAf 2Ch Linearity test vs Ibgm at Trigger 1 Channel



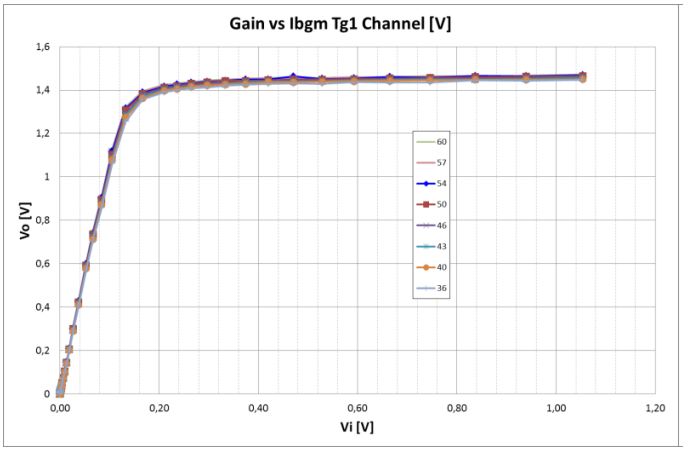
ACTAf 2Ch Linearity test vs Ibgm at Trigger 2 Channel



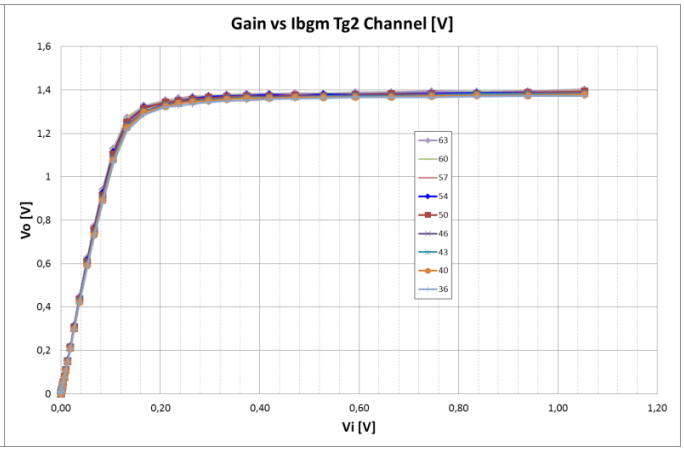
ACTAf 2Ch Gain test vs Ibgm at Trigger 1 Channel



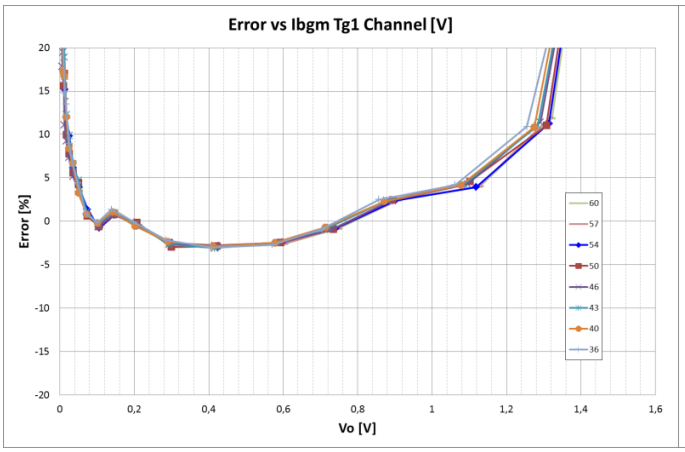
ACTAf 2Ch Gain test vs Ibgm at Trigger 2 Channel



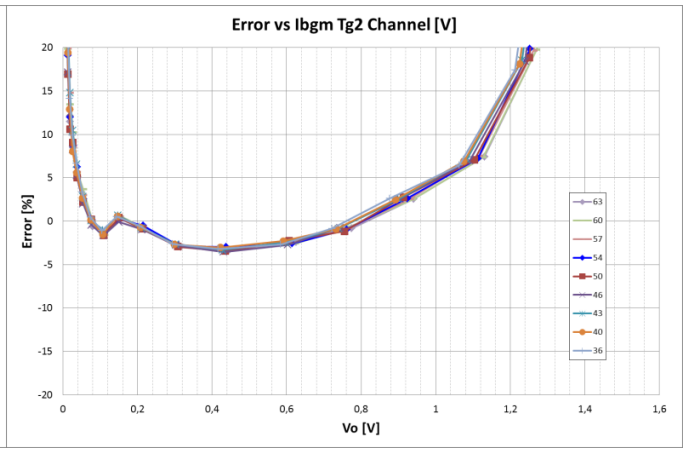
ACTAf 2Ch Gain (V) test vs Ibgm at Trigger 1 Channel



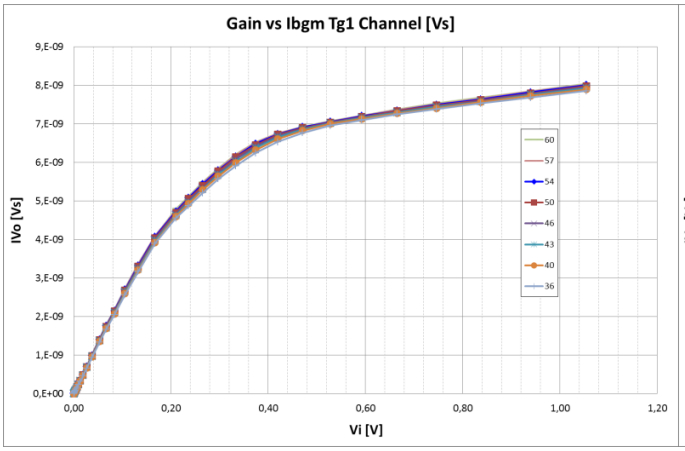
ACTAf 2Ch Gain (V) test vs Ibgm at Trigger 2 Channel



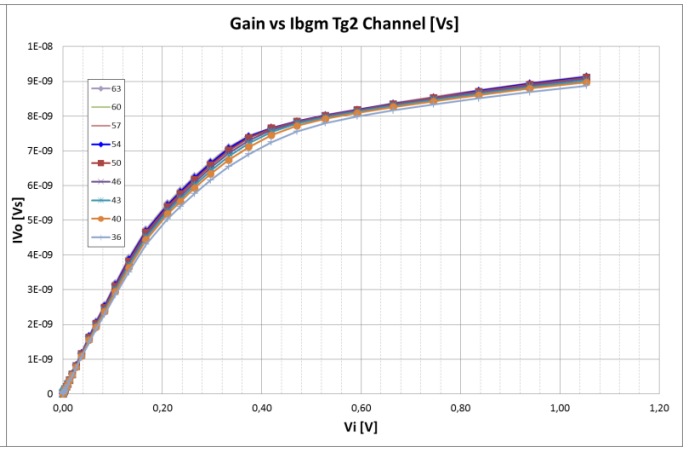
ACTAf 2Ch Error Gain (V) test vs Ibgm at Trigger 1 Channel



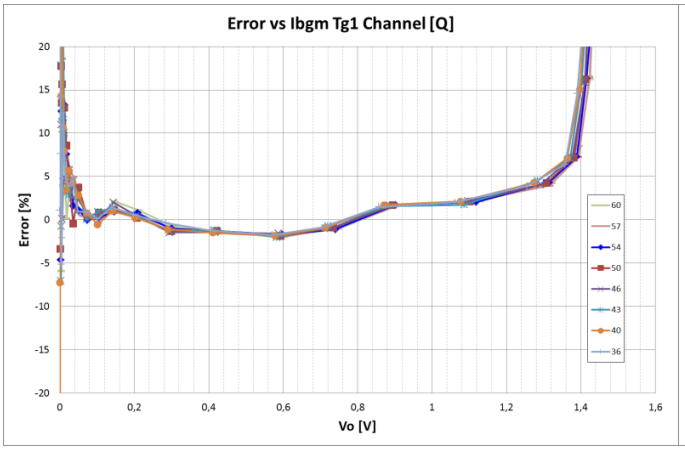
ACTAf 1Ch Error Gain (V) test vs Ibgm at Trigger 2 Channel



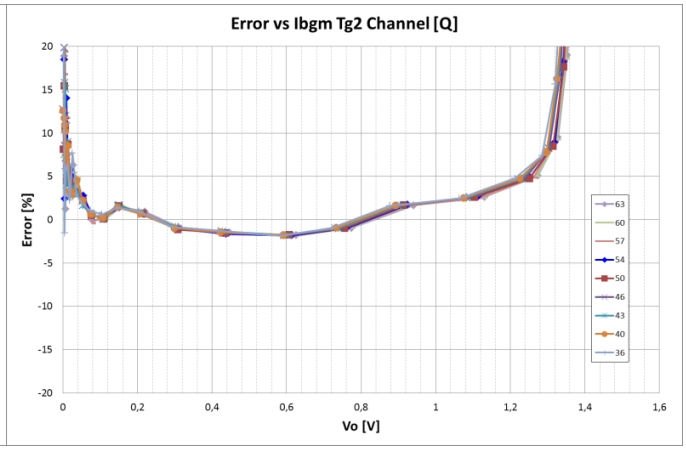
ACTAf 2Ch Gain (Q) test vs Ibgm at Trigger 1 Channel



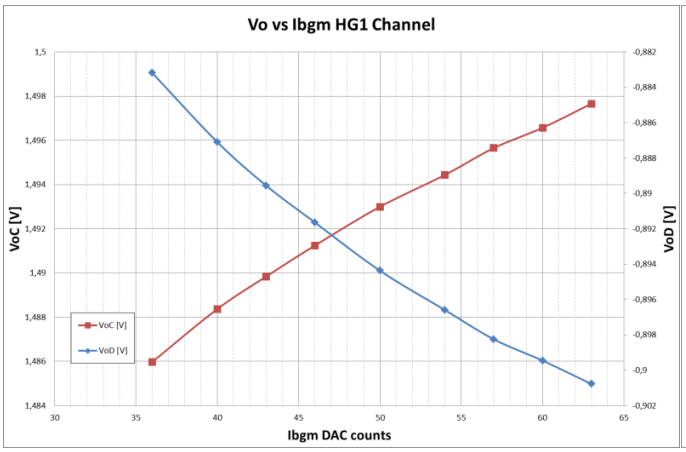
ACTAf 2Ch Gain (Q) test vs Ibgm at Trigger 2 Channel



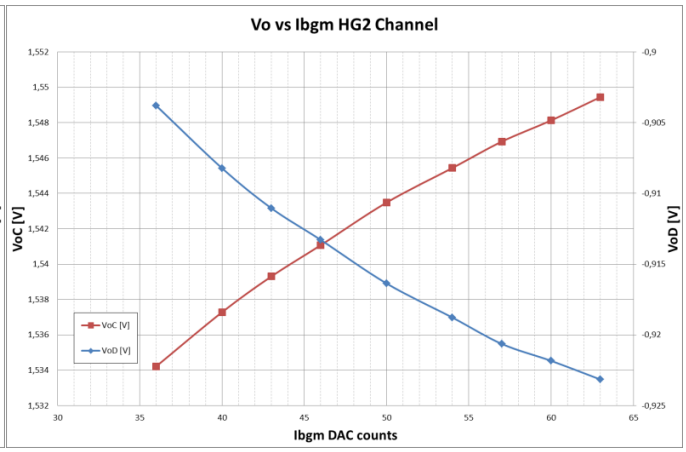
ACTAf 2Ch Error Gain (Q) test vs Ibgm at Trigger 1 Channel



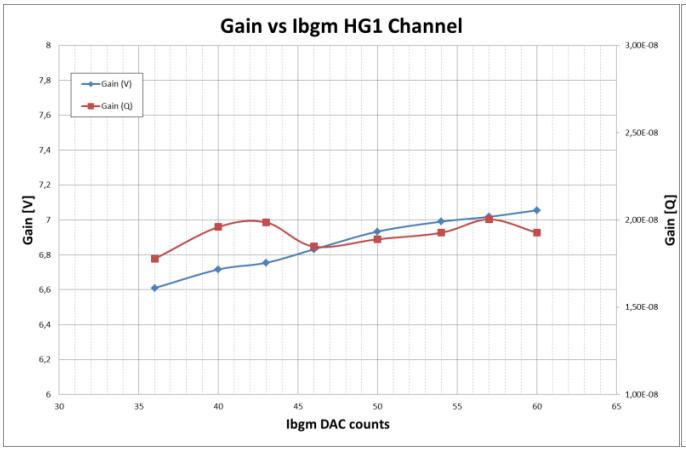
ACTAf 2Ch Error Gain (Q) test vs Ibgm at Trigger 2 Channel



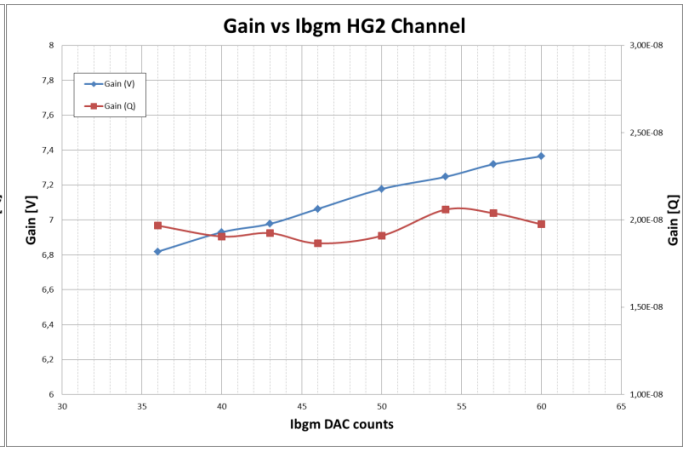
ACTAf 2Ch Linearity test vs Ibgm at High Gain 1 Channel



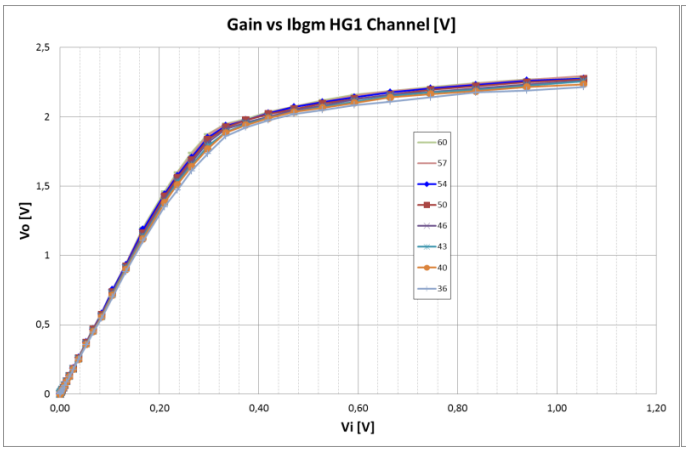
ACTAf 2Ch Linearity test vs Ibgm at High Gain 2 Channel



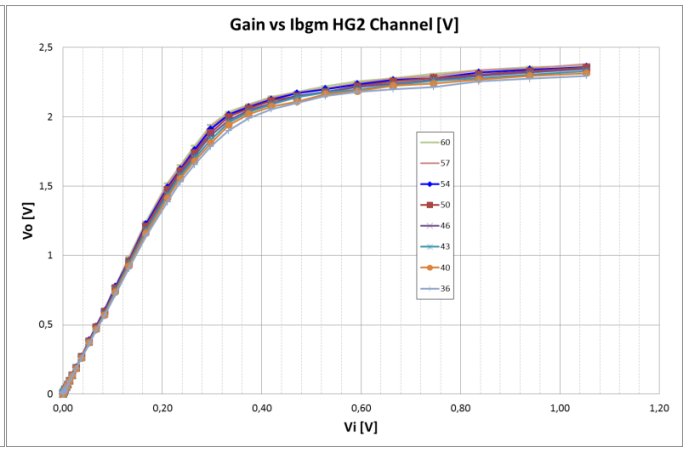
ACTAf 2Ch Gain test vs Ibgm at High Gain 1 Channel



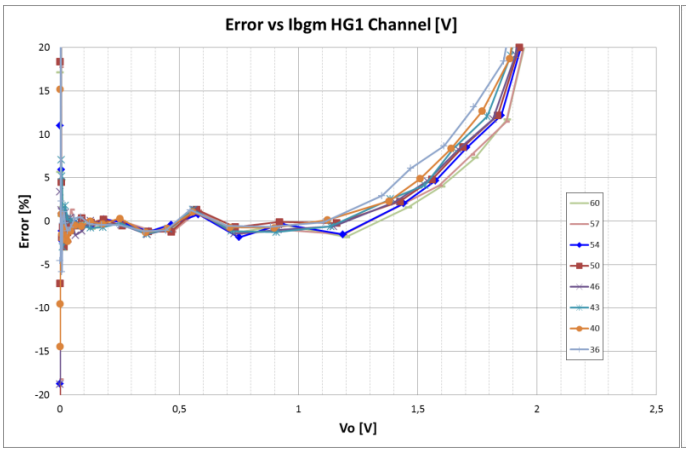
ACTAf 2Ch Gain test vs Ibgm at High Gain 2 Channel



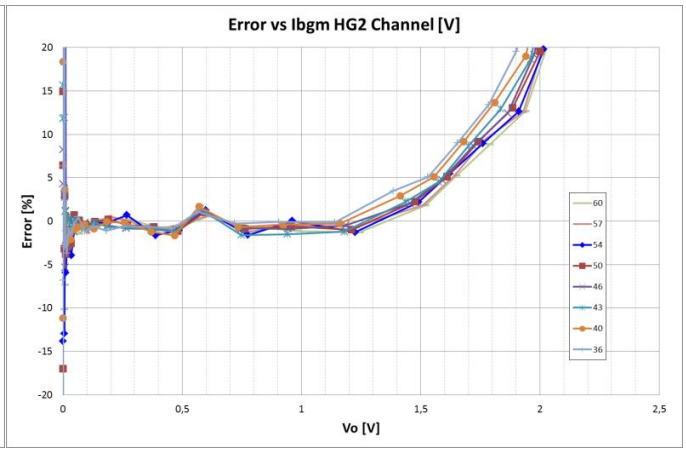
ACTAf 2Ch Gain (V) test vs Ibgm at High Gain 1 Channel



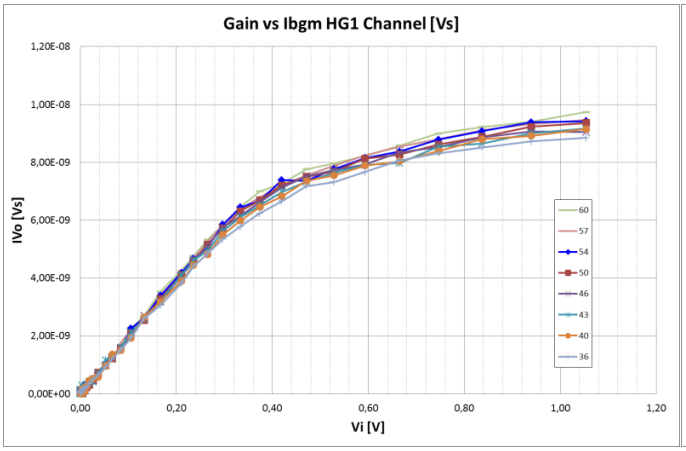
ACTAf 2Ch Gain (V) test vs Ibgm at High Gain 2 Channel



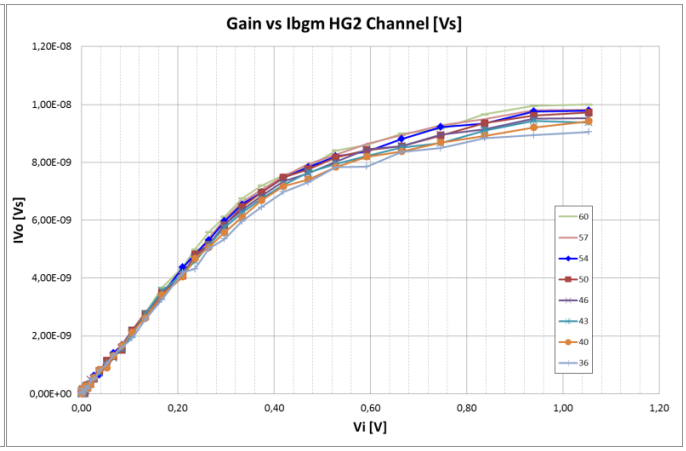
ACTAf 2Ch Error Gain (V) test vs Ibgm at High Gain 1 Channel



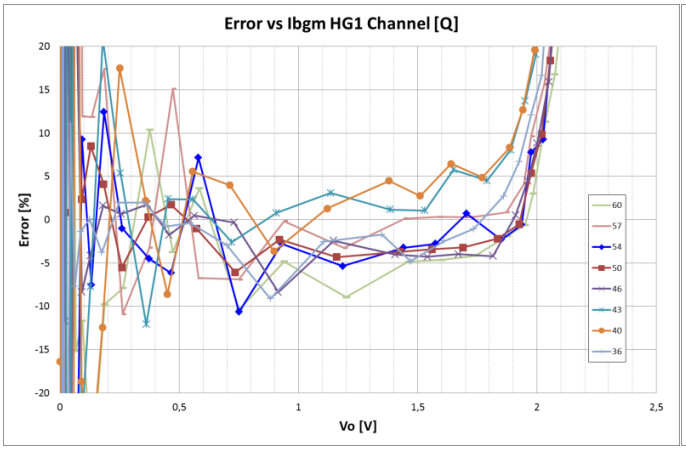
ACTAf 1Ch Error Gain (V) test vs Ibgm at High Gain 2 Channel



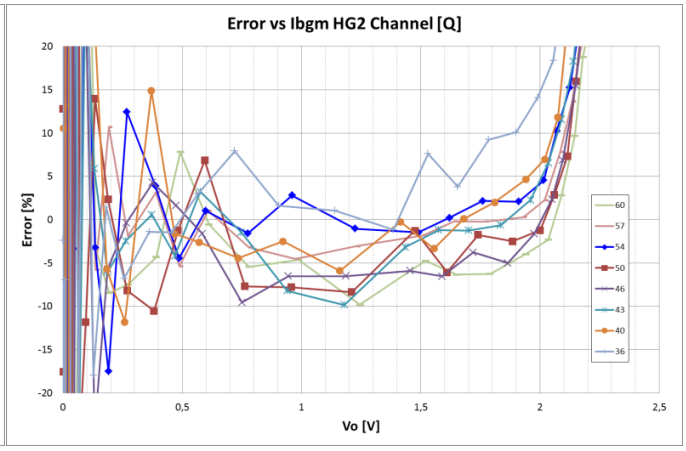
ACTAf 2Ch Gain (Q) test vs Ibgm at High Gain 1 Channel



ACTAf 2Ch Gain (Q) test vs Ibgm at High Gain 2 Channel



ACTAf 2Ch Error Gain (Q) test vs Ibgm at High Gain 1 Channel



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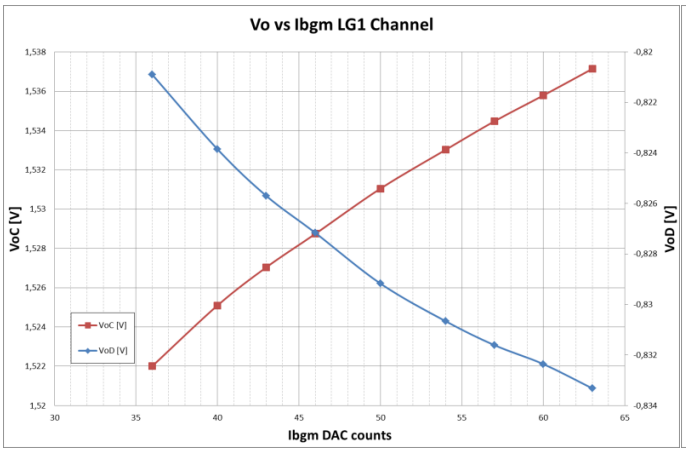
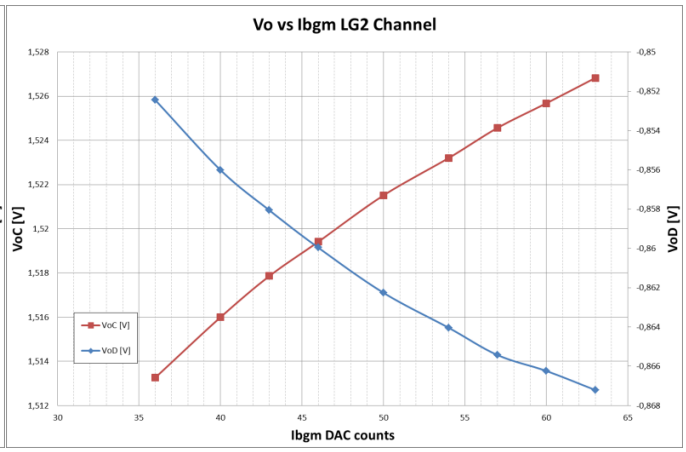
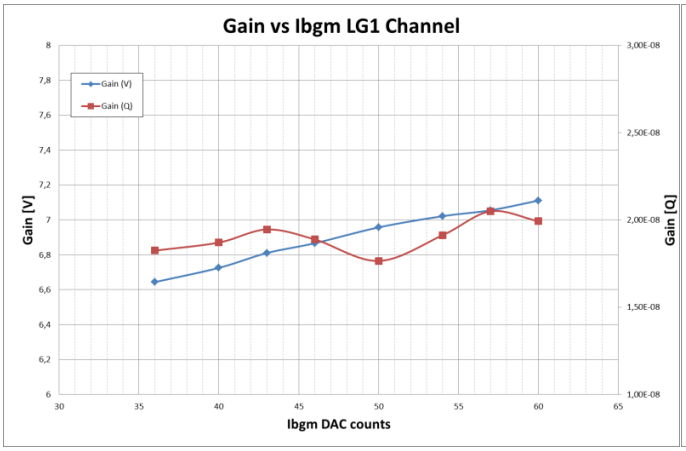


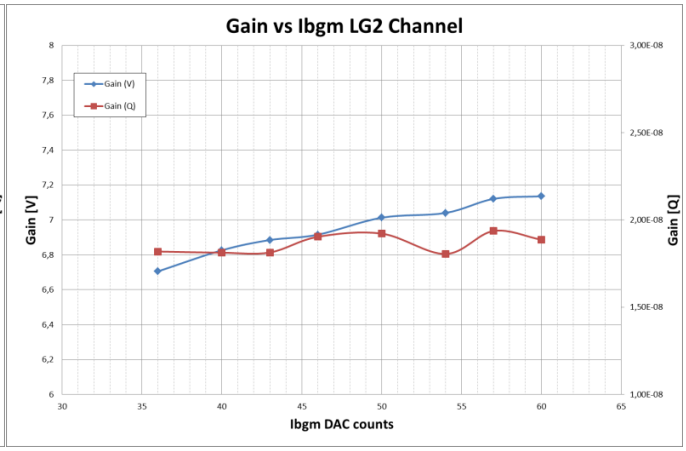
ACTAf 2Ch Linearity test vs Ibgm at Low Gain 1 Channel



ACTAf 2Ch Linearity test vs Ibgm at Low Gain 2 Channel



ACTAf 2Ch Gain test vs Ibgm at Low Gain 1 Channel



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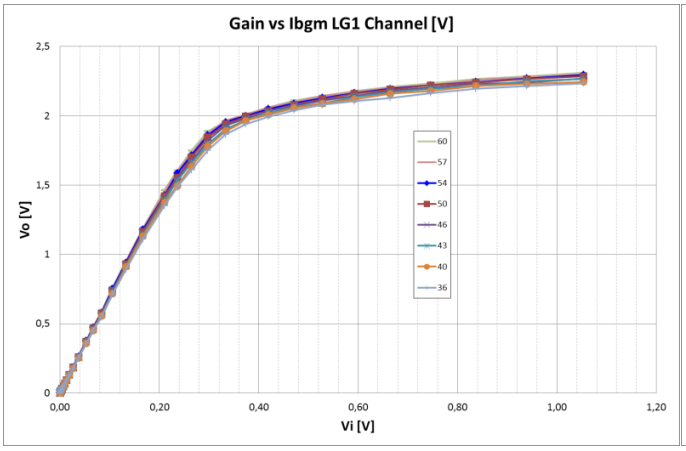
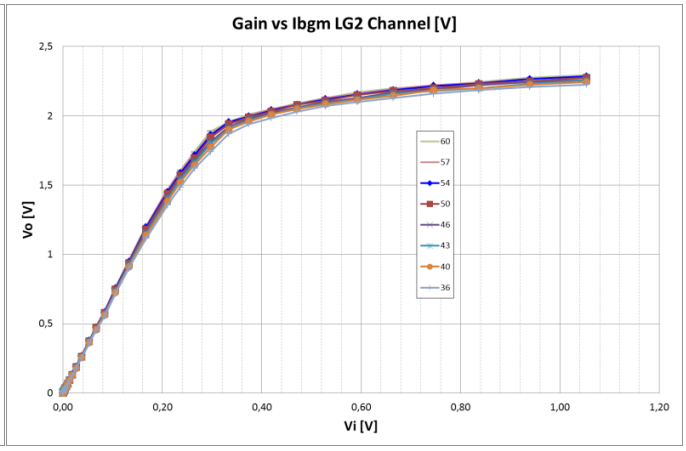
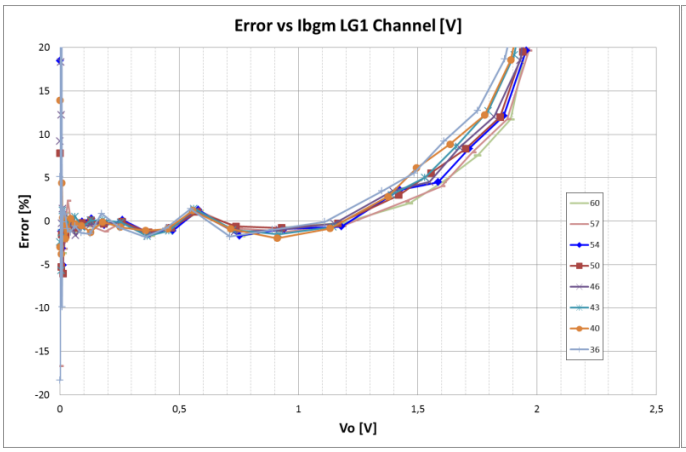


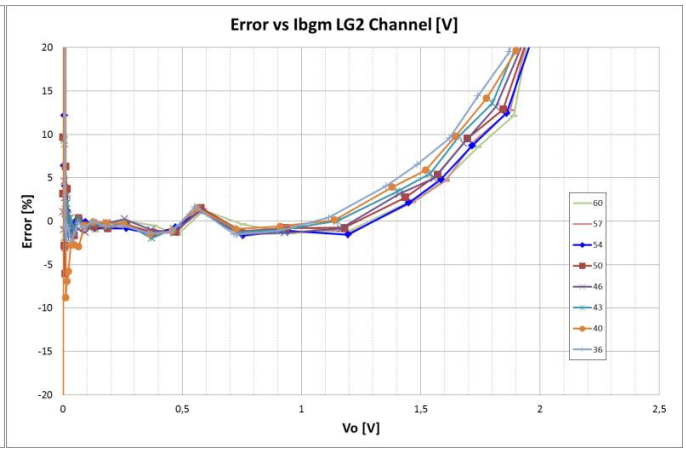
ACTAf 2Ch Gain (V) test vs Ibgm at Low Gain 1 Channel



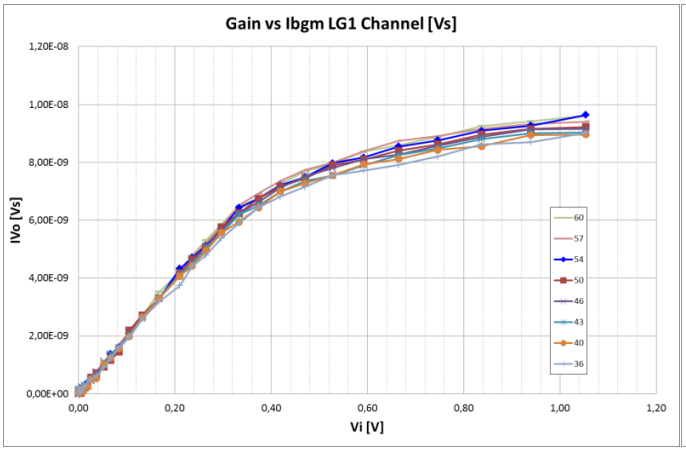
ACTAf 2Ch Gain (V) test vs Ibgm at Low Gain 2 Channel



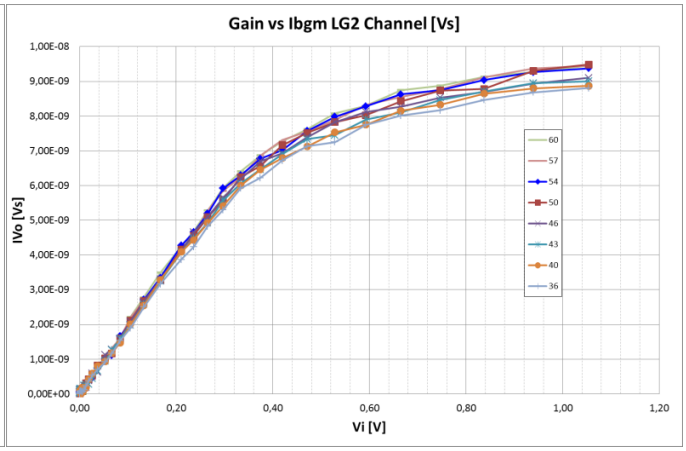
ACTAf 2Ch Error Gain (V) test vs Ibgm at Low Gain 1 Channel



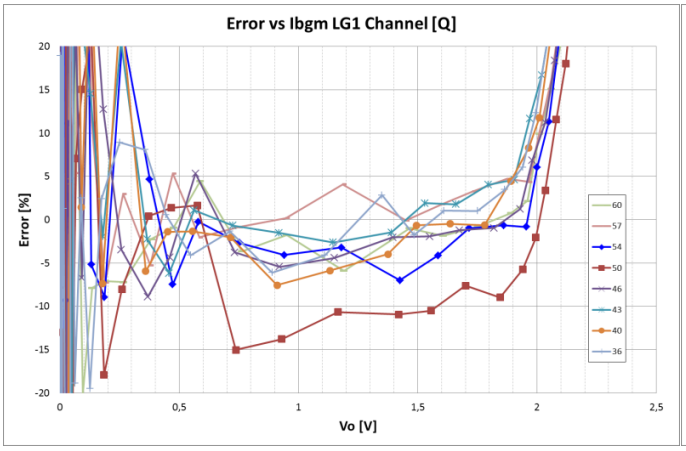
ACTAf 1Ch Error Gain (V) test vs Ibgm at Low Gain 2 Channel



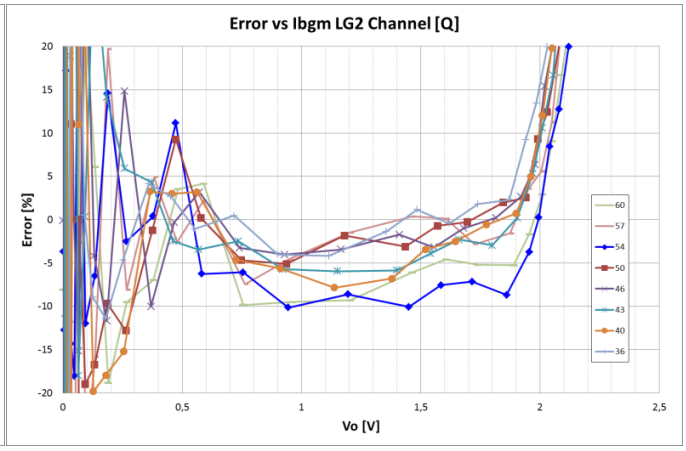
ACTAf 2Ch Gain (Q) test vs Ibgm at Low Gain 1 Channel



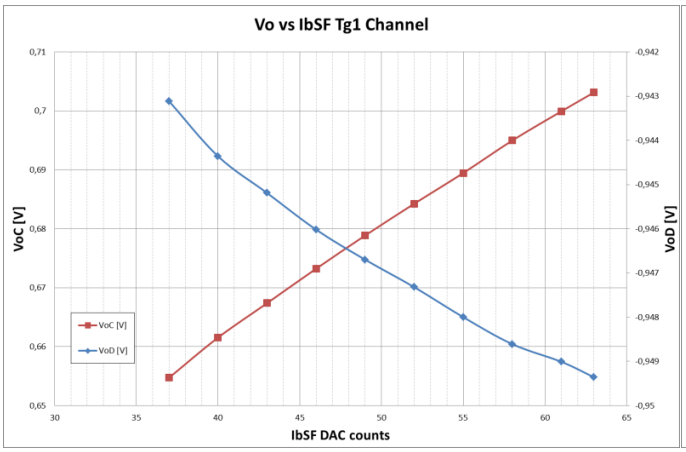
ACTAf 2Ch Gain (Q) test vs Ibgm at Low Gain 2 Channel



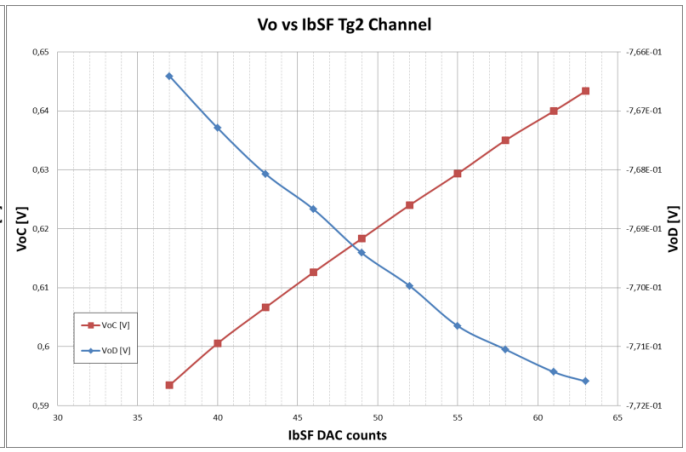
ACTAf 2Ch Error Gain (Q) test vs Ibgm at Low Gain 1 Channel



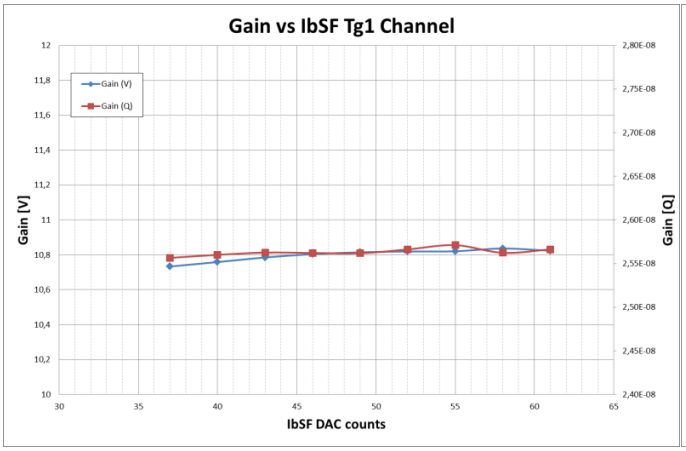
ACTAf 2Ch Error Gain (Q) test vs Ibgm at Low Gain 2 Channel



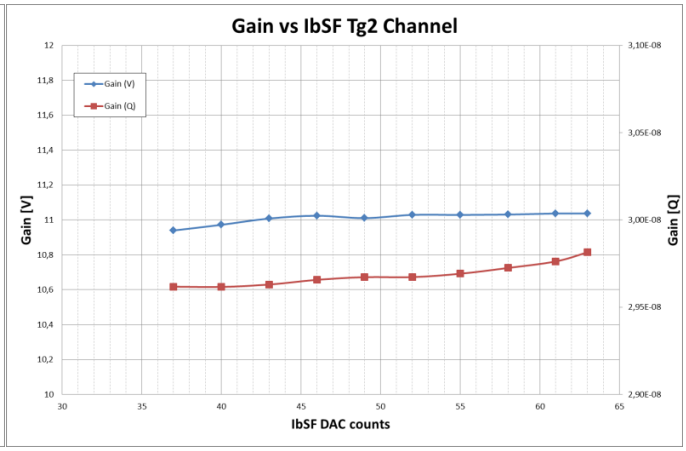
ACTAf 2Ch Linearity test vs IbSF at Trigger 1 Channel



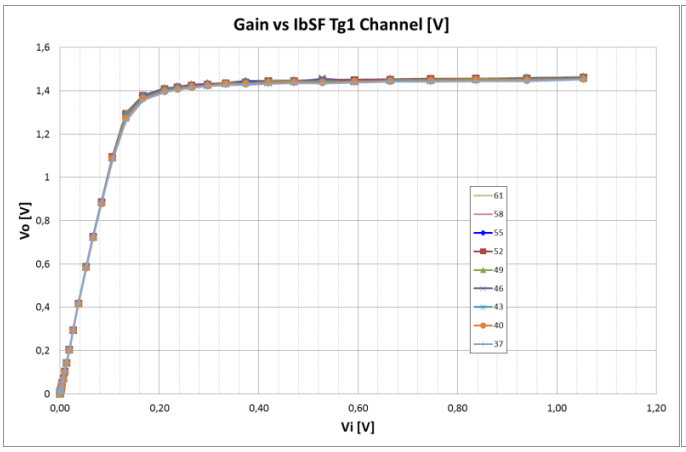
ACTAf 2Ch Linearity test vs IbSF at Trigger 2 Channel



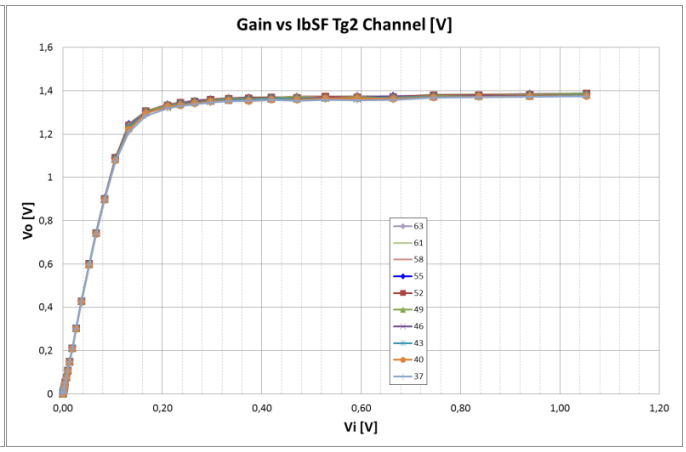
ACTAf 2Ch Gain test vs IbSF at Trigger 1 Channel



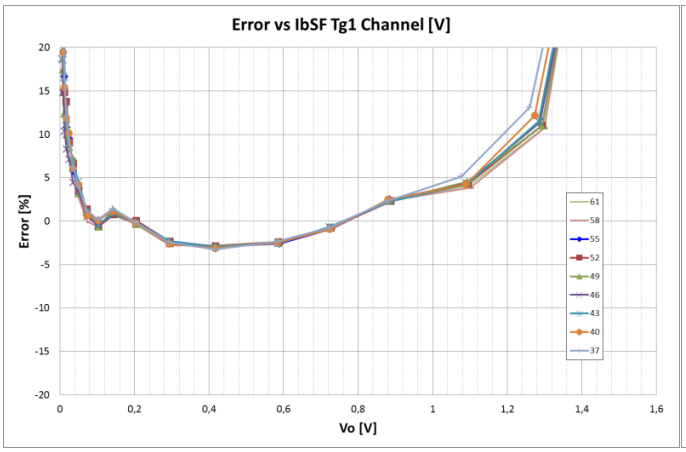
ACTAf 2Ch Gain test vs IbSF at Trigger 2 Channel



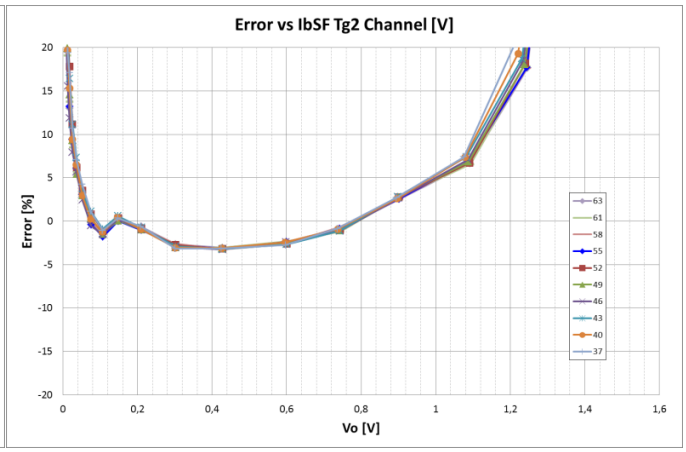
ACTAf 2Ch Gain (V) test vs IbSF at Trigger 1 Channel



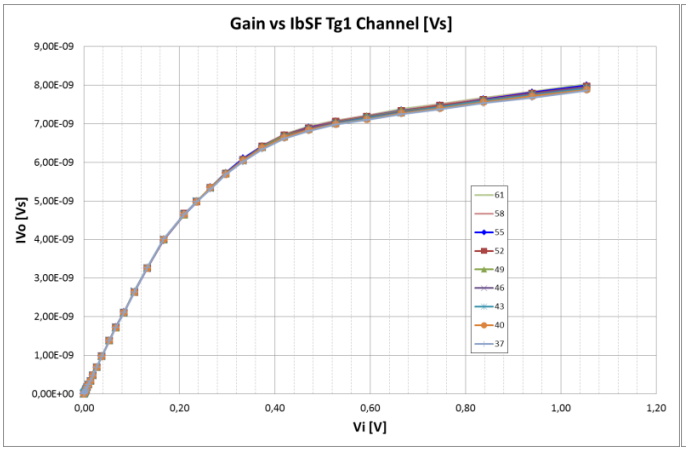
ACTAf 2Ch Gain (V) test vs IbSF at Trigger 2 Channel



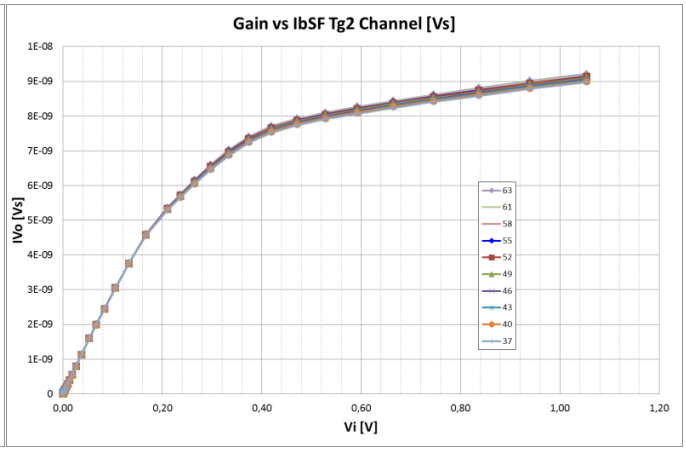
ACTAf 2Ch Error Gain (V) test vs IbSF at Trigger 1 Channel



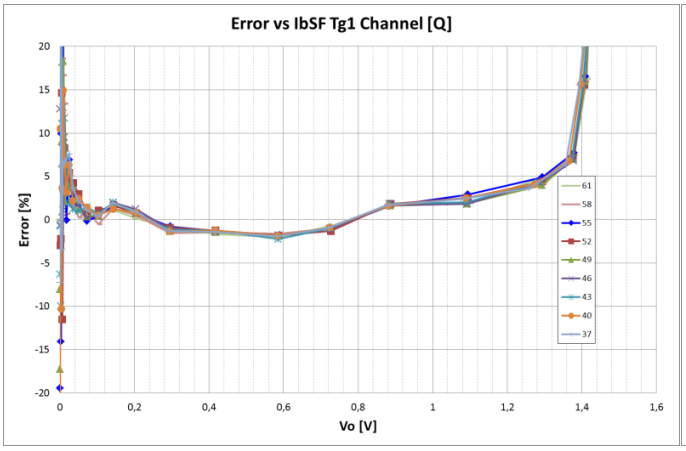
ACTAf 1Ch Error Gain (V) test vs IbSF at Trigger 2 Channel



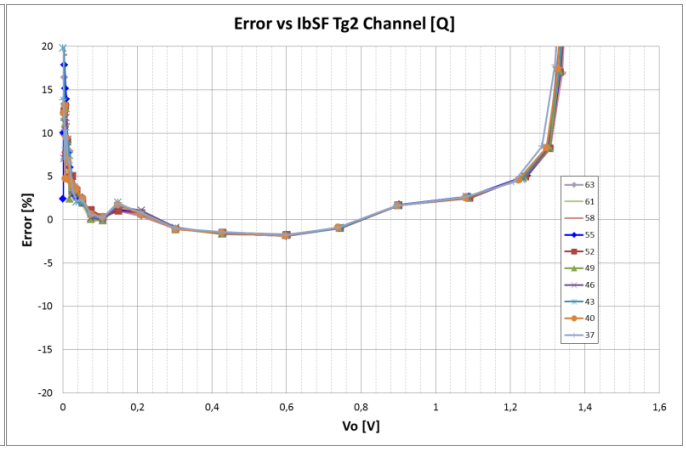
ACTAf 2Ch Gain (Q) test vs IbSF at Trigger 1 Channel



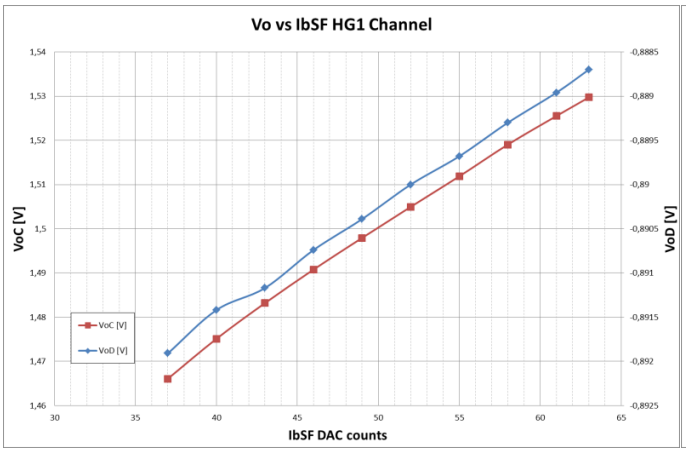
ACTAf 2Ch Gain (Q) test vs IbSF at Trigger 2 Channel



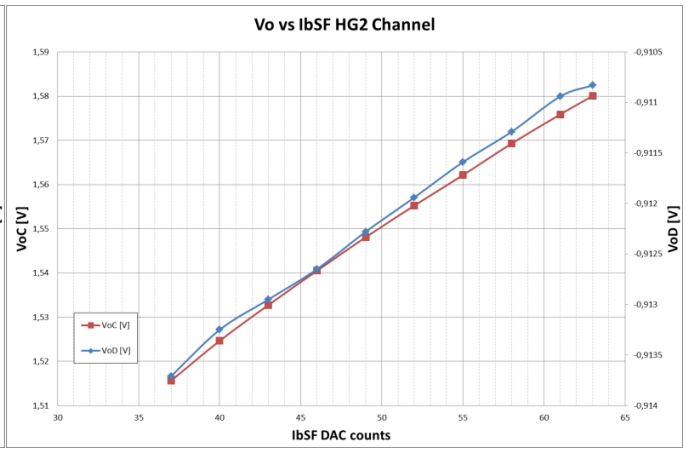
ACTAf 2Ch Error Gain (Q) test vs IbSF at Trigger 1 Channel



ACTAf 2Ch Error Gain (Q) test vs IbSF at Trigger 2 Channel



ACTAf 2Ch Linearity test vs IbSF at High Gain 1 Channel



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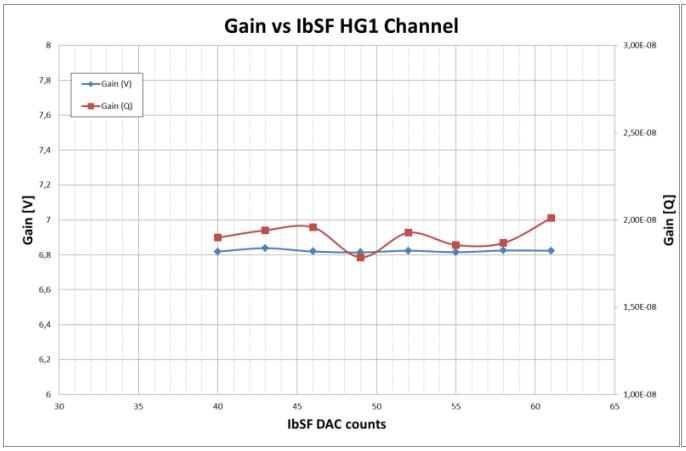
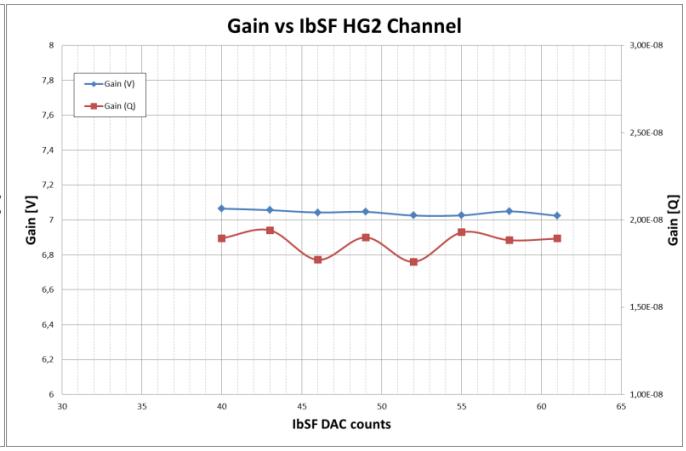
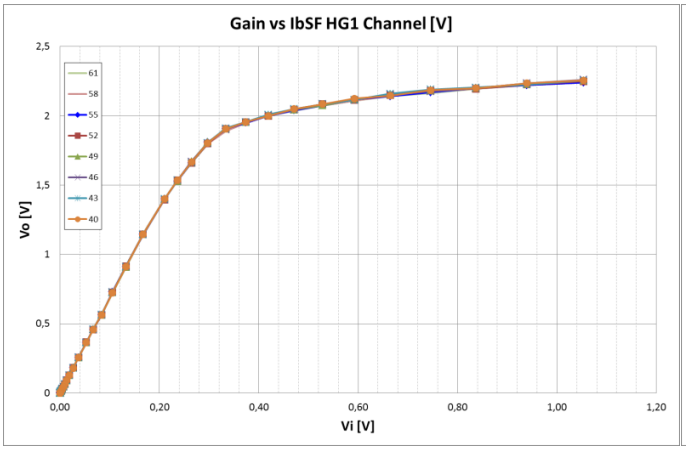


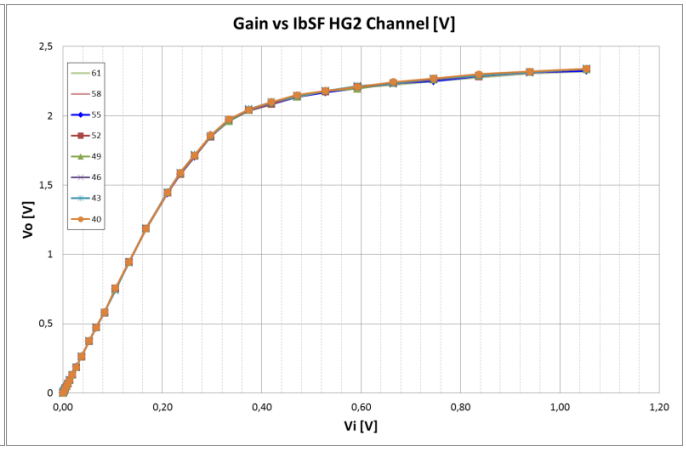
ACTAf 2Ch Gain test vs IbSF at High Gain 1 Channel



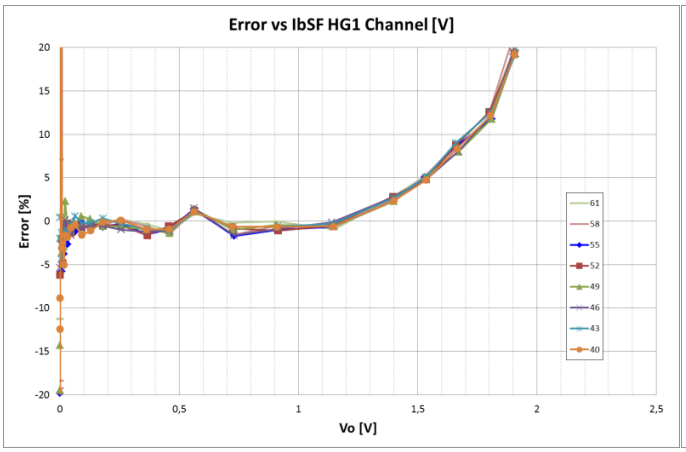
ACTAf 2Ch Gain test vs IbSF at High Gain 2 Channel



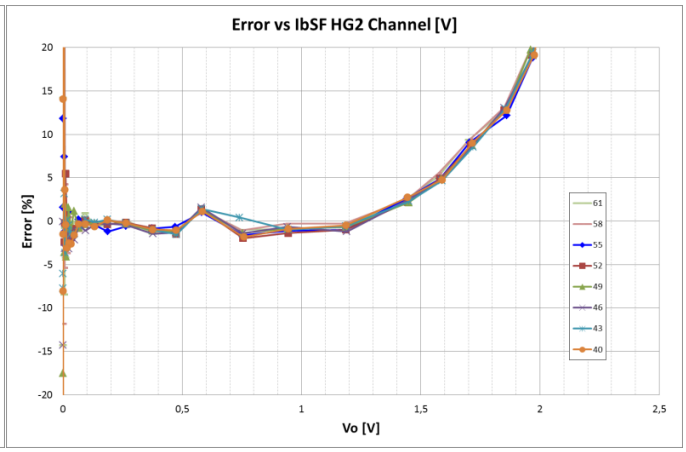
ACTAf 2Ch Gain (V) test vs IbSF at High Gain 1 Channel



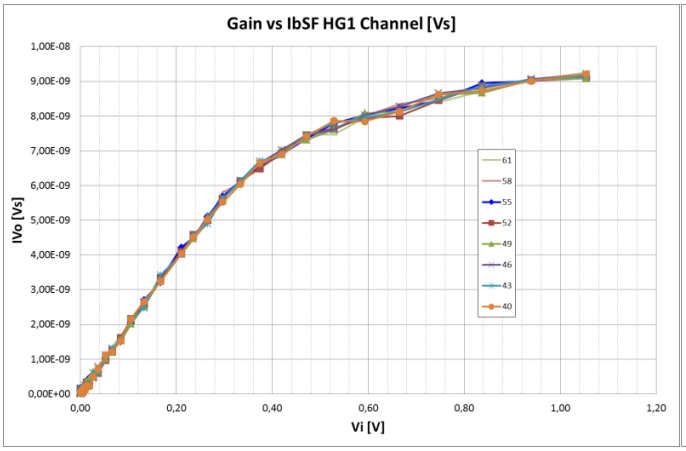
ACTAf 2Ch Gain (V) test vs IbSF at High Gain 2 Channel



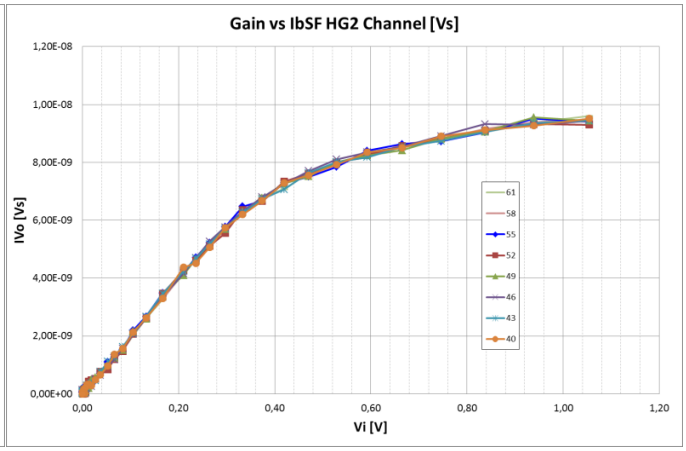
ACTAf 2Ch Error Gain (V) test vs IbSF at High Gain 1 Channel



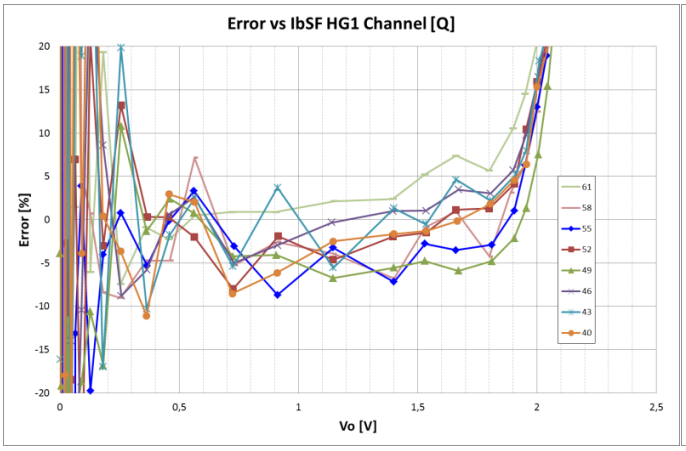
ACTAf 1Ch Error Gain (V) test vs IbSF at High Gain 2 Channel



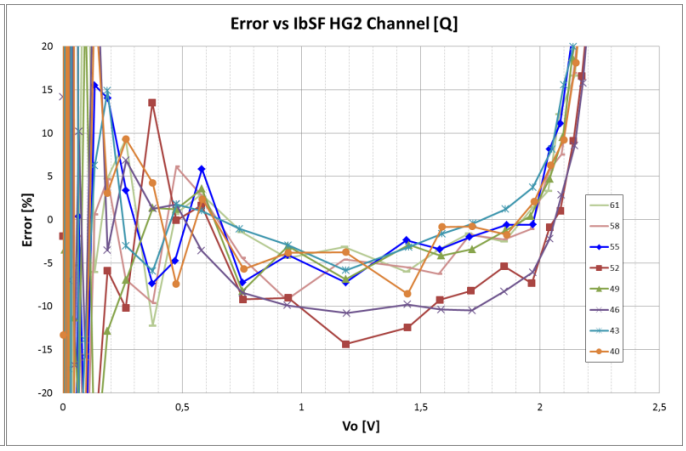
ACTAf 2Ch Gain (Q) test vs IbSF at High Gain 1 Channel



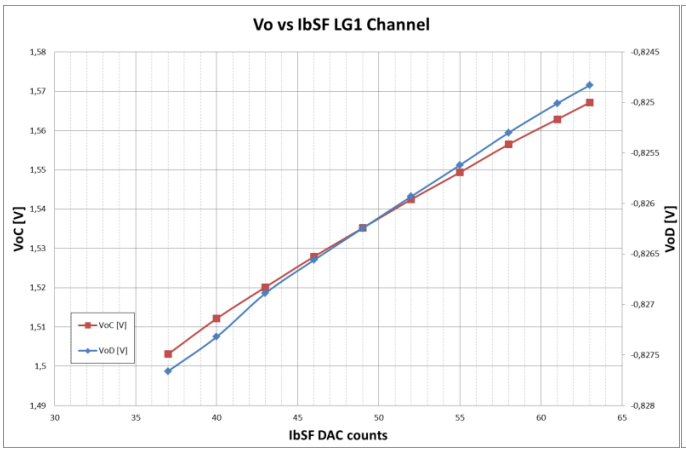
ACTAf 2Ch Gain (Q) test vs IbSF at High Gain 2 Channel



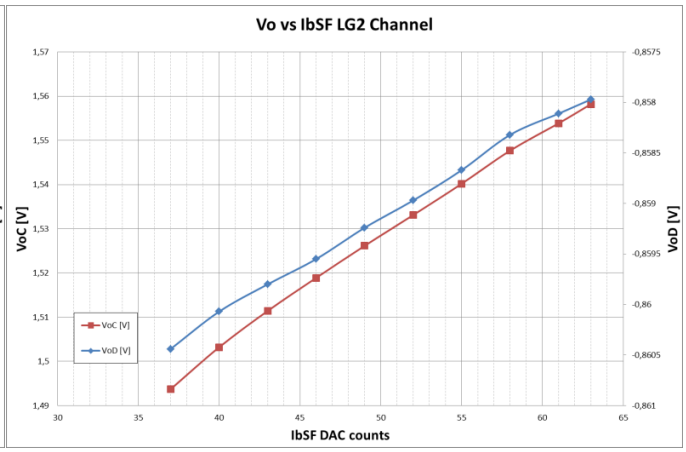
ACTAf 2Ch Error Gain (Q) test vs IbSF at High Gain 1 Channel



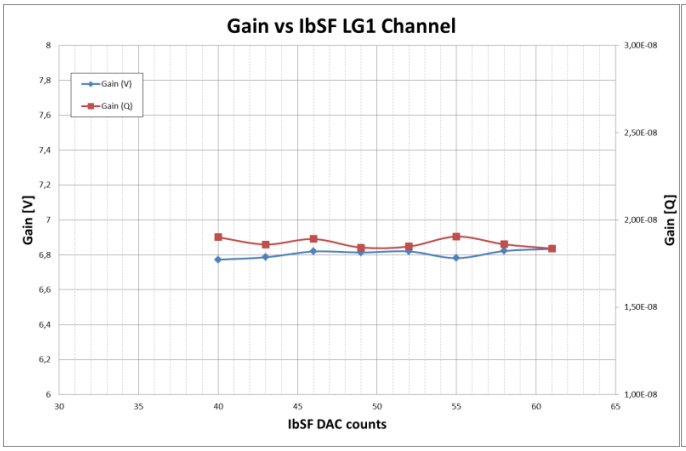
ACTAf 2Ch Error Gain (Q) test vs IbSF at High Gain 2 Channel



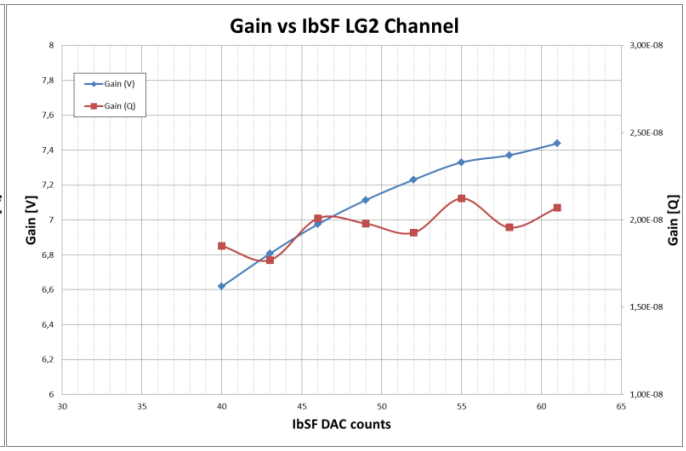
ACTAf 2Ch Linearity test vs IbSF at Low Gain 1 Channel



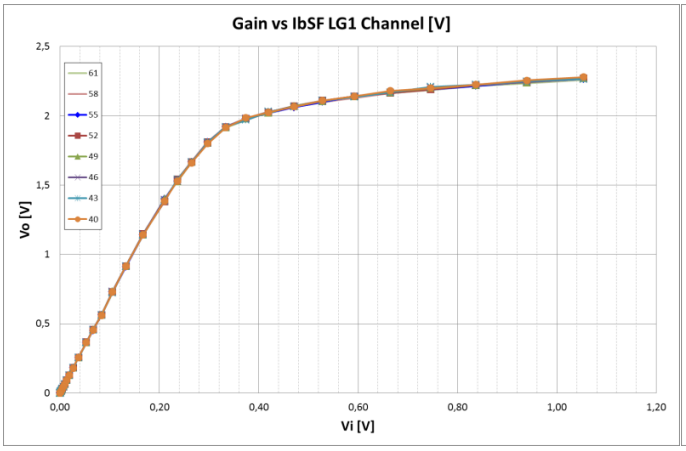
ACTAf 2Ch Linearity test vs IbSF at Low Gain 2 Channel



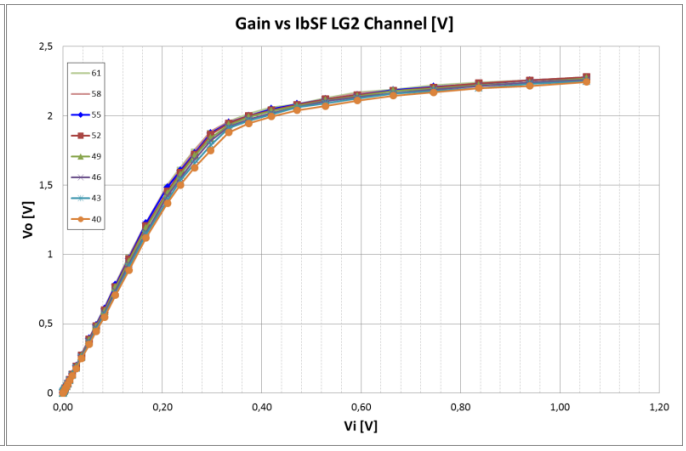
ACTAf 2Ch Gain test vs IbSF at Low Gain 1 Channel



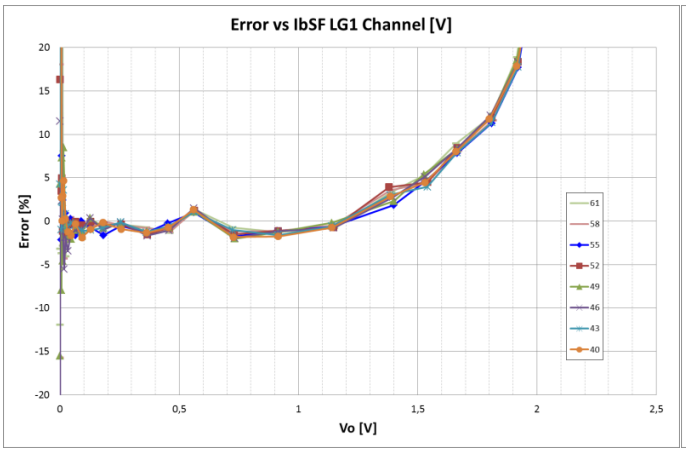
ACTAf 2Ch Gain test vs IbSF at Low Gain 2 Channel



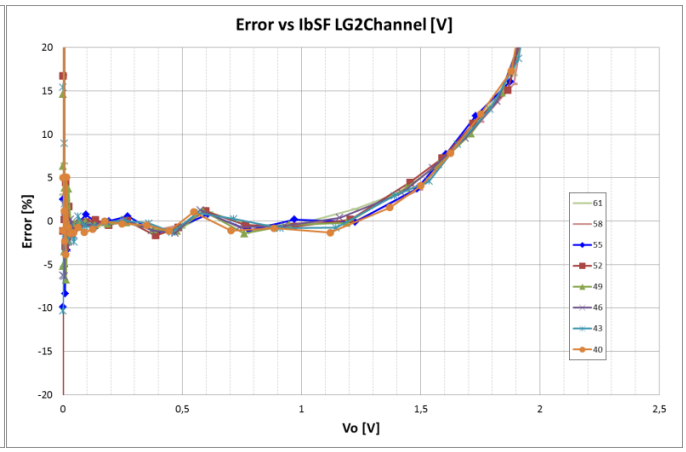
ACTAf 2Ch Gain (V) test vs IbSF at Low Gain 1 Channel



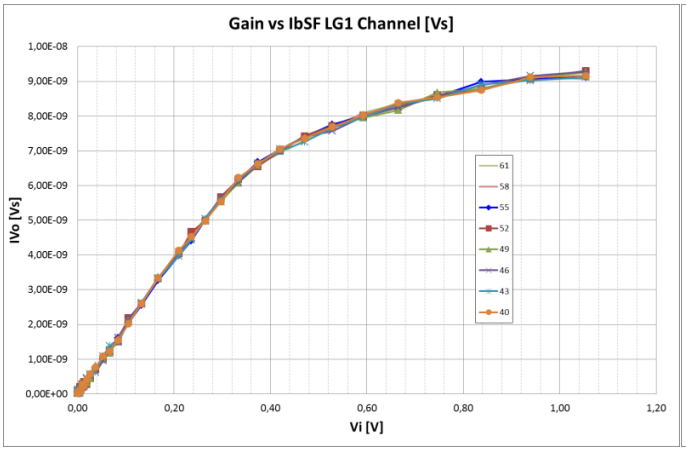
ACTAf 2Ch Gain (V) test vs IbSF at Low Gain 2 Channel



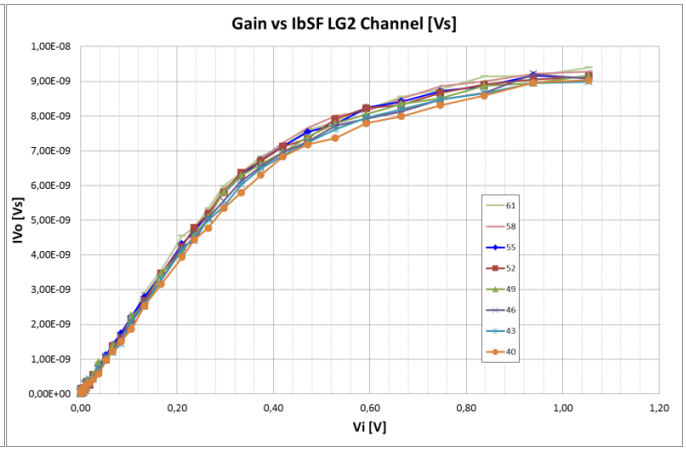
ACTAf 2Ch Error Gain (V) test vs IbSF at Low Gain 1 Channel



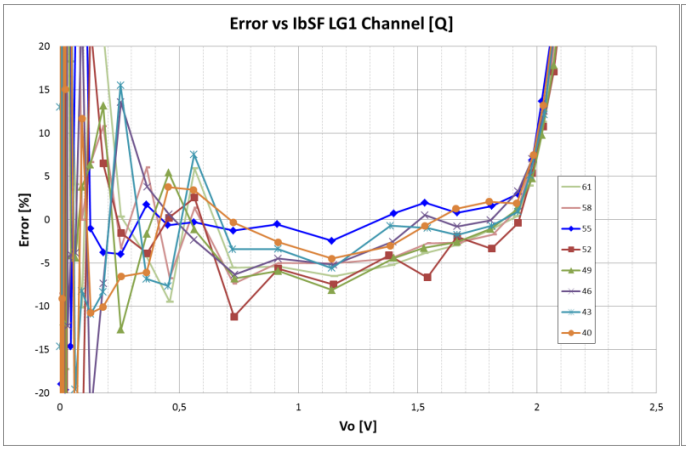
ACTAf 1Ch Error Gain (V) test vs IbSF at Low Gain 2 Channel



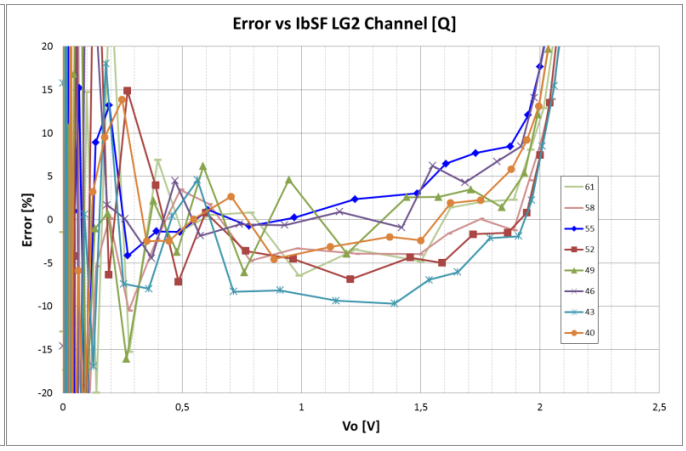
ACTAf 2Ch Gain (Q) test vs IbSF at Low Gain 1 Channel



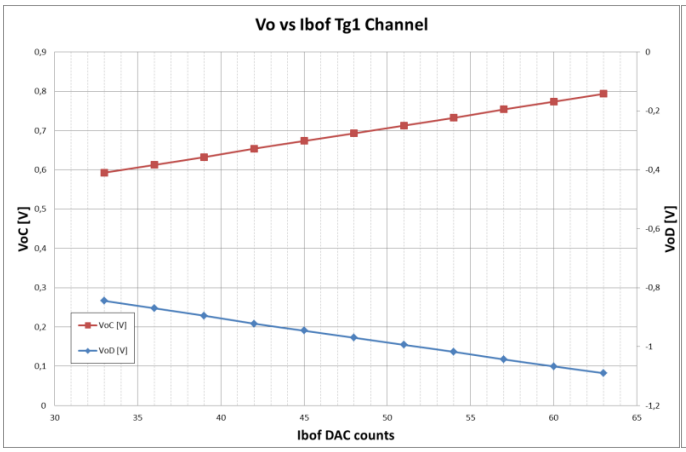
ACTAf 2Ch Gain (Q) test vs IbSF at Low Gain 2 Channel



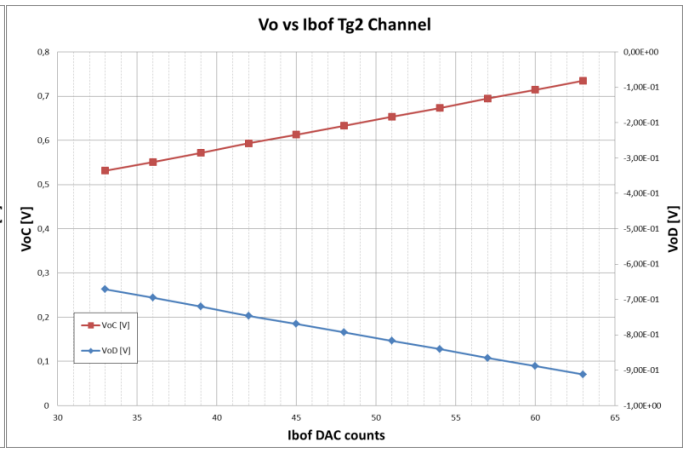
ACTAf 2Ch Error Gain (Q) test vs IbSF at Low Gain 1 Channel



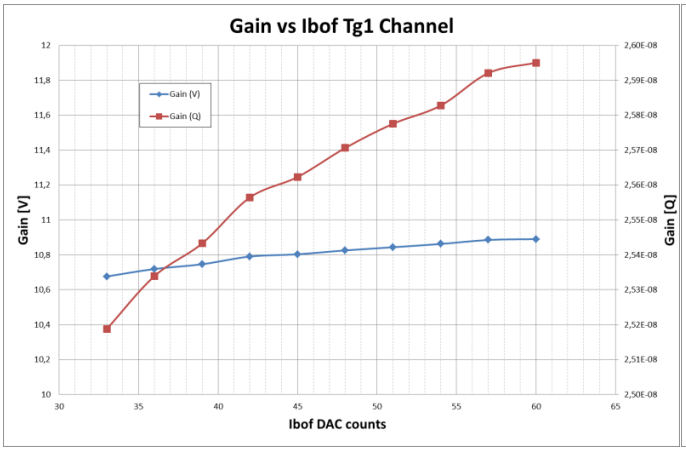
ACTAf 2Ch Error Gain (Q) test vs IbSF at Low Gain 2 Channel



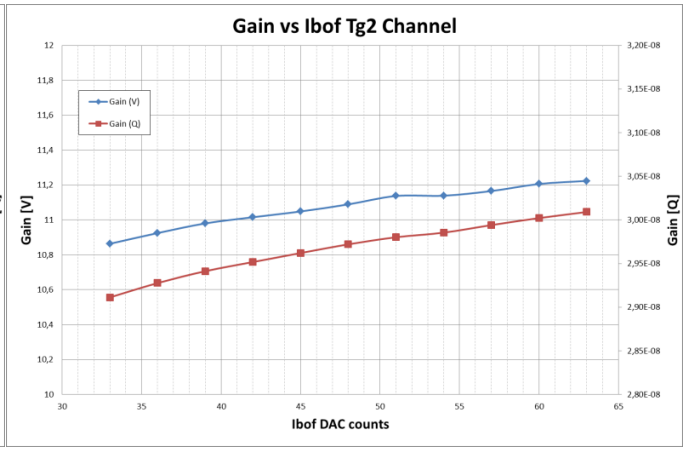
ACTAf 2Ch Linearity test vs Ibof at Trigger 1 Channel



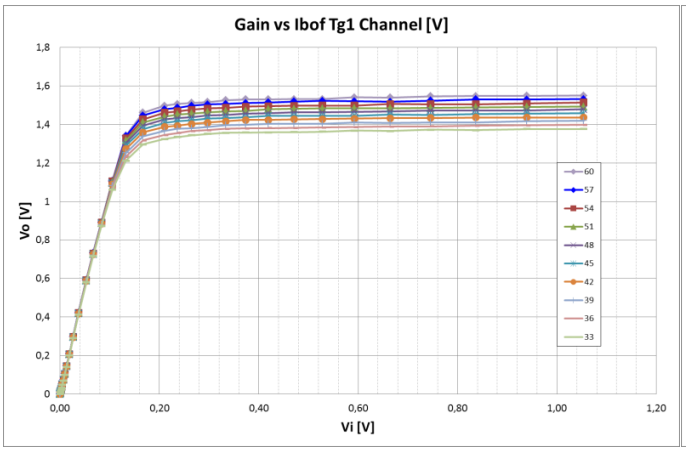
ACTAf 2Ch Linearity test vs Ibof at Trigger 2 Channel



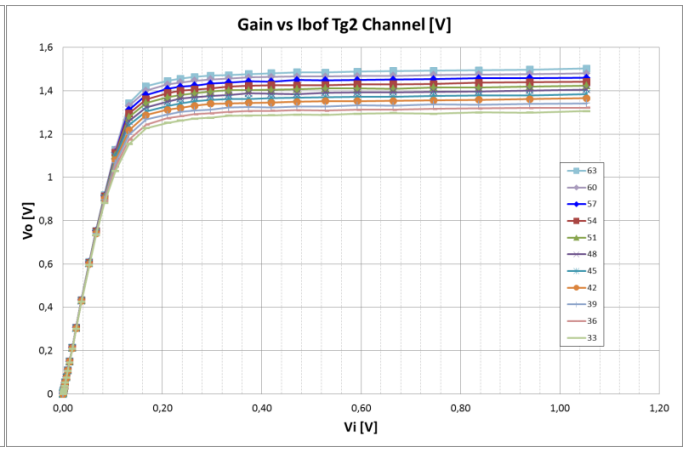
ACTAf 2Ch Gain test vs Ibof at Trigger 1 Channel



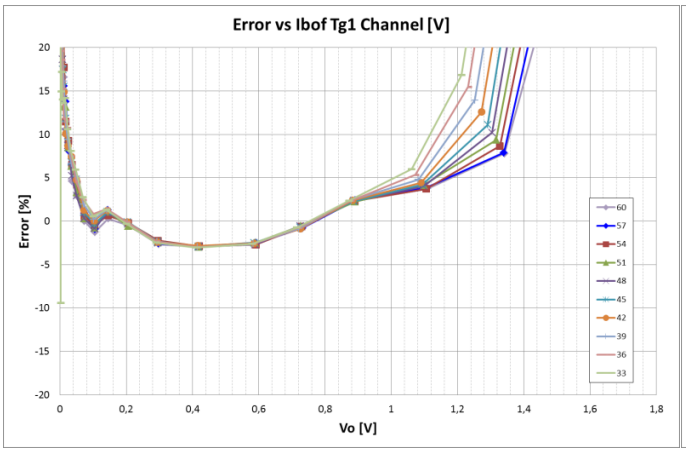
ACTAf 2Ch Gain test vs Ibof at Trigger 2 Channel



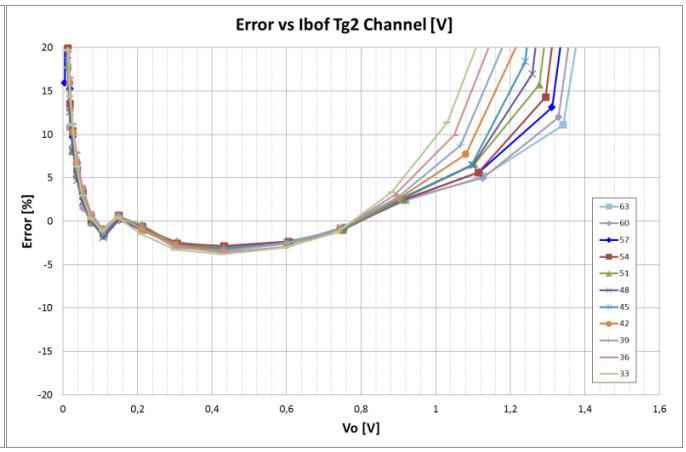
ACTAf 2Ch Gain (V) test vs Ibof at Trigger 1 Channel



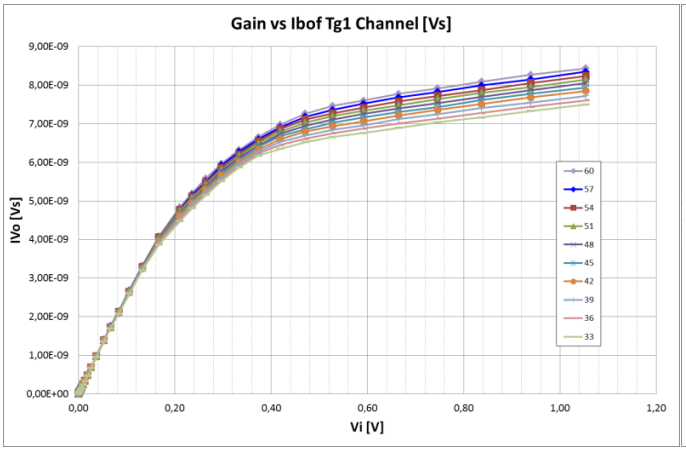
ACTAf 2Ch Gain (V) test vs Ibof at Trigger 2 Channel



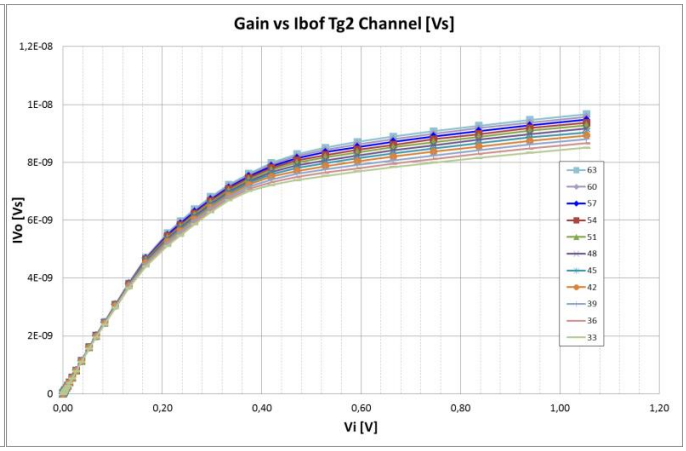
ACTAf 2Ch Error Gain (V) test vs Ibof at Trigger 1 Channel



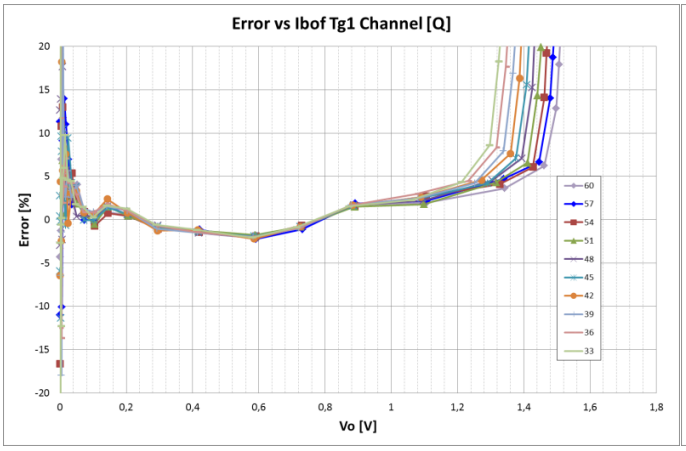
ACTAf 1Ch Error Gain (V) test vs Ibof at Trigger 2 Channel



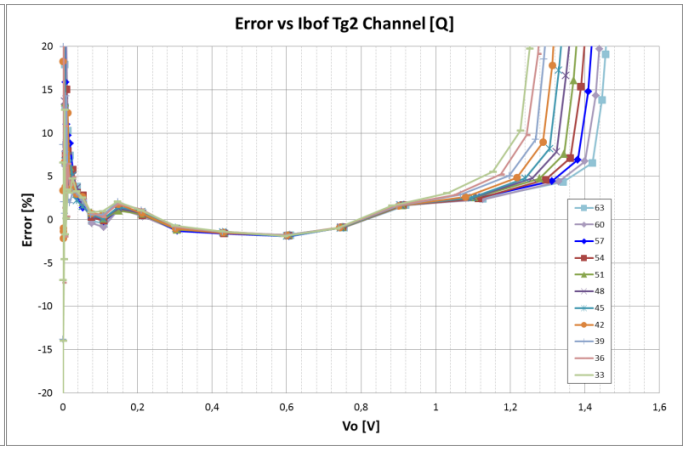
ACTAf 2Ch Gain (Q) test vs Ibof at Trigger 1 Channel



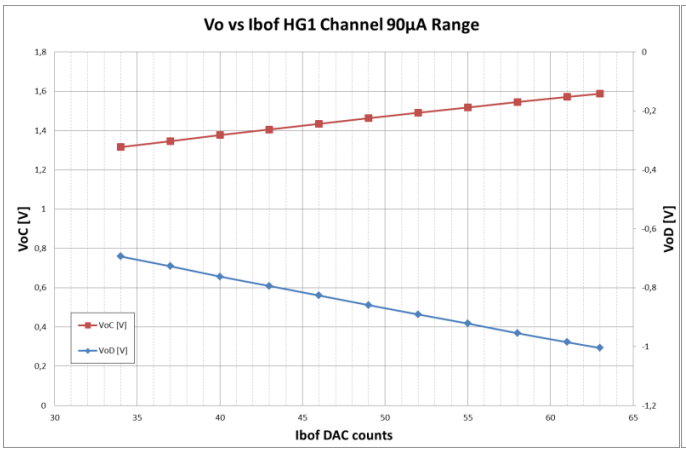
ACTAf 2Ch Gain (Q) test vs Ibof at Trigger 2 Channel



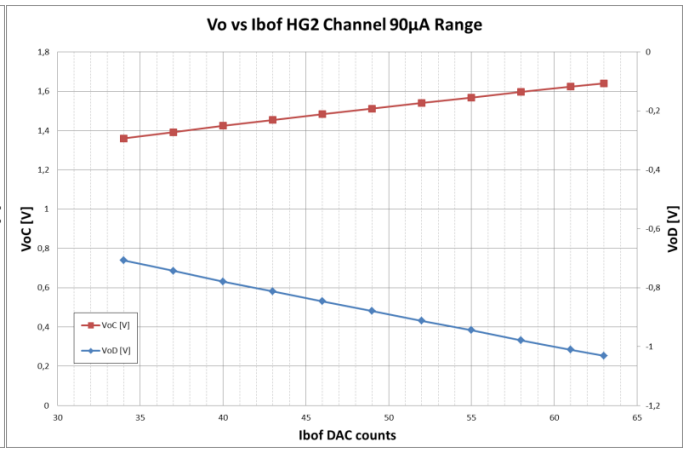
ACTAf 2Ch Error Gain (Q) test vs Ibof at Trigger 1 Channel



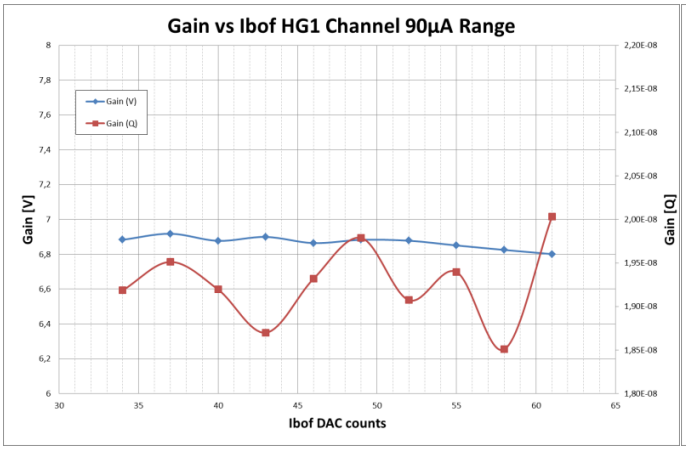
ACTAf 2Ch Error Gain (Q) test vs Ibof at Trigger 2 Channel



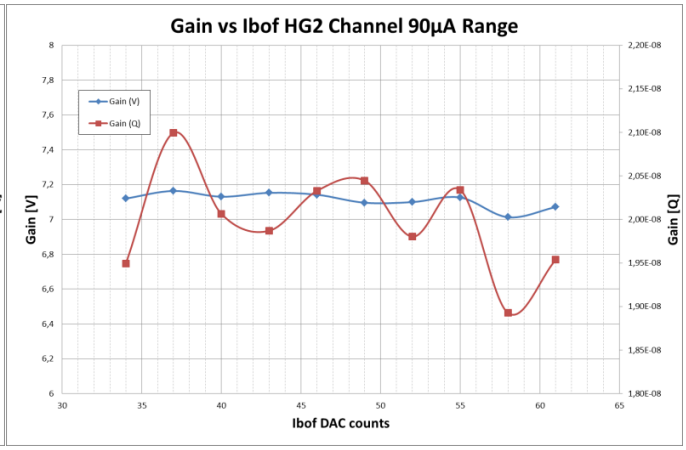
ACTAf 2Ch Linearity test vs Ibof (90µA Range) at High Gain 1 Channel



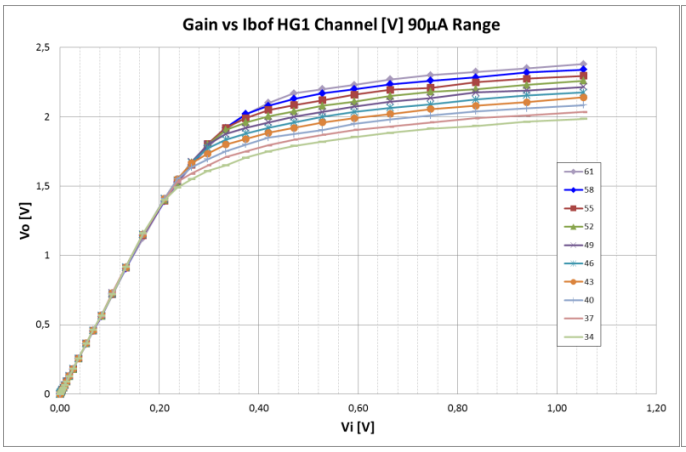
ACTAf 2Ch Linearity test vs Ibof at (90µA Range) High Gain 2 Channel



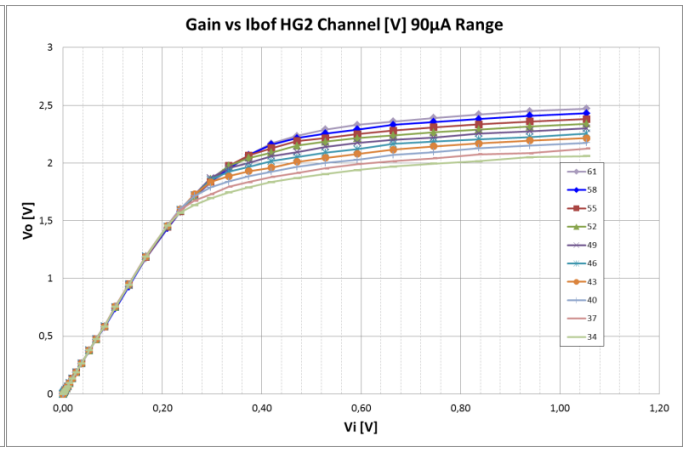
ACTAf 2Ch Gain test vs Ibof (90µA Range) at High Gain 1 Channel



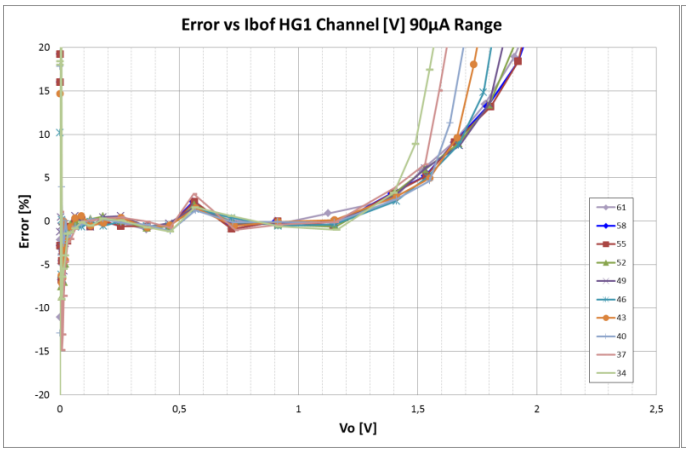
ACTAf 2Ch Gain test vs Ibof (90µA Range) at High Gain 2 Channel



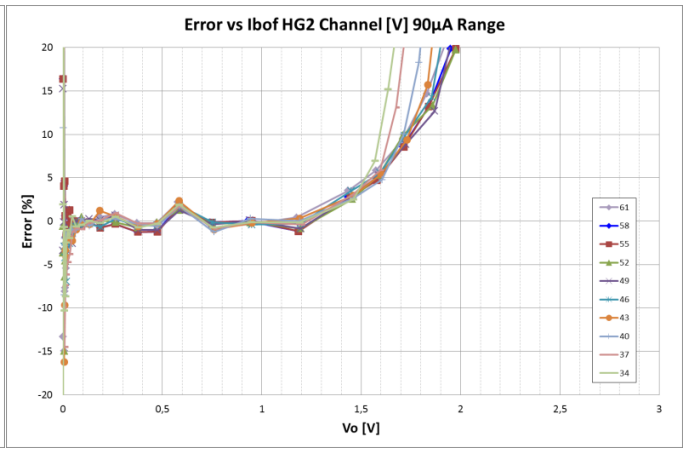
ACTAf 2Ch Gain (V) test vs Ibof (90µA Range) at High Gain 1 Channel



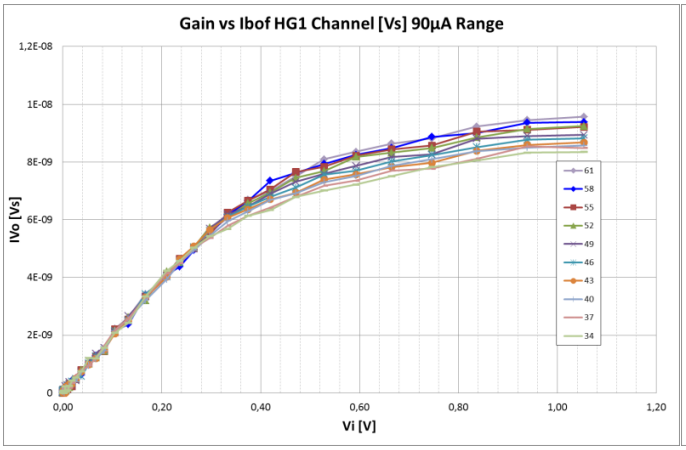
ACTAf 2Ch Gain (V) test vs Ibof (90µA Range) at High Gain 2 Channel



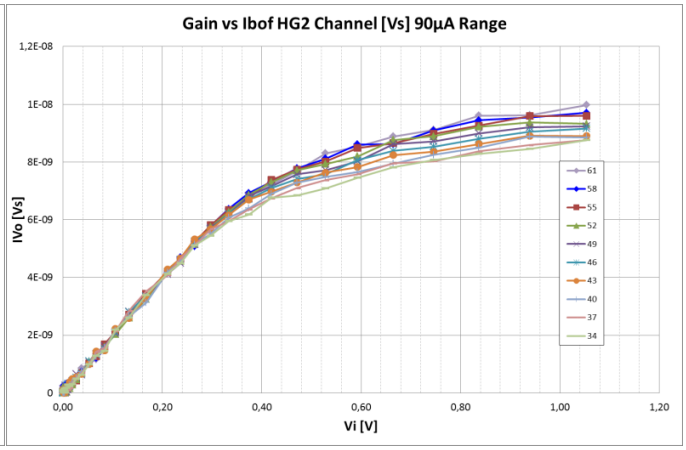
ACTAf 2Ch Error Gain (V) test vs Ibof (90µA Range) at High Gain 1 Channel



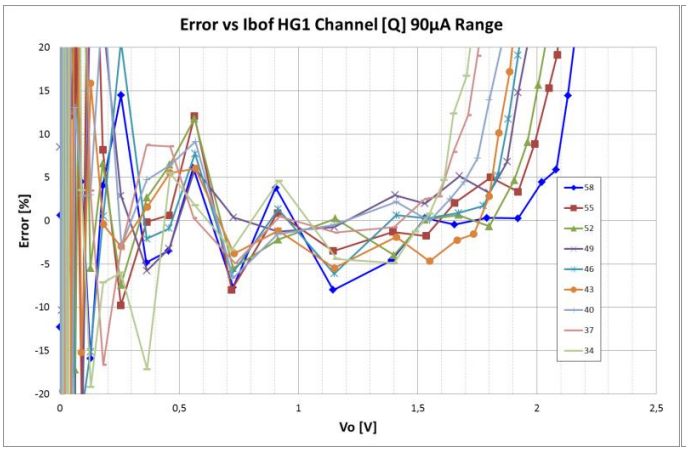
ACTAf 1Ch Error Gain (V) test vs Ibof (90µA Range) at High Gain 2 Channel



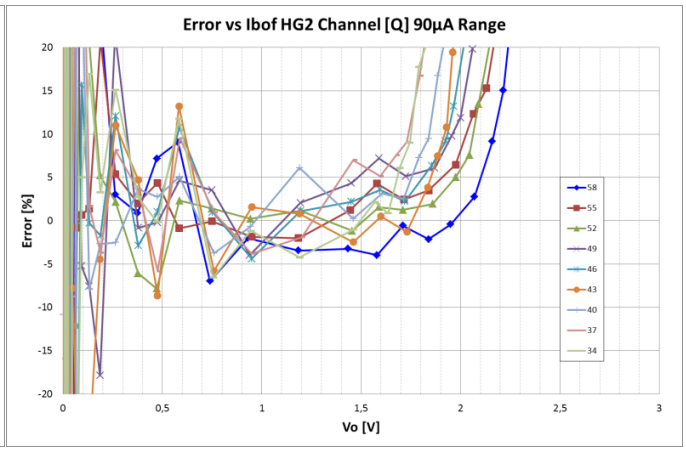
ACTAf 2Ch Gain (Q) test vs Ibof (90µA Range) at High Gain 1 Channel



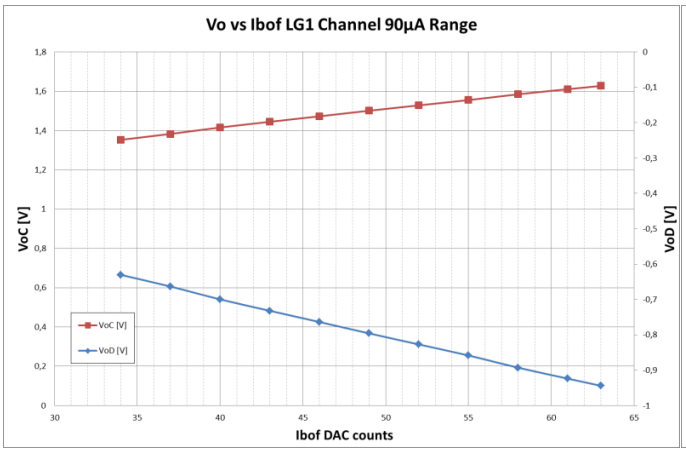
ACTAf 2Ch Gain (Q) test vs Ibof (90µA Range) at High Gain 2 Channel



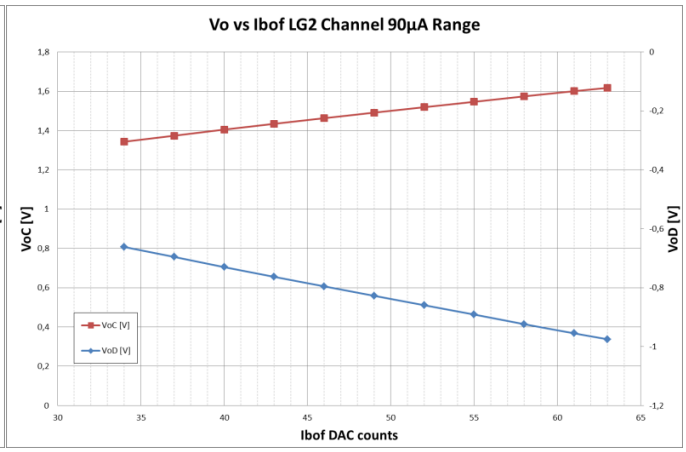
ACTAf 2Ch Error Gain (Q) test vs Ibof (90µA Range) at High Gain 1 Channel



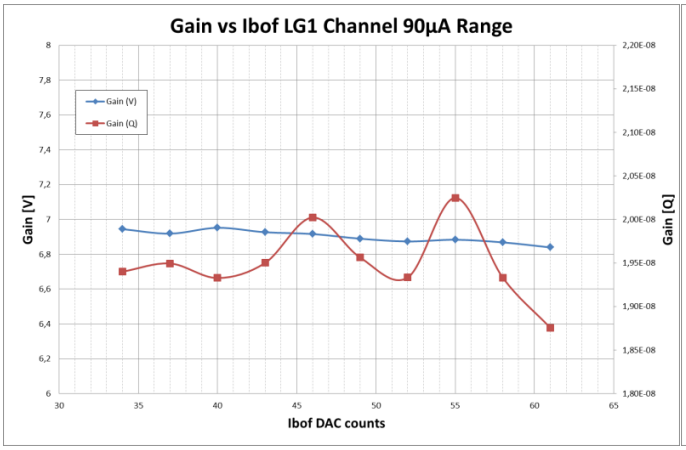
ACTAf 2Ch Error Gain (Q) test vs Ibof (90µA Range) at High Gain 2 Channel



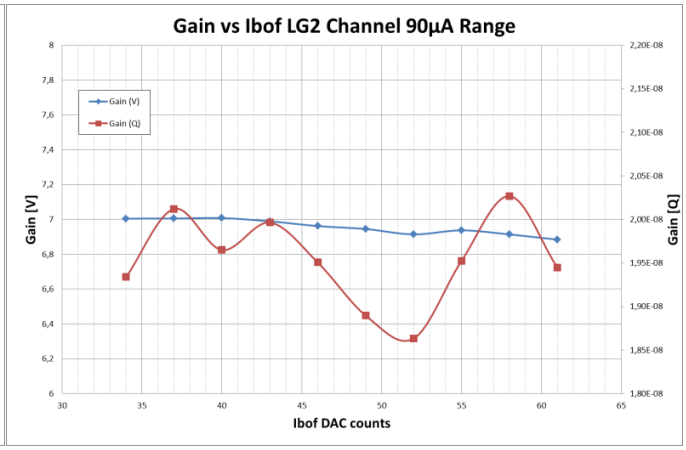
ACTAf 2Ch Linearity test vs Ibof (90µA Range) at Low Gain 1 Channel



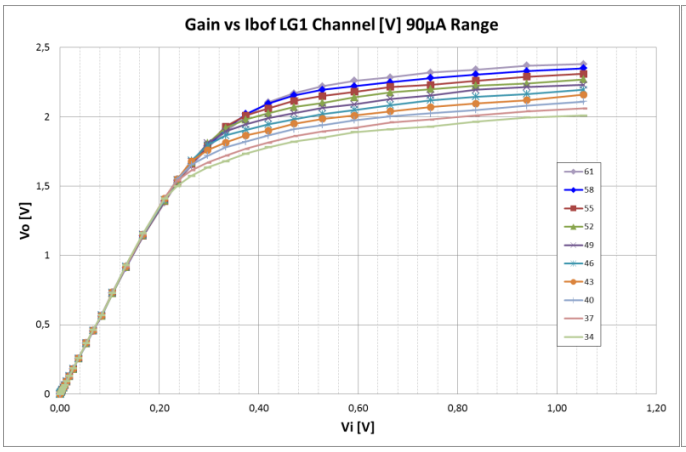
ACTAf 2Ch Linearity test vs Ibof (90µA Range) at Low Gain 2 Channel



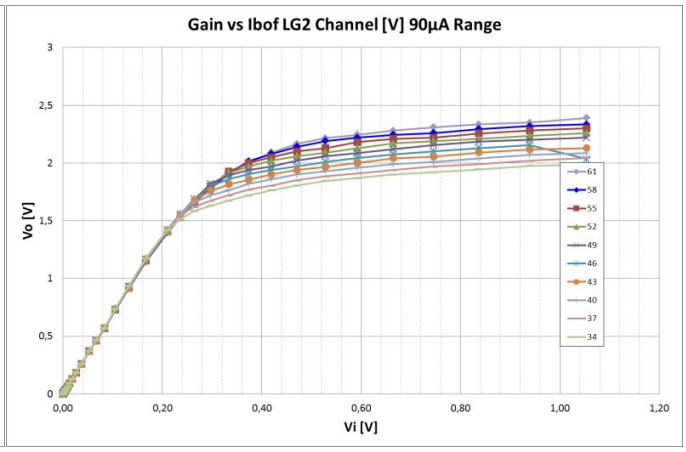
ACTAf 2Ch Gain test vs Ibof (90µA Range) at Low Gain 1 Channel



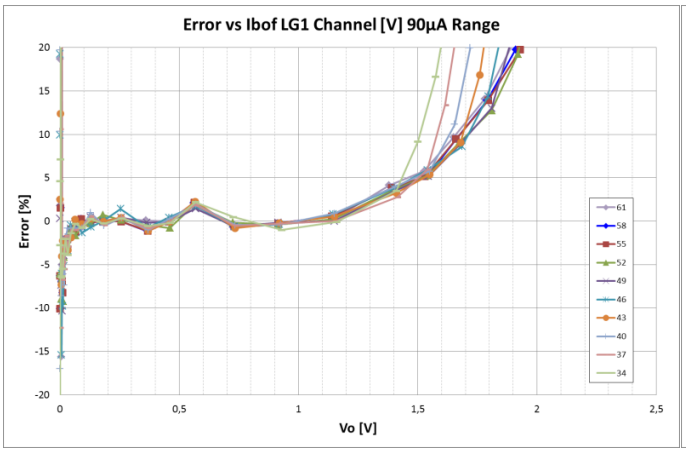
ACTAf 2Ch Gain test vs Ibof (90µA Range) at Low Gain 2 Channel



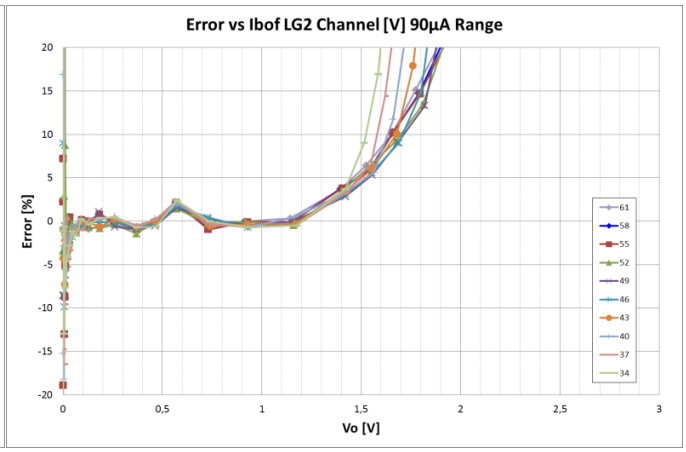
ACTAf 2Ch Gain (V) test vs Ibof (90µA Range) at Low Gain 1 Channel



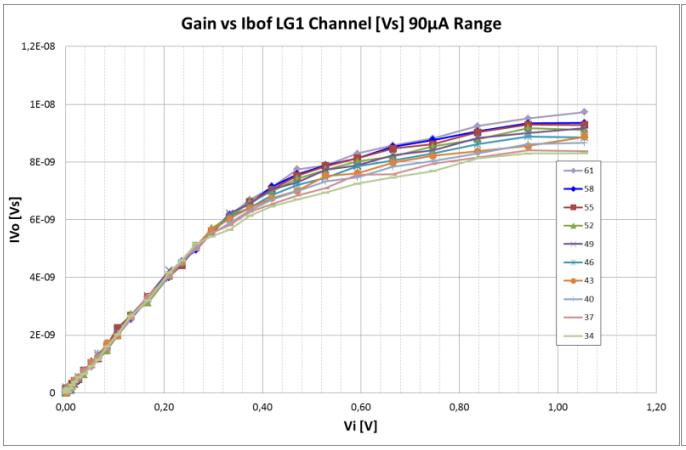
ACTAf 2Ch Gain (V) test vs Ibof (90µA Range) at Low Gain 2 Channel



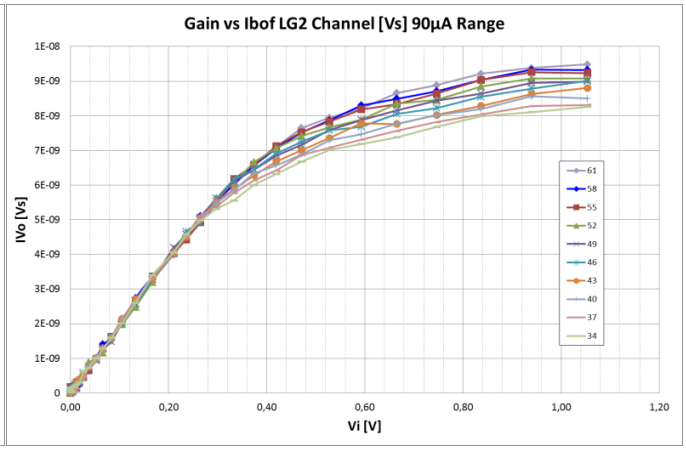
ACTAf 2Ch Error Gain (V) test vs Ibof (90µA Range) at Low Gain 1 Channel



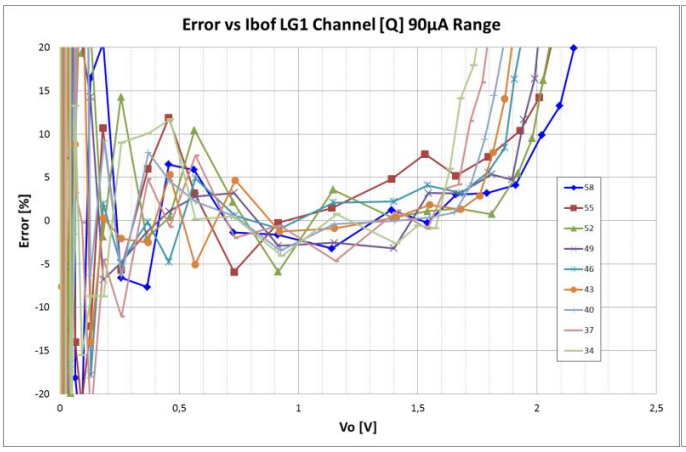
ACTAf 1Ch Error Gain (V) test vs Ibof (90µA Range) at Low Gain 2 Channel



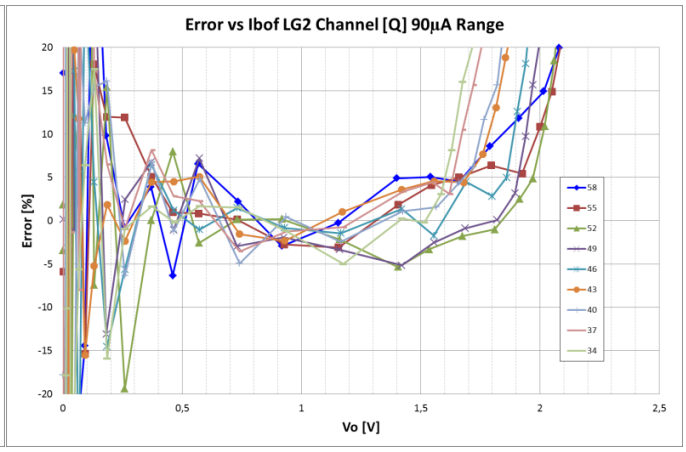
ACTAf 2Ch Gain (Q) test vs Ibof (90µA Range) at Low Gain 1 Channel



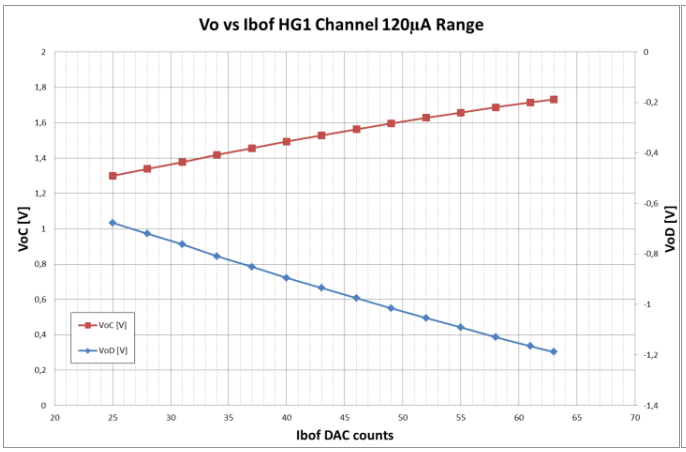
ACTAf 2Ch Gain (Q) test vs Ibof (90µA Range) at Low Gain 2 Channel



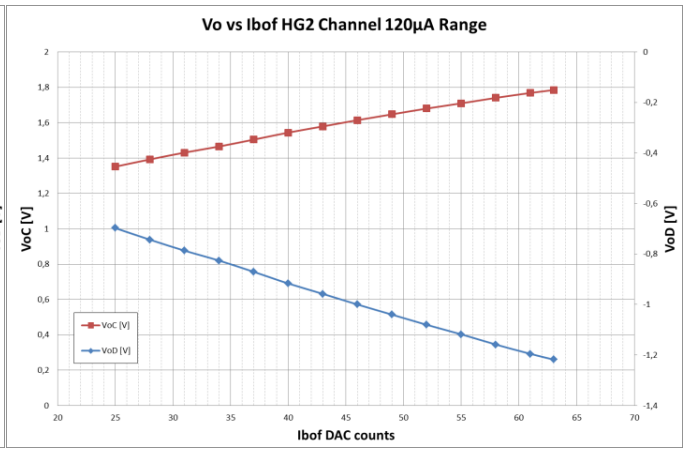
ACTAf 2Ch Error Gain (Q) test vs Ibof (90µA Range) at Low Gain 1 Channel



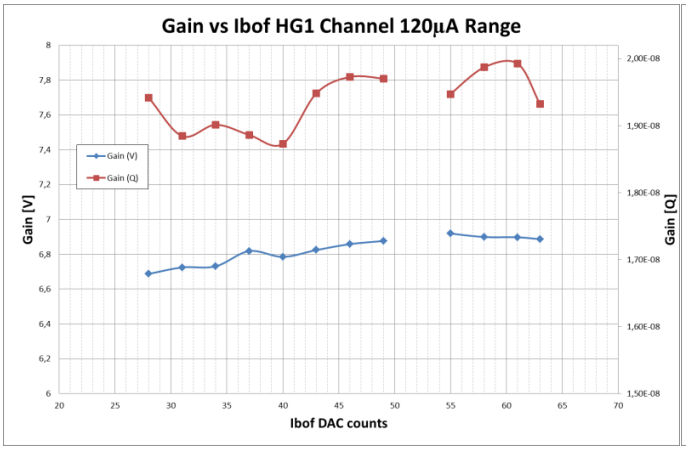
ACTAf 2Ch Error Gain (Q) test vs Ibof (90µA Range) at Low Gain 2 Channel



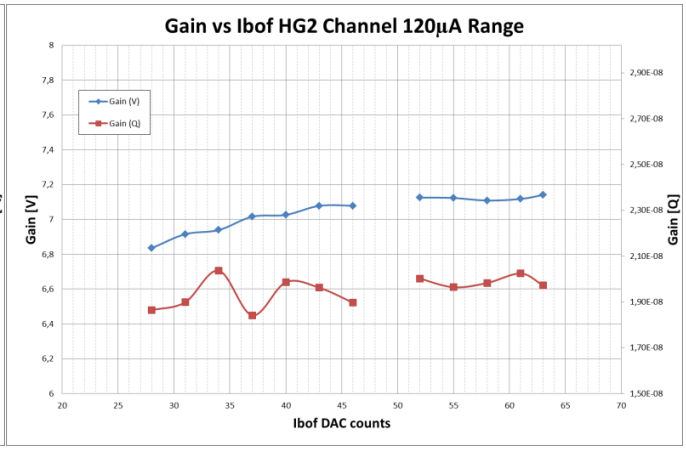
ACTAf 2Ch Linearity test vs Ibof (120µA Range) at High Gain 1 Channel



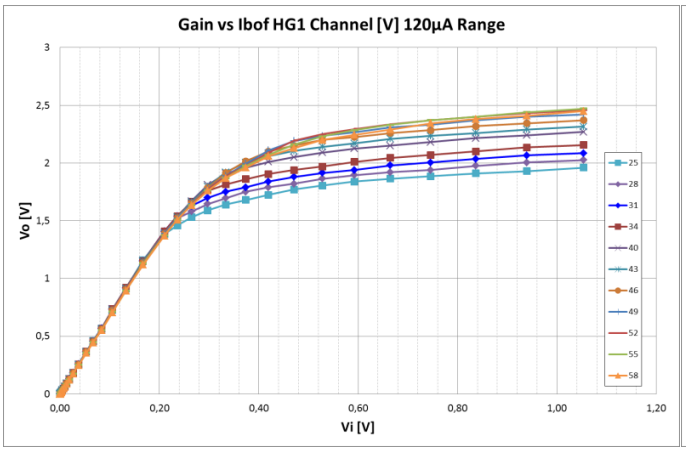
ACTAf 2Ch Linearity test vs Ibof (120µA Range) at High Gain 2 Channel



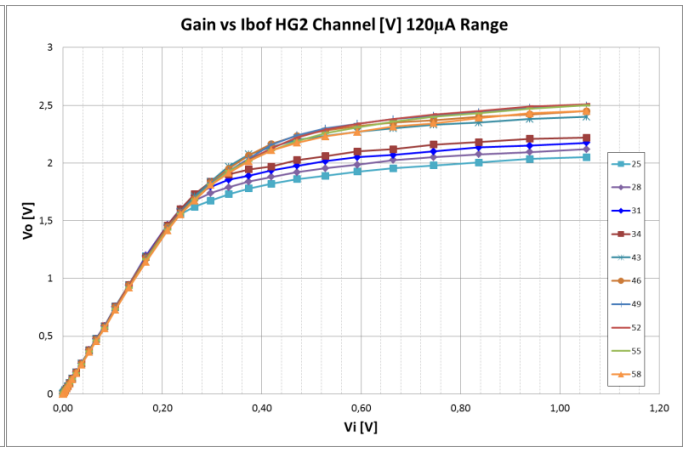
ACTAf 2Ch Gain test vs Ibof (120µA Range) at High Gain 1 Channel



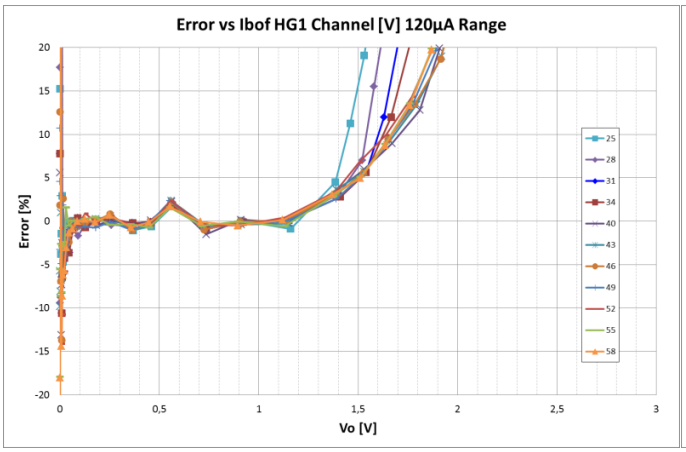
ACTAf 2Ch Gain test vs Ibof (120µA Range) at High Gain 2 Channel



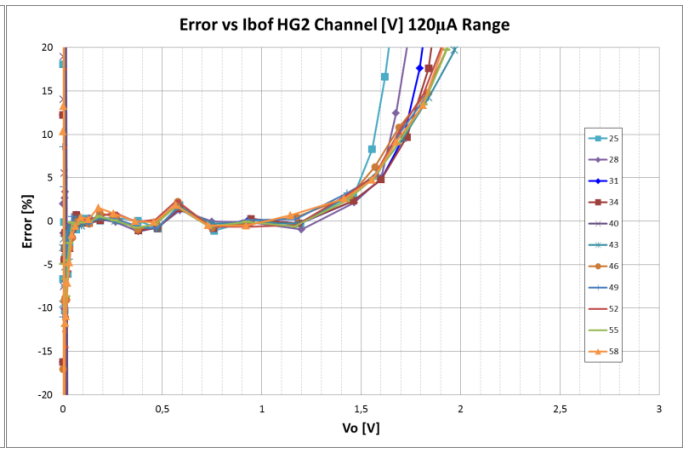
ACTAf 2Ch Gain (V) test vs Ibof (120µA Range) at High Gain 1 Channel



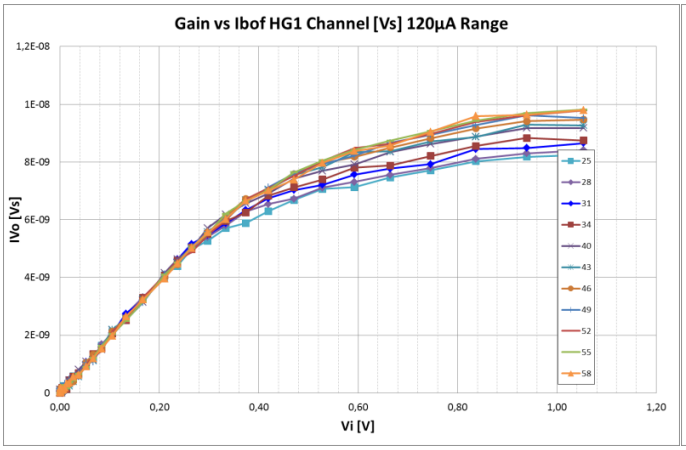
ACTAf 2Ch Gain (V) test vs Ibof (120µA Range) at High Gain 2 Channel



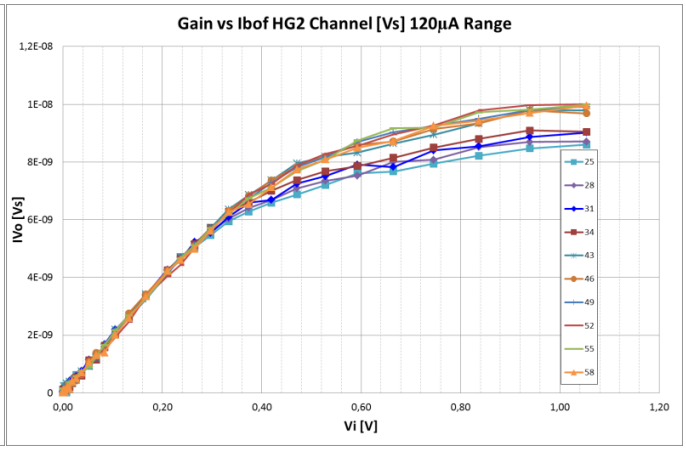
ACTAf 2Ch Error Gain (V) test vs Ibof (120µA Range) at High Gain 1 Channel



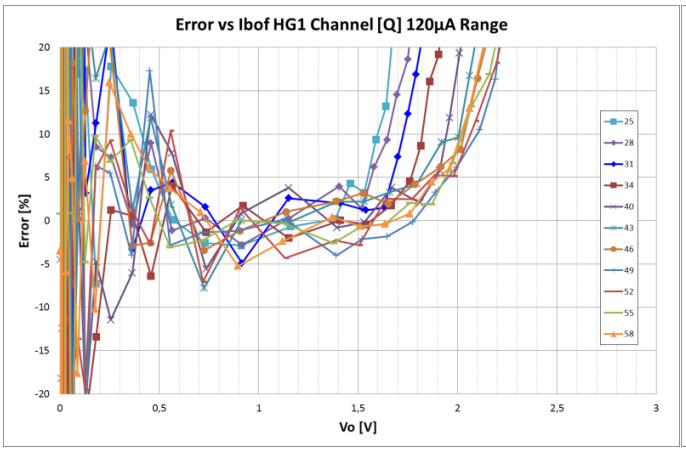
ACTAf 1Ch Error Gain (V) test vs Ibof (120µA Range) at High Gain 2 Channel



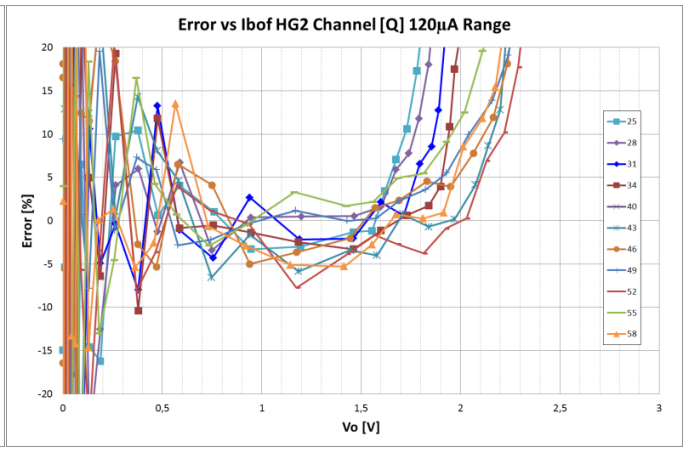
ACTAf 2Ch Gain (Q) test vs Ibof (120µA Range) at High Gain 1 Channel



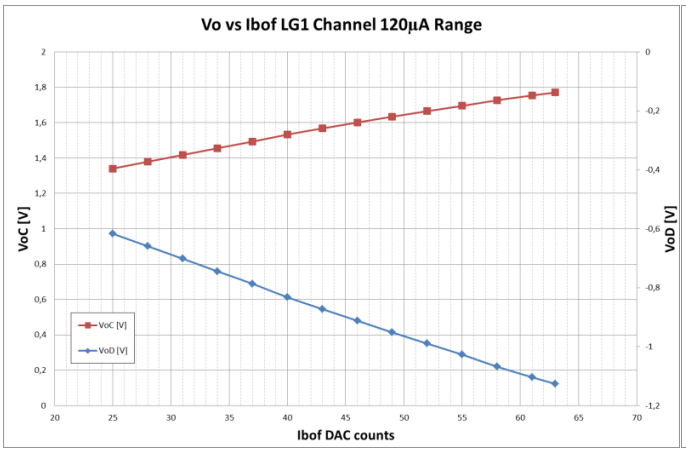
ACTAf 2Ch Gain (Q) test vs Ibof (120µA Range) at High Gain 2 Channel



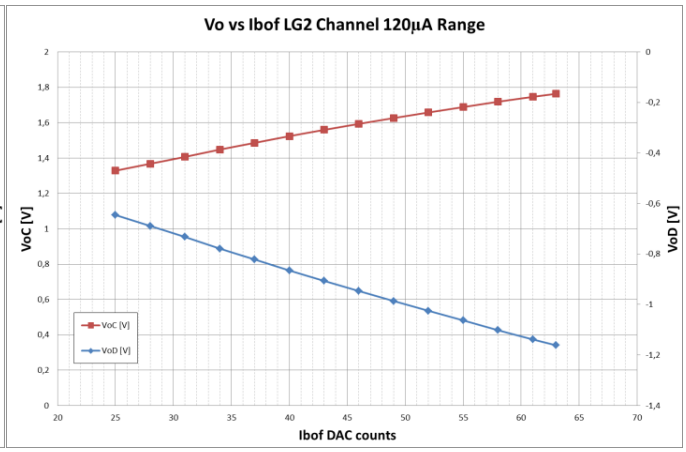
ACTAf 2Ch Error Gain (Q) test vs Ibof (120µA Range) at High Gain 1 Channel



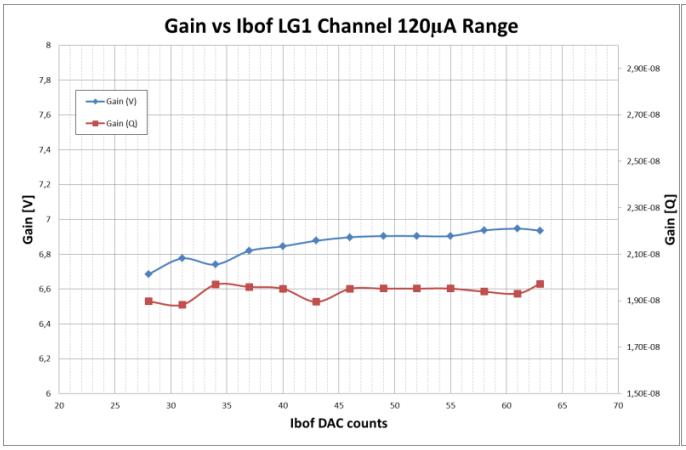
ACTAf 2Ch Error Gain (Q) test vs Ibof (120µA Range) at High Gain 2 Channel



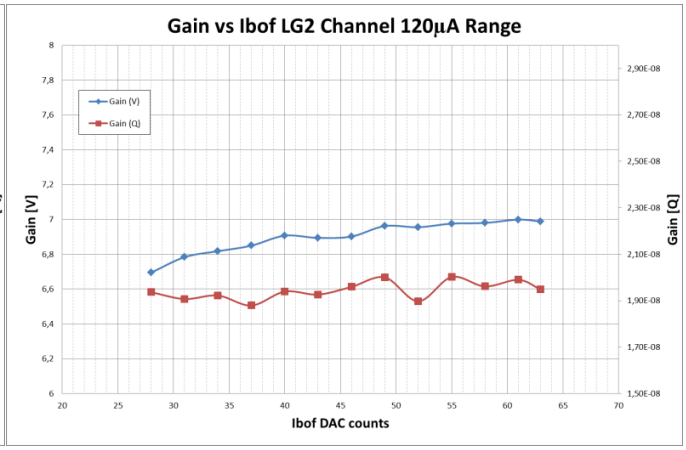
ACTAf 2Ch Linearity test vs Ibof (120µA Range) at Low Gain 1 Channel



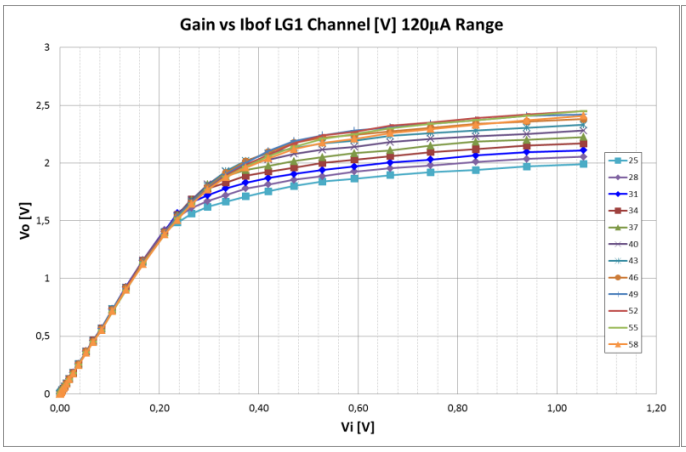
ACTAf 2Ch Linearity test vs Ibof (120µA Range) at Low Gain 2 Channel



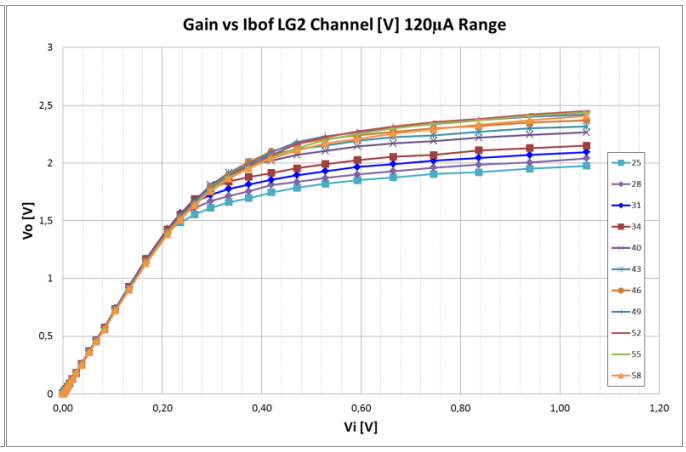
ACTAf 2Ch Gain test vs Ibof (120µA Range) at Low Gain 1 Channel



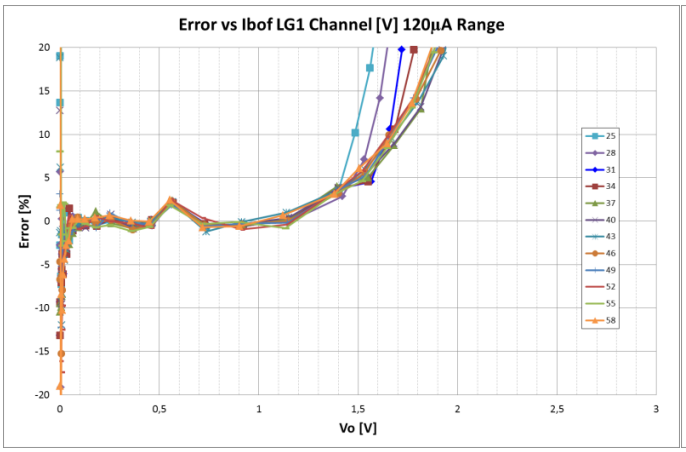
ACTAf 2Ch Gain test vs Ibof (120µA Range) at Low Gain 2 Channel



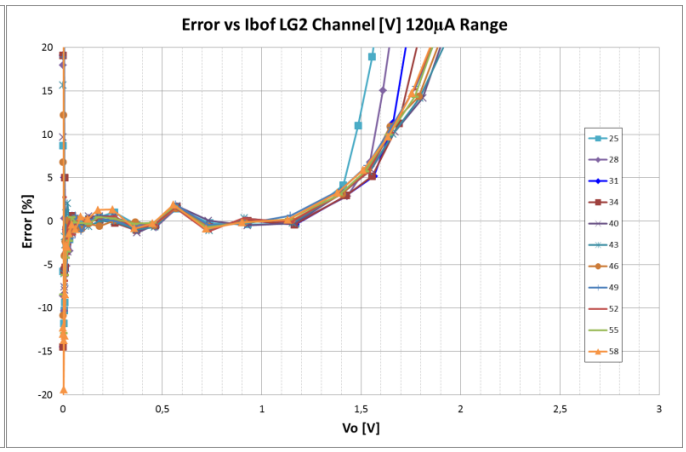
ACTAf 2Ch Gain (V) test vs Ibof (120µA Range) at Low Gain 1 Channel



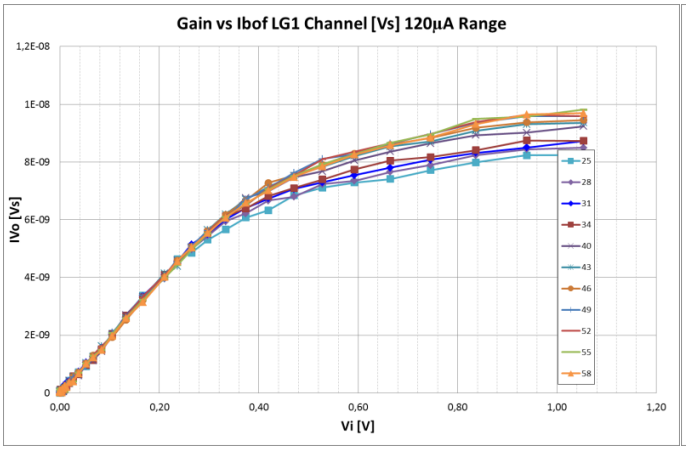
ACTAf 2Ch Gain (V) test vs Ibof (120µA Range) at Low Gain 2 Channel



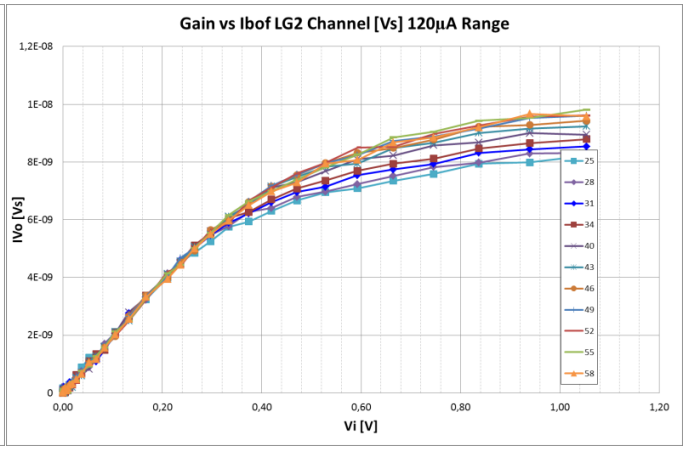
ACTAf 2Ch Error Gain (V) test vs Ibof (120µA Range) at Low Gain 1 Channel



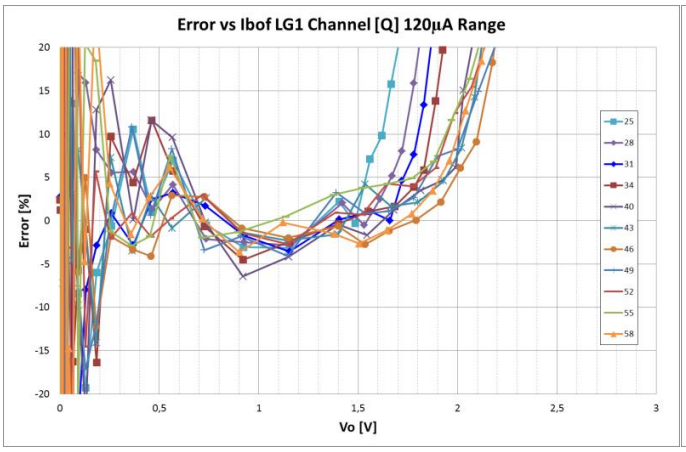
ACTAf 1Ch Error Gain (V) test vs Ibof (120µA Range) at Low Gain 2 Channel



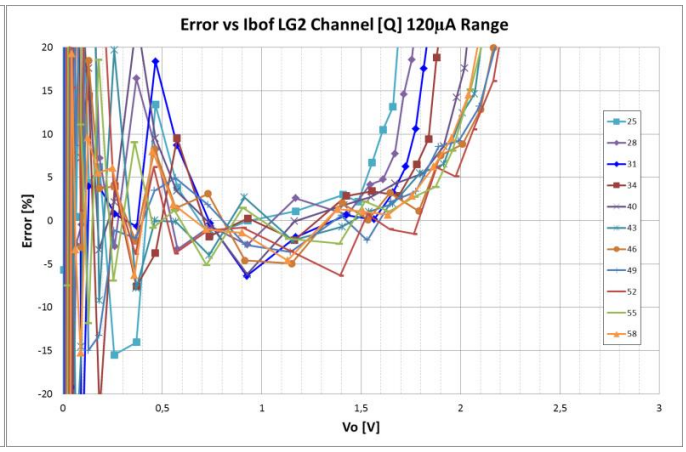
ACTAf 2Ch Gain (Q) test vs Ibof (120µA Range) at Low Gain 1 Channel



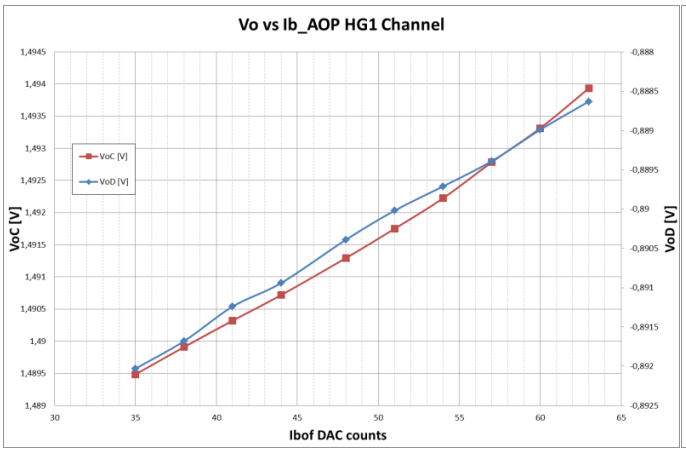
ACTAf 2Ch Gain (Q) test vs Ibof (120µA Range) at Low Gain 2 Channel



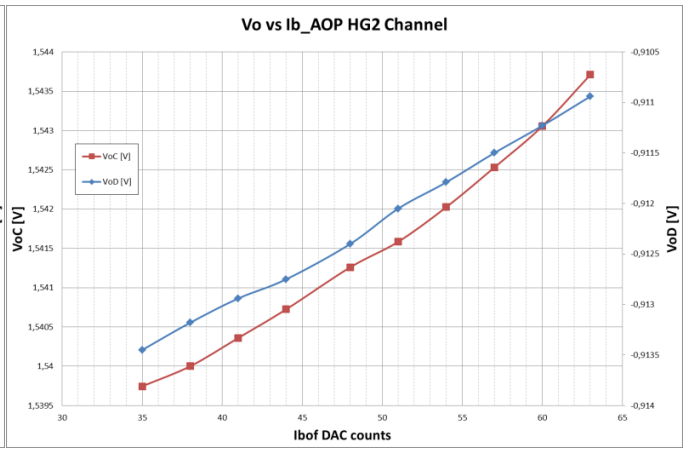
ACTAf 2Ch Error Gain (Q) test vs Ibof (120µA Range) at Low Gain 1 Channel



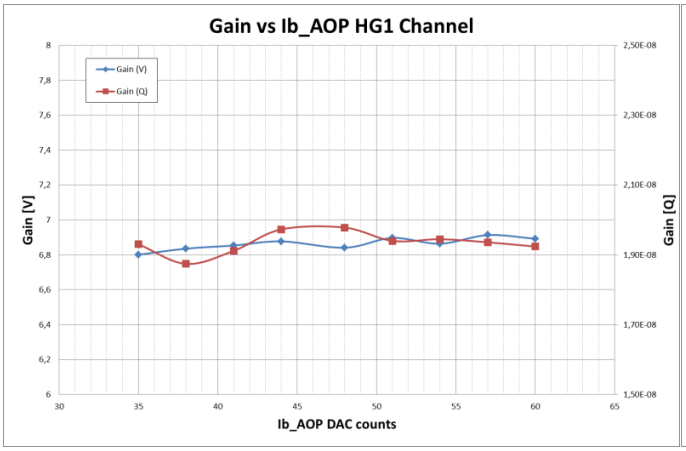
ACTAf 2Ch Error Gain (Q) test vs Ibof (90µA Range) at Low Gain 2 Channel



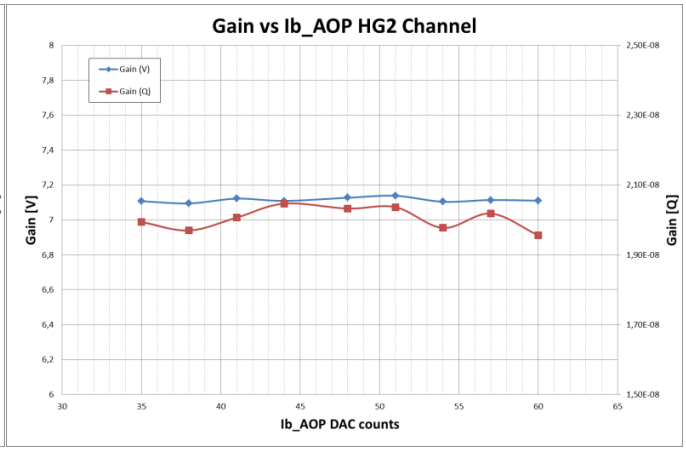
ACTAf 2Ch Linearity test vs Ib_AOP at High Gain 1 Channel



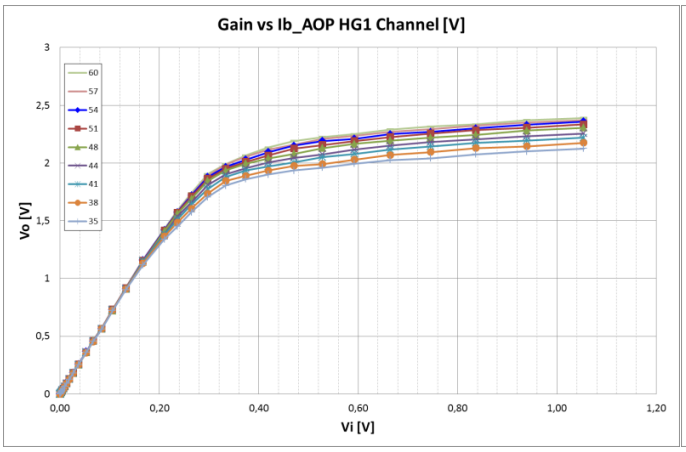
ACTAf 2Ch Linearity test vs Ib_AOP at High Gain 2 Channel



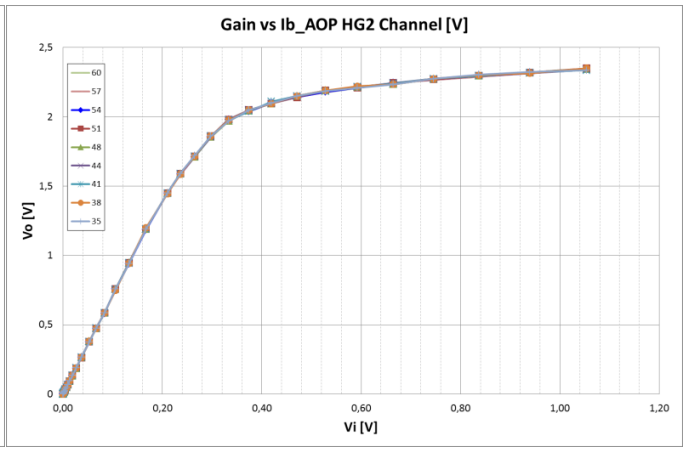
ACTAf 2Ch Gain test vs Ib_AOP at High Gain 1 Channel



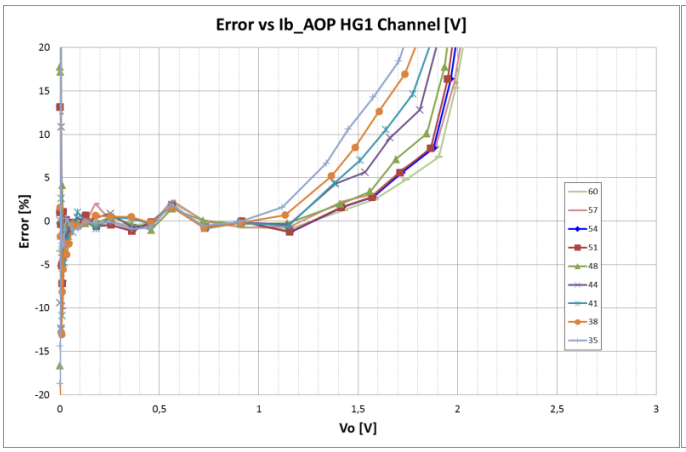
ACTAf 2Ch Gain test vs Ib_AOP at High Gain 2 Channel



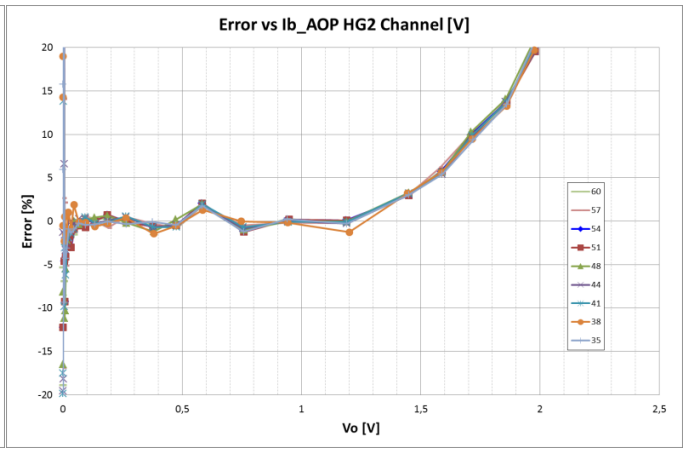
ACTAf 2Ch Gain (V) test vs Ib_AOP at High Gain 1 Channel



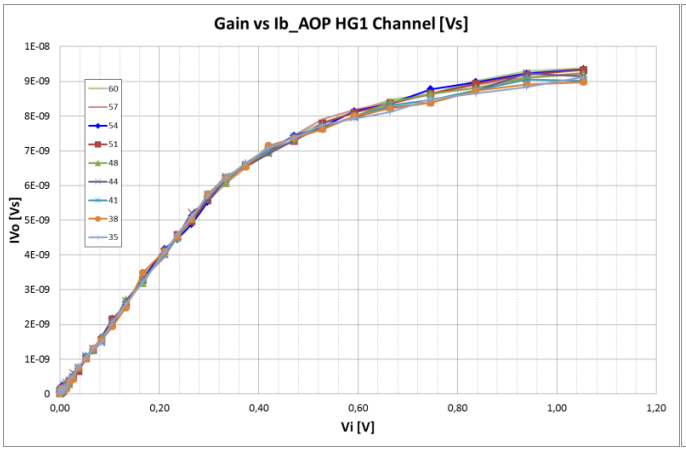
ACTAf 2Ch Gain (V) test vs Ib_AOP at High Gain 2 Channel



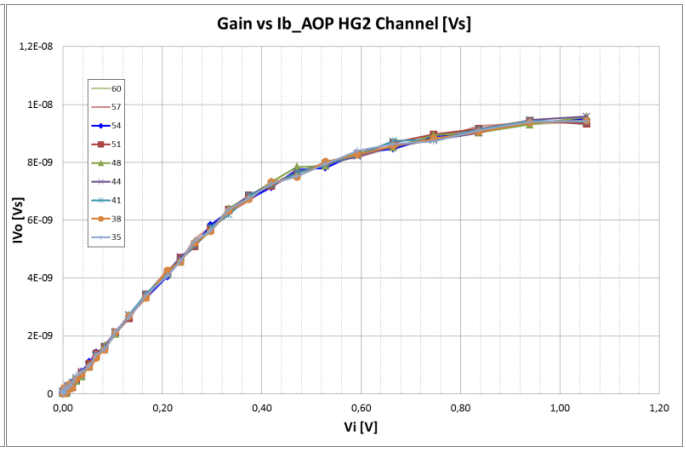
ACTAf 2Ch Error Gain (V) test vs Ib_AOP at High Gain 1 Channel



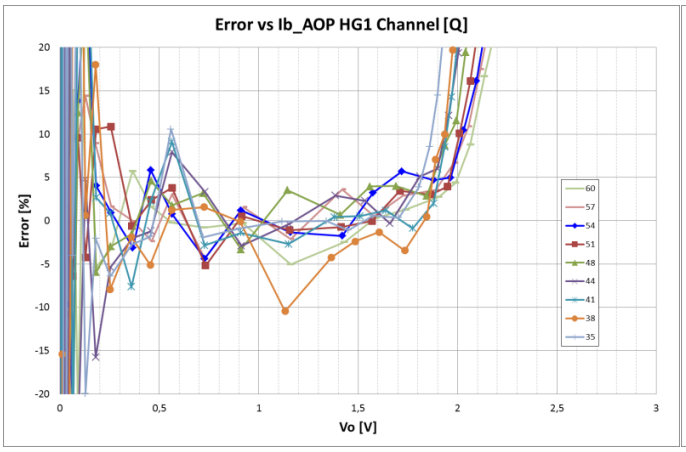
ACTAf 1Ch Error Gain (V) test vs Ib_AOP at High Gain 2 Channel



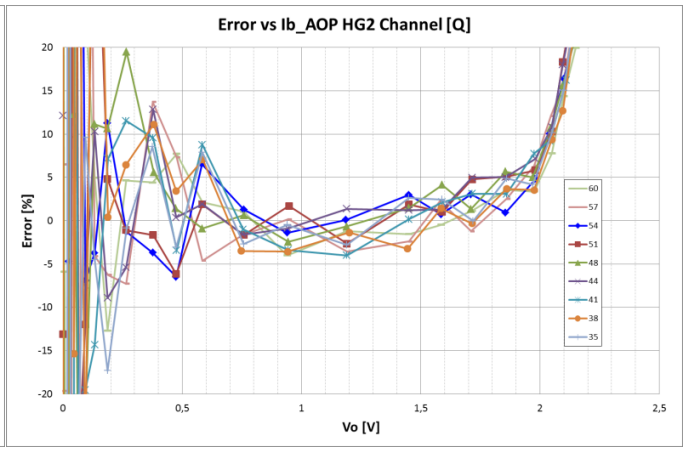
ACTAf 2Ch Gain (Q) test vs Ib_AOP at High Gain 1 Channel



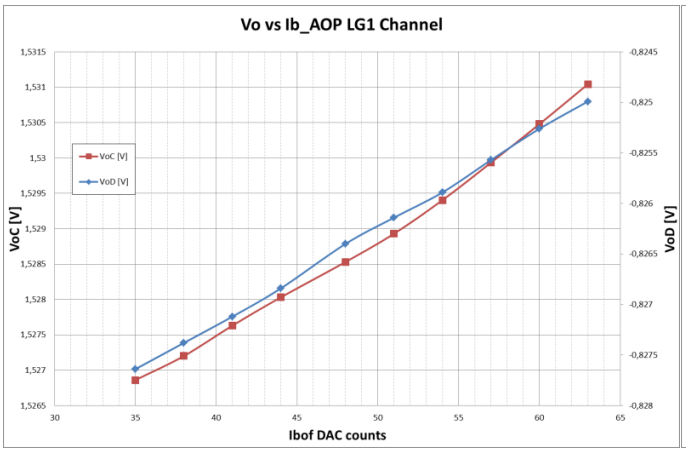
ACTAf 2Ch Gain (Q) test vs Ib_AOP at High Gain 2 Channel



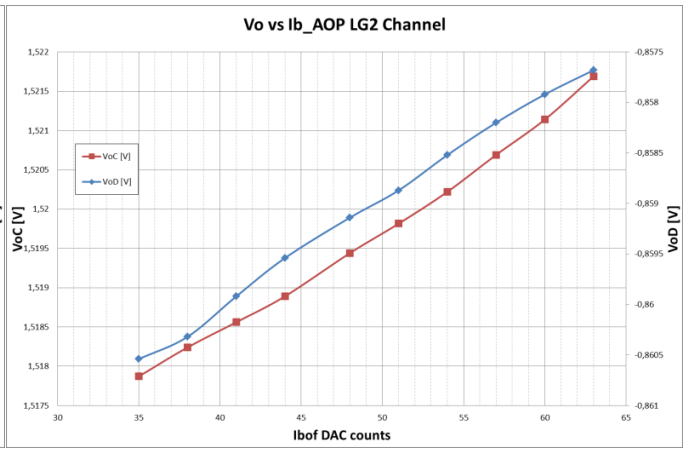
ACTAf 2Ch Error Gain (Q) test vs Ib_AOP at High Gain 1 Channel



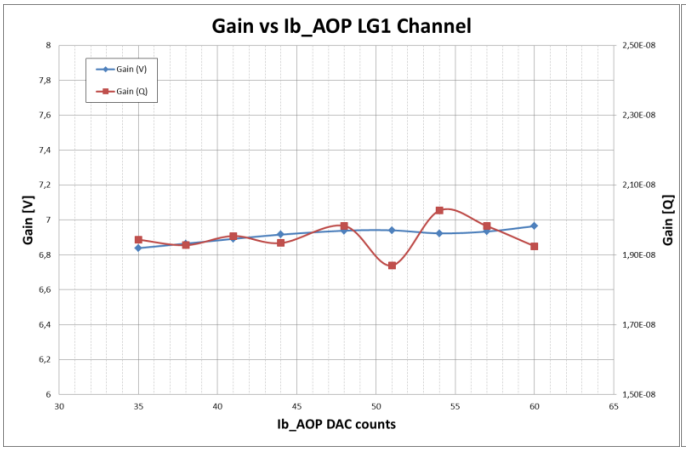
ACTAf 2Ch Error Gain (Q) test vs Ib_AOP at High Gain 2 Channel



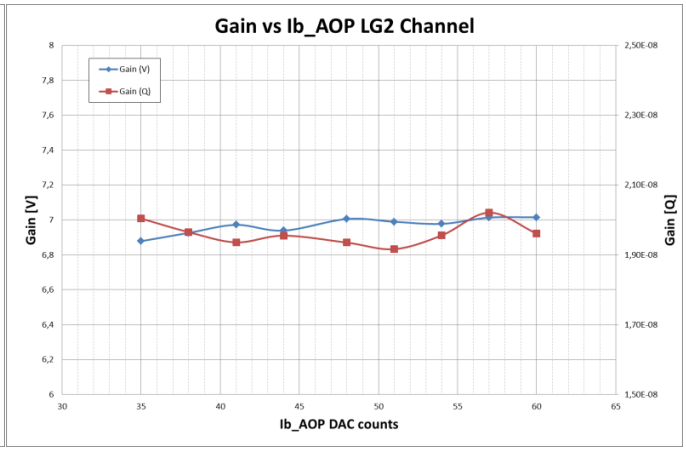
ACTAf 2Ch Linearity test vs Ib_AOP at Low Gain 1 Channel



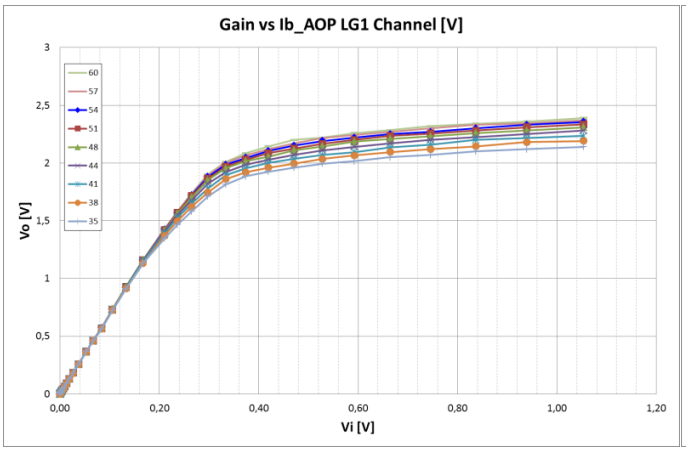
ACTAf 2Ch Linearity test vs Ib_AOP at Low Gain 2 Channel



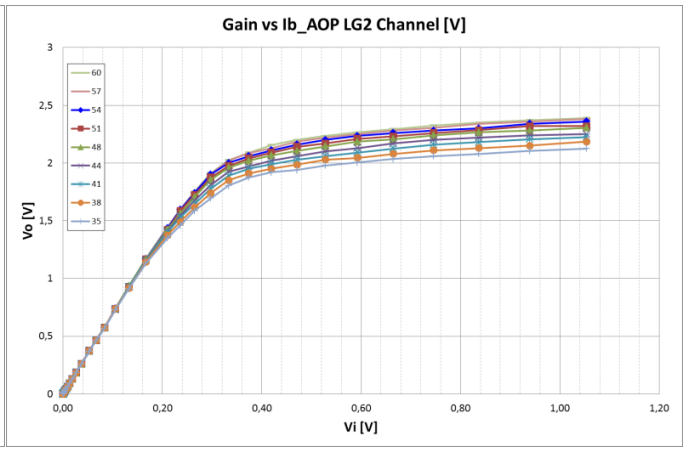
ACTAf 2Ch Gain test vs Ib_AOP at Low Gain 1 Channel



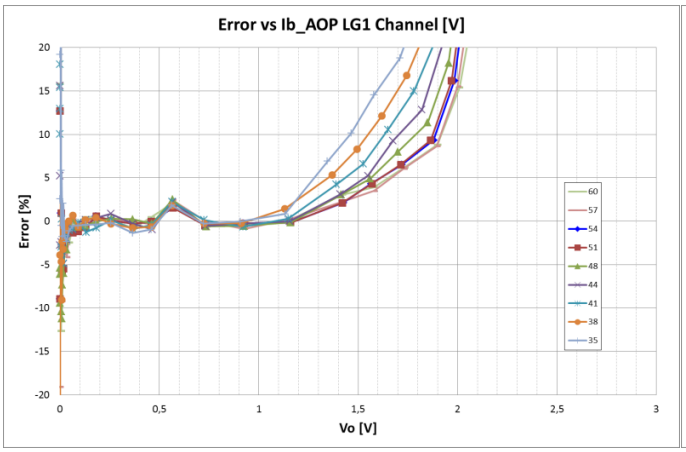
ACTAf 2Ch Gain test vs Ib_AOP at Low Gain 2 Channel



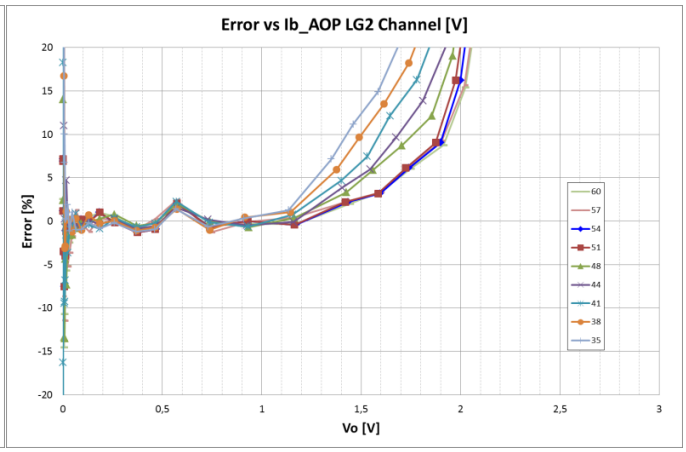
ACTAf 2Ch Gain (V) test vs Ib_AOP at Low Gain 1 Channel



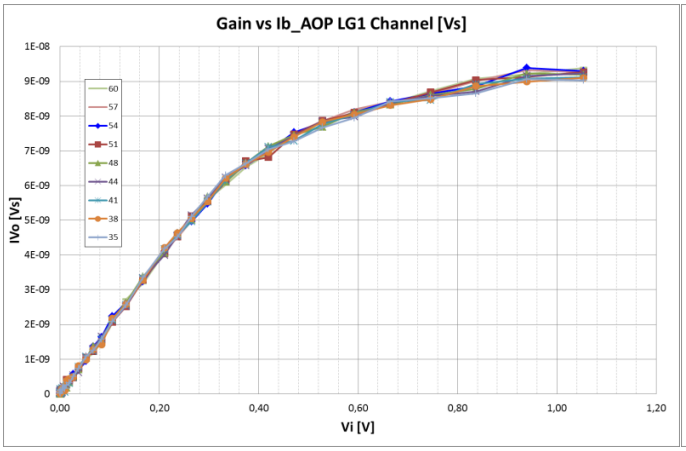
ACTAf 2Ch Gain (V) test vs Ib_AOP at Low Gain 2 Channel



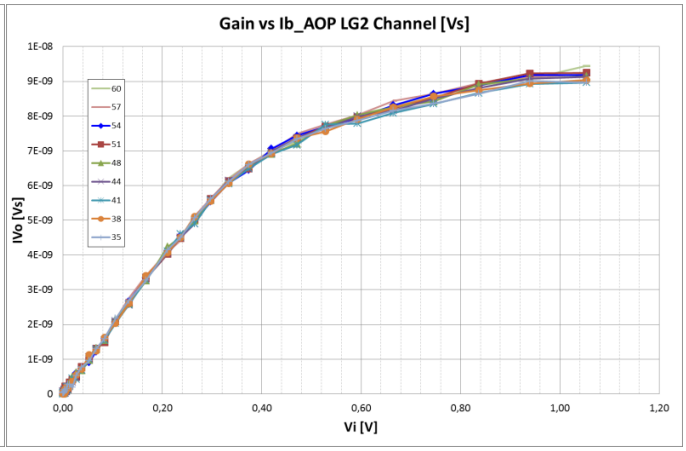
ACTAf 2Ch Error Gain (V) test vs Ib_AOP at Low Gain 1 Channel



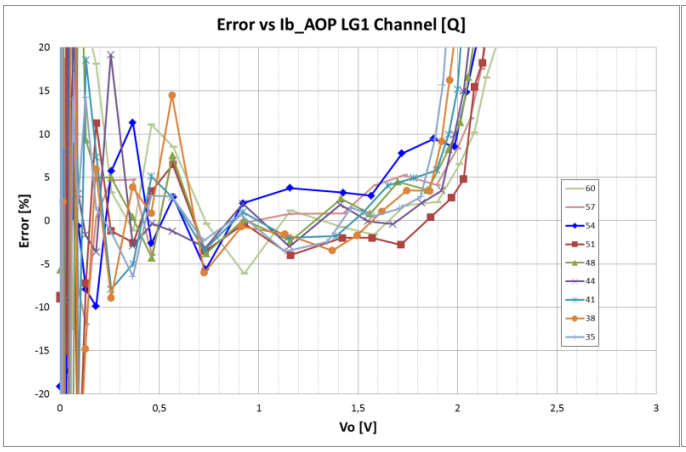
ACTAf 1Ch Error Gain (V) test vs Ib_AOP at Low Gain 2 Channel



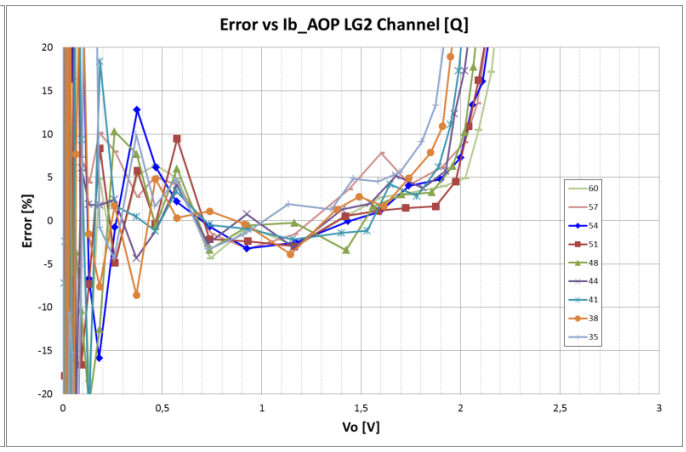
ACTAf 2Ch Gain (Q) test vs Ib_AOP at Low Gain 1 Channel



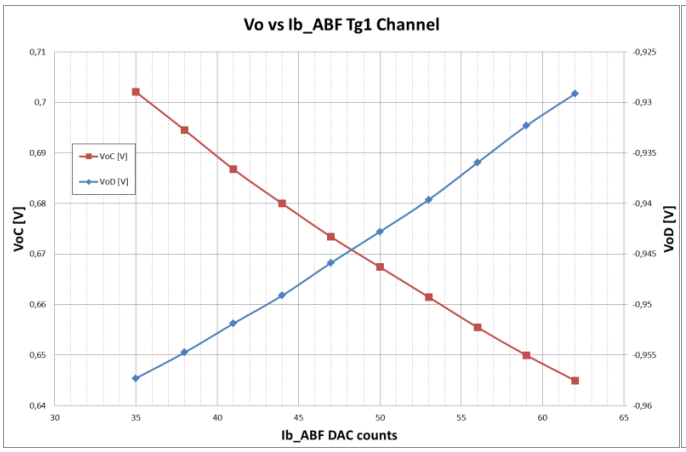
ACTAf 2Ch Gain (Q) test vs Ib_AOP at Low Gain 2 Channel



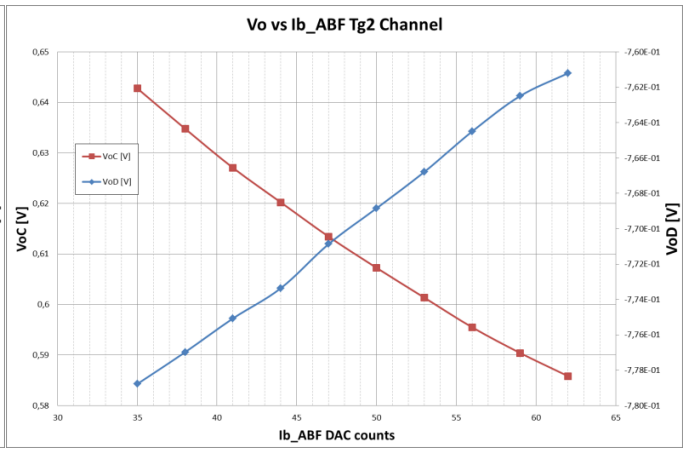
ACTAf 2Ch Error Gain (Q) test vs Ib_AOP at Low Gain 1 Channel



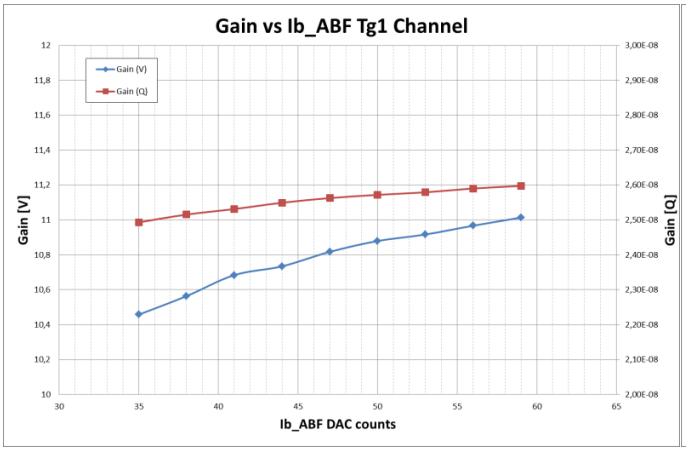
ACTAf 2Ch Error Gain (Q) test vs Ib_AOP at Low Gain 2 Channel



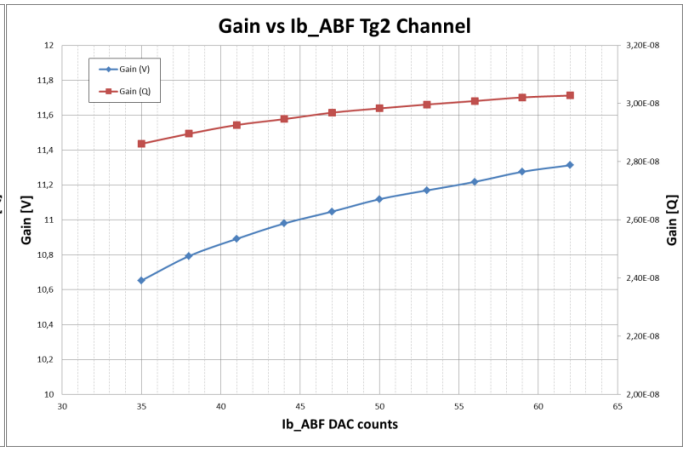
ACTAf 2Ch Linearity test vs Ib_ABF at Trigger 1 Channel



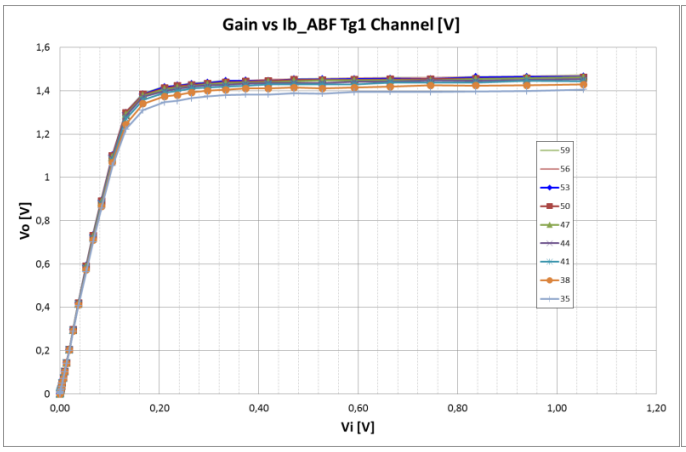
ACTAf 2Ch Linearity test vs Ib_ABF at Trigger 2 Channel



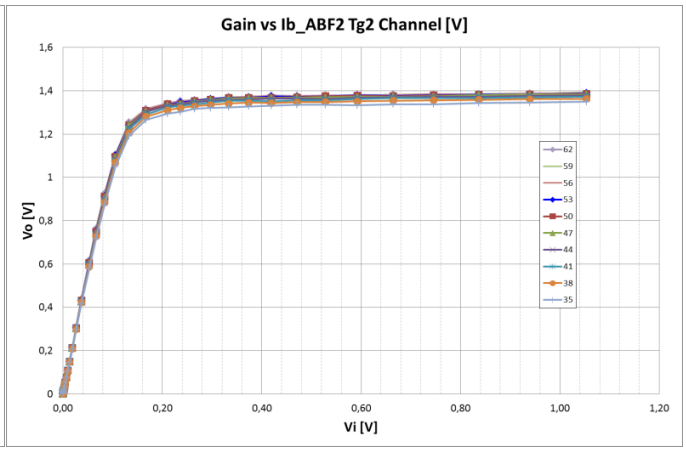
ACTAf 2Ch Gain test vs Ib_ABF at Trigger 1 Channel



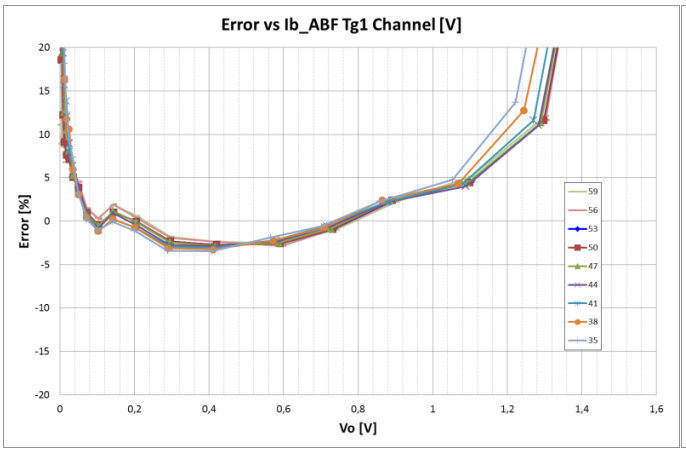
ACTAf 2Ch Gain test vs Ib_ABF at Trigger 2 Channel



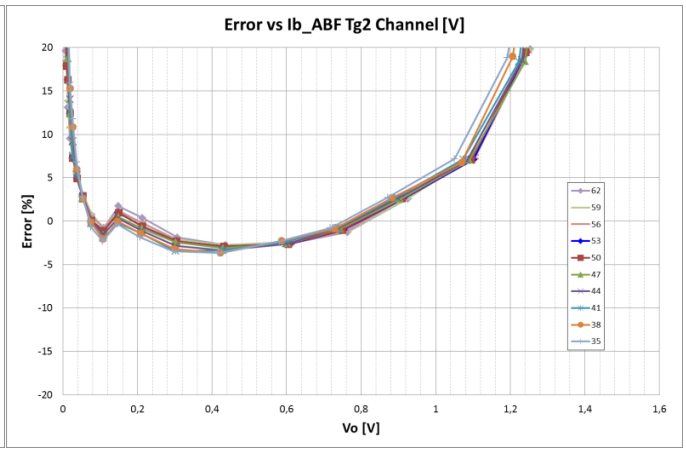
ACTAf 2Ch Gain (V) test vs Ib_ABF at Trigger 1 Channel



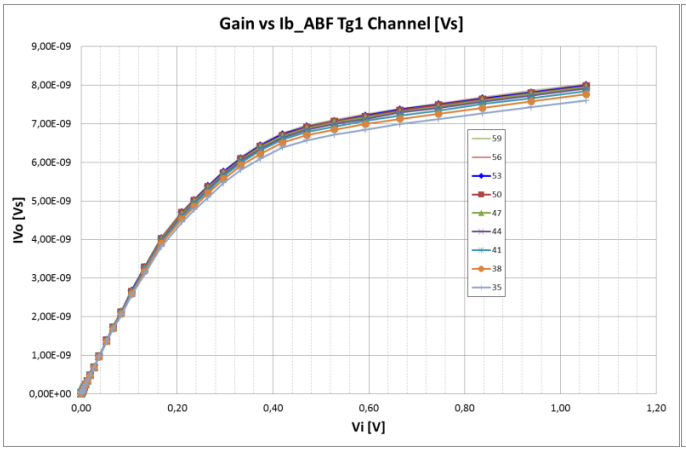
ACTAf 2Ch Gain (V) test vs Ib_ABF at Trigger 2 Channel



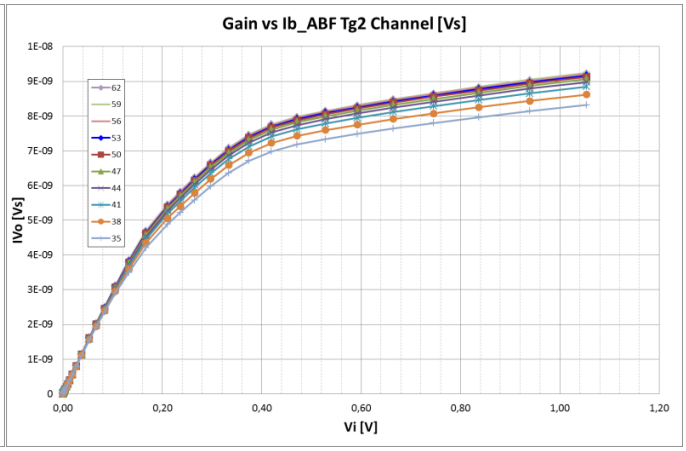
ACTAf 2Ch Error Gain (V) test vs Ib_ABF at Trigger 1 Channel



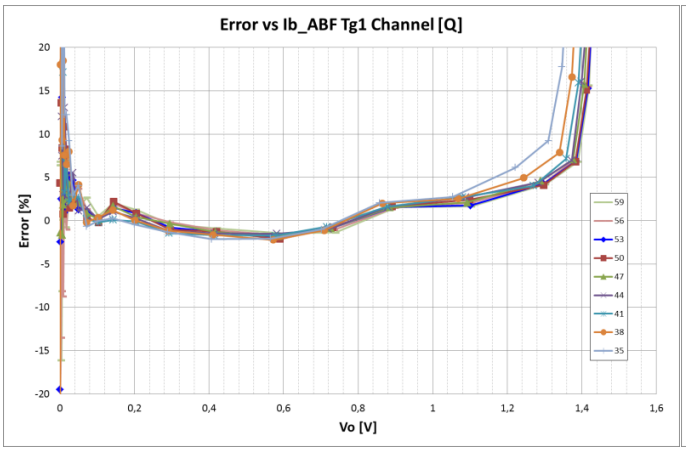
ACTAf 1Ch Error Gain (V) test vs Ib_ABF at Trigger 2 Channel



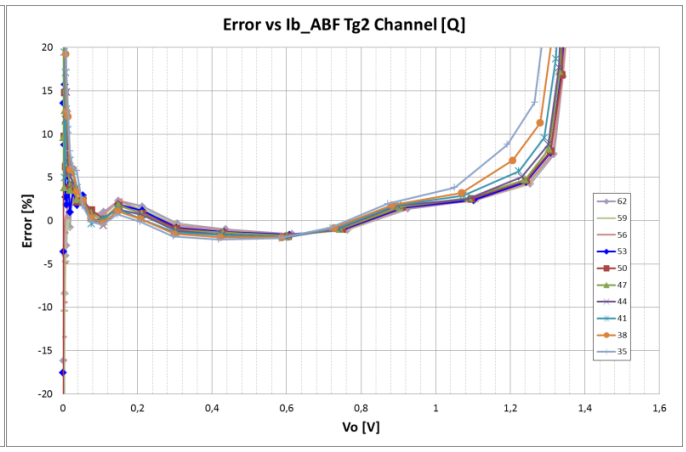
ACTAf 2Ch Gain (Q) test vs Ib_ABF at Trigger 1 Channel



ACTAf 2Ch Gain (Q) test vs Ib_ABF at Trigger 2 Channel



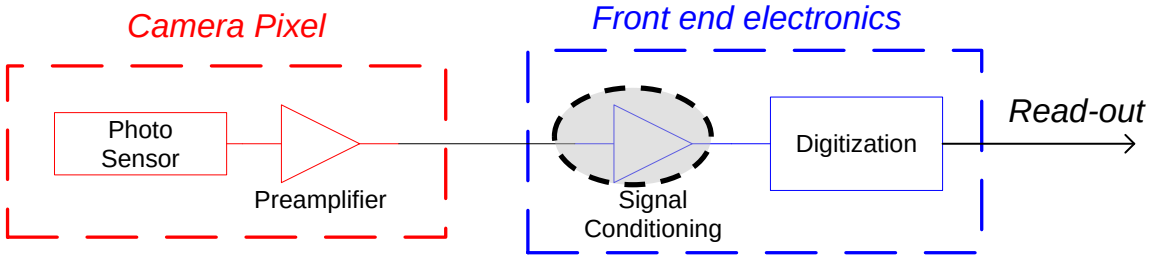
ACTAf 2Ch Error Gain (Q) test vs Ib_ABF at Trigger 1 Channel



ACTAf 2Ch Error Gain (Q) test vs Ib_ABF at Trigger 2 Channel

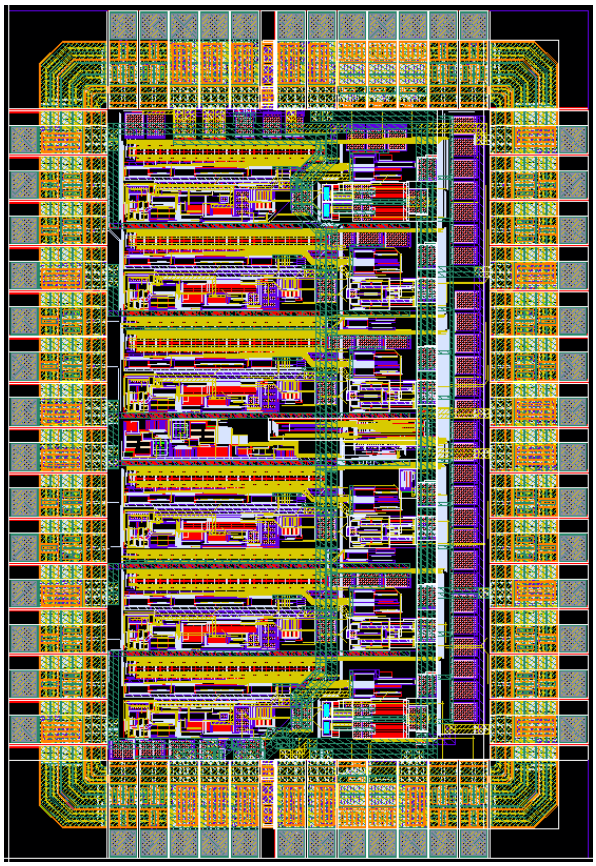
APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUITS



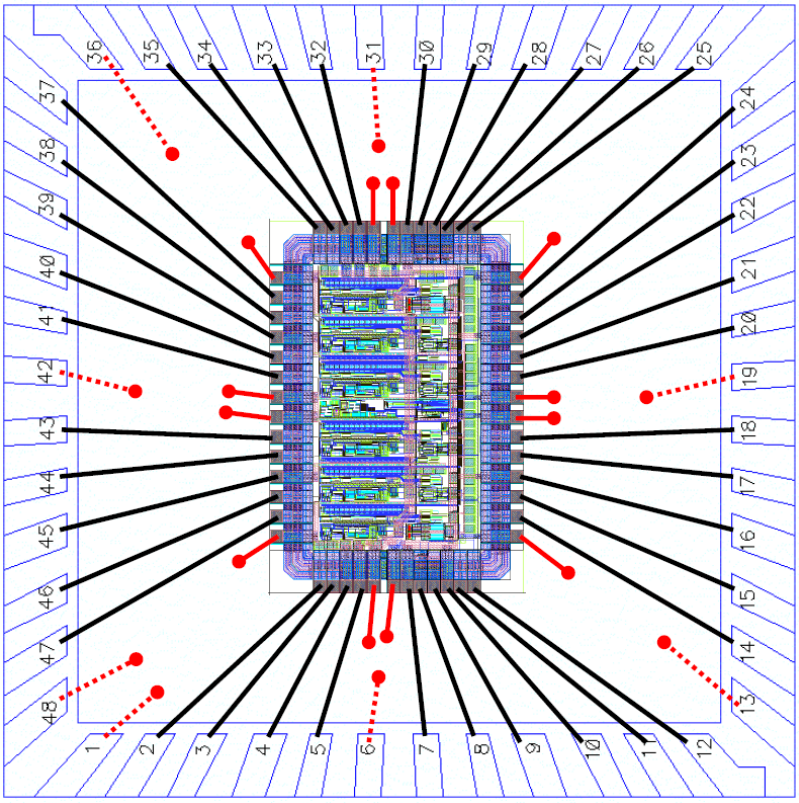
ACTAf typical application circuit diagram

LAYOUT



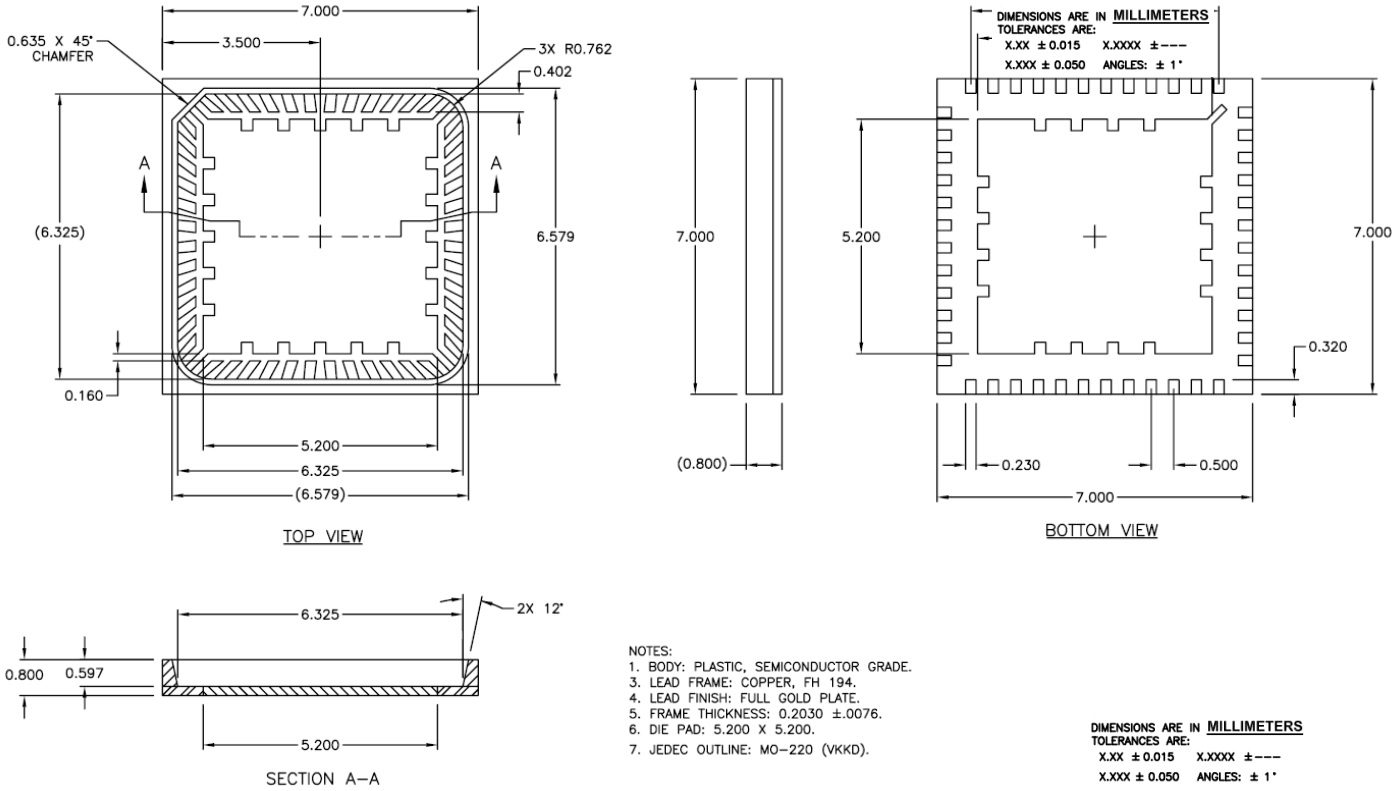
ACTAf 2 Ch version Layout picture

BONDING DIAGRAM



ACTAf 2 Ch version QFN48 7mm x 7mm Bonding Diagram with the DIE ground pads connected to the central package pad.

OUTLINE DIMENSIONS



48-Lead Lead Frame Chip Scale Package [QFN]
7 mm × 7 mm Body, Very Thin Quad
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range[1]	Package Description[2]	Package Option
ACTAf v1.23 2 Ch	−40°C to +125°C	48-Lead QFN	

[1]Temperature range for the ASIC technology used. To be tested at the next document revisions.
[2] Package dimensions without Lid (7 x 7 mm and 0.800 mm thickness).
[3] Lid dimensions (7 x 7 mm and 0.200 mm thickness).

NOTES

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