Doctorat en Enginyeria Electrònica

Departament D'Enginyeria Electrònica

Array of microfluidic beam resonators for mass sensing applications - Design, Fabrication and Testing

Doctoral Thesis – July 2016

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Chapter 3 Fabrication of HMB devices

Before the batch processing of MEMS devices, a couple of previous tasks must be fulfilled according to the specific requirements and standards inside a cleanroom facility. These tasks encompassed the design and printing of the photolithographic masks and a detailed description of the fabrication steps involved in the definition of the MEMS technology. The photolithographic masks are essential to outline the specific dimensions and features of the microdevices as is the width, length and shape of the resonators along with the microfluidic inlets according to the design proposed in the previous chapter. The manufacturing process included additive and subtractive tasks for removing materials deposited on the silicon substrate in a layer-by-layer fabrication process. Each of the fabrication strategies listed in this Thesis was carefully planned, discussed and verified by the clean room personnel along with the photolithographic masks design to investigate the feasibility to manufacture the HMB resonators technology with high yield and reproducibility. The HMB technology was manufactured at the Large Scale Facility (ICTS) of the IMB-CNM-CSIC.

In this Thesis work, we have developed three approaches to fabricate HMB devices. The first fabrication strategy consisted of both surface and bulk micromachining techniques to fabricate doubly clamped hollowed structures with excellent resonating capabilities, wherein silicon nitride and silicon oxide were used as structural and sacrificial layer, respectively. Instead, in the second fabrication scheme, polycrystalline silicon and doped silicon oxide were employed as structural and sacrificial materials correspondingly. In this approach, the fabrication of HMB devices was simplified by only executing surface micromachining with two photolithographic steps to obtain well-defined and hollowed structures with good filling capabilities. Finally, the purpose of the last fabrication strategy was to diminish the undercutting effect of the released resonators while etching the sacrificial layer observed in the previous fabrication schemes. Additionally, the on-chip integration of polymer-based microfluidics was included to facilitate the micro and macrofluidic interconnections, and packaging of the devices.

3.1 Fabrication process of HMB devices of the first generation

3.1.1 Mask design

The first batch of photolithographic masks was developed for two fabrication process, named RUN6570 and RUN6829. A set of three soda-lime photomasks, namely CNM677, was drawn in Klayout Software and printed by Compugraphics Company (Spain). The minimum feature size (MFS) for this type of masks was 1.5 μm, which complied well with the minimum dimensions required to fabricate our microstructures. Fig. 3-1 shows forty-five devices distributed all over the mask including the doubled size alignment marks located in the center whereby the dimensions of every device are 1 x 0.8 cm. For the step by step fabrication of devices, each mask has the following features:

- Mask CNM677-BRID1. This is the first alignment mask of the fabrication process that defines the following features of the microchannels: length (L), width (W), the number of microchannels in the array (B) and the separation distance between them (D). It also includes unique identification marks for every chip such as number, alignment motives and labels. Fig. 3-1 shows the marks included on each device.

- Mask CNM677-HOLE2. This mask is aligned with respect to CNM677-BRID1 mask to define the effective length of the resonators. It also uncovers the sacrificial layer by outlining access holes at both ends of the microchannels and includes an outer frame to release the devices from the substrate.

- Mask CNM677-GRID3. This mask is aligned with respect to CNM677-BRID1 mask using the double-sided alignment marks to release the structures from the silicon wafer during the bulk micromachining. Fig. 3–2 shows the alignment process of the three masks along with their corresponding alignment marks.

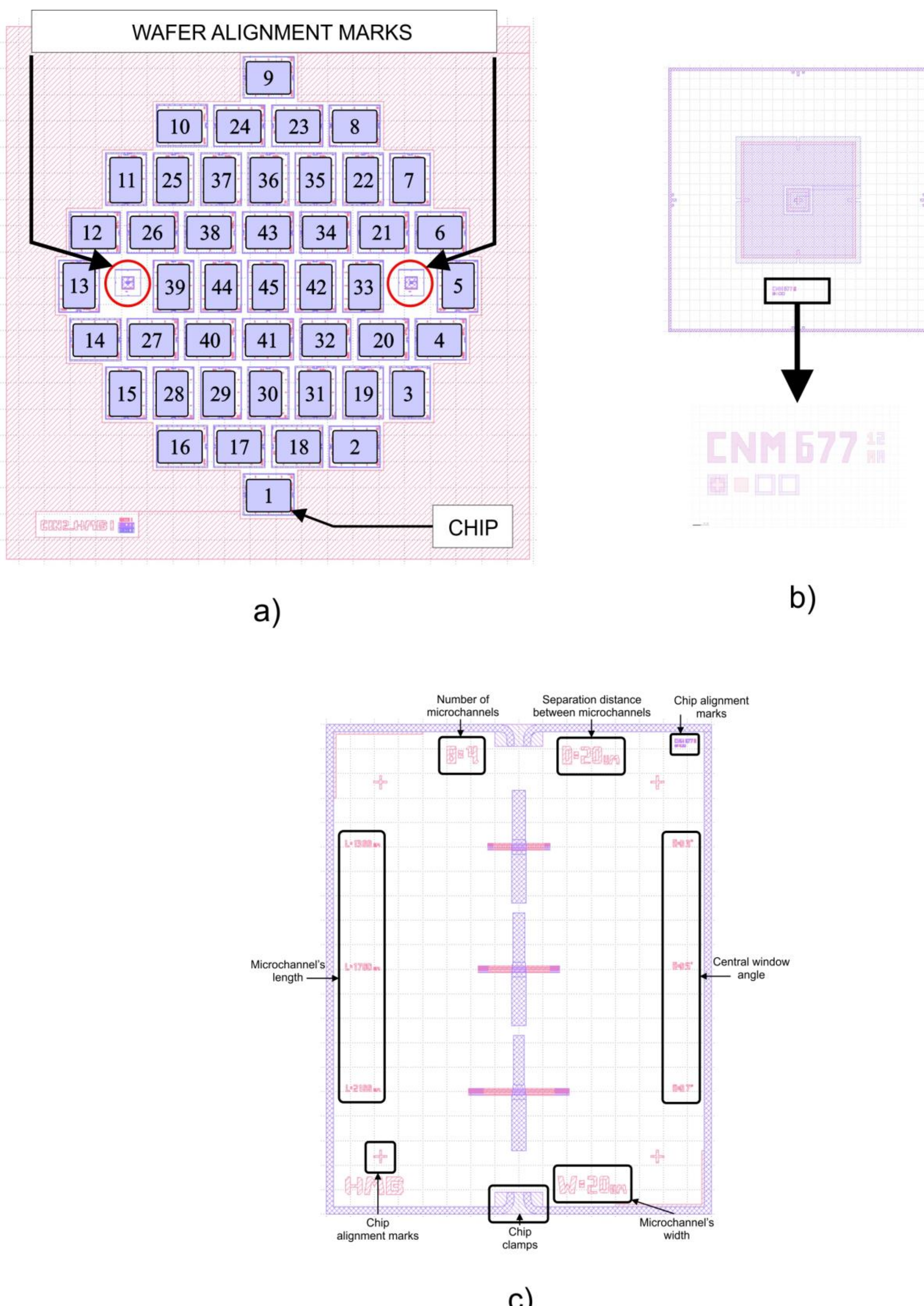
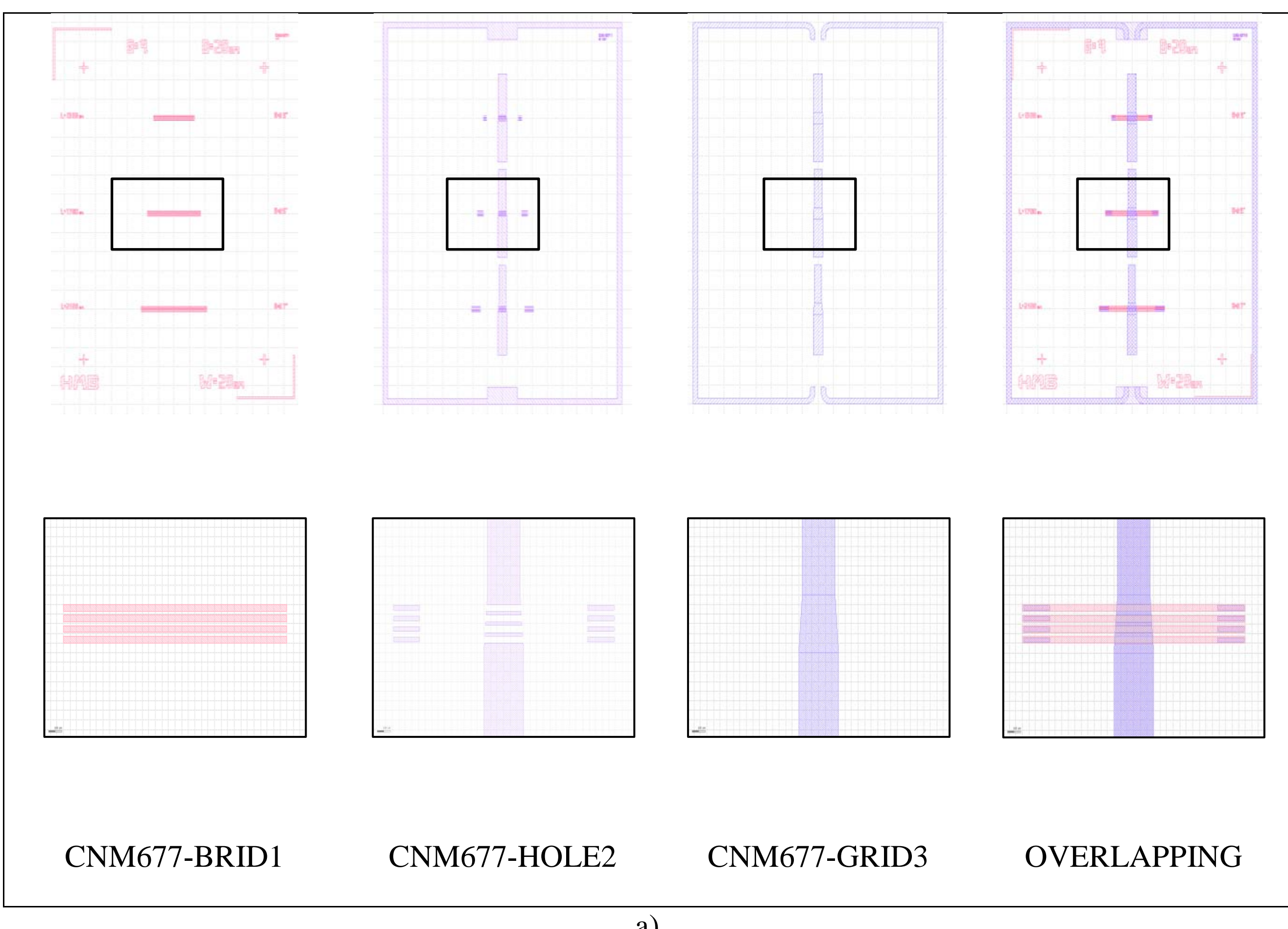


Fig. 3-1. a) Distribution of devices all over the mask design which has 5 inches in size, b) double-sided wafer alignment marks located in the center at a separation distance of 55 mm and c) main description labels that identify the fabrication features for each device.



a)

b)

Fig. 3–2. a) From left to right, consecutive alignment marks that define the HMB devices: microchannel dimensions, microfluidic inlets, effective length of the resonators and outer frame for chip release. A zoom-in of the marks indicates a detailed description of the microchannels masks and b) the principal alignment marks of each fabrication step.

3.1.2 Fabrication process at cleanroom facilities

Fig. 3-3 shows an overview of the fabrication steps and a general view of the device prototype. The process began by using silicon wafers type P of 300 µm thick and resistivity of 4-40 ohm-cm as based substrates. A general cleaning of the wafers with piranha solution removed any organic components. Next, a 500 Å layer of SiO_2 was thermally grown at 1000°C on both sides of the wafers (step 4). The silicon dioxide dielectric layer improved the adhesion of the following deposited layers and isolated the devices from the silicon substrate as required for the release of the final structures. From here, three groups of wafers were established to build microstructures with different dimensions based on the thickness of the structural and sacrificial layer. For the first batch of wafers (1-3), a 0.5 µm layer of Si_3N_4 was deposited by Low-Pressure Chemical Vapour Deposition (LPCVD).

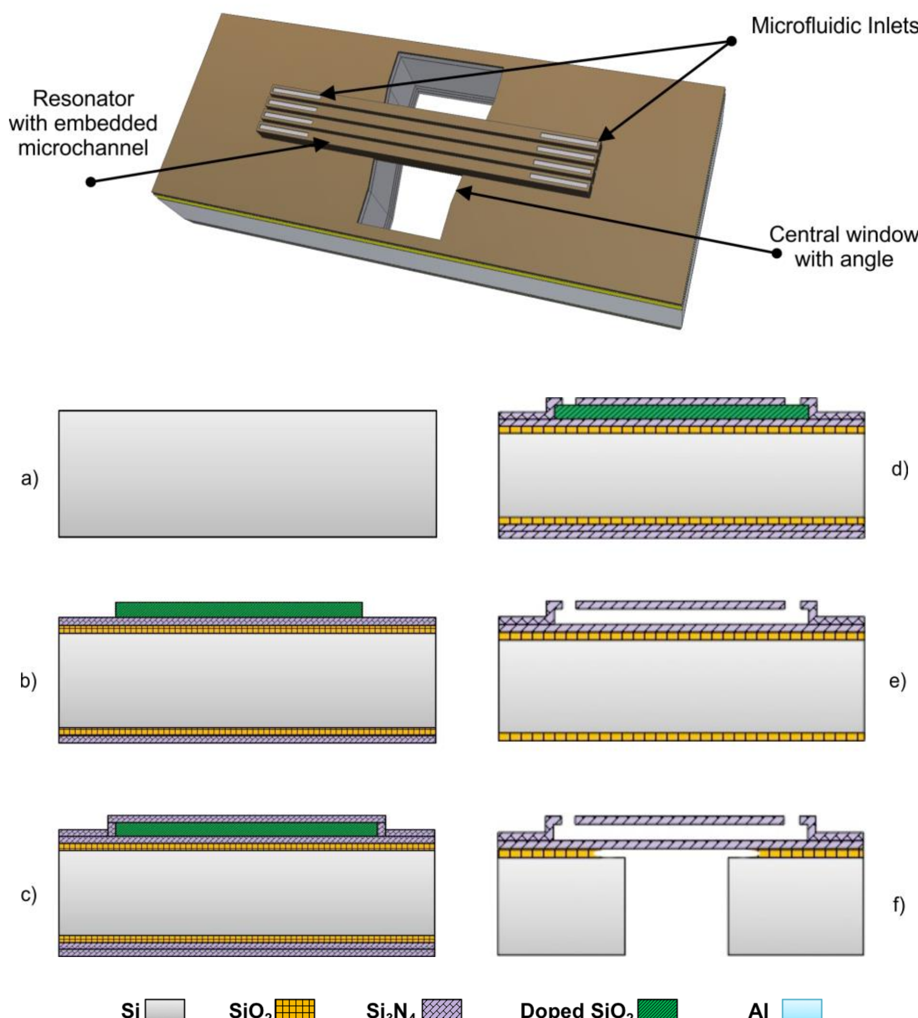


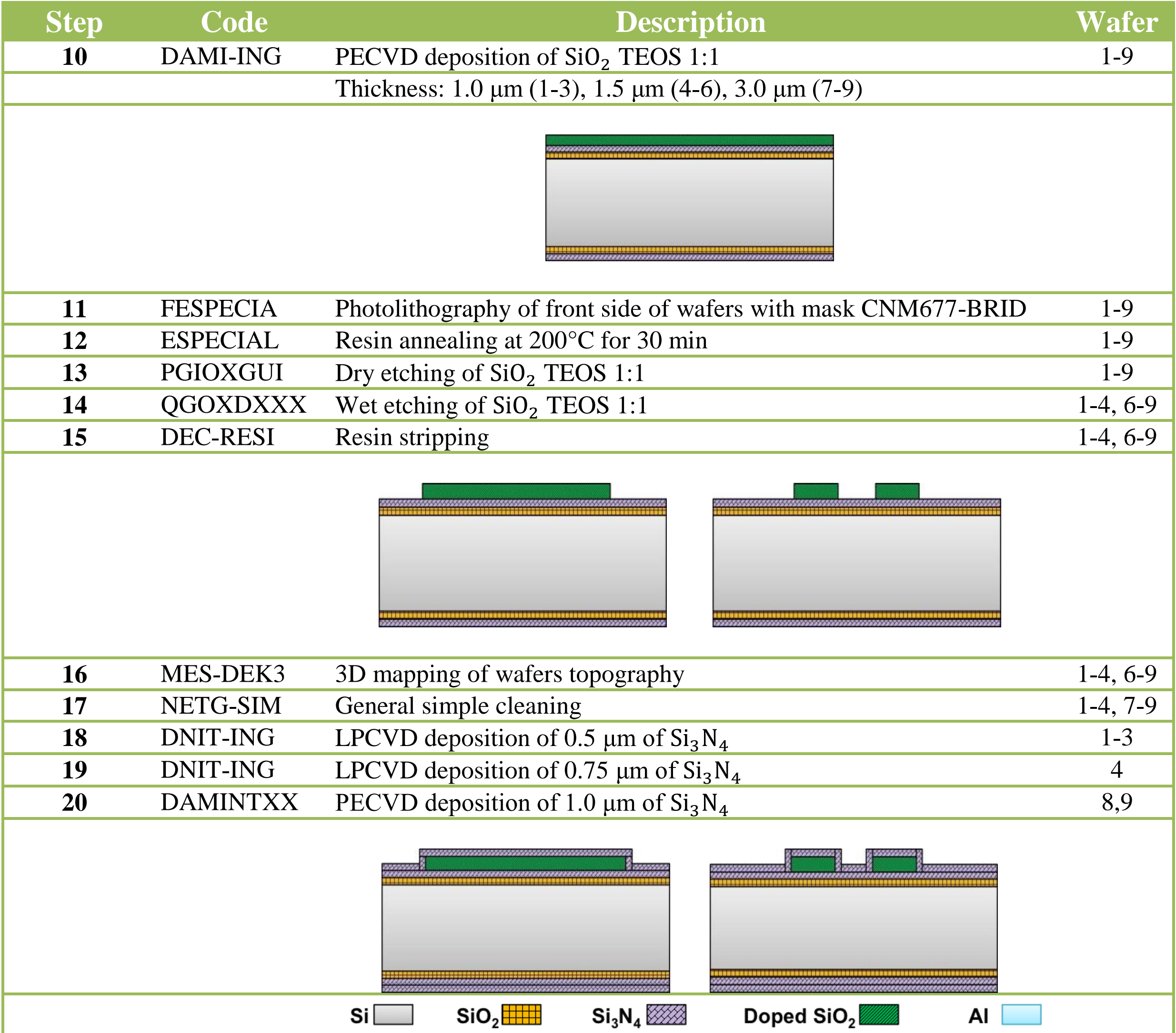
Fig. 3-3. On top, overview of a fabricated chip of the first generation of HMB devices. On bottom, a summary is presented for the most important fabrication steps in the procedure that include: a) initial wafer, b) patterning of the sacrificial layer, c) - d) enclosing and aperture of the microchannels, e) etching of the sacrificial layer and f) releasing the resonators from the silicon substrate.

Similarly, for the next group of wafers (4-6), a 0.7 µm layer of Si_3N_4 was deposited by LPCVD (steps 5&6). And for the latter group, a 1 µm layer of Si_3N_4 was deposited by Plasma-Enhanced Chemical Vapour Deposition (PECVD) to comply with the depth of the layer (step 7). The average thickness value was verified for each Si_3N_4 deposited layer by interferometric measurements in the visible range, with the Nanospec equipment (step 8), resulting the following mean values: 4915.40 ± 73.71 Å (wafers 1-3), 6981.33 ± 100.39 Å (wafers 4-6) and 9518.60 ± 153 Å (wafers 7-9).

Step	Code	Description	Wafer
1	INICIO	Preparation to begin RUN	1-9
2	MARC-PXA	Marking of silicon wafers	1-9
3	NET-GEN	General Cleaning	1-9
4	OSC-0500	Thermal grown of 500 Å of SiO_2 at 1000°C	1-9
5	DNIT-ING	LPCVD deposition of 0.5 µm of Si_3N_4	1-3
6	DNIT-ING	LPCVD deposition of 0.75 µm of Si_3N_4	4-6
7	DAMINTXX	PECVD deposition of 1 µm of Si_3N_4	7-9
8	MES-NANO	Thickness measurement of Si_3N_4 with Nanospec equipment	1-9
9	NETG-SIM	General simple cleaning	1-9

Si SiO_2 Si_3N_4 Doped SiO_2 Al

After a simple cleaning of wafers, the SiO_2 TEOS 1:1 (Tetraethyl Orthosilicate) sacrificial layer was deposited by PECVD (step 10). For each group of wafers, the thickness of the sacrificial layer was 9828 ± 362 Å, 14620 ± 378 Å and 28958 ± 400 Å, respectively. To achieve a 3 µm thickness, it was necessary to do three layer depositions of 1 µm thick each. During this process, particle traces appeared on the surface of the wafers along with other physical defects, which faded away after a cleaning with piranha solution over each deposition step. Next, vertically sidewalls of the sacrificial layer were patterned by soft-contact photolithography (step 11) and Reactive Ion Etching (RIE) in step 13. Any rest of the sacrificial layer was removed from Si_3N_4 using Buffered Hydrogen Fluoride solution (BHF: NH4F + HF + HzO) for approximately 60 s (step 14). Next, the topography of the microchannels was characterized with a Dektak 150 profilometer (step 16) to determine the real microchannel dimensions, see Fig. 3-4. In here, the corner sides of the microchannels were slightly smoothed during the wet etching step and also the center of the wafers showed a relatively compressive stress.



Step	Code	Description	Wafer
10	DAMI-ING	PECVD deposition of SiO_2 TEOS 1:1	1-9
		Thickness: 1.0 µm (1-3), 1.5 µm (4-6), 3.0 µm (7-9)	
11	FESPECIA	Photolithography of front side of wafers with mask CNM677-BRID	1-9
12	ESPECIAL	Resin annealing at 200°C for 30 min	1-9
13	PGIOXGUI	Dry etching of SiO_2 TEOS 1:1	1-9
14	QGOXDXXX	Wet etching of SiO_2 TEOS 1:1	1-4, 6-9
15	DEC-RESI	Resin stripping	1-4, 6-9
16	MES-DEK3	3D mapping of wafers topography	1-4, 6-9
17	NETG-SIM	General simple cleaning	1-4, 7-9
18	DNIT-ING	LPCVD deposition of 0.5 µm of Si_3N_4	1-3
19	DNIT-ING	LPCVD deposition of 0.75 µm of Si_3N_4	4
20	DAMINTXX	PECVD deposition of 1.0 µm of Si_3N_4	8,9

After a simple cleaning of the wafers, a second Si_3N_4 layer was deposited to enclose the structures (steps 18, 19 and 20). The thickness of each deposited layer was assigned according to each group of wafers, as described in early steps, and taking into account the symmetry of the microchannels. The Si_3N_4 thickness of each group of wafers was 4993 ± 71 Å, 6902 ± 104 Å and 10038 ± 88 Å, respectively. Afterwards, the effective length of the doubly clamped beams and the fluidic inlets of the microchannels were defined by soft-contact photolithography (step 21). To completely cover the microstructure topography of approximately 5 µm height, a 6 µm thick photoresist was deposited. The aperture of the exposed areas was etched by a dry etching process of the Si_3N_4 top layer until exposing the underlying thermally grown SiO_2 (step 23). Then, the protective photoresist was stripped from the wafers by oxygen plasma. Fig. 3-5 shows the revealed silicon dioxide layer at both ends of the microchannels and the outlined effective length of the beams.

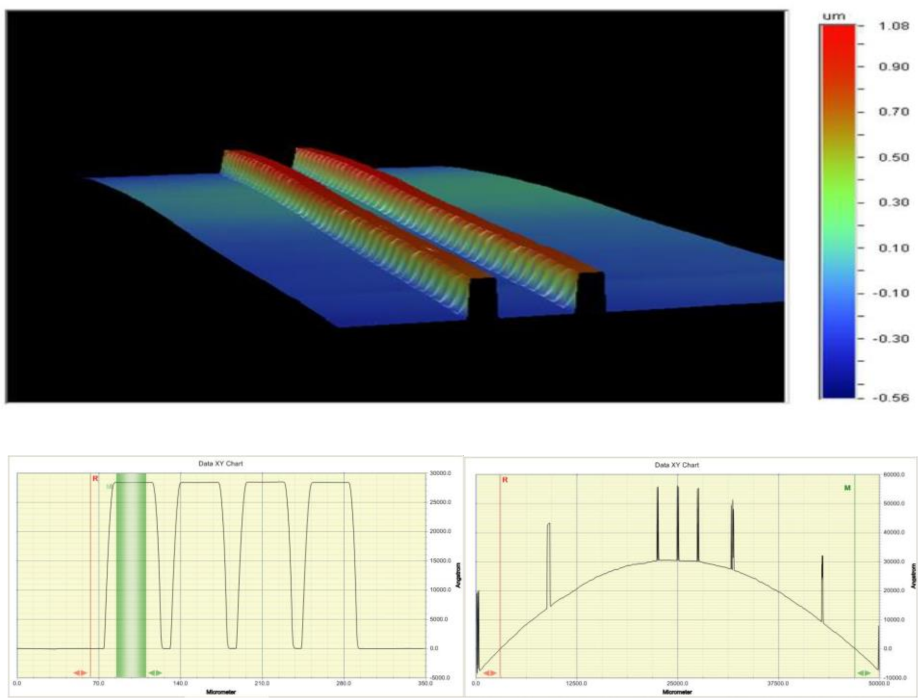
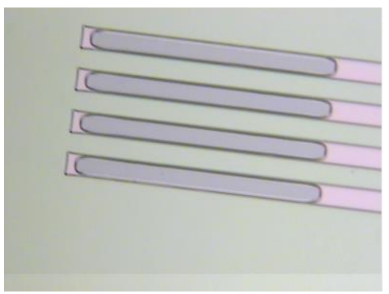


Fig. 3-4. (*Top*) 3D structural characterization of the patterned microchannels with a profilometer. Edges of the microstructures are slightly smoothed after the wet etching step with BHF solution. (*Bottom*) Topography of an array of four microchannels of 35 µm width. The wafers present a compressive stress along the "x" and "y" axis after the deposition of the Si_3N_4.

Step	Code	Description	Wafer
21	FOTO-ESP	Photolithography of the front wafers side with mask CNM677-HOLE2	1, 2, 3, 4 & 8
22	ESPECIAL	Resin annealing at 200°C for 30 min	2, 3, 4 & 8
23	GGIR-ING	Dry etching of Si_3N_4	2, 3, 4 & 8
24	DEC-RESI	Resin stripping	2, 3, 4 & 8
25	GHUM-ESP	Wet etching of SiO_2 TEOS 1:1 sacrificial layer	2, 3, 4 & 8
25b	MES-DEK3	3D mapping of wafers topography	2, 3, 4 & 8
		Si · SiO_2 · Si_3N_4 · Doped SiO_2 · Al	



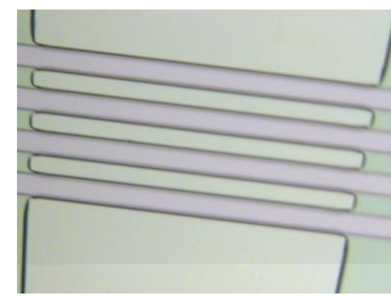


Fig. 3-5. Aperture of the Si_3N_4 structural layer to uncover the embedded sacrificial layer of silicon oxide. Also, the photo shows the specific width and length of the resonators in the central window.

The following steps consisted of removing the embedded sacrificial layer to constitute hollow cavities using a wet etching process. To set the optimum etching time of the sacrificial layer, not only the length of the largest structure (1480 µm) was taken into account but also the etch directions coming from the two openings located at both ends of the microchannels. Thus, it was determined that the effective sacrificial layer length to be etched was approximately 740 µm. For this task, two etchant solutions were considered based on their etching ratios shown in Table 3-1. If the BHF solution is employed to dissolve the sacrificial layer, then it is necessary to immerse the wafers for 3470 min, which will cause an over-etching of the Si_3N_4 of approximately 26 µm. Instead, if the HF 49% acid is used, a 20 µm over-etching of the Si_3N_4 will be expected for the 210 min required to etch the sacrificial layer. In sum, for this fabrication process, the selectivity between the sacrificial and structural materials was very low, and therefore it was not possible to create hollowed microfluidic channels. Nevertheless, the wafers were submerged in the BHF solution at different times, ranging from 8 to 12 min, to study the wet etching effects (step 25). The topography of the microchannels was characterized with the profilometer (step 25b) to determine the modifications of the microchannel dimensions, as can be seen in Fig. 3-6 and Fig. 3-7.

Table 3-1. Etching ratios of several materials at the cleanroom facilities of IMB-CNM

Material	BHF (µm /min)	HF 49% acid (µm /min)
PSG	0.5671	20.200
SiO_2 PECVD TEOS (1:1)	0.2132	3.5000
SiO_2 PECVD TEOS (1:2)	0.1605	2.4000
Si_3N_4 LPCVD	0.0007	0.0125
Si_3N_4 PECVD	0.0076	0.0980
SiO_2 PECVD	0.2132	3.0000

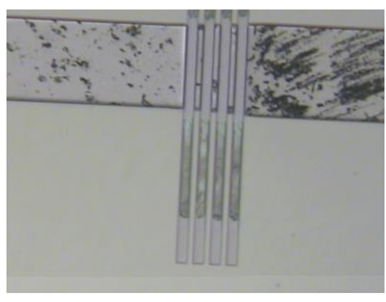
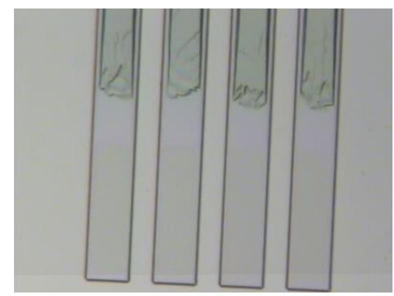
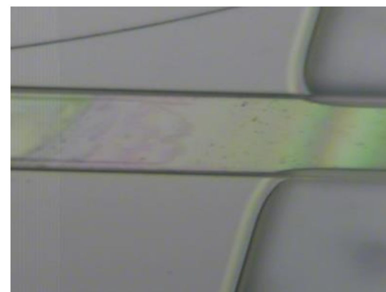




Fig. 3-6. Aspect of the microchannels after the wet etching of the sacrificial layer in which the structural layer was etched due to the low selectivity between the materials.

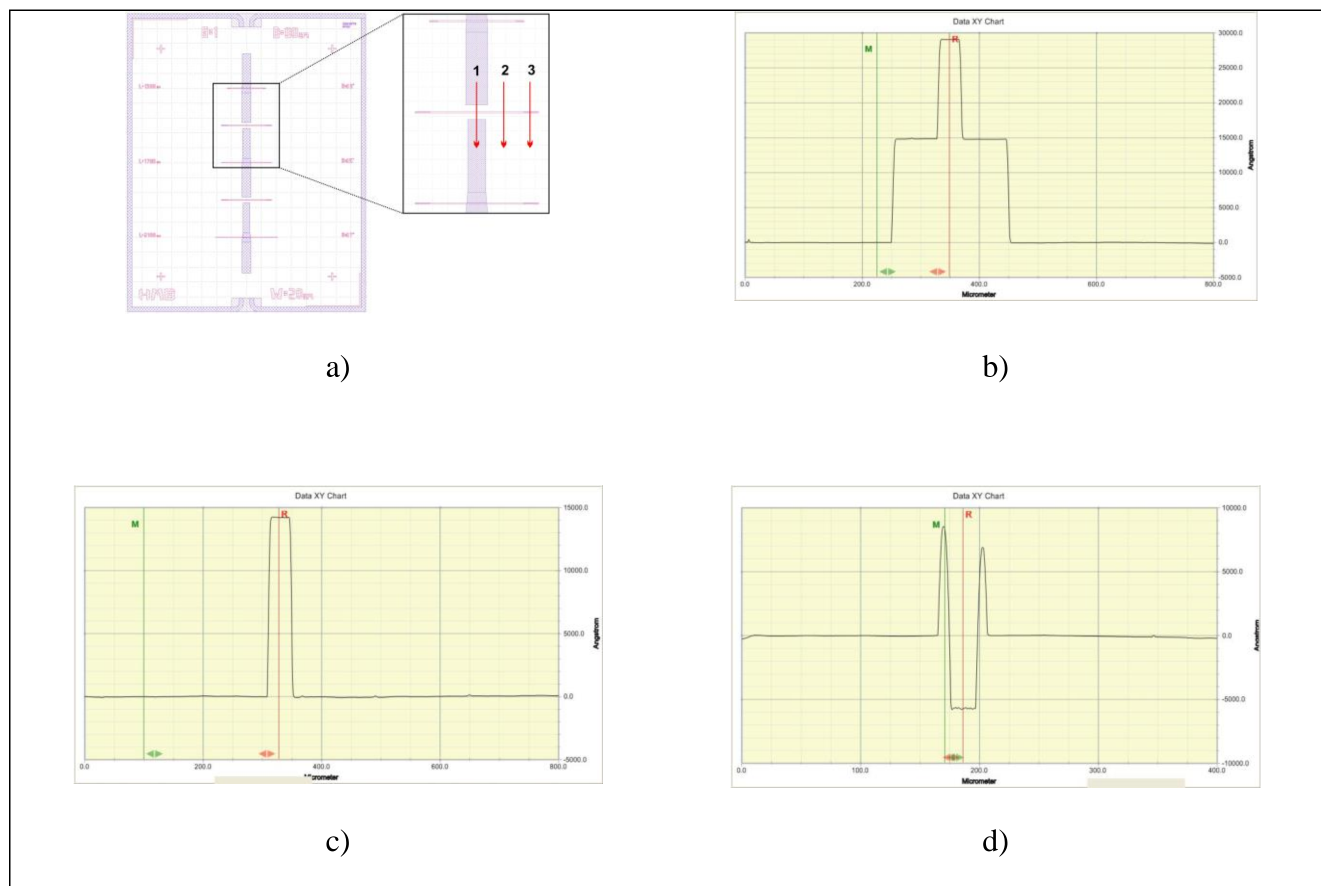
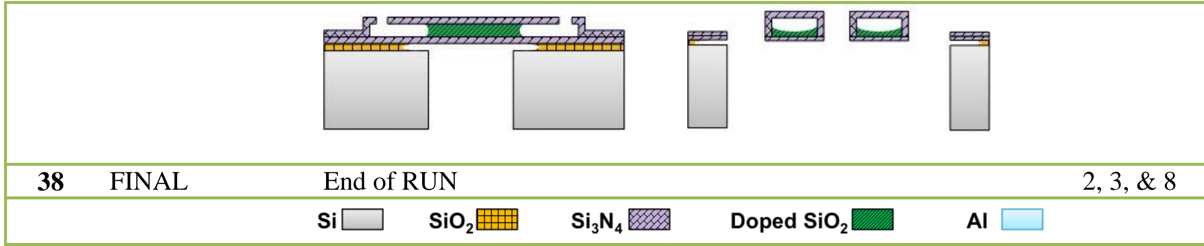


Fig. 3-7. Topography of the microchannels after wet etching the silicon oxide layer with BHF solution. Three features were captured by the profilometer at different locations of the microchannels. Besides, the structural layer was affected by the etchant solution due to the poor selectivity of both materials.

Despite the previous results, the fabrication process continued to probe the feasibility to release the structures from the substrate. At this point, several wafers were broken due to the exceeding residual stress of the Si_3N_4 layers, which increased with the thickness of the layers. For example , the wafers of the second group (4 , 5 and 6) were removed from the manufacturing process because

they fractures and imperfections across its surface. Thereafter, the two deposited layers of Si_3N_4 from the backside of wafers were removed using RIE until exposing the underlying thermally grown SiO_2 (step 27). In this step, a 6 µm resin was deposited on the front side of the wafers to protect the microstructures. Afterwards, a 0.5 µm layer of aluminium was deposited on the backside of wafers using electron beam evaporation (EBV) in step 29. This aluminium layer was used as a mask when releasing the structures from the front side of wafers by a deep silicon etching process (DRIE).

Step	Code	Description	Wafer
26	FESPECIA	Deposition of 6 µm of resin	2, 3, 4 & 8
27	GGIR-ING	Dry etching of Si_3N_4 from the backside of wafers	2, 3, & 8
28	DEC-RESI	Resin stripping	2, 3, & 8
29	MZ550ING	Deposition of 0.5 µm of Aluminium	2, 3, & 8
30	FOTO-ESP	Photolithography of backside of wafers with mask CNM677-GRID	2, 3, & 8
31	QUAD-ESP	Dry etching of 0.5 µm of Aluminium from back side of wafers	2, 3, & 8
32	PGIOXXXX	Dry etching of 50 nm of SiO_2 from the backside of wafers	2, 3, & 8
33	P601DEEP	Deep dry etching of 295 µm of silicon	2, 3, & 8
34	QGALCXXX	Wet etching of 0.5 µm of aluminium	2, 3, & 8
35	DEC-RESI	Resin stripping	2, 3, & 8
36	MSTMHXXX	Wet etching of silicon with TMAH 25% @ 80°C	2, 3, & 8
37	MST-ESP	Wet etching of 500 Å of thermal SiO_2	2, 3, & 8



Rectangular marks underneath the resonators were defined at the backside of the wafers using soft-contact photolithography (step 30) and RIE. The aluminium material (step 31) and after that the thermally grown SiO_2 (step 32) were removed until uncovering the silicon substrate. Next, a helium pressure of 500 Pa was adjusted in the Alcatel 601E equipment chamber to start the DRIE process of silicon (step 33). For each wafer, an average etching time of 25 min was necessary to remove approximately 275 µm of silicon. After stripping the protective resin, the aluminium layer was removed using a diluted acid etchant for 4 min (step 34). The remaining 25 µm of silicon material were etched using a TMAH 25% (Tetramethylammonium Hydroxide) solvent at 80°C for approximately 1h and 50 min until revealing the thermally grown SiO_2 (step 36). Finally, the SiO_2 layer was removed by immersing the wafers for 45 s in BHF solution until releasing the microstructures (step 37).

3.1.3 General overview and evaluation of the fabrication process

Fig. 3–8 shows a final device fabricated according to the first microfabrication approach. After ending the fabrication process, there were only three wafers left (2, 3 & 8) with half the number of chips (24) completely released. Devices with parallel alignment respect to the flat of the wafer were only released from the substrate because the last mask (CNM677_GRID3 mask), used to release the structures, was printed backwards and thus, some of the motives were overlapped. We noticed an increase in the residual stress of the wafers in both the substrate and the deposited film. Particularly for wafers with silicon nitrate deposited by LPCVD since the deposited silicon nitride layer was thicker. The excessive film stresses led to deformation and cracking of the microchannels which in the end produced unusable devices. Furthermore, the structural layer of devices from wafer 8 was highly affected during the wet etching process of the sacrificial layer. The etching ratio of the silicon nitride deposited by PECVD (7.6 nm/min) was tenfold higher than that deposited by LPCVD (0.7 nm/min), and therefore it was more easily affected by the BHF solution. Fig. 3–8d shows the uncovered sacrificial layer after the wet etching process for devices with silicon nitride deposited by PECVD.

On the other hand, devices from wafers 2 and 3 had well-defined structures with slightly tensile residual stress. Nevertheless, at both clamps sides of the beams some devices had undercut. Fig. 3–8c and Fig. 3–8d describe the differences between well-released structures and those with an undercut. The dimensions of the undercut surface complied well with the zone designated for the angular clamping support (up to 25 µm). This can be explained due to the non-uniformity of the DRIE process throughout the wafer. In the center of the wafer, the silicon etching ratio was slower

than that outside the wafer, and therefore during the anisotropic wet etching of the silicon substrate some devices were rapidly released.

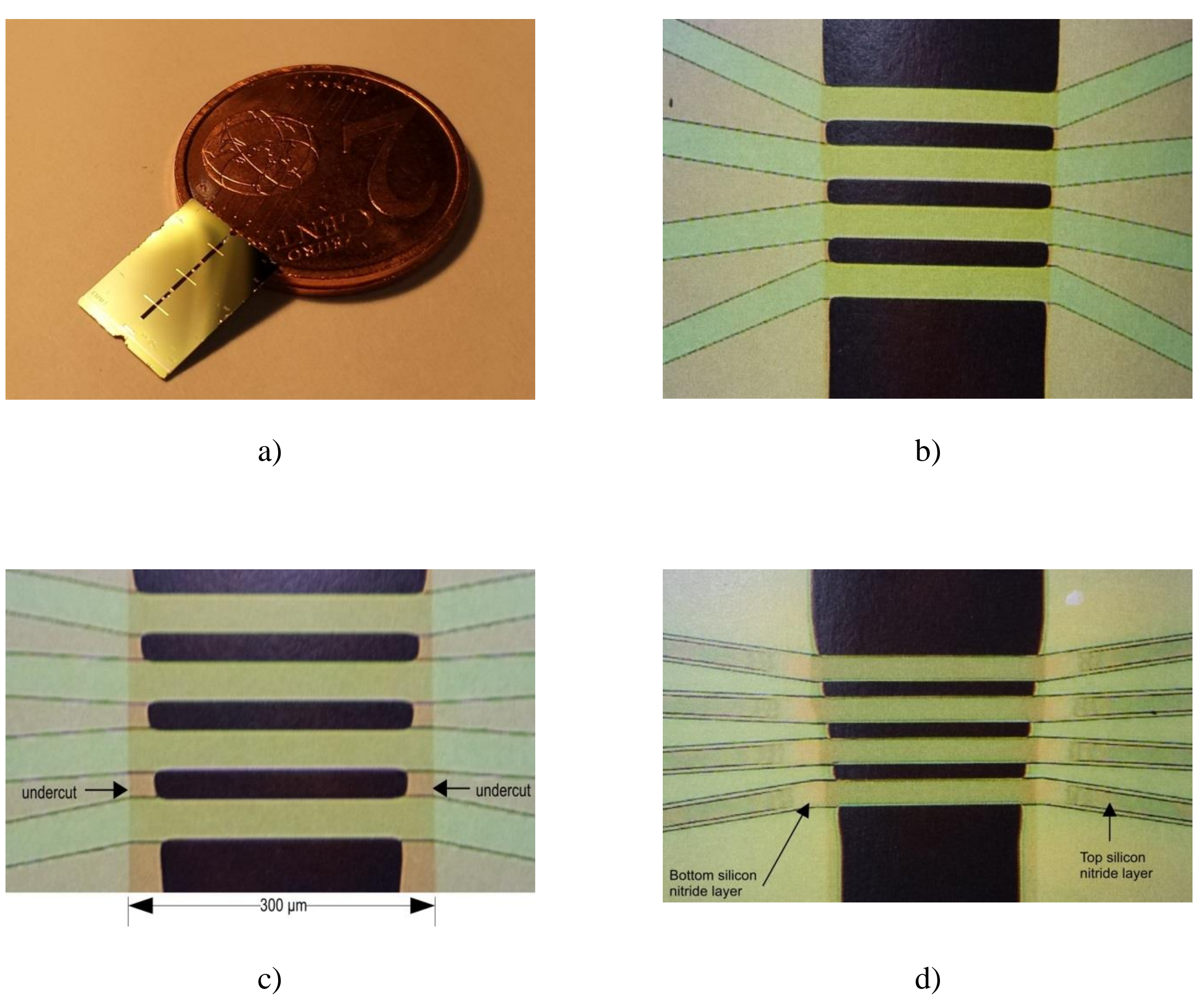


Fig. 3–8 a) Final view of a fabricated device using silicon nitride as structural material. b) An array of four suspended silicon nitride beams. c) Undercut produced after releasing the structures from the substrate which depended on the location of the device over the wafer. d) Partial etching of the silicon nitride material for devices with structural layer deposited by PECVD.

The dry etching process that outlined the effective length of the beams also affected the integrity of some structures, as detailed by the SEM micrographs of Fig. 3–9. The lateral edges of the beams were partially etched uncovering the embedded sacrificial layer for devices with silicon nitride thickness of 0.5 μm and 0.75 μm. Thus, the alignment of the photolithographic mask (CNM677-HOLE2) resulted challenging to outline features below 1.5 μm, as was the case of these edges.

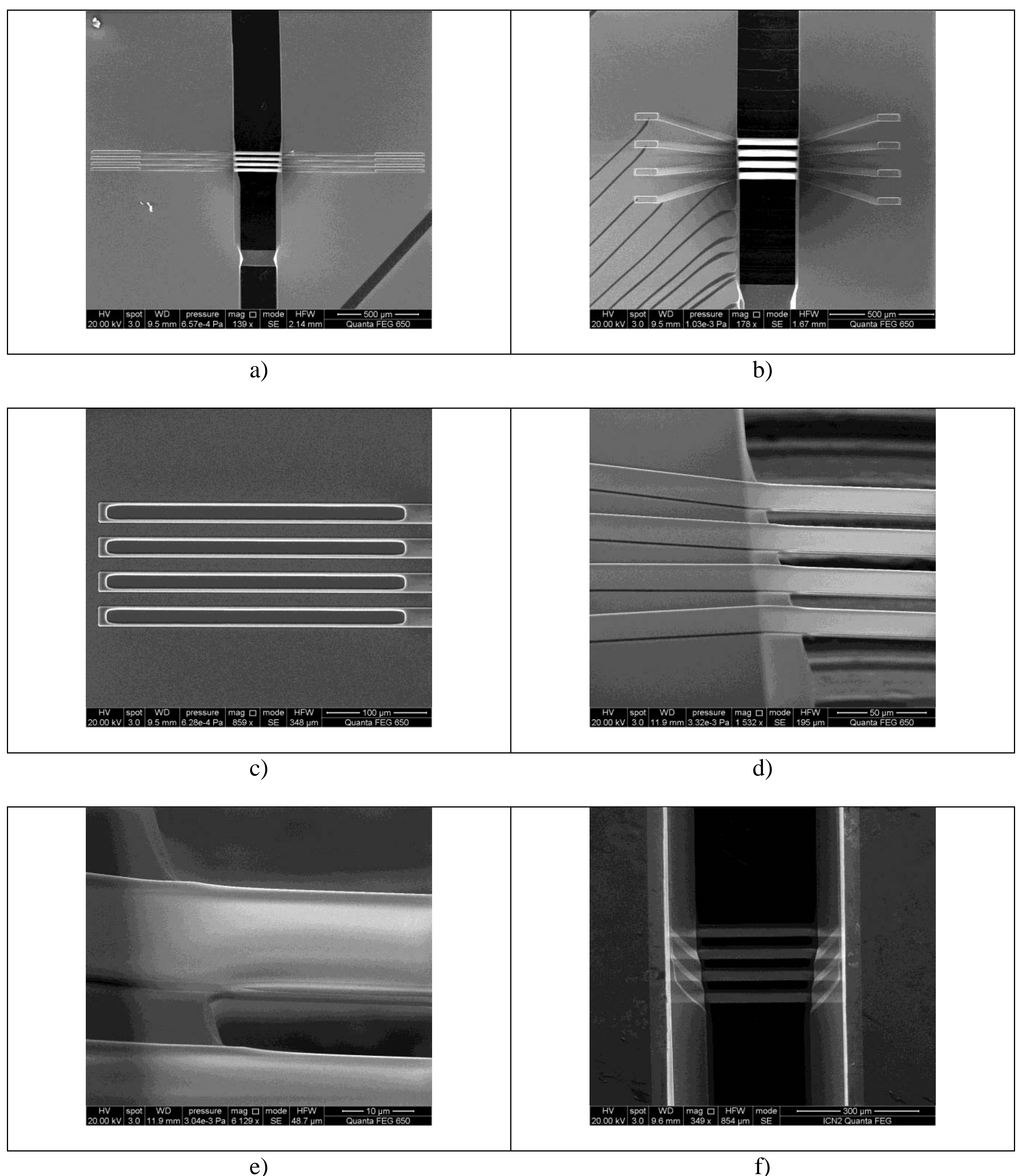


Fig. 3–9. SEM micrographs of a) - c) suspended silicon nitride beams with microfluidic inlets, d) undercut at the clamp region of the microbeams, e) partial etching of lateral walls of the microbeams and f) a bottom view of the beams after the bulk micromachining processes.

3.2 Fabrication process of HMB devices of the second generation

For the second fabrication of the resonators -low cost and well-known- surface micromachining techniques were employed. Fig. 3-10 shows an overview of the final device and the fabrication steps used in this technological process. Hollow microbridges were fabricated using 4-in, type P silicon wafers of 500 µm thick, double side polished and with a resistivity of 10-20 ohm-cm. Polycrystalline silicon was used as structural layer and borophosphosilicate glass (BPSG) as sacrificial layer because of their high selectivity and high etching rate of the latter when using HF 49% acid as etchant solution.

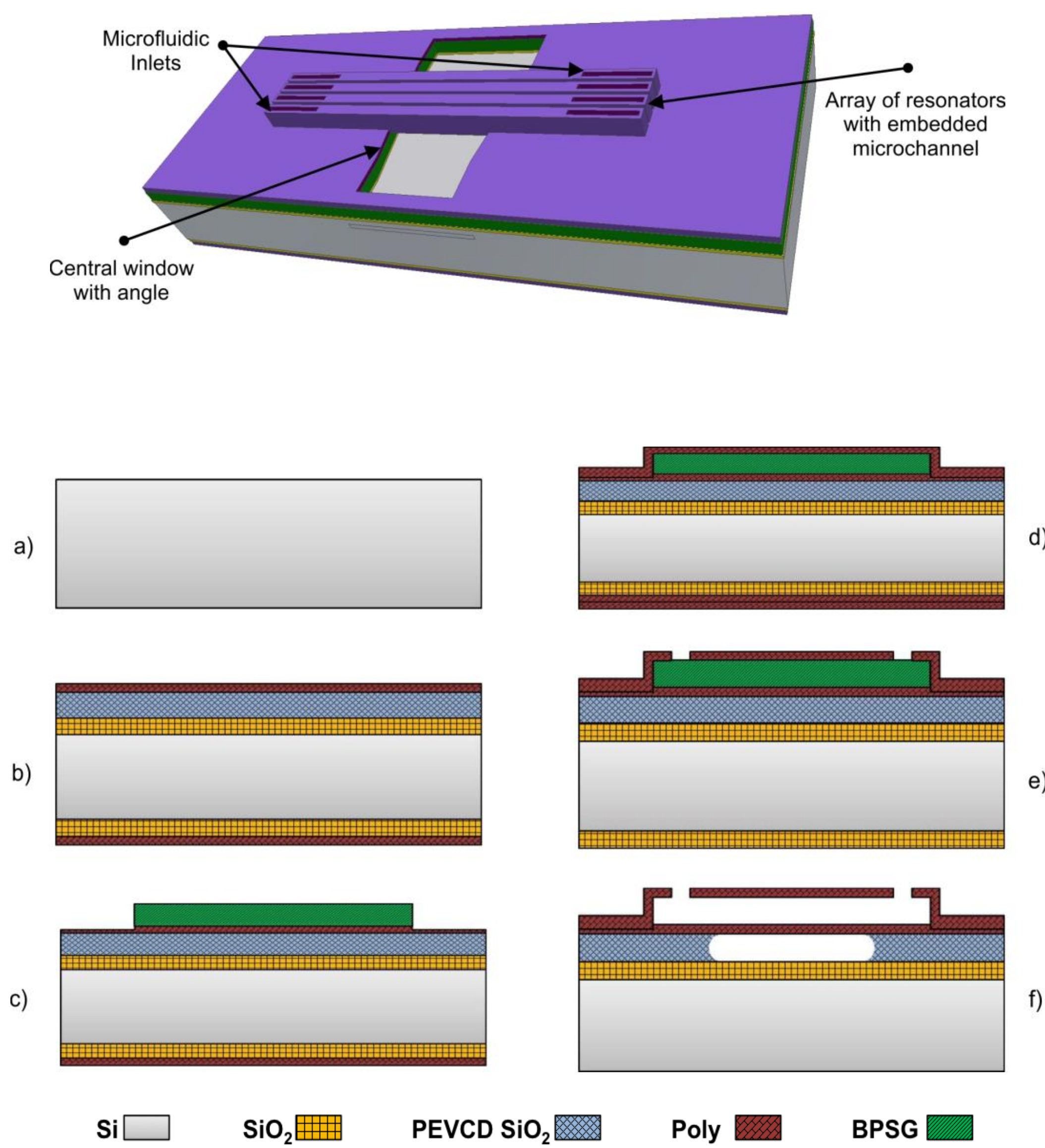


Fig. 3-10. (*Top*) single device showing the architecture of the array of polysilicon beams with embedded microfluidic channels. (*Bottom*) a summary of the principal fabrication steps: a) silicon wafer, b) deposition of layers, c) patterning of microchannels, d)-e) channel enclosing and patterning of microfluidic inlets and f) wet etching of the sacrificial layer.

The process began by using three silicon wafers as based substrates. The curvature of the wafers was then measured along the 0° and 90° axes of the wafers with Dektak 150 profilometer equipment (step 3). This procedure showed a maximum deformation of 3 µm in the center of the wafers. After a simple cleaning with piranha solution, a dielectric layer of SiO_2 of approximately 1.5 µm thick was thermally grown on both sides of the wafers (step 5). Then, a SiO_2 (TEOS 2:1) layer was deposited by PECVD on top of the wafers until achieving a 4 µm thickness (steps 7 and 8). This process was done in two consecutive depositions of 2 µm without cleaning the surface of the wafers. The thickness of this layer (4 µm) was chosen to avoid stiction while releasing the microstructures from the substrate. The stiction occurs while drying two paralleled and closely spaced microstructures after a wet etching process, which can cause the collapsing of the suspended microstructures due to capillary forces. Measurements with the Nanospec equipment verified that the final thickness of the deposited SiO_2 layer was approximately 53173 ± 951 Å.

Step	Code	Description	Wafer
1	INICIO	Preparation to begin RUN	1-3
2	MARC-PXB	Marking of silicon wafers	1-3
3	MES-DEKS	Wafer curvature measurement along 0° and 90° axes	1-3
4	NET-GEN	General cleaning	1-3
5	OHC-1M5	Thermal growth of 1.5 µm of SiO_2 at 1100°C	1-3
6	NETG-SIM	General simple cleaning	1-3
7	DAMIOX21	PECVD deposition of 2 µm of SiO_2 TEOS 2:1	1-3
8	DAMIOX21	PECVD deposition of 2 µm of SiO_2 TEOS 2:1	1-3
9	MES-NANO	Measurement of the SiO_2 thickness with Nanospec equipment	1-3
10	NETG-SIM	General simple cleaning	1-3

Si SiO_2 PEVCD SiO_2 Poly   BPSG

Thereafter, a 1 µm thick layer of polycrystalline silicon was deposited by LPCVD at 580° C and 380 mtorr (step 11) followed by the deposition of 4 µm of BPSG. The deposition of the sacrificial layer was done in two consecutive steps similar to the process described above. Nevertheless, the wafers presented lots of particles located on the surface and embedded in between the layers. For this reason, the 4 µm sacrificial layer was stripped with BHF solution and the process was repeated (step 12). This time, four consecutive depositions of 1 µm thick were done along with a cleaning process

with dip HF solution for 15 s and H_2O after each deposition. To finally remove any residues, dirt or particles, the wafers were immersed in an ultrasonic bath with water for 10 min.

Step	Code	Description	Wafer
11	DPOLSENA	LPCVD deposition of 1 µm of polycrystalline silicon (580°C/350 mTorr)	1-3
12	DBPTEOSX	PECVD deposition of 1 µm of doped SiO_2 BPSG	1-3
		PECVD deposition of 1 µm of doped SiO_2 BPSG	1-3
		PECVD deposition of 1 µm of doped SiO_2 BPSG	1-3
		PECVD deposition of 1 µm of doped SiO_2 BPSG	1-3
13	HOLDRESP	Particles on surface are removed using an ultrasonic bath for 10 min	1-3
14	FOTO-ESP	Photolithographic process of front wafer side with mask CNM677-BRID	1-3
15	ESPECIAL	Resin annealing at 200°C for 30 min	1-3
16	PGIOXGUI	Dry etching of doped SiO_2 BPSG	1-3
17	QGOXDXXX	Wet etching of doped SiO_2 BPSG	1-3
18	AMRIEING	Dry etching of 200 nm of polycrystalline silicon	1-3
19	DEC-RESI	Resin stripping	1-3
20	QDRACXXX	Resin stripping with acid	1-3
21	MES-DEK3	3D mapping of the wafers topography	1-3
22	NETG-SIM	General simple cleaning	1-3

Si SiO_2 PEVCD SiO_2 Poly   BPSG

The morphology of the microfluidic channels was patterned by soft-contact photolithography with mask CNM677-BRID (step 14) and the sacrificial layer etching with RIE (step 16). The dry etching equipment was operated at 90 mTorr, and at constant flow rate of 60 sccm of CHF_3 gas. The etching time for the BPSG layer was 600 s. To completely remove the BPSG material from the exposed areas, a wet etching step with BHF solution was done at different times for each wafer (step 17). Subsequently, another dry etching process of 200 nm of polycrystalline silicon was done for 70 s using the same photolithographic pattern and considering that the polycrystalline silicon material has an etching rate of 1900 Å /min (step 18). The purpose of this step was to improve the adhesion between the top and bottom structural layers by completely covering the sacrificial layer topology. The polycrystalline silicon material that remained after this etching step was 11754 Å. The next step

consisted of stripping the protective resin with acid to do a 3D mapping of the wafer topography with the profilometer (step 21), as shown in Fig. 3-11.

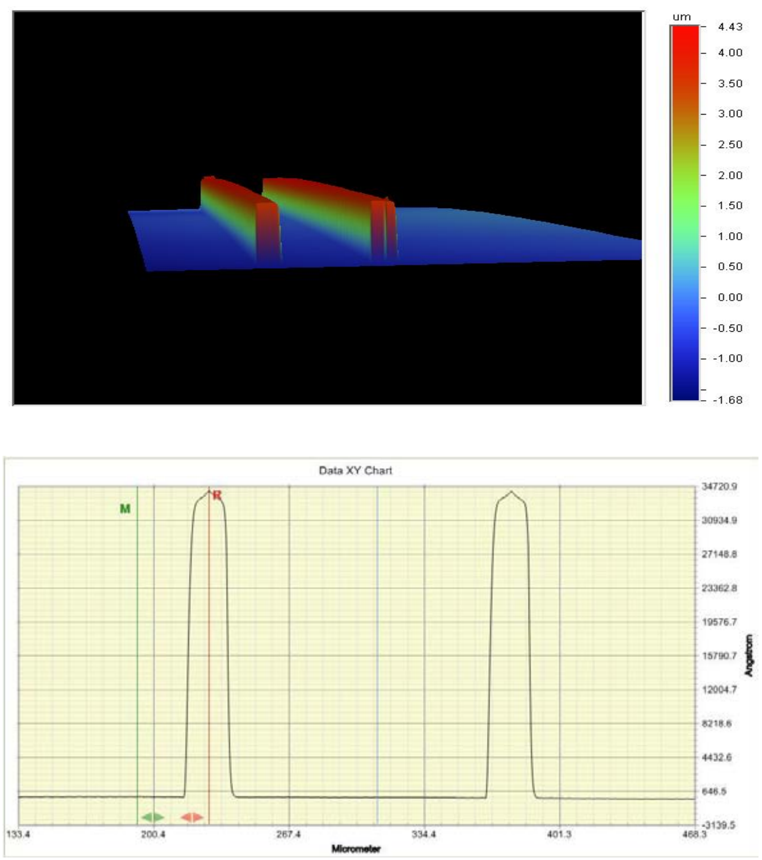
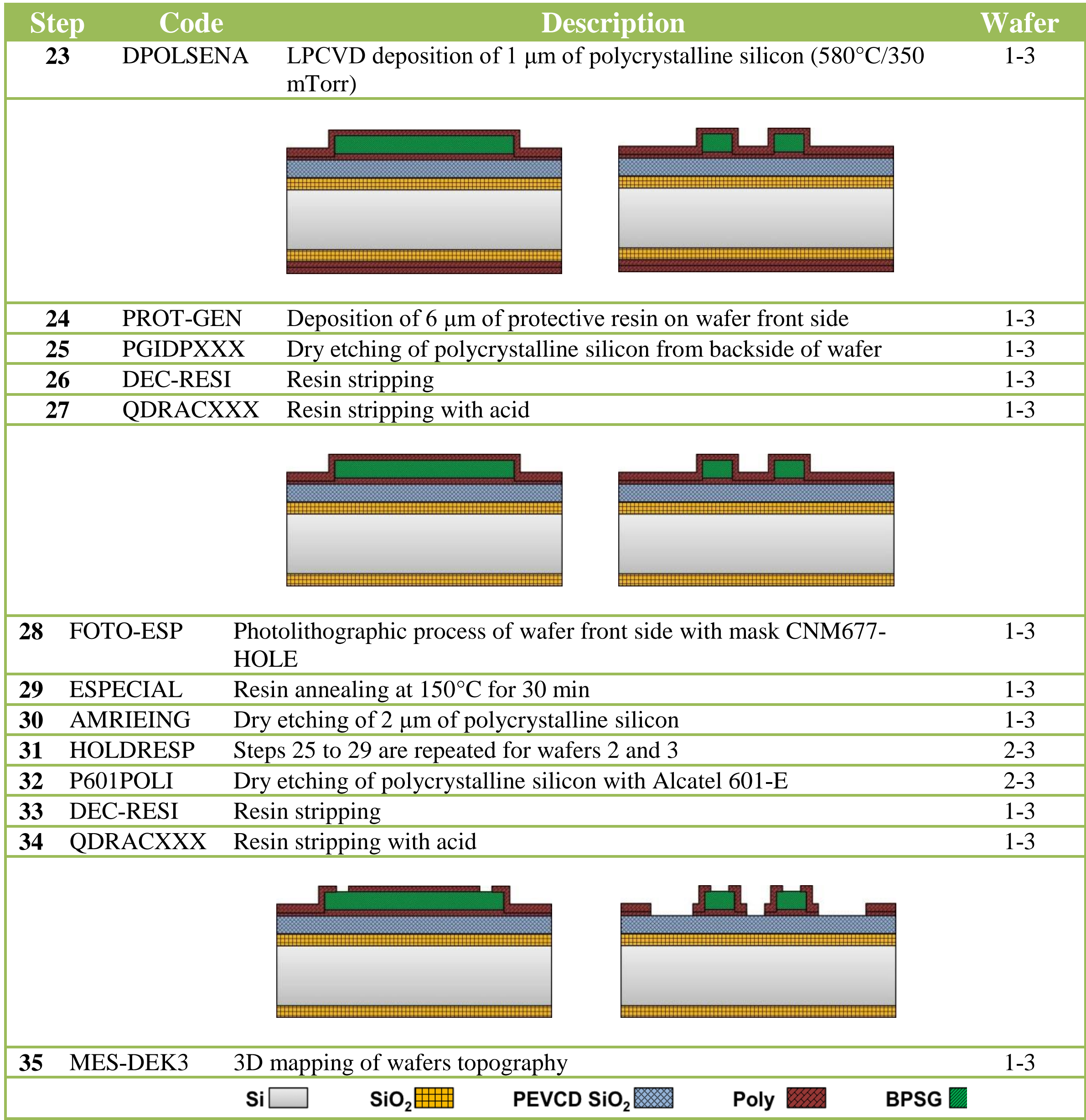


Fig. 3-11. (*Top*) 3D mapping of two BPSG microchannels with 4 µm height. (*Bottom*) the edges of the microchannel were slightly smoothed after the wet etching process with BHF etchant solution to remove residues of the sacrificial layer.

After a simple cleaning of wafers, another 1 µm layer of polycrystalline silicon was coated in order to enclose the microstructures and create a three-layer structure with the sacrificial layer in the middle (step 23). To remove the polycrystalline silicon deposited underneath the wafers, a 6 µm thick layer of protective resin was spun on the front side. Then, a RIE process etched the polycrystalline silicon material until uncovering the thermally grown SiO_2 layer (step 25). After stripping the protective resin on the front with reactive plasma and acid, access holes located at both ends of the microchannels and at the central trapezoidal frame that outlines the effective length the resonators were defined by soft-contact photolithography with MASK CNM677-HOLE (step 28). During this process, it was necessary to anneal the resin at 150°C for 30 min to stand for the dry etching of 2 µm of polycrystalline silicon material (step 32). The optimum dry etching time was conditioned based on the dry etching of wafer 1. Thereafter, a new 3D mapping of the structures was done after stripping the resin of the photolithographic process (step 35), as Fig. 3–12 describes.



Step	Code	Description	Wafer
23	DPOLSENA	LPCVD deposition of 1 μm of polycrystalline silicon (580°C/350 mTorr)	1-3
24	PROT-GEN	Deposition of 6 μm of protective resin on wafer front side	1-3
25	PGIDPXXX	Dry etching of polycrystalline silicon from backside of wafer	1-3
26	DEC-RESI	Resin stripping	1-3
27	QDRACXXX	Resin stripping with acid	1-3
28	FOTO-ESP	Photolithographic process of wafer front side with mask CNM677-HOLE	1-3
29	ESPECIAL	Resin annealing at 150°C for 30 min	1-3
30	AMRIEING	Dry etching of 2 μm of polycrystalline silicon	1-3
31	HOLDRESP	Steps 25 to 29 are repeated for wafers 2 and 3	2-3
32	P601POLI	Dry etching of polycrystalline silicon with Alcatel 601-E	2-3
33	DEC-RESI	Resin stripping	1-3
34	QDRACXXX	Resin stripping with acid	1-3
35	MES-DEK3	3D mapping of wafers topography	1-3
		Si, SiO_2, PEVCD SiO_2, Poly, BPSG	

From here, all the fabrication steps were done solely on wafer 1; the rest of wafers were put on hold. Wafer 1 was manually diced (step 36) into four pieces (M1, M2, M3 and M4) to find the optimum etching rates of the sacrificial layer using HF 49% acid solution as etchant. Each piece was assigned with a different etching times: 30 min, 5 min, 1 min and 20 min, correspondingly (steps 37 and 38). The resonators were released from the substrate in this procedure by dissolving the underlying silicon oxide (TEOS 2:1) at a lower etching rate (2.4 μm/min) than the BPSG sacrificial layer. After each isotropic wet etching, the samples were washed with deionized water and isopropyl alcohol and then dried in an oven at 100°C. For the case of sample M1, all microstructures vanished due to the over-etching of the underlying SiO_2. As a result, the effective length of structures exceeded more than 300 μm and thus the released beams became fragile to manipulate while drying off the structures, as Fig. 3–13a shows.

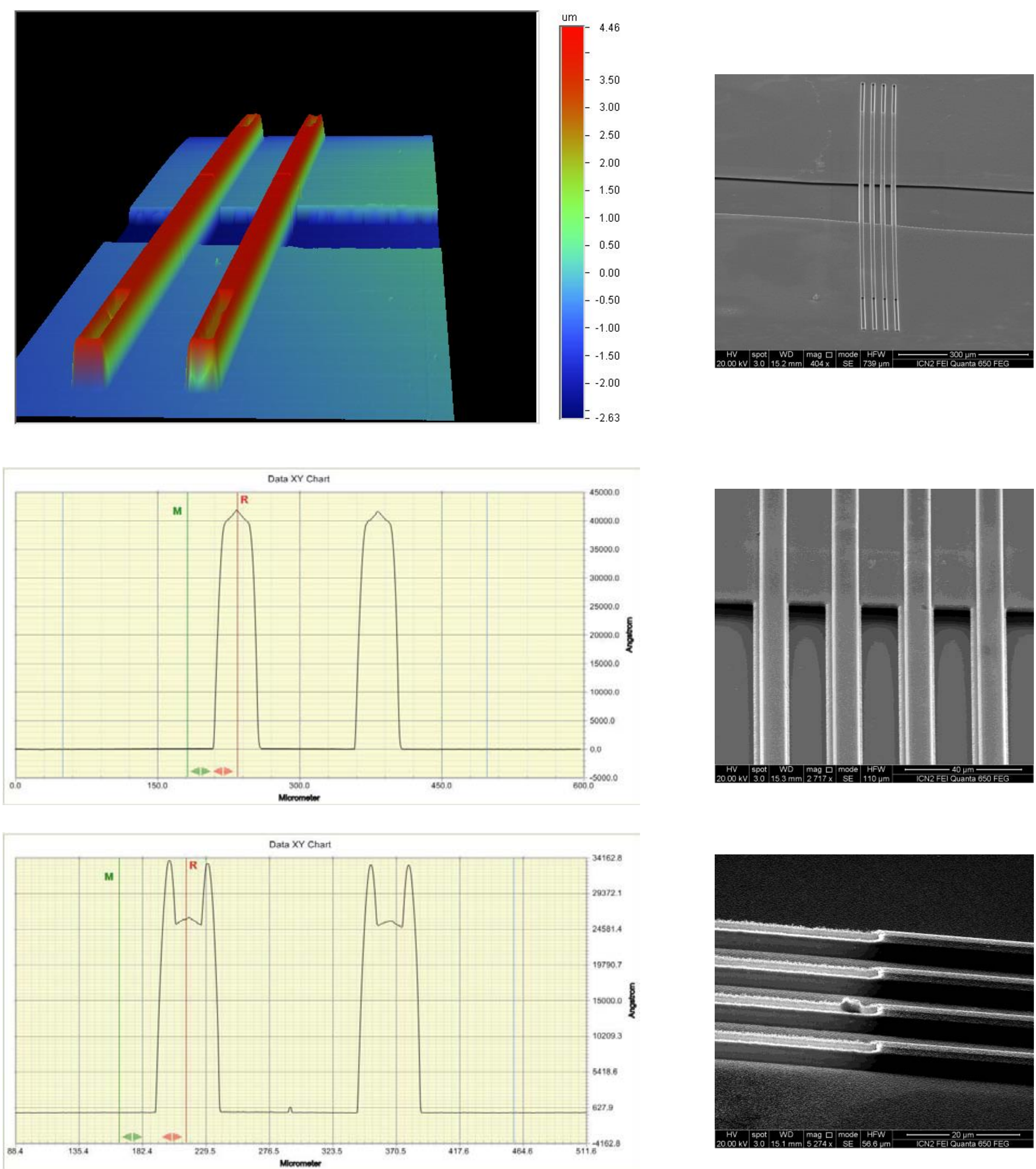
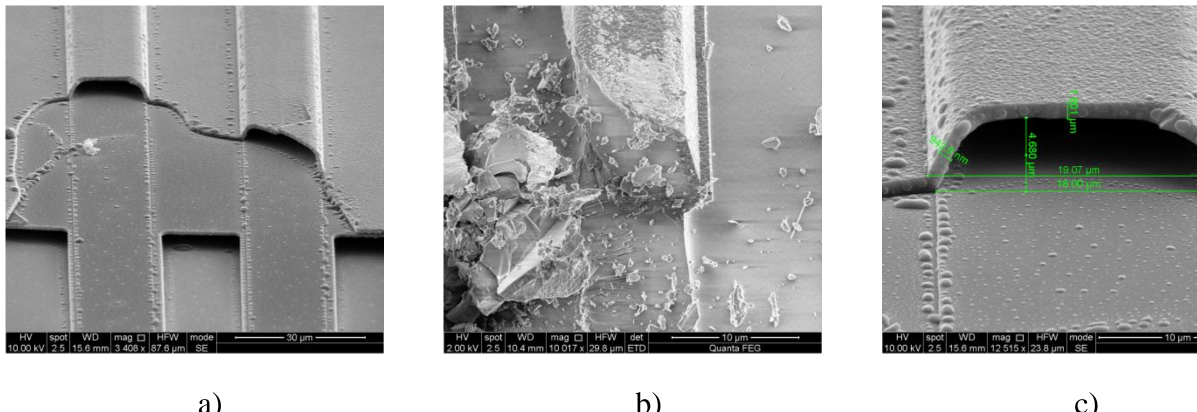


Fig. 3–12. (*Left*) morphology of two microchannels after the aperture of the microfluidic inlets. Also in this step the effective length of the beams was defined. The topography of the channels was taken from two locations: close to the clamp side of the beams and on top of the microfluidic inlets. (*Right*) SEM micrographs illustrating the corresponding topography of the microchannels.



a) b) c)

Fig. 3–13. a) Sample M1 after the sacrificial layer wet etching. The underlying silicon oxide layer was over-etched which caused the collapsing of the beams at both clamp zones; b) cross section view of the embedded sacrificial layer in sample M2. Timing was not enough to empty and release the cavities and c) sample M4 shows the dimensions of a hollowed cavity after 20 min of isotropic wet etching with HF 49% acid.

For the cases of samples M2 and M3, the etching time was insufficient to empty and release the microstructures as can be seen in Fig. 3–13b. It was found that the optimum etching time was 20 min for the case of sample M4 with an average etching rate of 20 µm/min for the sacrificial layer. Fig. 3–13c shows a cross-sectional view and dimensions of a hollow cavity after this process. Then, a protective layer of 6 µm thick was deposited over sample M4 to dice the wafer manually into individual chips of 1 cm x 1 cm in size. The rest of the wafers were processed in a similar way after considering the optimized wet etching times. Afterwards, the protective resin was removed from devices using acetone for 10 min at room temperature, rinsing with isopropyl alcohol and drying the samples under nitrogen. Then, piranha solution for 10 min was employed to remove any organic traces. Samples were further rinsed with Mili-Q water and dried in an oven at 150ºC to start the visual inspection by SEM micrographs of the devices with successfully fabricated microfluidic channels.

Step	Code	Description	Wafer
36	FEIN-ESP	Wafer is diced into four pieces (M1, M2, M3 and M4)	1
37	MST-ESP	Wet etching of doped SiO_2 BPSG	1
38	MST-ESP	Manual deposition of 6 µm of protective resin on front wafer side of M4 and resin annealing at 100°C for 60 min	1
39	FEIN-ESP	M4 sample is diced into 26 individual chips	1
40	DEC-ESP	Resin stripping with plasma and piranha solution (t = 10 min)	1
41	FIN-OBL	End of process for wafer 1	1
42	HOLDRESP	Stages 37 to 40 are repeated with optimum conditions	2-3
43	FINAL	End of RUN	2-3

Si **SiO_2** **PEVCD SiO_2** **Poly** **BPSG**

3.2.1 General overview and evaluation of the fabrication process

We have successfully built arrays of HMB resonators with the present fabrication approach. Fig. 3–14 shows a single device after finishing the process flow. Two completed wafers (2 & 3) were finished along with some devices from wafer 1 (only M4 sample). The resulted devices had dimensions of 0.8 x 1.0 cm a bit larger than those resulted from the first generation of HMB devices. The flow process allowed us to set optimum conditions on wafer 1 that influenced on the results of the rest of the wafers. As follows, we summarize the advantages and drawbacks of the present fabrication procedure.

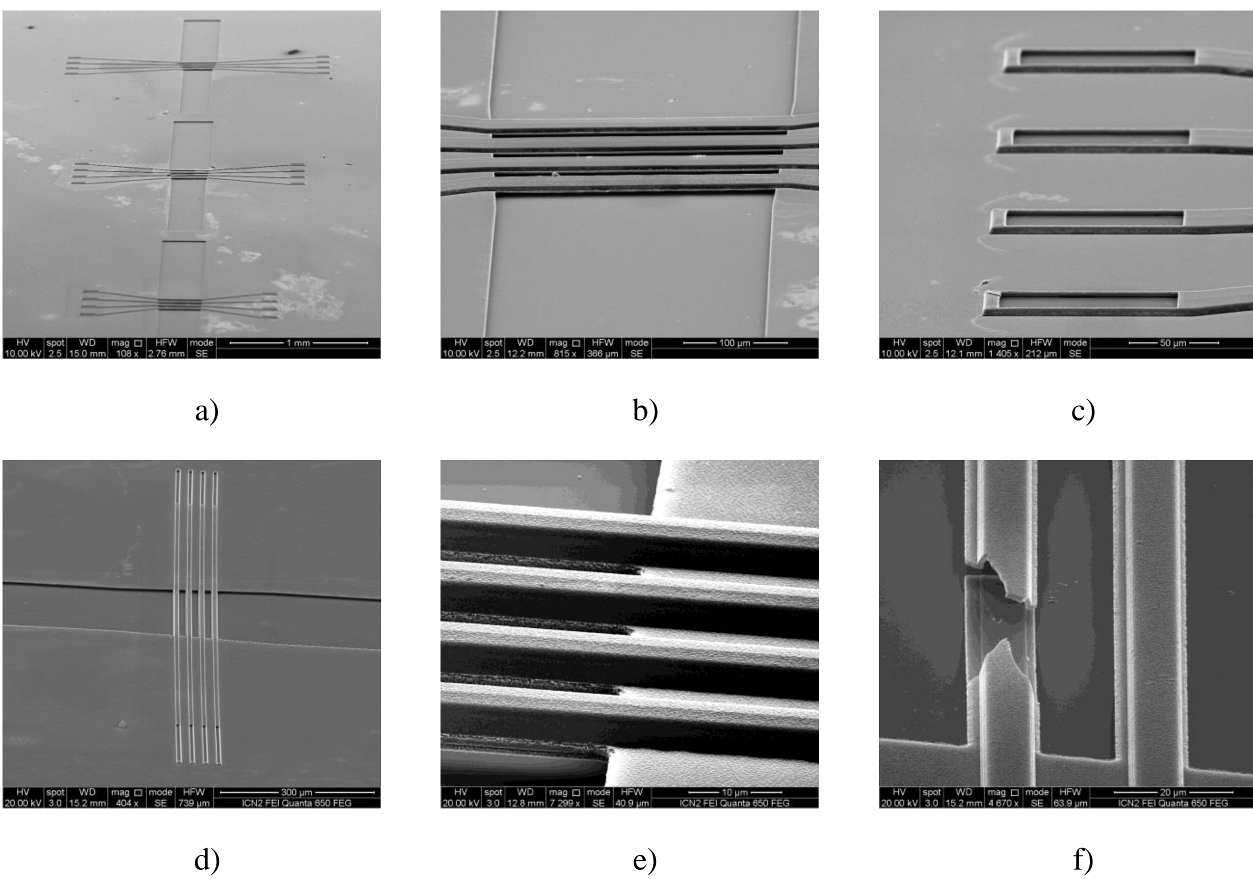
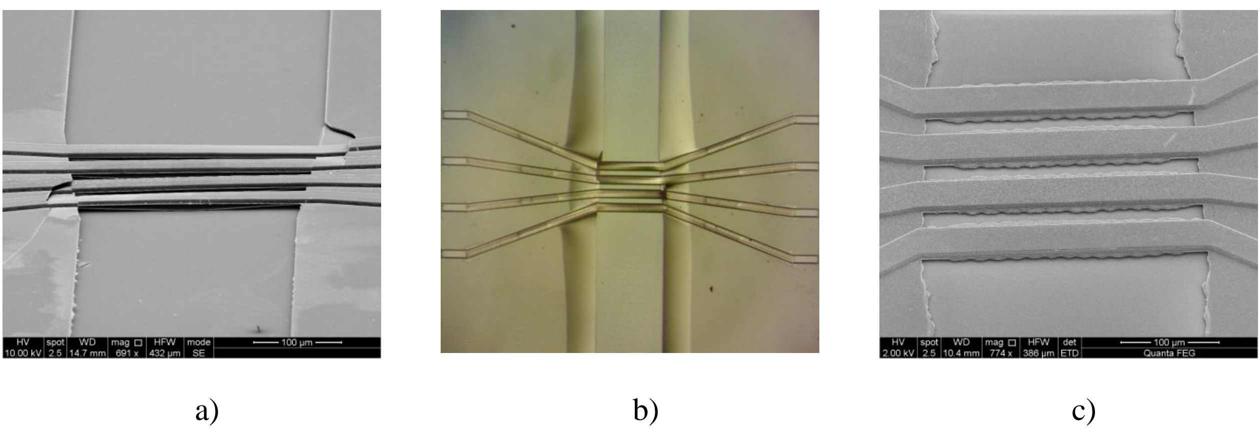


Fig. 3–14. a) General on-chip distribution of three arrays of HMB resonators; b) Close view of a well-defined array of HMB resonators with a tilt angle of 5° at both clamp sides; c) Microfluidic inlets at both ends of each microfluidic channel; d) An array of four parallel HMB resonators of 20 µm width; e) The microchannels protrude out from the substrate approximately 5 µm and f) Successful wet etching of the sacrificial layer in the central part of the microbeams.

A visual inspection of the microstructures showed that the majority of released beams had collapsed after stripping the on top 6 µm protective resin spun over the devices to manually dice them. During the thermal annealing of this resin, the solvents evaporated, and thus the resin shrank causing that the released beams were under a compressive stress. As a result, the excessive stress broke the doubly clamp supports of the beams, see Fig. 3–15a. In other devices, the top polycrystalline silicon

layer was released from the substrate and also the microfluidic inlets cracked. Moreover, the resonators became more fragile as a funtion of the over-etching of the underlying silicon oxide. The etching ratio of the underlying silicon oxide was tenfold lower than the BPSG material and thus some undercut of the resonators was expected. Fig. 3–15b shows a lateral over-etching of approximately 25 µm at each clamp side of the resonators. The undercut of resonators can be substantially reduced by including another photolithography mask to empty and release the resonators in two different wet etching processes.



a) b) c)

Fig. 3–15. a) Collapsing of an array of beams after stripping the protective resin with acetone and water. Tensile forces yielded a breakdown of the structures making them non-functional. b) A 25 µm undercut of the released beams located at each clamp region. c) Deformation of resonator edges after the photolithography of mask CNM677-HOLE using a wrinkled resin.

Another important issue occurred on devices from wafer 1. During the photolithography with mask CNM677-HOLE the aspect of the deposited resin was wrinkled. This defect could be derived from the UV source light aging or by the quality of the deposited resin. Therefore, the wrinkled pattern was transferred onto wafer 1 producing an irregular definition of the microchannel edges. Fig. 3–15a shows this effect on a microstructure with 35 µm width. Hence, to prevent the deformation of devices from other wafers, both the deposition of the resin and irradiation of the mask were carried out manually.

Unlike the first generation of devices, the effective wet etching of the sacrificial layer was due to the high selectivity between the structural (polycrystalline silicon) and sacrificial layer (BPSG). In the previous process, the sacrificial layer consisted of an undoped oxide layer that rendered low selectivity with respect to the silicon nitride structural layer. Interestingly, the wet etching ratio of the BPSG layer, in the second generation of HMB devices, was even faster than expected. Generally, the etching ratio of BPSG material is 20 µm/min, if we consider the size of the longest microfluidic channel of about 740 µm. Theoretically the expected time to completely remove the sacrificial layer should be 37 min. In here, the time was reduced to 20 min. This can be explained regarding the doping conditions of the sacrificial layer. Some studies have demonstrated that doping the oxide exclusively with phosphorous material can render even higher etching ratios [7].

Finally, deposition of polycrystalline silicon material by LPCVD showed good step coverage of the microchannels. However, the quality of the deposited layers was influenced by the properties of the underlying material. For example, polycrystalline silicon deposited on top of the microchannels showed a better distribution of grains with more compact boundaries than those deposited over the rest of the wafer. In this case, the underlying crystalline phase of polycrystalline silicon affected the properties of the top polycrystalline silicon layer yielding a rough surface with greater grain growth. Polycrystalline silicon is a polycrystalline material that can experience grain growth and phase transitions into other crystal structures while being deposited in thin films. This aspect is of great importance because a non-uniform layer can create zones of low material density leading to long-term instabilities.

3.2.2 Oxidation schemes

Silicon dioxide material plays an important role, like silicon, in the fabrication of MEMS devices. Throughout a fabrication process, silicon dioxide has various functions such as passivation layer, electric isolation layer and capacitor dielectric. Additionally, thick oxides (100 - 1000 nm) can be used as masking layers for diffusion and etching processes, and even as sacrificial layers. One of the major advantages that silicon oxide offers is with respect to its hydrophilic properties given that this material is amorphous and produces planar surfaces when deposited over substrates. For instance, thin films of silicon dioxide have contact angles in the range of 45° to 65°. This property makes silicon dioxide suitable for the integration of new devices compatible with microfluidics.

In the fabrication of HMB devices we used polycrystalline silicon material as the structural layer of the resonators for several reasons. Deposition of polycrystalline silicon layers by the present fabrication scheme resulted in low-tensile strength structures with values between 800 to 1100 MPa [8], which prevented the deformation of the structures. Moreover, using polycrystalline silicon as structural material reduced the etching time of the embedded sacrificial layer to a few minutes. However, despite the excellent mechanical and thermal properties of MEMS devices fabricated with polycrystalline silicon material, their compatibility with liquid phase analytes results challenging. Polycrystalline silicon has hydrophobic properties that can yield contact angles between 85° and 110°, and so liquid samples, such as water, can easily be repelled. On the other hand, one of the advantages that polycrystalline silicon outstands with respect to devices fabricated with silicon nitride is that it can easily be oxidized by different methods such as thermal oxidation or by direct streaming of oxidation agents. This advantage is of importance, i.e. in modifying the hydrophilic properties of the inner microfluidics walls to facilitate the filling of resonators with fluids of different viscosities. Furthermore, a thin oxide grown on the polycrystalline silicon layer can be used as a cleaning method to reveal a smoother surface when removed by an etchant solution such as HF 49% acid.

Oxide layers can easily be obtained through various methods. For instance, thin oxides can grow under ambient conditions to conform nanometric thick layers. Unfortunately, these oxides are not stoichiometric and have poor density and quality. In silicon microtechnology, there are two basic oxidation schemes based on thermal processes: wet and dry. A typical thermal process of a silicon

wafer is carried out at temperatures of 950-1100°C inside a furnace, and can last a couple of hours, depending on the final oxide thickness. Thermal oxidation is a slow process that depends on several conditions such as silicon crystal orientation and doping level. For instance, the oxidation rate of <111> silicon is higher than that of <100> silicon, and lightly doped substrates oxidize slower than highly doped [7]. Furthermore, when a thermal oxidation process takes place, the resulting oxide is approximate twice the volume of silicon it replaces. As shown in Fig. 3-16, for a silicon dioxide layer of thickness D, the replaced silicon thickness is about 0.54D. These oxide layers are usually measured by optical methods such as ellipsometry, interferometry or reflectometry. A quick and easy way to determine their thicknesses is by comparing the oxide colour with a specific colour chart of oxides given that each oxide thickness has a corresponding colour. Deal and Grove have also proposed a model to estimate the oxide thickness; this model predicts a linear oxidation rate initially, followed by a parabolic behaviour for the case of thicker oxides [7].

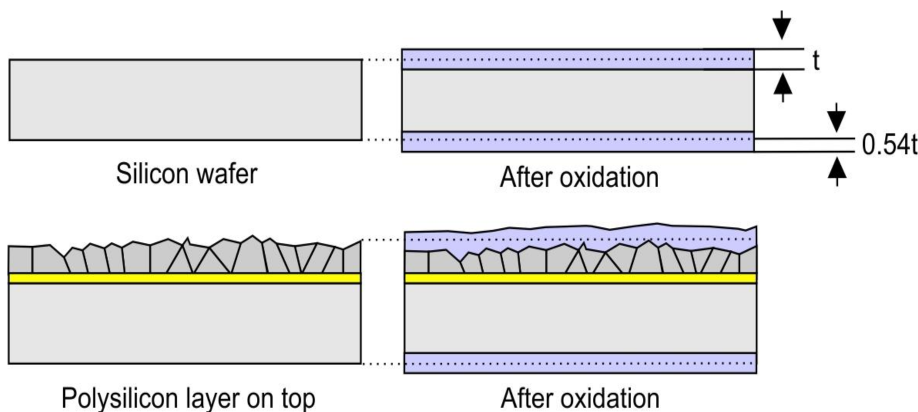


Fig. 3-16. Comparison of a silicon wafer oxidized with a thickness "t" to an oxidation scheme of polycrystalline silicon. The replaced volume of silicon material corresponds to a thickness of 0.54t.

We have done a study to take advantage of the hydrophilic properties of silicon oxide to enhance the wettability of the structural polycrystalline silicon layers of the resonators. In this way, the microchannel intrinsic resistance will be reduced to facilitate the filling of the microcavities by capillary forces. Consequently, once the microchannels were already filled, less applied hydrostatic pressure would be required to allow the fluidic samples to flow freely. Henceforth, we have proposed five schemes to oxidize the structural layer of some of our devices of the second generation using the model proposed by Deal and Grove to estimate the oxidation time according to the desired oxide thickness. Oxide thickness of approximately 50 nm, 100 nm, 150 nm and 200 nm were thermally grown by dry oxidation at 1100°C. An 1 µm oxide layer was also thermally grown at 1150°C by wet oxidation. These procedures were carried out at the Autonomous University of Barcelona (UAB) cleanroom facilities under non-contaminant conditions, according to the parameters shown in Table 3-2. Before the oxidation process, a visual inspection of the selected chips revealed that the majority of released microbeams had collapsed after stripping the top protective resin. The morphology of the microstructures can also influence on the uniform oxidation

of the substrates, particularly over convex and concave corners of the patterned structures. Afterwards, the devices were properly cleaned before the thermal process with piranha solution, rinsed with plenty of water and dried in an oven at 200ºC for 1h. A test silicon wafer was also introduced into the furnace to evaluate the oxide thickness by ellipsometry after the oxidation process.

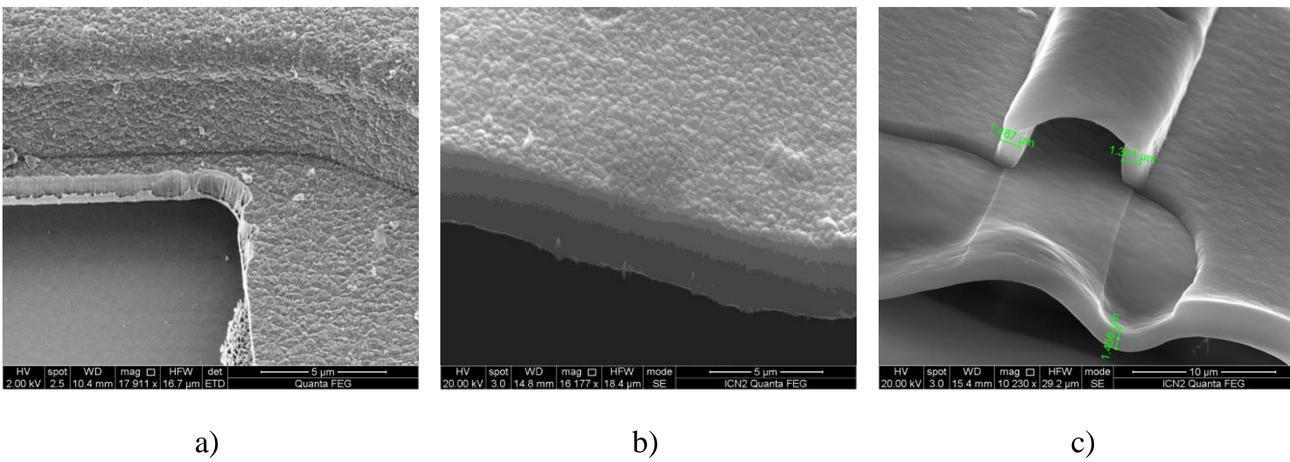
Table 3-2. Oxidation conditions for devices with polycrystalline silicon material. The time was determined according to the desired thickness of the oxidation layer.

750ºC in N_2 atmosphere for 55 min	Temperature ramp increases with a positive slope of 7ºC/min	Dry oxidation process at 1100ºC with 0_2 at a flow rate of 120 sccm for T_{dry} = TBD min Wet oxidation process at 1150ºC with water vapour for T_{water} = TBD min	Temperature ramp decreases with a negative slope of -7ºC/min	750ºC in N_2 atmosphere for 55 min

After the oxidation process, all samples were characterized using SEM to study the morphology and thickness of the conformally grown oxide layer. Measurements by ellipsometry provided imprecise oxide thicknesses given the lack of surface planarization of the wafer. The resulted non-uniformity can be associated with the following reasons: i) polycrystalline silicon consists of grains with various orientations and thus different oxidation rates can be expected according to the orientation of these grains (which are commonly orientated towards to (110) direction), ii) polycrystalline materials have two different diffusion paths, through the bulk and along the grain boundaries producing localized regions of thicker oxide layers, and thus more advanced models are required to estimate the final oxide layer thickness, as illustrated in Fig. 3-16, and iii) polycrystalline silicon is also more easily consumed than silicon material during the oxidation process given that the oxidation rate of undoped polycrystalline silicon lies between (100) and (111) silicon oxidation rates.

Furthermore, after the oxidation process of the devices, the majority of the released structures were under compressive stress forces. Thermally grown oxides are under compressive stress because the oxide volume is larger than the volume of substrate material they replace. Typical stress values are on the order of 300 MPa [7]. As seen in Fig. 3–17, the middle part of the beams was distorted upwards. The distortion ratio of the suspended beams was directly influenced by the width of the microchannels: wider structures had lower structural deformation than thinner ones. Since the temperature of both wet and dry oxidation processes was properly stabilized and monitored, time was the only varying parameter that might have influenced over the deformation of the structures. Furthermore, zones that were affected by the over-etching with HF 49% acid along the border of the central grid were contorted. It has been demonstrated that the stress of microstructures can be

reduced by performing annealing processes above 1000ºC [7], but in our case, those suspended structures were highly susceptible to be deformed because of their reduce thicknesses.



a) b) c)

Fig. 3–17. a) Grain size and distribution of an undoped polycrystalline silicon sample. The surface is rough and grains have a different orientation. b) A structural polycrystalline silicon layer with a 200 nm of grown oxide in which the grain size is smaller and compact, and the original polycrystalline silicon volume is consumed on both sides of the structural layer. c) A microchannel with a 1 µm thick layer of oxide where the original polycrystalline silicon layer was completely consumed. The surfaces of the channel are clearly smooth with a more uniform grain distribution.

An appropriate cleaning of the substrates was predominant to achieve oxide layers with high quality. Devices whereby a 50 nm layer of oxide was grown displayed black spots throughout the chip surface. These spots might have come from contaminated residues or zones that still had moisture as Table 3-3 resumes. Furthermore, wider microchannels suffered from clogging of the structural layers. Regarding the quality of the grown oxide layer, the visual inspection of the structures showed that the grain density of wider microchannels (35 µm) was greater than the exhibited by thinner microchannels (10 µm) for all the oxidation schemes. Smoother and more planar surfaces were created by increasing the oxide thickness. For instance, the wet oxidation scheme allowed the complete replacement of the whole polycrystalline silicon layer by conformally creating an 1 µm thick oxide structural layer as Fig. 3–17c shows. The quality of the polycrystalline silicon material deposited by LPCVD during the fabrication process also influenced on the porosity and density distribution of grains of the thermally grown oxides. For example, the device of Fig. 3–18f, with a 200 nm oxide layer, displayed holes along some of its grain boundaries. In here, the replacement of polycrystalline silicon material uncovered areas with poor grain density and thus they were not easily conformed by the oxide layer. In general, the dry oxidation was slower than the wet oxidation approach because the concentration of the oxidant was much greater in the latter one. For instance, the time to produce a polycrystalline silicon oxidation of about 1 µm was reduced by half (90 min) with respect to the dry oxidation layer of 200 nm (180 min). In sum, the oxidation of the structured devices was constrained because the compressive stress upon the microchannels walls became excessively large particularly for suspended structures, leading to deformation of their

original morphology. Table 3-3 shows an overview of the visual characterization of the oxidation processes for several devices.

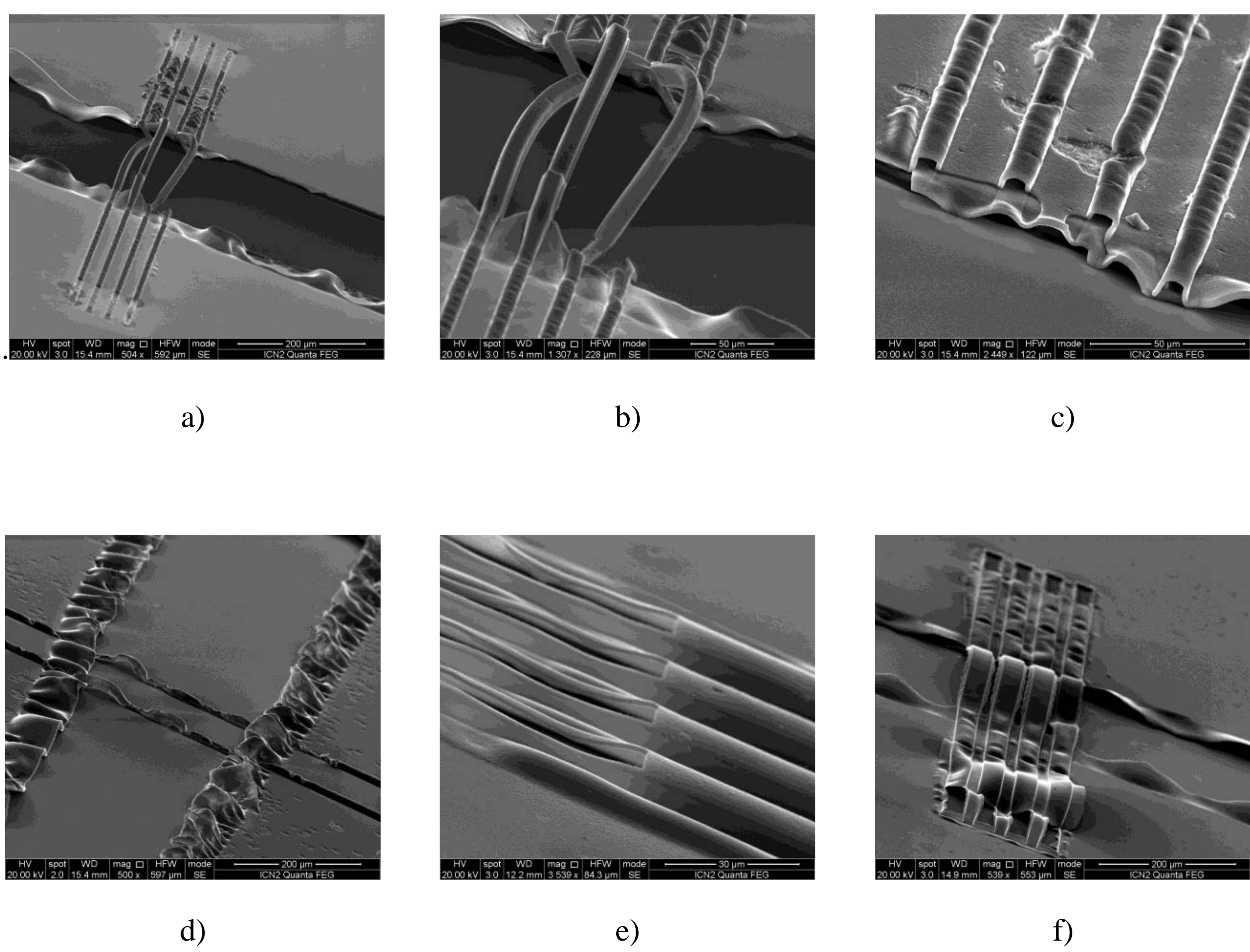
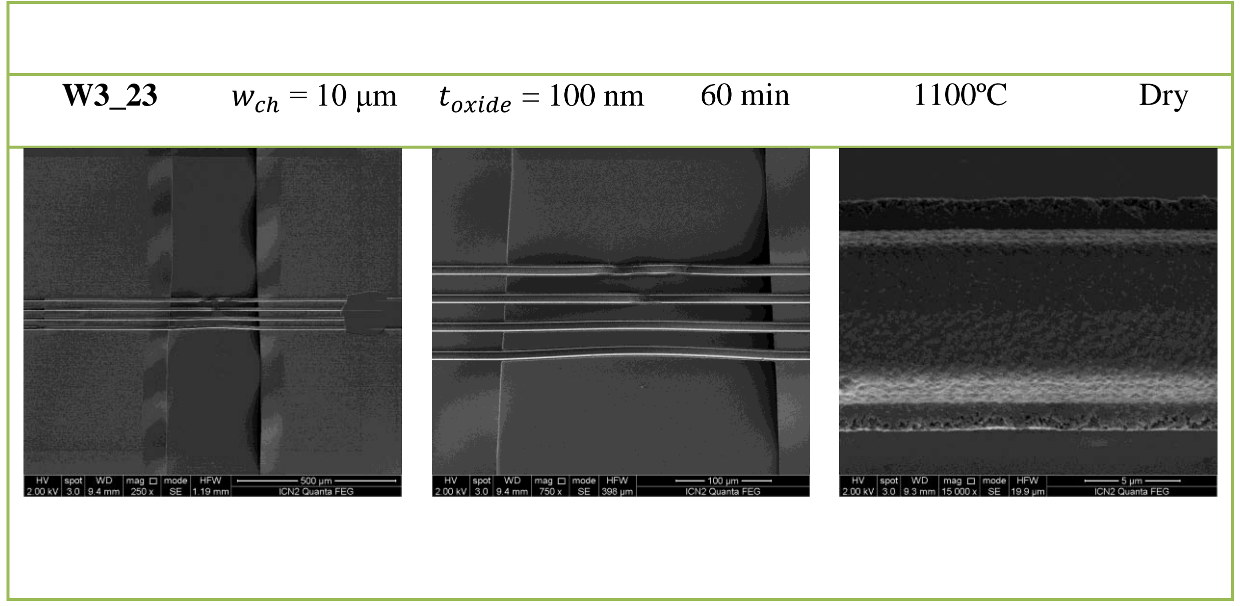


Fig. 3–18. a) - c) Aspect of the array of resonators after growing 1 µm layer of oxide by wet oxidation in which the structures are under compressive stress. d) - e) Contortion of the edges of the central grid were affected by the over-etching with HF 49% acid after growing an oxide layer of 150 nm. Also, the inlets of the microchannels were partially closed. f) The top structural layer was slightly detached from the substrate is some devices with a grown oxide of 200 nm.

Table 3-3. Summary of the oxidation schemes for polycrystalline silicon resonators

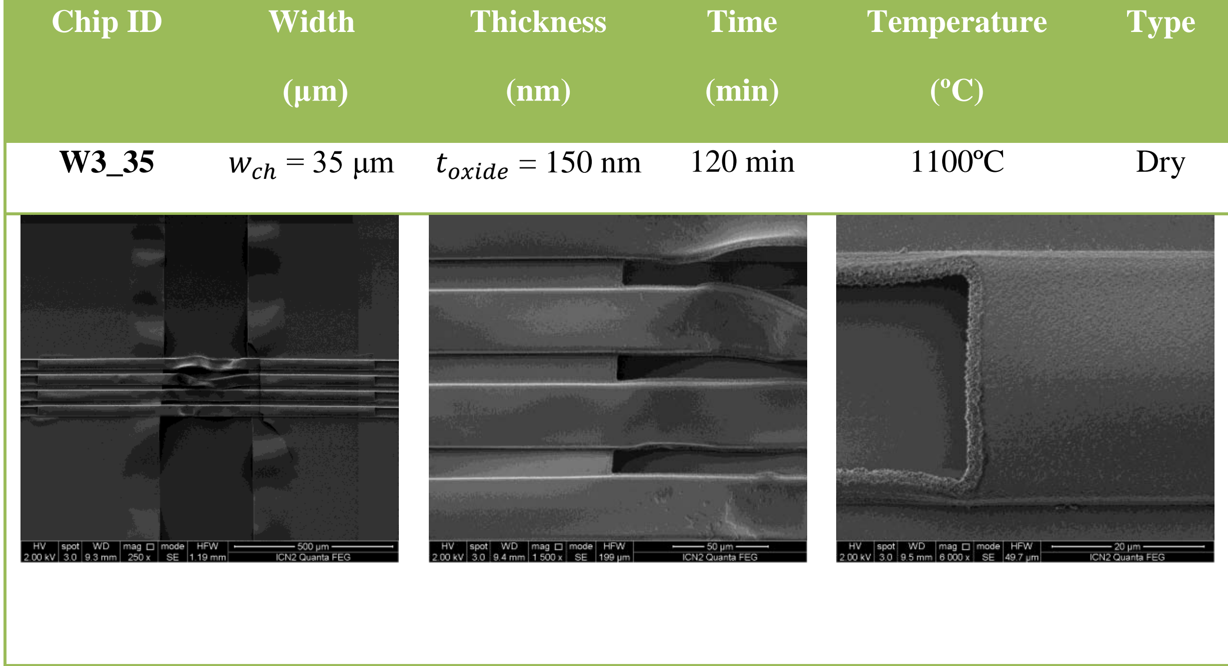
Chip ID	Width (µm)	Thickness (nm)	Time (min)	Temperature (ºC)	Type
W3_18	w_{ch} = 10 µm	t_{oxide} = 50 nm	15 min	1100ºC	Dry
W3_19	w_{ch} = 20 µm	t_{oxide} = 50 nm	15 min	1100ºC	Dry
W3_20	w_{ch} = 35 µm	t_{oxide} = 50 nm	15 min	1100ºC	Dry

W3_23	w_{ch} = 10 µm	t_{oxide} = 100 nm	60 min	1100ºC	Dry

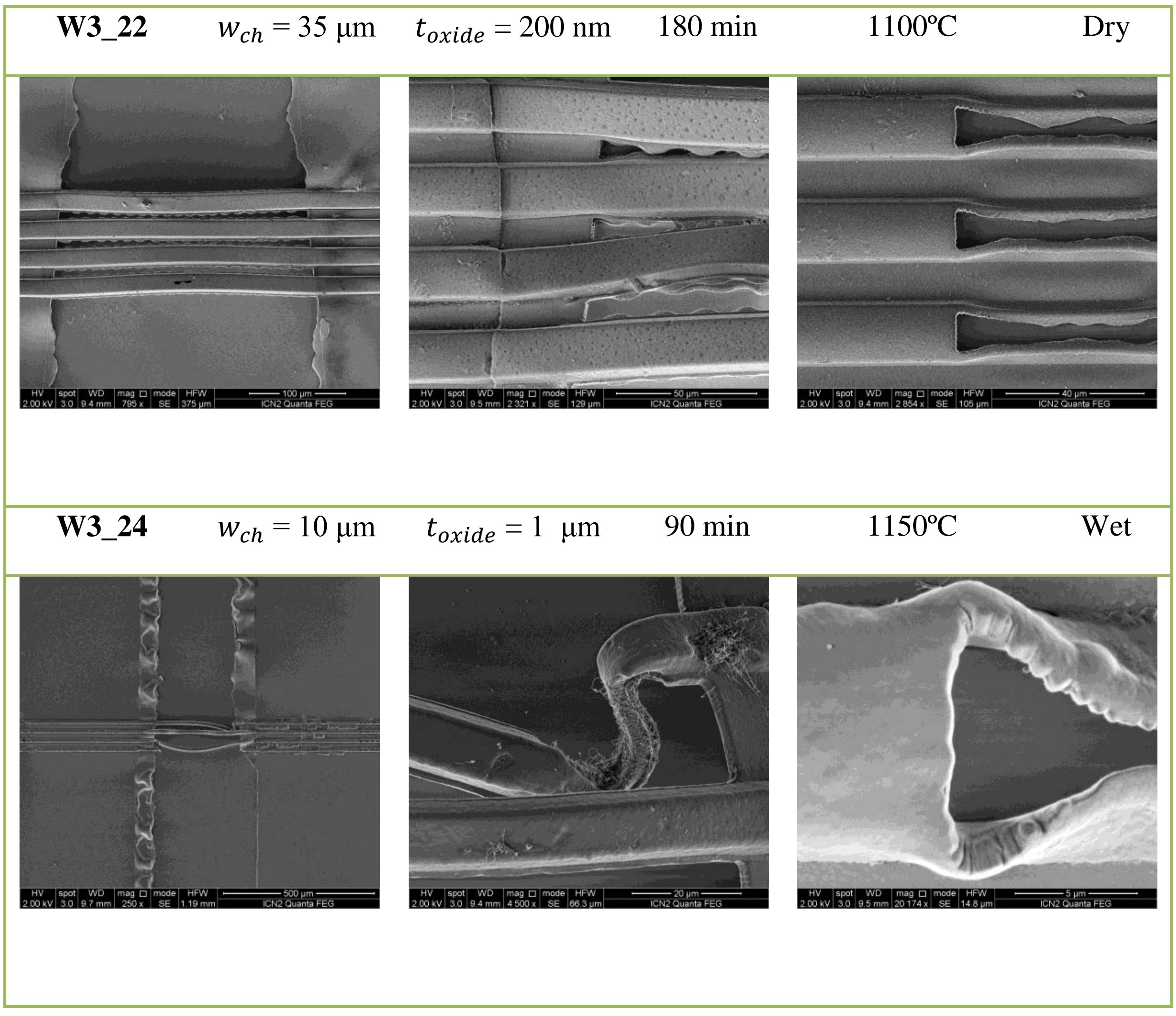


Chip ID	Width (µm)	Thickness (nm)	Time (min)	Temperature (ºC)	Type
W3_22	w_{ch} = 20 µm	t_{oxide} = 100 nm	60 min	1100ºC	Dry
W3_21	w_{ch} = 35 µm	t_{oxide} = 100 nm	60 min	1100ºC	Dry

W3_43	w_{ch} = 10 µm	t_{oxide} = 150 nm	120 min	1100ºC	Dry
W3_40	w_{ch} = 20 µm	t_{oxide} = 150 nm	120 min	1100ºC	Dry



Chip ID	Width (µm)	Thickness (nm)	Time (min)	Temperature (ºC)	Type
W3_35	w_{ch} = 35 µm	t_{oxide} = 150 nm	120 min	1100ºC	Dry


W3_22 w_{ch} = 35 µm t_{oxide} = 200 nm 180 min 1100ºC Dry
W3_24 w_{ch} = 10 µm t_{oxide} = 1 µm 90 min 1150ºC Wet

3.3 Fabrication process of HMB devices of the third generation

In this approach, the manufacture consisted of a sacrificial layer process of borophosphosilicate glass (BPSG) material, using polycrystalline silicon as a structural layer as in the previous fabrication process, but considering two objectives mainly: integrating on-chip microfluidics for fluid delivery and reducing the over-etching effect of the resonators as much as possible. The microfluidic delivery network for filling the embedded microchannels was built of SU-8 polymer, which demonstrated a good coverage step over the structures. The bypass microchannels were enclosed using a novel technique of SUEX lamination on top of the SU-8 resin. Also in this procedure, access through-holes were etched across the wafers using a combination of both surface and bulk micromachining techniques to inject the fluid sample from beneath the resonators

Fig. 3-19 shows the most important features of the HMB devices included in this fabrication scheme and a general overview of the main fabrication steps is introduced in Fig. 3-20.

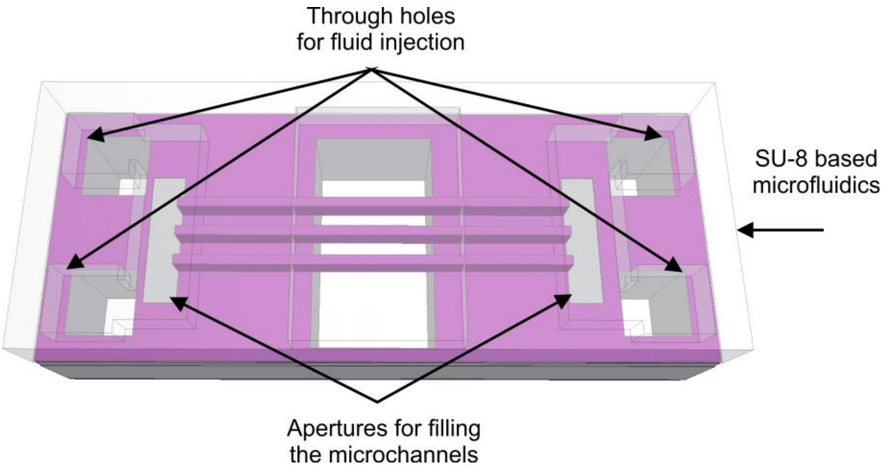


Fig. 3-19. General view of the main features implemented for the fabrication of HMB devices. Surface and bulk micromachining techniques define the suspended structures with embedded microfluidic channels. Access through-holes are etched across the wafer for liquid injection from below the structures. SU-8 and SUEX polymers are used to integrate the microfluidic delivery channels on top of the structures.

3.3.1 Mask design

The second batch of masks was designed specifically for the fabrication process using SU-8. In this case, six soda-lime photomasks of 5 inches in size were drawn in Klayout Software and printed by Compugraphics Company (Spain). The MFS for this type of mask was 1.5 µm. Additionally, another mask was included in the fabrication process to pattern an alternative design for the bypass microfluidic channels. This mask was made of acetate with MFS of 7 µm.

Fig. 3-21 shows twenty-seven devices distributed all over the mask design, including the doubled side alignment marks located in the center at a separation distance of 55 mm. Unlike the first batch

of masks, specific marks were designed throughout the wafer to monitor the main fabrication processes. The distribution of these motives facilitated various processes such as wafer inspection, layer thickness measurements, and dry and wet etching steps, among others. The dimensions of each device were 1.5 x 1 cm and the alignment of the masks is presented schematically in Annex 2.

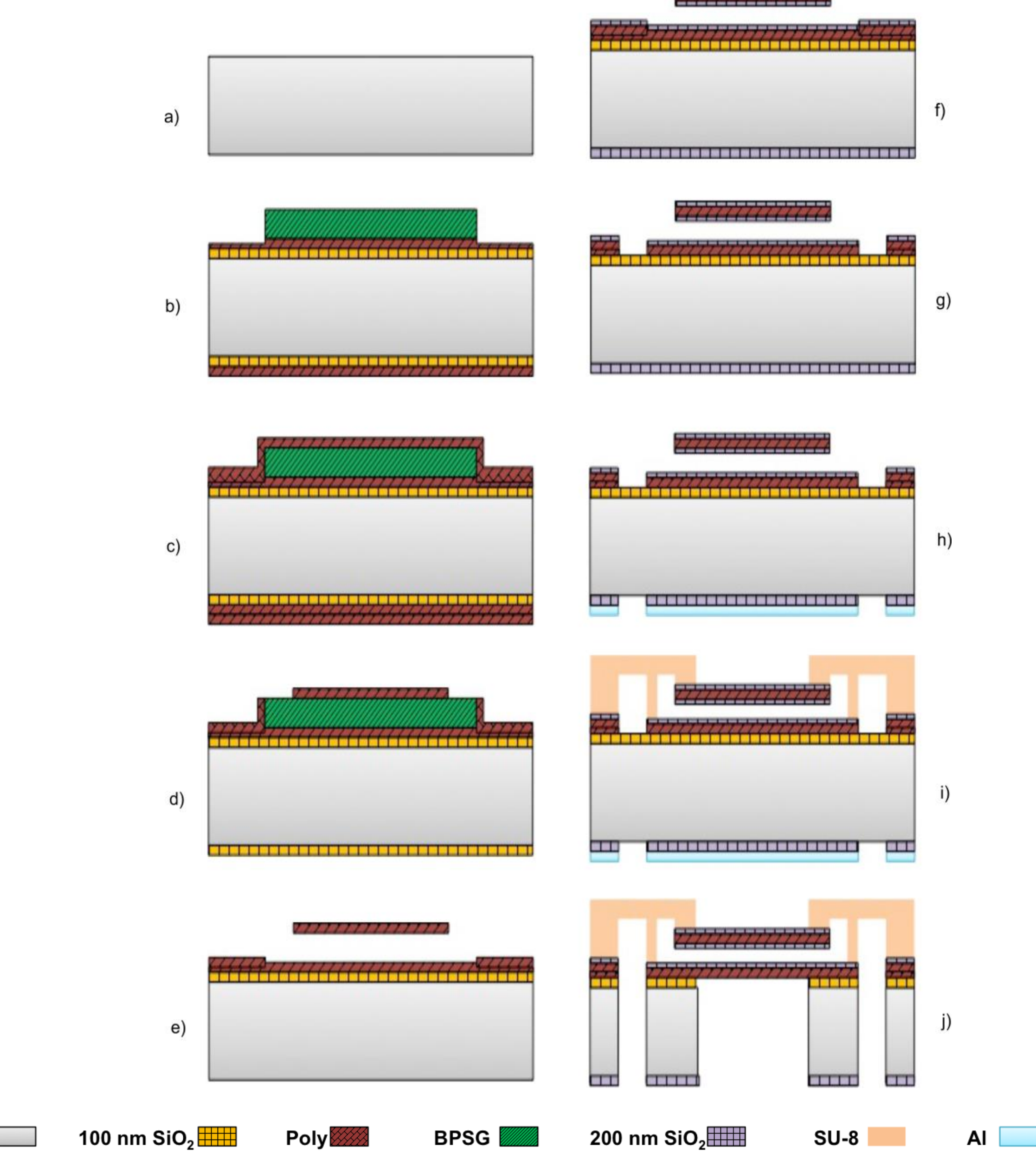


Fig. 3-20. Summary of the main fabrication steps: a) Initial silicon substrate, b) patterning of microchannels, c) microchannels enclosing, d) patterning of microfluidic inlets, e) wet etching of the sacrificial layer, f) oxidation of microchannels, g) patterning of fluid delivery inlets and definition of resonators, h) bulk micromachining steps, i) patterning and enclosing of polymer based microfluidics with SU-8 resin and SUEX epoxy and j) release of resonators and etching of fluidic inlets for liquid injection.

The content of each mask is described in detail as follows:

CNM788 HMB-BRID1. Similar to mask CNM677-BRID1, this is the first alignment mask that defines the dimensions of the microchannels. As

Fig. 3-21 shows, each device includes two configurations: a single microchannel (upper position) and an array of three microchannels (bottom position). Based on the experience from previous fabrication processes, the length of the microchannels was set to 900 µm to reduce the etching time of the sacrificial layer. For configurations that included an array of microchannels, the separation distance between each beam was set to 500 µm to overcome the superposition of the mechanical response of resonators with and effective length set to 200 µm, 250 µm and 300 µm correspondingly. Also, the design of some resonators included a rectangular square in the middle of the microchannels. This section of the microchannel can work as a mechanical trap with the aim of increasing the residence time of fluids or streaming analytes.

The microfluidic inlets for all the microchannels were connected together to facilitate the entrance of fluids inside the cavities. This mask also included labels for indicating the device number, microchannels width, and alignment marks, as

Fig. 3-21c shows.

CNM788 HMB-HOLE2. This mask is aligned with respect to CNM788 HMB-BRID1 mask to define the fluidic inlets of the microchannels. Two aperture holes of 1500 x 110 µm of size located at both ends of the microchannels are outlined to uncover the sacrificial layer. Unlike mask CNM677-HOLE2, this mask just defines the fluidic inlets of the microchannels (see Fig. 3-22a). The effective length of the resonator and the outer frame motives were included in the next alignment mask to avoid the over-etching of resonators while removing the sacrificial layer with HF 49% acid.

CNM788 HMB-OPEN3. In this mask, the effective length of the resonators is defined including the outer frame to release the devices from the substrate. Clamp supports are designed on every corner side of a single device. During the fabrication process, this mask is aligned with respect to CNM788 HMB-HOLE2 mask. Moreover, four square holes (of 400 µm x 400 µm in size) are outlined around every configuration for the microfluidic inlets of the bypass channels as can be seen in Fig. 3-22a.

CNM788 HMB-GRID6. This mask is aligned with respect to CNM788 HMB-BRID1 mask using the double-sided alignment marks. The main features of this mask are like those from CNM788 HMB-OPEN3 mask with the exception that bulk micromachining steps are carried out to release the structures from beneath the silicon wafer (see Fig. 3-22a). Access through-holes are also defined for the bypass microfluidic channels inlets along with the outer frame of the devices.

CNM788 HMB-SU8A. In this mask, the polymer bypass fluidic channels are designed to fill the microfluidic channels of the resonators. Both channels of 200 µm width are placed along the fluidic inlets of the microchannels constituting an H-shaped microfluidic network, see Fig. 3-22a. During the fabrication process, this mask is aligned with respect to CNM788 HMB-OPEN3 mask.

CNM788 HMB-SU8A(ACETATE). Similar to mask CNM788 HMB-SU8A this design includes polymer channels to fill the resonators but with a single input/output fluidic configuration, also known as in-line. Initially, the channel has a 200 µm width, and then, it gradually expands to 1200 µm to cover all the fluidic entrances of the microchannels (see Fig. 3-22b). The same design is patterned on the other side of the microchannels. To reduce chances of clogging over wider areas of the microchannels, the mask design includes well-distributed pillar supports of 50 µm x 50 µm in size. This mask is made of acetate and therefore, the resolution is lower that the soda-lime counterpart. Nevertheless, the MFS complies well with the minimum feature size of motives.

CNM788 HMB-SU8B. This mask is aligned with respect to CNM788 HMB-SU8A mask and it is used during the lamination process of SUEX epoxy to enclose the bypass fluidic channels. Basically, it uncovers the epoxy from above the microstructures to allow the incidence of light for the mechanical characterization of the beams. It also uncovers the epoxy from the cutting marks of the devices to release them from the wafer, Fig. 3-22.

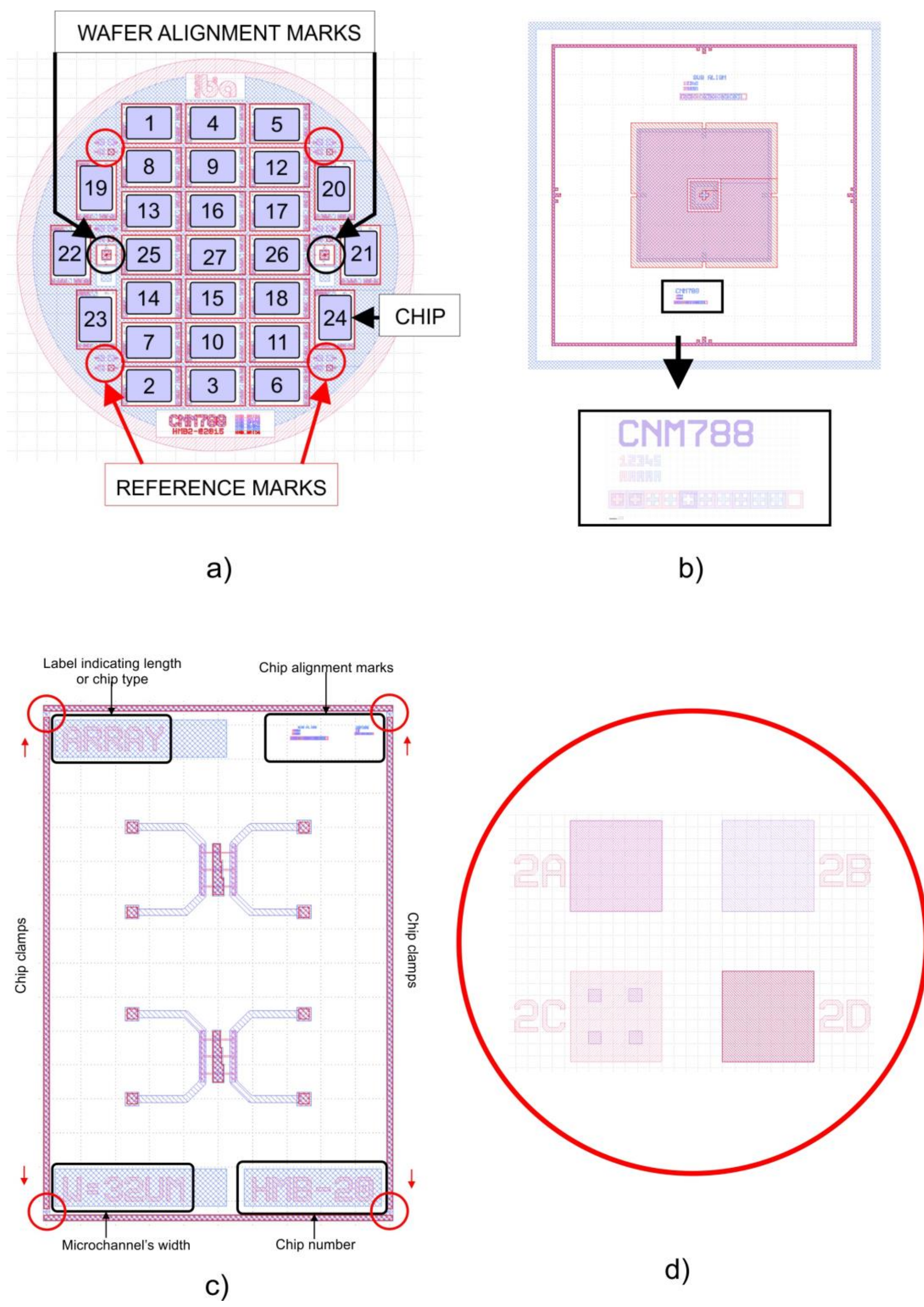
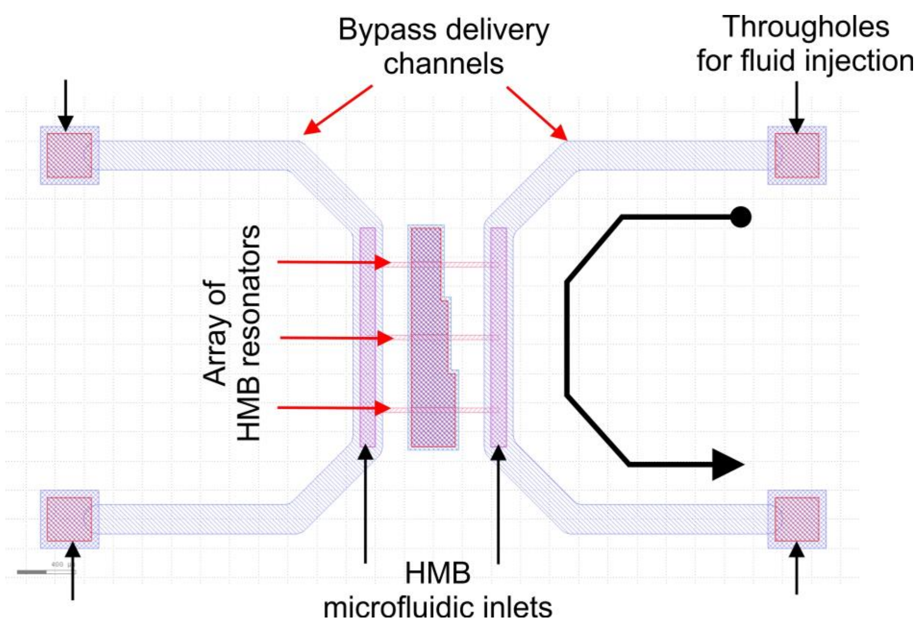
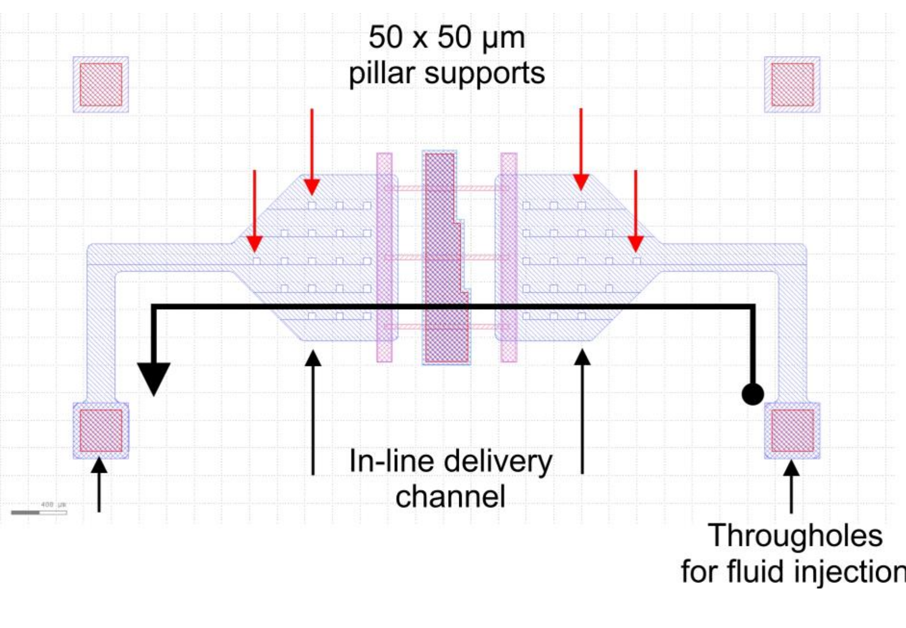


Fig. 3-21. General view of the main features in the mask design: a) twenty-seven devices distributed all over the mask design, b) double-sided wafer alignment marks and on-chip reference marks, c) design of a single device that integrates two configurations of HMB resonators, identification labels and outer frame with four clamps on every corner and d) reference marks to follow up and verify specific fabrication steps.



a)



b)

Fig. 3-22. Main features of the HMB devices: a) an array of three resonators with lengths of 200 µm, 250 µm and 300 µm, respectively. Wide fluidic inlets (1500 µm x 110 µm) are incorporated at both ends of the microchannels. Also, access through-holes are outlined for injection of fluid beneath the wafer. In this design, an H-shaped microfluidic configuration fills up the inner cavities and b) a simple input/output microfluidic configuration fills up the microchannels. It also integrates well-distributed pillar supports to avoid clogging of the polymer channels.

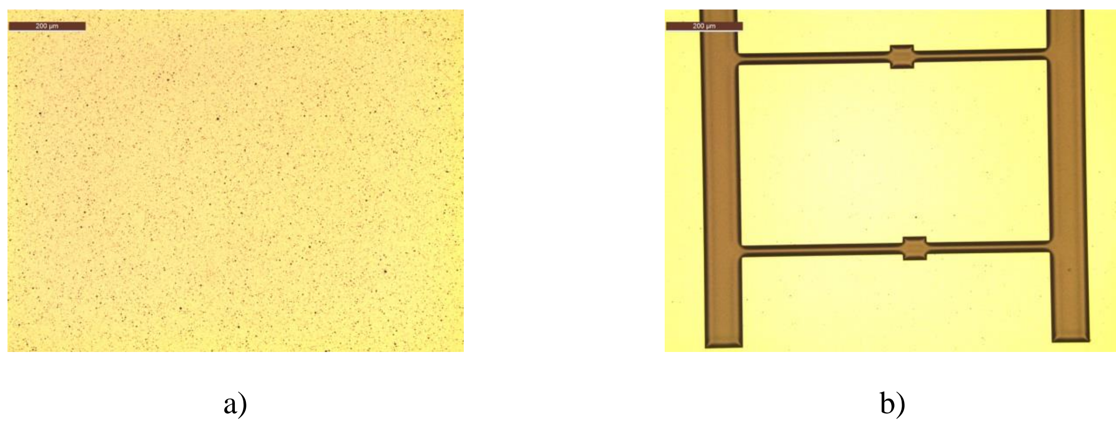
3.3.2 Fabrication process at cleanroom facilities

The microchannels were built using 4-in two side polished, type P silicon wafers of 300 μm thick with a resistivity of 10-20 ohm-cm. Four silicon wafers were used as substrates, and their curvature was measured in the profilometer along the 0° and 90° axes (step 3) which yielded a compressive stress of wafers according to their curvature values (up to 4.5 μm).

Step	Code	Description	Wafer
1	INICIO	Preparation to begin RUN	1-4
2	MARC-PXA	Marking of silicon wafers	1-4
3	MES-PRO	Curvature measurement of backside of wafer	1-4
4	NET-GEN	General cleaning	1-4
5	OHC-1000	Thermal growth of 100 nm of SiO_2 at 950°C	1-4
6	NETG-SIM	General simple cleaning	1-4
7	DPOLSENA	LPCVD deposition of 1 μm of polycrystalline silicon (580°C/350 mTorr)	1-4

Si · 100 nm SiO_2 · Poly · BPSG · 200 nm SiO_2 · SU-8 · Al

Then, a 100 nm layer of SiO_2 was thermally grown to isolate the silicon substrate from the following processes (step 5). As follows, a 1 μm layer of polycrystalline silicon was coated by LPCVD (step 7). In this step, a variation in the flow rate of the source gases produced an irregular deposition of polycrystalline silicon, which formed a ring of varying polycrystalline silicon thickness over the wafer perimeter. A two consecutive deposition of 2 μm of doped SiO_2(BPSG) was further carried out (step 8). After the deposition, however, there were particle counts on the surface and embedded in between the deposited layers as Fig. 3–23a shows. These particles and residues were reduced by immersing the wafers in a dip HF 5% solution for 15 s and doing an ultrasonic bath with water for 10 min.



a) b)

Fig. 3–23. a) Multiple particle counts after the two consecutive layer depositions of the BPSG material and b) patterning of the microfluidic channels using photolithography and RIE with a protective resin of 4 µm. Some microchannels include a rectangular square in the middle of the doubly clamped resonator as a mechanical trap for increasing the residence time of fluid samples.

Step	Code	Description	Wafer
8	DBPTEOSX	PECVD deposition of 2 µm of doped SiO_2 BPSG	1-4
		PECVD deposition of 2 µm of doped SiO_2 BPSG	1-4
	NETG-ESP	Special cleaning of wafers	1-4
9	FOTO-ESP	Photolithography of front wafer side with mask CNM788 HMB-BRID1	1-4
10	ESPECIAL	Resin annealing at 200°C for 30 min	1-4
11	PAMI-ESP	Dry etching of doped SiO_2 BPSG	1-4
12	P601POLI	Dry etching of 200 nm of polycrystalline silicon	1-4
13	DEC-RESI	Resin stripping	1-4
14	ASEM-ING	Inspection using the Scanning Electron Microscope LEO1530	1-4
15	NETG-ESP	Special cleaning of wafers with stripping agent	1-4
16	NETG-SIM	General simple cleaning	1-4
17	DPOLSENA	LPCVD deposition of 1 µm of polycrystalline silicon (580°C/350 mTorr)	1-4

Si 100 nm SiO_2 Poly BPSG 200 nm SiO_2 SU-8 Al

The patterning of the microchannels was done by soft-contact photolithography with mask CNM788 HMB-BRID1 (step 9) following by RIE of the BPSG. Another dry etching of 200 nm of polycrystalline silicon followed to completely remove the BPSG material from the wafers (step 12). This step preserved the integrity of the sacrificial layer topography, since it was unnecessary to wet etch the silicon oxide residues, which in previous fabrication procedures smoothed the microchannels edges. Fig. 3–24 shows SEM micrographs of the outlined topography of the doped SiO_2 sacrificial layer (step 14). However, some structures were still covered by the protective resin, and thus a special cleaning with stripping agent was necessary to remove any residue. Afterwards, a LPCVD deposition of 1 μm of polycrystalline silicon enclosed the microchannels with good step coverage (step 17). Polycrystalline silicon deposited on top of the microchannels showed a smoother grain pattern than that deposited on the rest of the wafer. This demonstrates the influence of the underlying substrate properties on the quality of deposited thin-films, as Fig. 3–25 shows. After spinning the protective photoresin onto the front side of wafers, a dry etching process was used to remove 2 μm of polycrystalline silicon material from the backside of the wafers (step 20). In some areas, polycrystalline silicon particles served as a mask layer to create small pillars that were difficult to remove, as Fig. 3–25c illustrates. For the case of wafer 4, these pillar were removed by lifting off the underneath silicon dioxide layer (step 21) with BHF solution for 15 s.

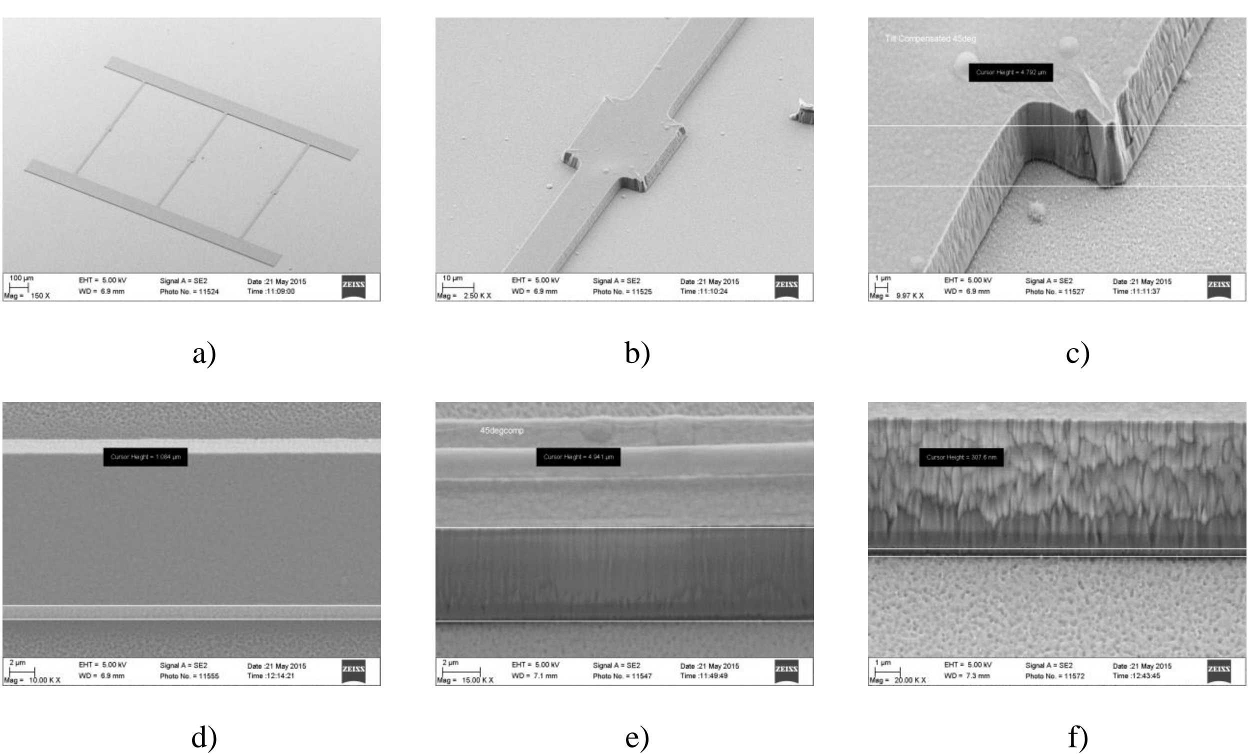
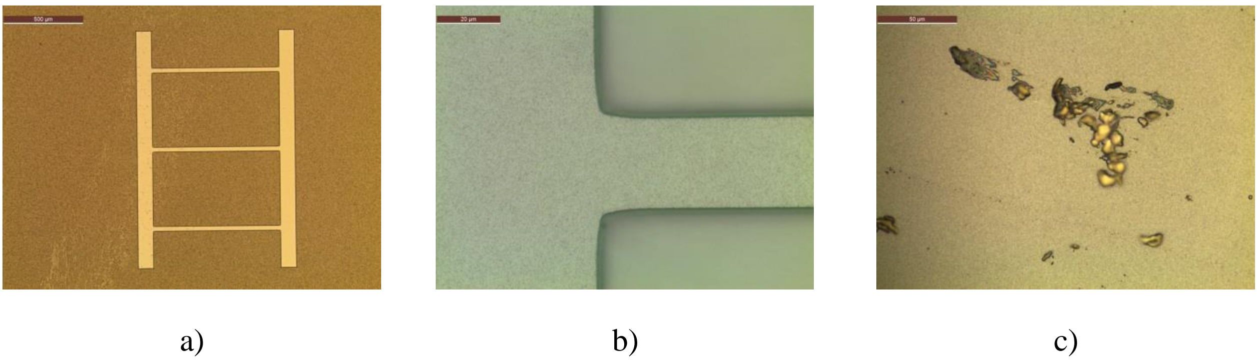


Fig. 3–24. a) - c) Patterning of the sacrificial layer and definition of the microfluidic channels with an average height of 4 μm, d) top view of a microfluidic channel showing the vertical sidewalls of the channels and e) - f) cross sectional view of the channel and the partially etched polycrystalline silicon layer; resin residues are noticeable on top of some microchannels.



a) b) c)

Fig. 3–25. a) - b) Enclosing of microchannels with polycrystalline silicon material showing good step coverage; the quality of the deposited material relies on the layer thickness and on the underlying material properties and c) particles counts on the wafer backside that served as a mask layer while dry etching the polycrystalline silicon from below the wafer.

Step	Code	Description	Wafer
18	FESPECIA	Deposition of 6 μm of protective resin on wafer's front side	1-4
19	HOLDICTS	Protective resin is stripped and wafers are cleaned with piranha solution	4
20	PAMI-ESP	Dry etching of polycrystalline silicon from the backside of wafers	1-4
21	GHUM-ESP	Wet etching of the backside silicon dioxide	4
22	DEC-RESI	Resin stripping	1-3
23	NETG-SIM	General simple cleaning	1-3
24	MES-NANO	Thickness measurement of SiO_2 on the backside of wafers	1-4
25	QDRACXXX	Resin stripping with acid	1-4
26	FOTO-ESP	Photolithography of front wafer side with mask CNM788 HMB-HOLE2	1-4
27	P601POLI	Dry etching of 1 μm of polycrystalline silicon	1-4
28	DEC-RESI	Resin stripping	1-4
29	QDRACXXX	Resin stripping with acid	1-4
30	MST-ESP	Wet etching of doped SiO_2 BPSG with HF 49% acid	1-4
31	NETG-SIM	General simple cleaning	1-4

Si 100 nm SiO_2 Poly BPSG 200 nm SiO_2 SU-8 Al

Next, access holes to etch the sacrificial layer were defined by soft-contact photolithography (step 26) with mask CNM788 HMB-HOLE2 and RIE (step 27) on top of the polycrystalline silicon material. The etching process was monitored at specific motives (2C) that were vertically distributed on top and below the double-sided marks of the wafers, as shown in Fig. 3–26. The opening of these marks was more rapid than the aperture of the microfluidic inlets. Hence, the etching selectivity of polycrystalline silicon was influenced by the dimensions of the apertures and also by the location of the devices throughout the wafer. Fig. 3–26 shows the uncovered sacrificial layer after removing the protective resin.

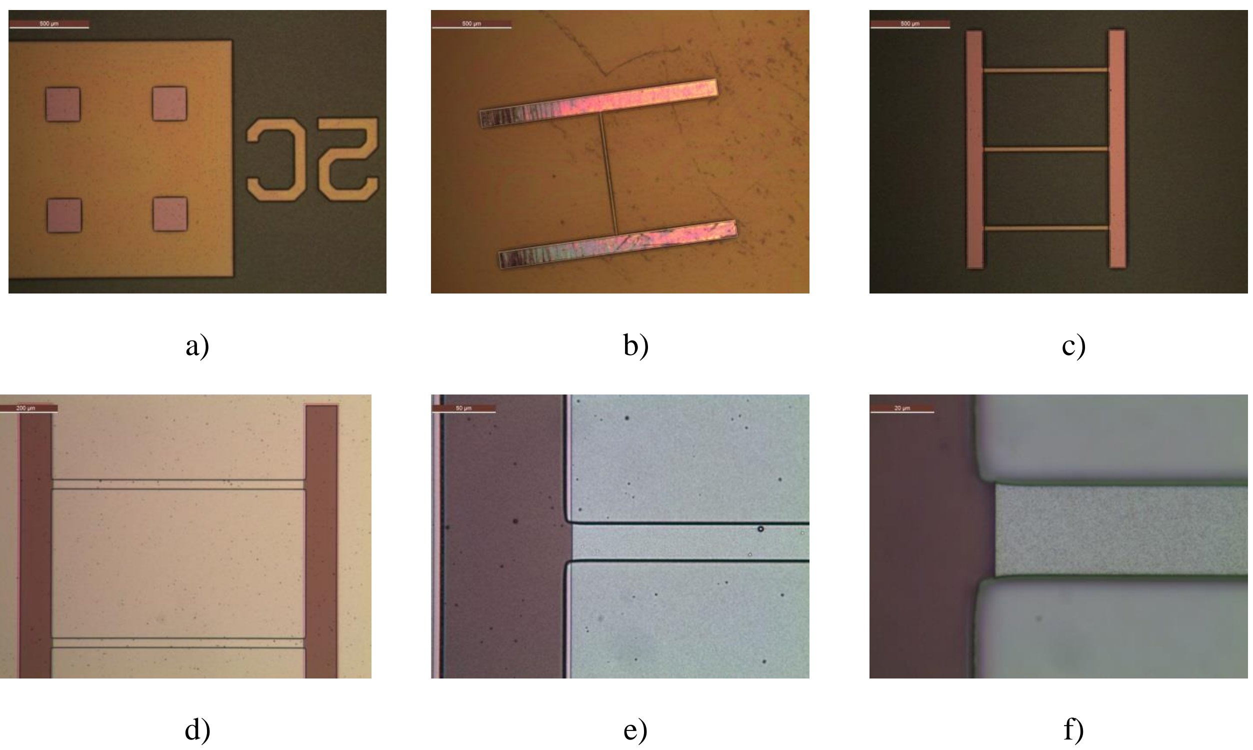


Fig. 3–26. a) Specific wafer marks that were designed to monitor several fabrication steps. The aperture of the microfluidic inlets was verified during the polycrystalline silicon dry etching process. b) - c) the etching selectivity was roughly influenced by the dimensions of the apertures and location of devices and d) - f) uncovering of the sacrificial layer at both ends of the microfluidic channels (*light rose colour*).

The sacrificial layer was etched immersing the wafers in HF %49 solution for about 60 min to guarantee the complete removal of the BPSG (step 30). This time was calculated based on the maximum lateral length of the microchannels and on the etching ratio of the BPSG layer. To verify that the embedded sacrificial layer was etched, some of the structures were carefully scratched using fine tweezers. As a result, the sacrificial layer was effectively etched because all devices showed a hollow cavity. For higher etching times (67 min for the case of wafer 4) the structural material of some devices was partially etched by the solution, as shown in Fig. 3–27. The adhesion of the polycrystalline silicon layers was also affected along the edges of the microfluidic inlets.

Although the top polycrystalline silicon layer was softly detached from the substrate in some devices, the entire integrity of the structures was maintained as can be seen in Fig. 3–27c. Then, a 200 nm oxide layer was thermally grown at 950°C within and all over the walls of the microchannels to improve the hydrophilic properties of the structural material (step 32), based on the analysis done in the section 3.2.2. This step deformed the edges of the microfluidic inlets due to the high temperatures of the oxidation process that caused a compressive stress over the structural material.

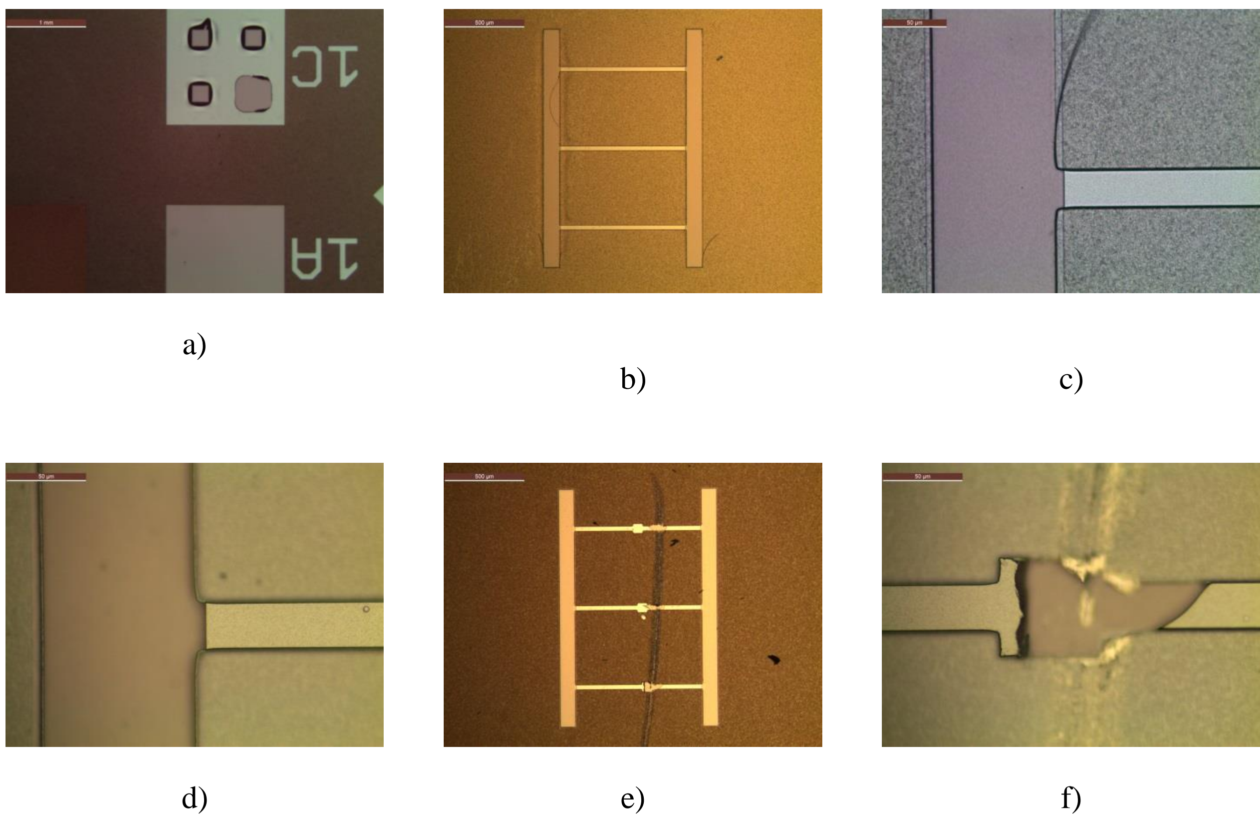
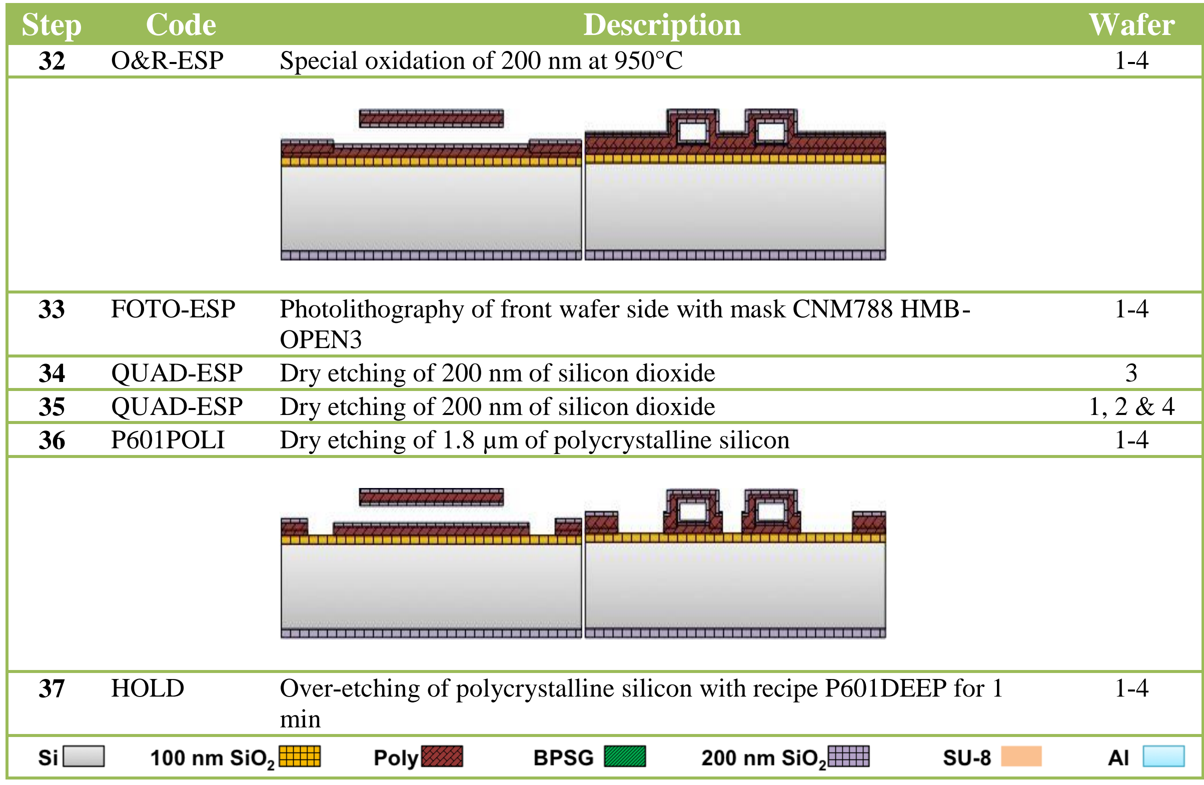


Fig. 3–27. Wet etching process of the BPSG sacrificial layer: a) test structures to verify the lateral etching of the sacrificial layer, b) - d) final view of the microchannels after the etching process. In general the integrity of the polycrystalline silicon layer was maintained, yet some devices were over-etched along the sidewalls of the structures and e) - f) the top layer of some microchannels was scratched to verify the formation of hollowed cavities.

In the next step, the effective length of the resonators and the access through-holes for the injection of liquid were outlined by soft-contact photolithography (step 33) on the wafers front side with mask HMB-OPEN3. First, the thermally grown oxide layer was removed by RIE (step 34). This processed was visually monitored until the colour of the underlying polycrystalline silicon material was revealed (a light yellow colour).Thereafter, the unmasked polycrystalline silicon material was also removed by RIE until revealing the underlying silicon oxide (step 36), which had a light blue colour. During this step, the polycrystalline silicon material was not completely etched in some microchannels specifically along the sides that define the resonators shape (see Fig. 3–28).

Therefore, wafer 1 was over-etched for 1 min more but no effect was noticeable. Then, all wafers were over-etched for 1 min more using DRIE. As a result, some structures improved their shape definition but others still had material excess, which formed a strip of different colours on both sides of the structures.



Step	Code	Description	Wafer
32	O&R-ESP	Special oxidation of 200 nm at 950°C	1-4
33	FOTO-ESP	Photolithography of front wafer side with mask CNM788 HMB-OPEN3	1-4
34	QUAD-ESP	Dry etching of 200 nm of silicon dioxide	3
35	QUAD-ESP	Dry etching of 200 nm of silicon dioxide	1, 2 & 4
36	P601POLI	Dry etching of 1.8 µm of polycrystalline silicon	1-4
37	HOLD	Over-etching of polycrystalline silicon with recipe P601DEEP for 1 min	1-4

This effect was because of the 200 nm silicon dioxide layer that was not completely removed in the previous step. As follows, the resin of the wafer front side was used as a protective layer while depositing 500 nm of aluminium over the backside of wafers by electron beam evaporation (step 38). Traces of particles were removed using nitrogen. From here, the fabrication process continued only with wafer 1 to analyse the feasibility of the following steps. Access holes for the injection of fluids and for releasing the microstructures were patterned on the backside of wafer 1 by photolithography (step 39) using mask CNM788 HMB-GRID6. First, the aluminium material was etched (step 40) and then the protective layer from the water front side was removed. The dry etching of the underneath silicon oxide required that the protective resin was annealed to stand for the RIE conditions (step 41 and 42). A special cleaning with plasma was then done after the dry etching of silicon dioxide to remove any trace of resin from both sides of the wafer. Microscope images and SEM micrographs show the hollow cavity and the topology of microchannels in Fig. 3–29 and

Fig. 3–30. Nevertheless, in some microchannels, the polycrystalline silicon layer was also removed due to the long-term adhesion of the protective layer on the front side of the wafers.

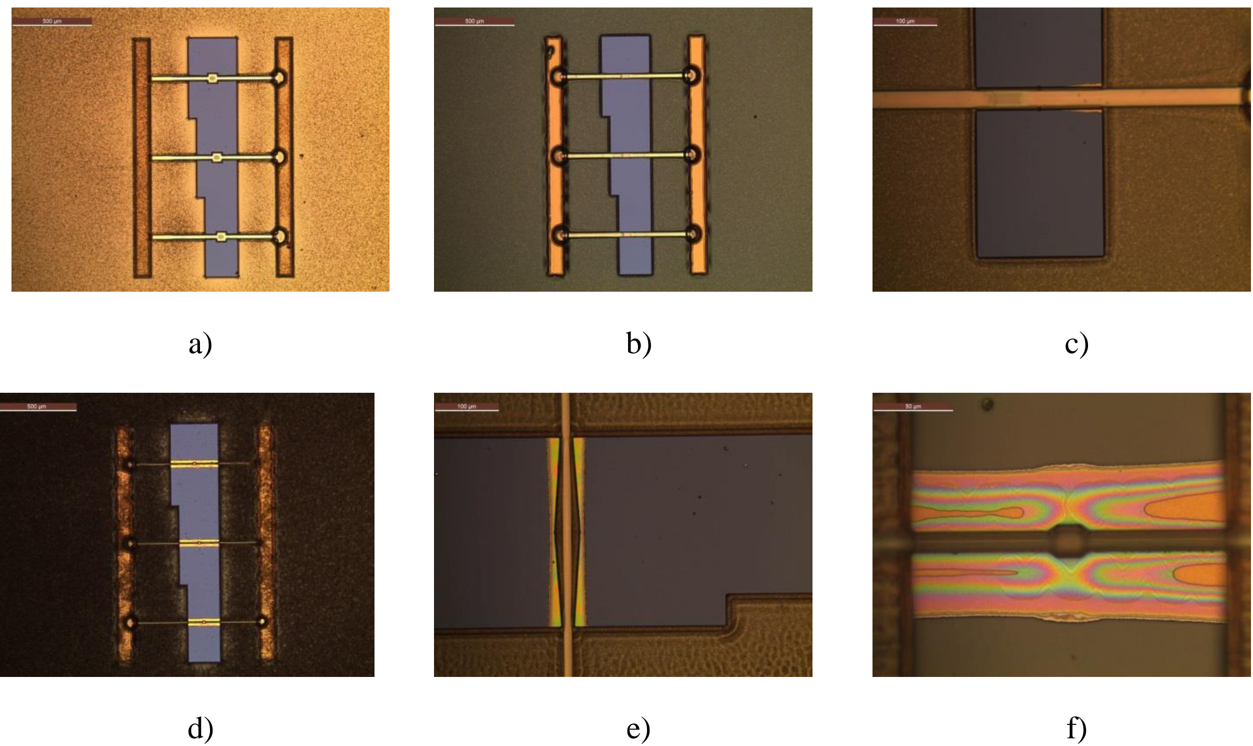


Fig. 3–28. a) - c) Dry etching of polycrystalline silicon layers to uncover the underlying silicon dioxide layer. The process was easily monitored by tracking the coloration shift of the polycrystalline silicon from *light yellow* to *light blue* colour. d) - f) Polycrystalline silicon was not completely removed along the edges of some microstructures owing to traces of silicon dioxide material that decreased the etching selectivity of the polycrystalline silicon over these areas.

Step	Code	Description	Wafer
38	MEVPKING	Deposition of 500 nm of aluminium over the backside of wafers	1-4
39	FOTO-ESP	Photolithography of the backside of wafer with mask CNM788 HMB-GRID6.	1
40	PQ2ALXXX	Dry etching of 500 nm of aluminium	1
41	ESPECIAL	Stripping of resin on the front side of the wafer	1
42	ESPECIAL	Annealing of backside resin at 200°C for 30 min	1
43	PGIOXXXX	Dry etching of silicon dioxide from backside of wafer	1
44	DEC-RESI	Resin stripping in both sides of the wafer	1
45	NETG-ESP	Special cleaning	1

Si; 100 nm SiO_2; Poly; BPSG; 200 nm SiO_2; SU-8; Al

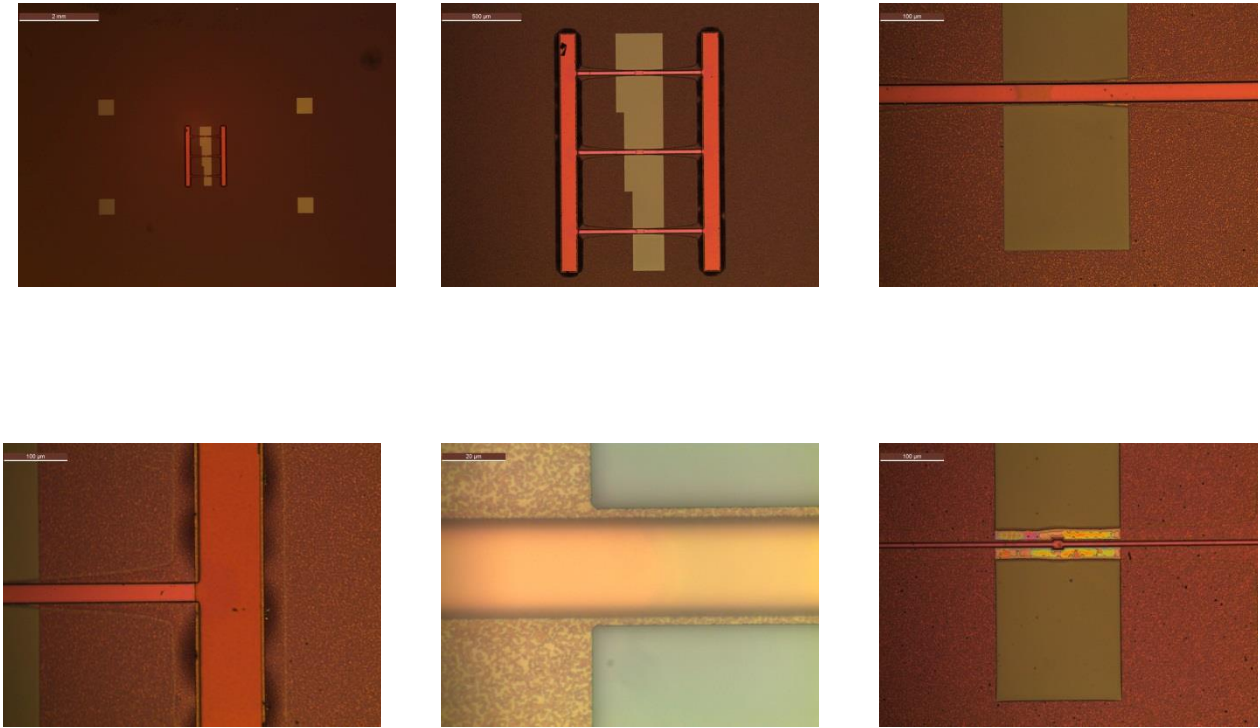


Fig. 3–29. Aspect of the microchannels after removing the front side protective resin. The *light rose* colour indicates the oxidation of the polycrystalline silicon layer (270 nm thick). Deformation of the edges of the microfluidic inlets was due to the over-etching of the sacrificial layer and the compressive stress during the thermal oxidation of the structures. However, the definition of the resonators improved after the DRIE process.

A 25 µm layer of SU-8 resin was patterned on the front side of the wafer to define the microfluidic bypass channels using the protocol described in detailed in section 4.1.2. The thickness of the SU-8 layer showed good step coverage over the 5 µm topography of microchannels. It is important to isolate the resonators bending motion from the fluid sample delivery system to avoid an overdamped response of the beams. Thereafter, to enclose the bypass microchannels, a 100 µm layer of laminated SU-8 resin (SUEX) was deposited and patterned using the protocol described in the next section 3.3.3. The underneath SU-8 layer protected the embedded microchannels during the lamination process.

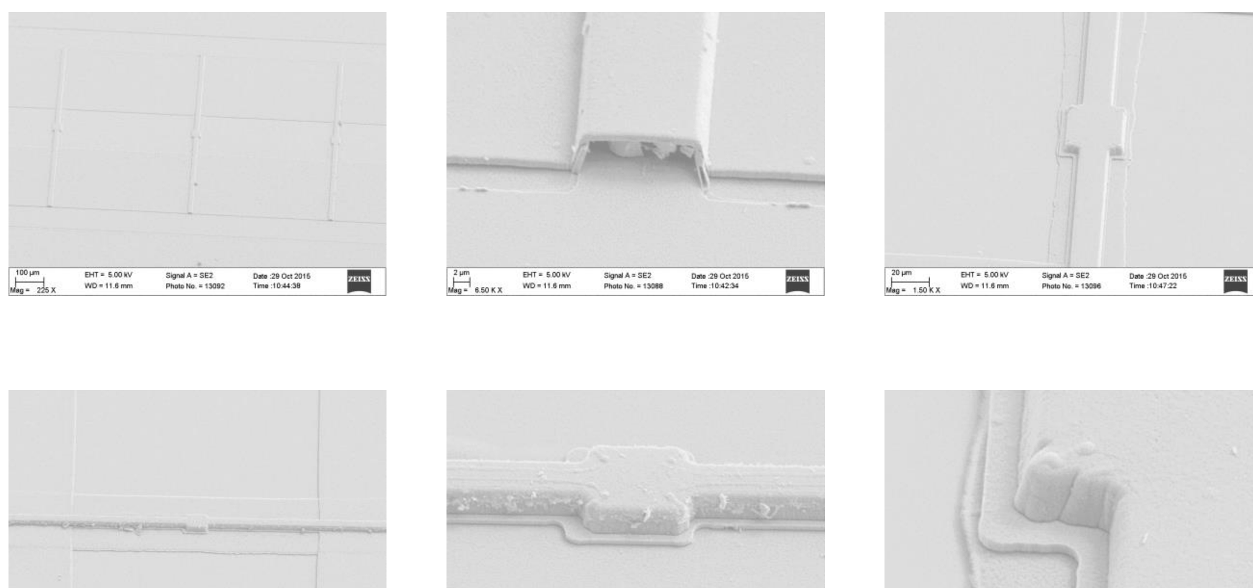


Fig. 3–30. SEM micrographs that show the morphology of the microchannels. The long-term adhesion of the resin filled up the inner cavities. Clogging of microchannels was reduced by cleaning the wafers with piranha solution; also the polycrystalline silicon material could not be completely removed to correctly define the beams morphology.

Step	Code	Description	Wafer
46	FOTO-ING	Patterning of 25 µm of SU-8 negative resin on the front side of wafer using mask CNM788 HMB-SU8A	1
47	FOTO-ING	Patterning of 100 µm of laminated SUEX film on the front side of wafer using mask CNM788 HMB-SU8B	1

Si | 100 nm SiO_2 | Poly | BPSG | 200 nm SiO_2 | SU-8 | Al

3.3.3 Fluidic integration with polymers

Recently, the SUEX epoxy Thick Dry film Sheets (TDFS) has emerged as a promising material for several applications that include polymer MEMS, microfluidics, BioMEMs, medical devices, wafer level packaging, optical spacers and embedded devices [8]–[12]. The varying thickness of the epoxy (ranging from 100 to 1000 µm) offers additional advantages over the use of conventional resins, such as polymethyl methacrylate (PMMA), to create multi-level designs with high aspect ratios. Moreover, the lamination process for depositing the SUEX epoxy is relatively simple, fast and flexible to be used on different substrates to pattern designs using either UV or X-ray lithography.

Taking into account the above advantages, we used negative SUEX 100 µm TDFS to enclose the bypass SU-8 microfluidic channels. The process consisted of putting in contact the wafer with the dry resist film using a commercial laminator equipment (GBP Proseries 3500 Laminator) according to the protocol provided by DJ DEVCorp company [10]. The first step consisted on cleaning the surface of the wafer and placing it onto an aluminium sheet, see Fig. 3–31a. Only one of the two protective polyester layers (PET) was removed from the SUEX dry film to allow direct contact of the epoxy with the patterned wafer (see Fig. 3–31b). Moreover, to ensure best lamination results, the wafer was totally covered by another PET sheet which prevented sticking of the resin with the rollers and moving parts during the lamination process, as Fig. 3–31c shows. The aluminium stack was then moved through the heated rollers at a temperature of 80°C and speed of 6 ft/min. Generally, this lamination process is carried out at lower speed (1 ft/min) and at lower temperature (65°C) depending on the resist thickness and type of substrate. In our case, we reduced the chances of damaging the hollowed microstructures by optimizing the temperature of the rollers and velocity of the laminator, since the control of the applied pressure was not adjustable (see Fig. 3–31d).

To ensure good step coverage of the resin and for obtaining smoother surfaces, a post lamination bake (PLB) with the PET coversheet still in place was done using a levelled hot plate at 40°C for 40 min (see Fig. 3–31e). The wafer was irradiated using a UV exposure dose of 600 mJ/cm^2 on a contact aligner with a 350 nm cut-off light filter to transfer the pattern of mask CNM788 HMB-SU8B. Then, a Post Exposure Bake (PEB) was performed to obtain an optimum resolution and good edge quality in two consecutive steps. The first step was at 65°C for 30 min followed by another at 95°C for 5 min. During the PEB stage some air bubbles appeared in between the interface of the SU-8 resin and the SUEX laminated layer (see Fig. 3–31f). Generally, the standard spin coating of SU-8 creates large annular edge beads producing a non-uniform SU-8 thickness profile. Therefore, the lack of surface planarization formed an air gap between the SU-8 resist surface and the SUEX film, which caused the expansion of the upper laminated layer during the PEB step. Furthermore, since no hard bake was done after depositing the SU-8 on wafers 1, 2 and 3 to harden the resist and evaporate solvent residues, these solvents were also released during the following thermal processes.

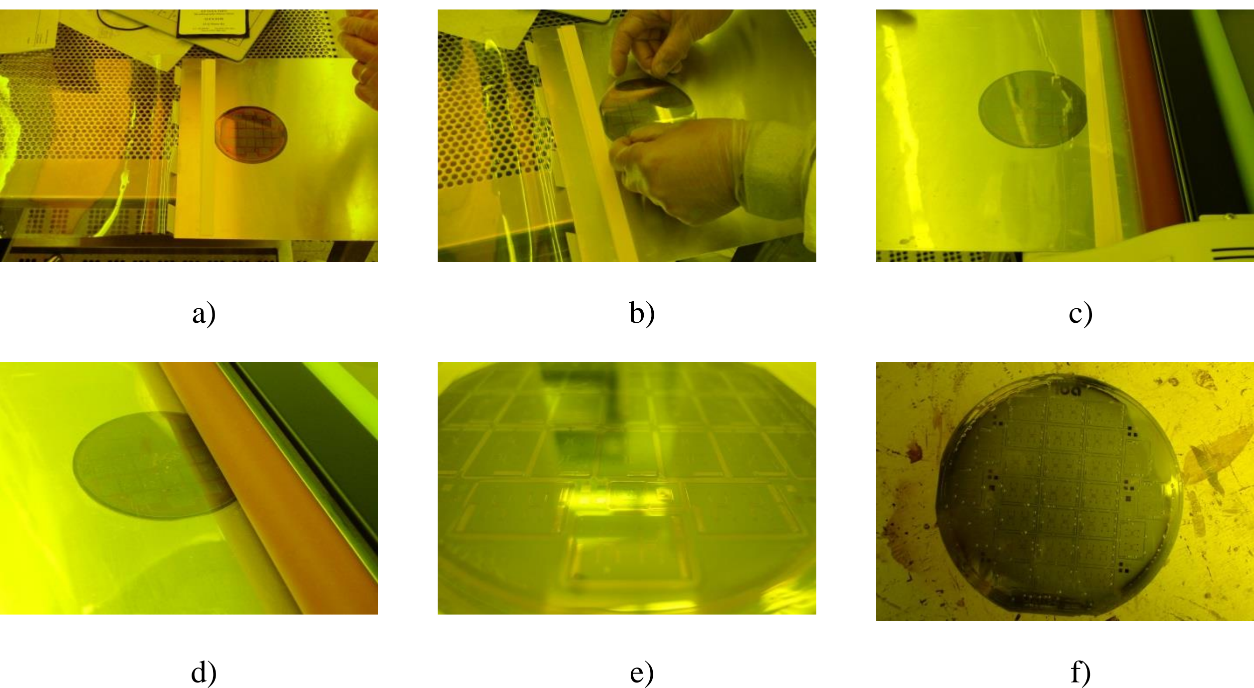


Fig. 3–31. a) Placement of the patterned wafer on the aluminium sheet, b) the SUEX dry film covers the wafer with a protective PET sheet on top, c) another PET coversheet covers the entire wafer to avoid moving parts and also to avoid sticking of resin with the heated rollers during lamination, d) lamination process at a speed of 6 ft/min at 80°C, e) aspect of the wafer after the lamination process and f) bubble formation during the Post-exposure bake.

Next, the resin was developed at room temperature in Propylene Glycol Methyl Ether Acetate (PGMEA) developer agitating gently for 7 min. The process was verified by visual inspection on a microscope until uncovering the finer marks in the wafer with 200 µm in dimension. Development was completed by immersing the wafer in fresh PGMEA for cleaning residues, rinsing with IPA (Isopropyl alcohol) solution for 1 min and drying under nitrogen. After development, the hard bake step was not performed in all wafers to avoid the clogging of the bypass channels given their low aspect ratio (H/W = 125 µm/200 µm). Hence, a hardbake process at 80°C for 13 min was only done on wafer 4 to diffuse both layers by means of a thermal bonding and to enhance their adhesion.

The advantage of using SUEX dry films was the ease of integrating a two-level microfluidic structure. Fig. 3–32 shows the wafer with integrated polymer microfluidics. However, the deposition of the polymeric layers strongly influenced on the manufacturability and quality of the bypass microchannels for two main reasons. Firstly, using SU-8 resist as the first coating layer ensured good step coverage over the microchannels. Secondly, the structures were not directly under any applied pressure that might have caused them to collapse as occurs during a lamination process. This latter technique is not easily applicable to fragile samples, since the control of the applied pressure is not precise. Thus, the first SU-8 layer was used as a protective layer for the lamination process with good results in our fabrication approach.

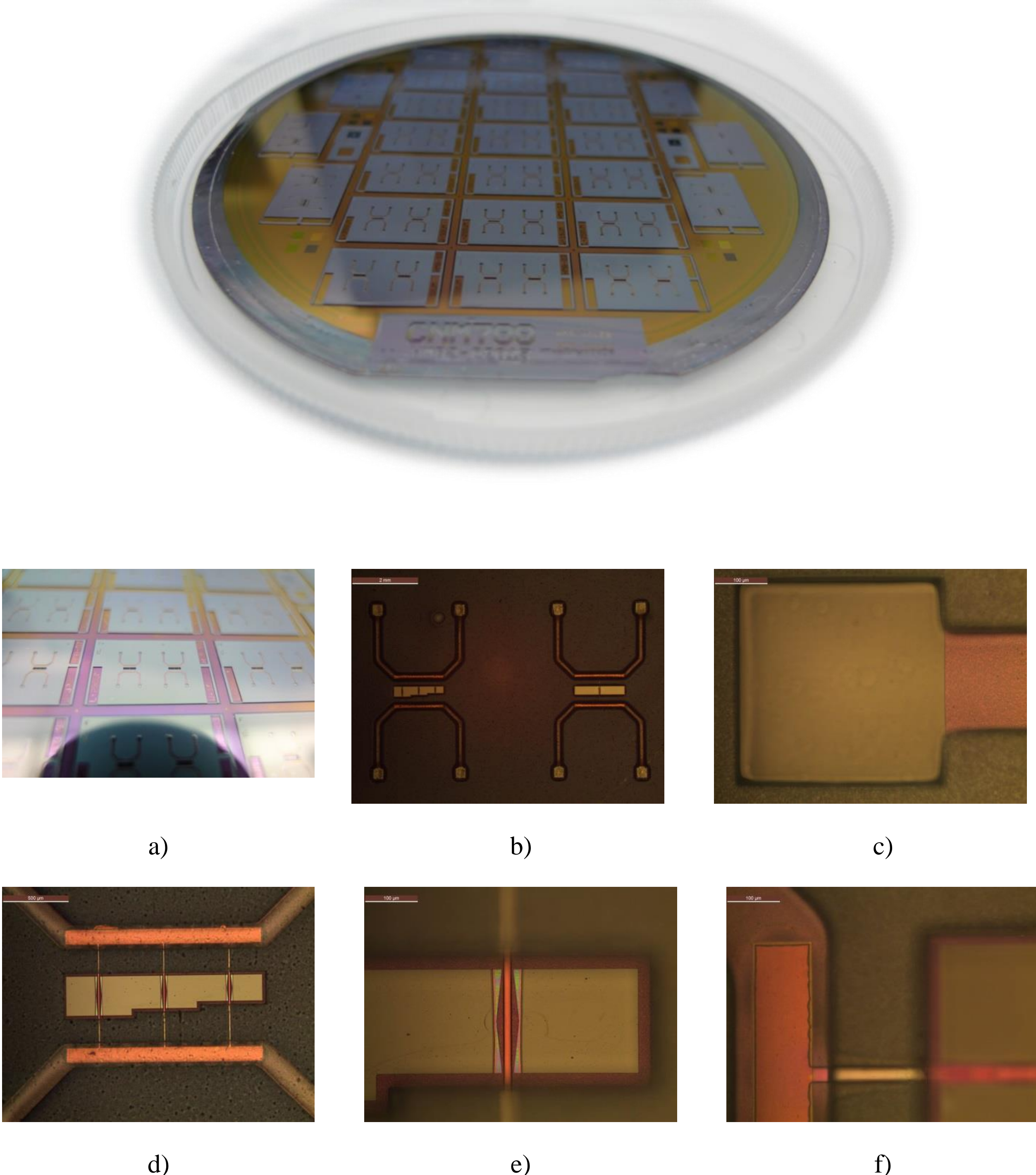
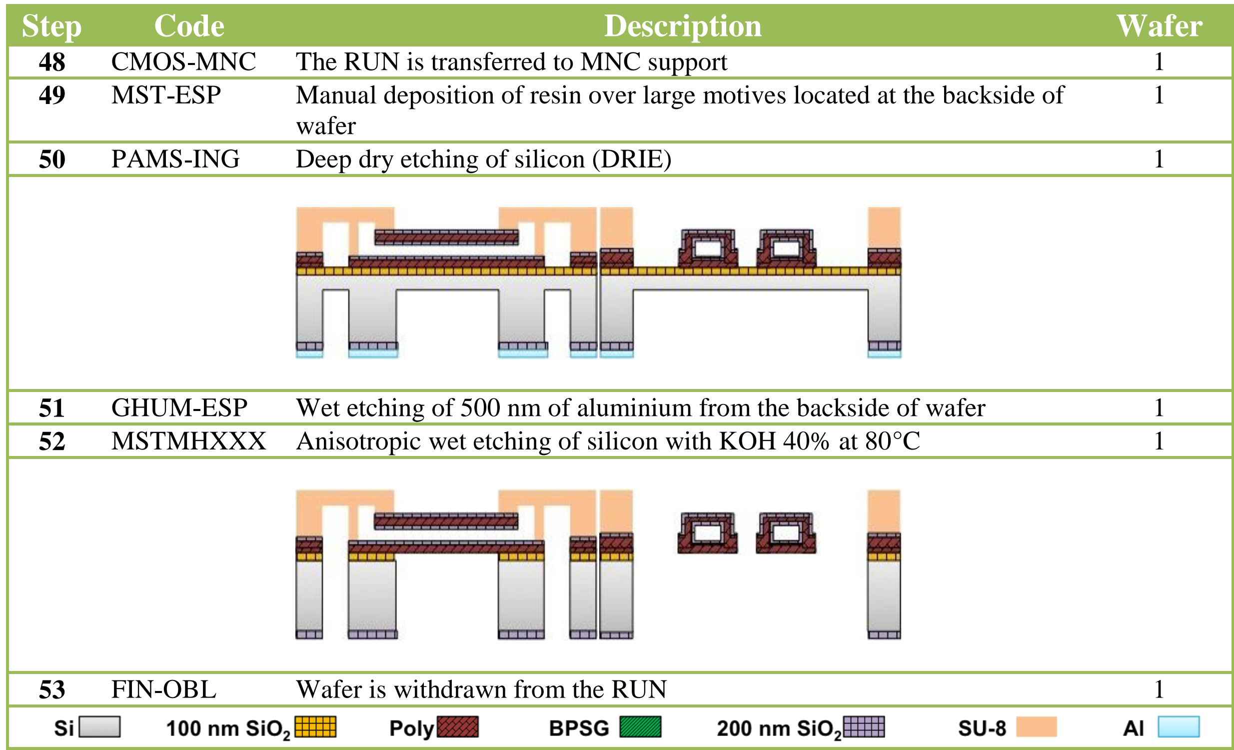


Fig. 3–32. General view of wafer 1 integrated with polymer microfluidic channels: a) aspect of the devices after applying the lamination protocol of SUEX epoxy, b) overview of the polymer H-shape microfluidic channels of two devices on a single chip, c) outlining of microfluidic inlets for fluid injection of samples, d) view of an array of three HMB devices with bypass channels on each entrance, e) SUEX resin is developed on top of the beams to improve laser beam reflectivity during the dynamic characterization of resonators and f) isolation of the fluid bypass channel from the displacement area of the resonators.

3.3.4 Bulk micromachining of devices

The next step consisted of releasing the resonators from the substrate by bulk micromachining. Prior to the DRIE process, it was necessary to manually deposit resin over large motives located at the backside of the wafer such as letters and the identification number of the fabrication process (step 49). This protective resin helped to maintain a uniform deep etching process all over the wafer surface since the etching rate of the silicon material was higher for motives with large dimensions.



Step	Code	Description	Wafer
48	CMOS-MNC	The RUN is transferred to MNC support	1
49	MST-ESP	Manual deposition of resin over large motives located at the backside of wafer	1
50	PAMS-ING	Deep dry etching of silicon (DRIE)	1
51	GHUM-ESP	Wet etching of 500 nm of aluminium from the backside of wafer	1
52	MSTMHXXX	Anisotropic wet etching of silicon with KOH 40% at 80°C	1
53	FIN-OBL	Wafer is withdrawn from the RUN	1

After processing the wafer for 45 min with DRIE (step 50), the majority of structures located in the center of the wafer were released, which means that the underlying silicon oxide had also been etched. However, silicon material still remained over the wafer perimeter. As the helium pressure inside the DRIE chamber could not be maintained in the range of 500 Pa after the aperture of some motives, the process was stopped. Regarding the polymer microfluidics, some bubbles were formed in between the polymer layers; the vacuum pressure inside the chamber must have affected the adhesion of both layers while trying to suck the residual air inside the bypass channels. The manually deposited resin was stripped using acetone and water to avoid any damage to the polymer-based microfluidics on the front side of the wafer. The wafer was then immersed in DAE (Defreckling Aluminium Etchant) solution to wet etch the underlying aluminium (step 51). Rests of aluminium remained on the wafer perimeter outside the location of the chips. Before the anisotropic wet etching of silicon with KOH 40% at 80°C, the wafer was cleaned with HF 5% for 10 s. Then, the wafer was immersed in KOH solution for 10 min (step 52). During the wet etching step, some of the chips were released from the substrate and the SU-8 layer was peeled off from the surface given that the KOH solution etched the underlying 200 nm SiO_2 as can be seen in Fig. 3–33 and Fig. 3–34.

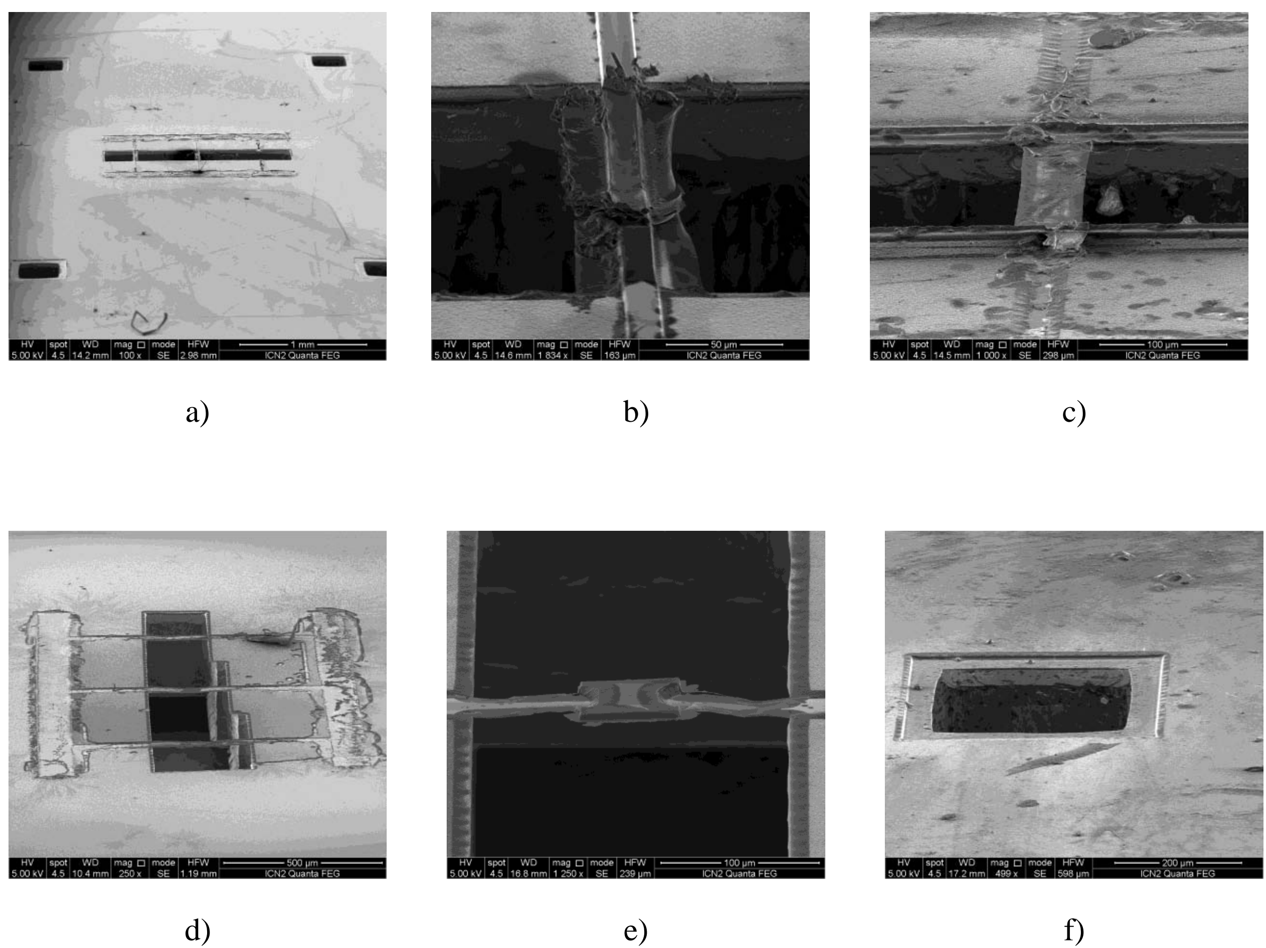
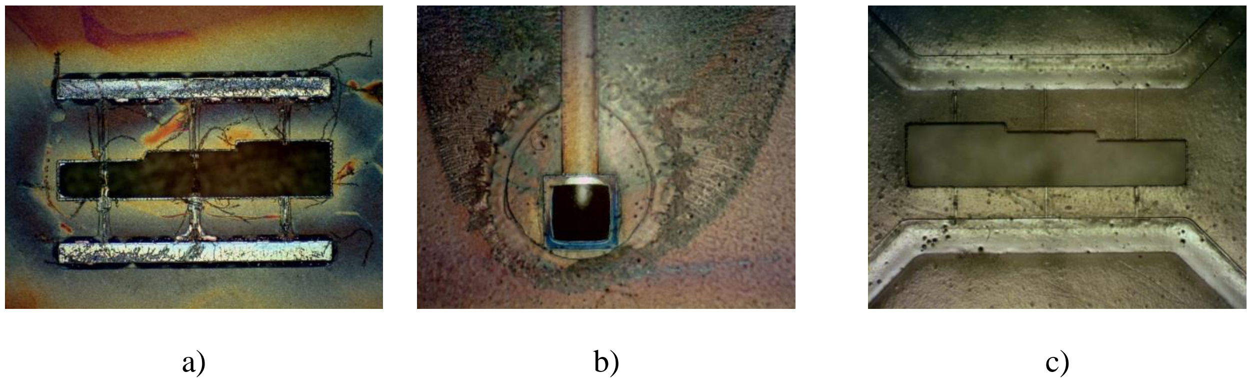


Fig. 3–33. a) Aspect of a single device from wafer 1 after the wet etching step with KOH solution. The polymer bypass channels were stripped from the substrate due to the etching of the underlying silicon dioxide. b) - d) In some resonators the top structural layer was completely removed modifying the morphology of the hollowed resonators. e) Etching of the edges of a paddle resonator demonstrates the low etching selectivity of polycrystalline silicon to KOH solution and f) view of a well-defined through-hole for fluid injection.

Also, the structural layer of the microchannels was substantially damaged; the etching process modified the integrity of the resonators given that the etching rate of polycrystalline silicon to KOH is approximately 0.67 μm/min [15]. Fig. 3–33 shows the state of the microchannels after the wet etching with KOH solution and the stripped polymer layers. During this step, the integrity of the polymer microfluidics was not affected by the KOH solution and it was only detached from the wafer surface, as displayed in Fig. 3–34.



a) b) c)

Fig. 3–34 Microscope images after the wet etching of wafer 1 with KOH solution a) the solution started etching the edges of the central window until revealing the underlying polycrystalline silicon (represented in *light yellow colour*). Darker areas represents silicon dioxide residues; b) around the through-holes for fluid injection, the first coating of SU-8 started to peeling off from the substrate and c) view of the polymer-based microfluidics released from the substrate indicating good adhesion between both polymer layers after etching with KOH and BHF solutions.

Step	Code	Description	Wafer
54	HOLDRESP	Pending decision to continue with wafers 2-4	2-4
55	FOTO-ESP	Photolithography of the backside of the wafer with mask CNM788 HMB-GRID6	4
56	QUAD-ESP	Dry etching of 500 nm of aluminium	4
57	ESPECIAL	Resin stripping on front side of wafer	4
58	ESPECIAL	Annealing of backside resin at 200°C for 30 min	4
59	PGIOXXXX	Dry etching of silicon dioxide from backside of wafer	4
60	DEC-RESI	Resin stripping on both sides of the wafer	4
61	HOLDRESP	Wafer inspection due to particles and residues on the front side	4
62	CMOS-ING	The RUN is transferred to MNC support	4
63	FOTO-ING	Patterning of 25 µm of SU-8 negative resin on the front side of wafer using mask CNM788 HMB-SU8A	4
64	FOTO-ING	Patterning of 100 µm of laminated SUEX film on the front side of wafer using mask CNM788 HMB-SU8B	4
65	MST-ESP	Manual deposition of resin over large motives located at the backside of wafer	4
66	PAMS-ING	Deep dry etching of silicon	4
57	GHUM-ESP	Wet etching of 500 nm of aluminium from the backside of wafer	4
58	MST-ESP	Wet etching of 100 nm of silicon dioxide	
59	FIN-OBL	Wafer is withdrawn from the RUN	4
Si	**100 nm SiO_2**	**Poly** **BPSG** **200 nm SiO_2** **SU-8**	**Al**

From here the process flow continued with wafer 4; steps 39 to 53 were repeated with some modifications in order to maintain the polymer-based microfluidics and to reduce the etching of the resonators while releasing the structures from the substrate. The adhesion of the SU-8 layer and the laminated SUEX layer were improved by doing a hardbake step at 80°C for 13 min after the lamination process. Eventually, the formation of air bubbles started along the edges of the bypass microfluidic channels because of the contained air that pushed away the laminated SUEX. The protuberance of such areas slightly increased during the DRIE process due to the effect of the vacuum, but the deformation of the microfluidic channels was minor than that of wafer 1. The DRIE process etched the majority of the remaining silicon until revealing the underlying silicon dioxide, which had a wrinkled aspect (see Fig. 3–35).

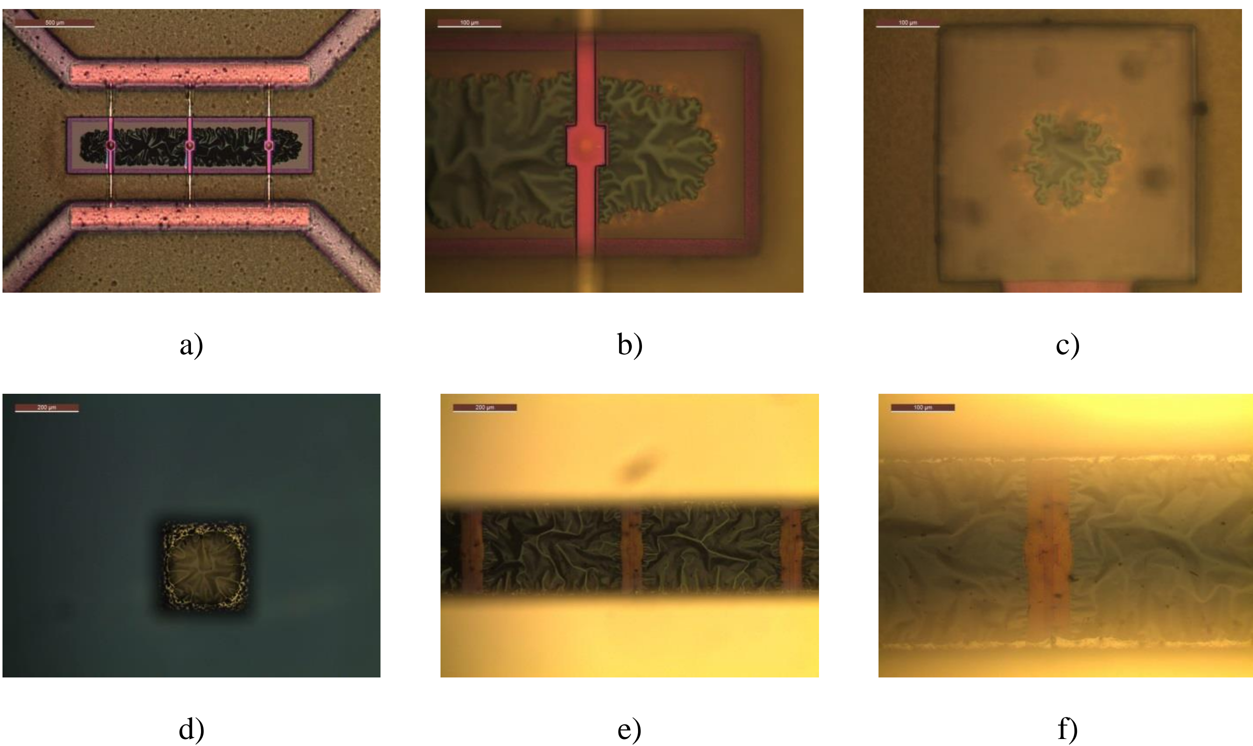


Fig. 3–35. a) - c) Top view of wafer 4 after DRIE of the silicon material. The silicon was etched more easily in marks with larger dimensions. For instance, the underlying silicon dioxide was slightly uncover on the access through-holes of 400 µm x 400 µm. d) - f) Bottom view of wafer 4 after DRIE of silicon. The aspect of the silicon dioxide is wrinkled given its thin thickness. The conditions for the DRIE process were accordingly to the properties of each wafer in order to achieve a more uniform etching.

A holder support was then used to protect the front side of the wafer during the wet etching of aluminium. As a result, some of the chips were released from the substrate given that the DAE solution also etched the silicon dioxide material. Finally, to completely release the resonators from the substrate a wet etching with BHF solution was carried out for 1 min, see Fig. 3–36. In this case, the shape of the structures was preserved and also the polymer microfluidics network was not peel

off from the substrate for devices located in the center of the wafer. Nevertheless, a thin layer of silicon dioxide still remained inside the smaller through-holes for the injection of fluids. These motives of 400 x 400 μm were opened using a thin needle tip to avoid peeling off the polymer layers by over-etching the wafer with BHF solution. Fig. 3–35 shows a visual characterization of structures from wafer 4 with SEM micrographs.

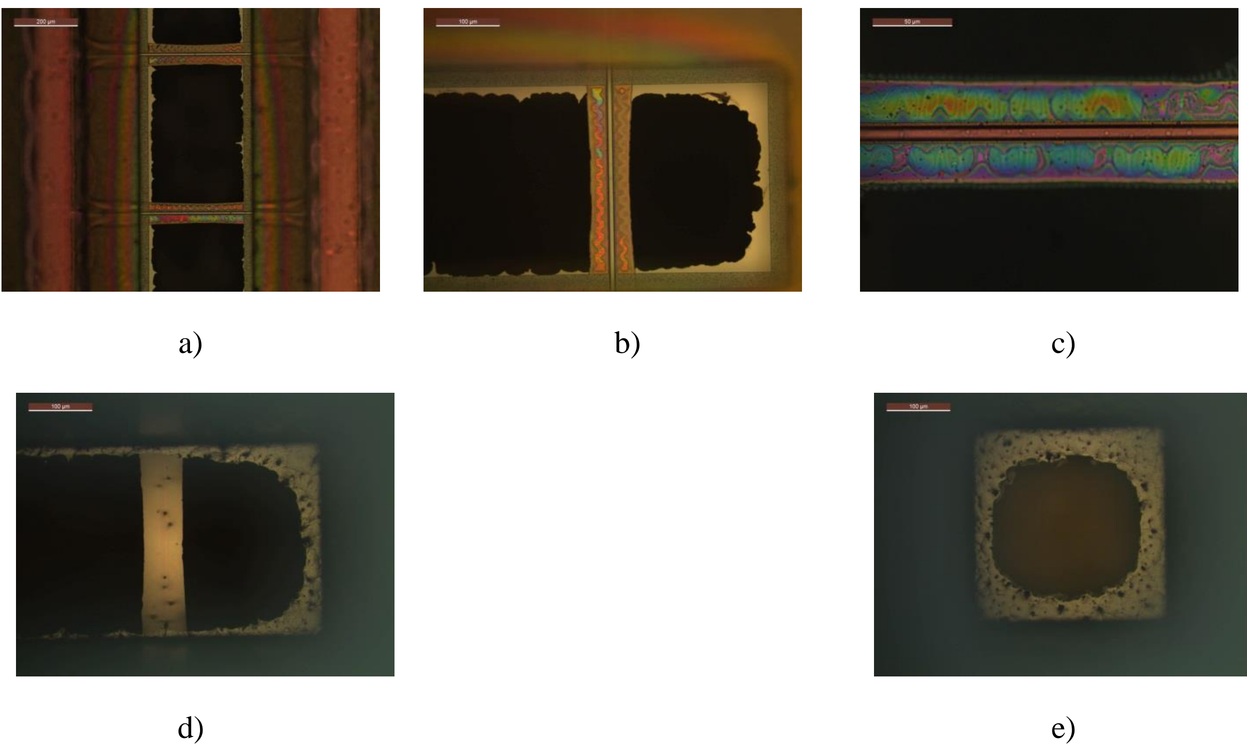
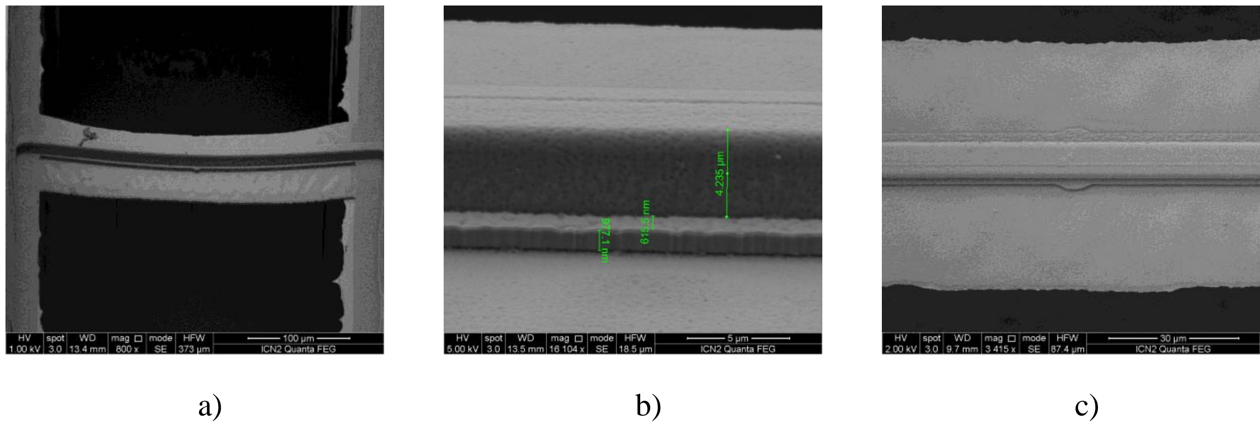


Fig. 3–36. Aspect of a single device after the wet etching step of wafer 4 with BHF solution: a) after 1 min, the solution started to etch the underlying silicon dioxide and thus the first SU-8 coating was partially stripped, b) released beams were not defined properly due to the silicon residues along the edges, c) the BHF solution partially etched the thermally grown silicon dioxide on the microstructures producing a smoother polycrystalline silicon surface, d) and e) visual inspection from the bottom side of the wafer to verify the aperture of the access through-holes and release of the beams.



a) b) c)

Fig. 3–37. Inspection of devices from wafer 4 with SEM micrographs. Some devices showed tensile stress which produced a downward displacement of the resonators. The resonators have a modified morphology because the structural layer along the edges was not completely removed, but the depth of the devices resulted as expected (4 µm).

From here the process flow continued with wafers 2 and 3 by repeating the fabrication steps 39 to 53 with the following modifications. To skip the steps for the manual deposition and stripping of the protective resin over the large motives from the backside of the wafers, these motives were covered during the photolithography process with mask CNM788 HMB-GRID6. Then, during the deposition and lamination of the polymer layers (SU-8 & SUEX), an acetate mask that included in-line microfluidic interconnections was patterned on wafer 3. High resolution of these motives was not substantial because the smallest motive size for this microfluidic design was 50 µm, as shown in Fig. 3–38. For the case of wafer 2, the original microfluidic design using the soda-lime mask was used to pattern the H-shaped bypass microchannels. After the lamination of the SUEX resin layer, the hardbake step of the wafers was unnecessary because it did not prevent at all the formation of air bubbles. After the DRIE process of wafer 2, the remaining silicon layer was approximately 25 µm. Although a holder support was used during the wet etching process of silicon material to protect the front side of the wafer, some of the chips were released from the substrate. Apertures close to the edge of the wafer were etched more rapidly than those in the center due to the etching gradient produced during the DRIE process of silicon (see Fig. 3–39). Hence, the holder support did not longer protect the water front side and the wet etching process had to stop. Finally, the BHF solution was used to dissolve the silicon dioxide revealed in some devices, but the polymer layers were peeled off from the substrate, as Fig. 3–39 shows.

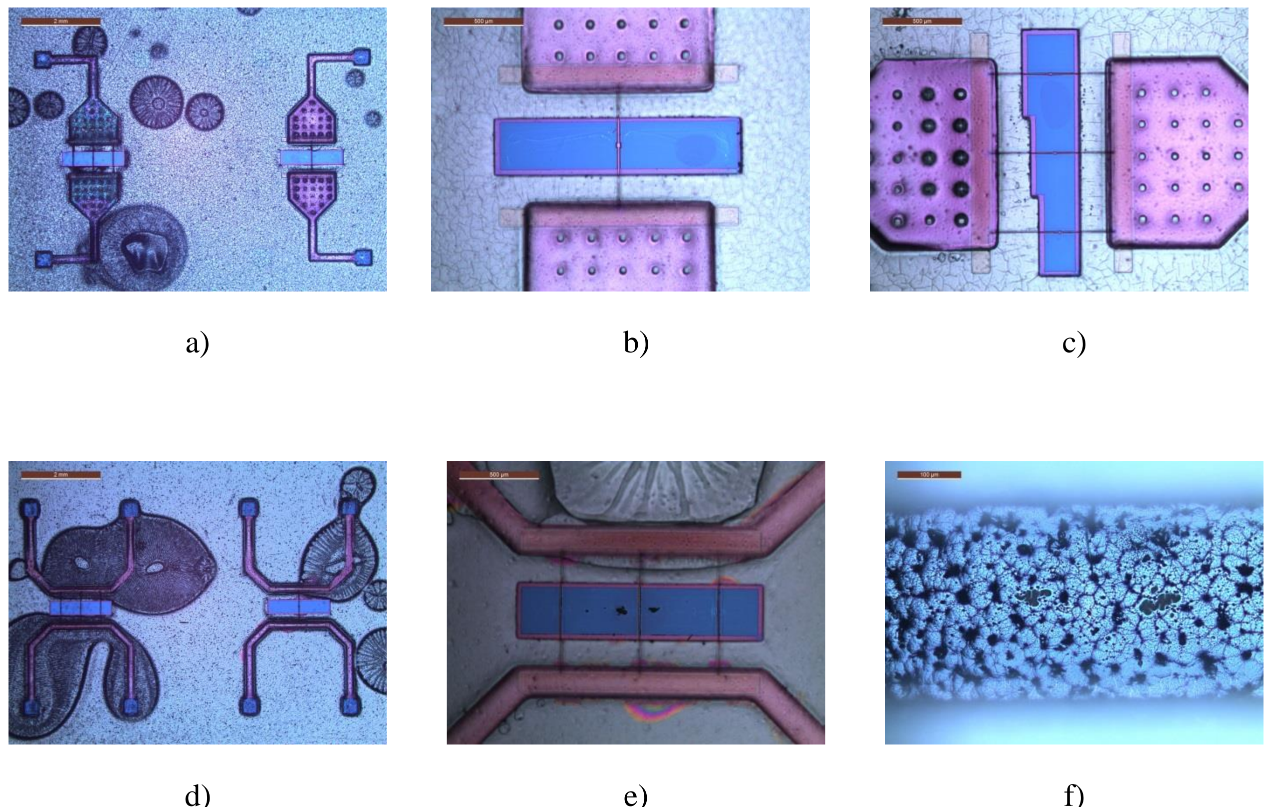


Fig. 3–38. Microscope images of wafers 2 and 3 after DRIE of silicon. a) - c) The adhesion of the polymer layers became poor in specific areas of the devices after exposing the wafer 2 under vacuum. A temperature gradient throughout the wafer caused the clogging of a few pillar supports during thermal processes. d) - e) The polymer-based microfluidics of wafer 3 were also affected by the DRIE; in some areas these layers were peeled off from the substrate. f) The selectivity of the dry etching was higher on devices near the edges of the wafer. A bottom view of the wafer shows the aspect of silicon before the wet etching process with KOH solution.

For the case of wafer 3, a silicon dioxide layer of 400 nm was deposited by PECVD as a protective layer on the front side of the wafer, on top of the polymer layers (see
Fig. 3–40). The purpose was to increase the etching time while removing the remaining silicon material underneath the resonators during the wet etching with KOH solution. In sum, the outcome was the same as the previous wafer. The DRIE etching of the silicon material was more rapid in some apertures located at the edge of the wafer than those in the center. It was therefore impossible to completely remove the silicon material in all the devices without removing the polymer-based microfluidics. Preliminary results while etching a monitor wafer showed that the etching rate for the 400 nm oxide deposited by PECVD was 328.7 Å/min in BHF solution. Therefore, after 30 s of wet etching in BHF, the PECVD oxide layer was completely removed.

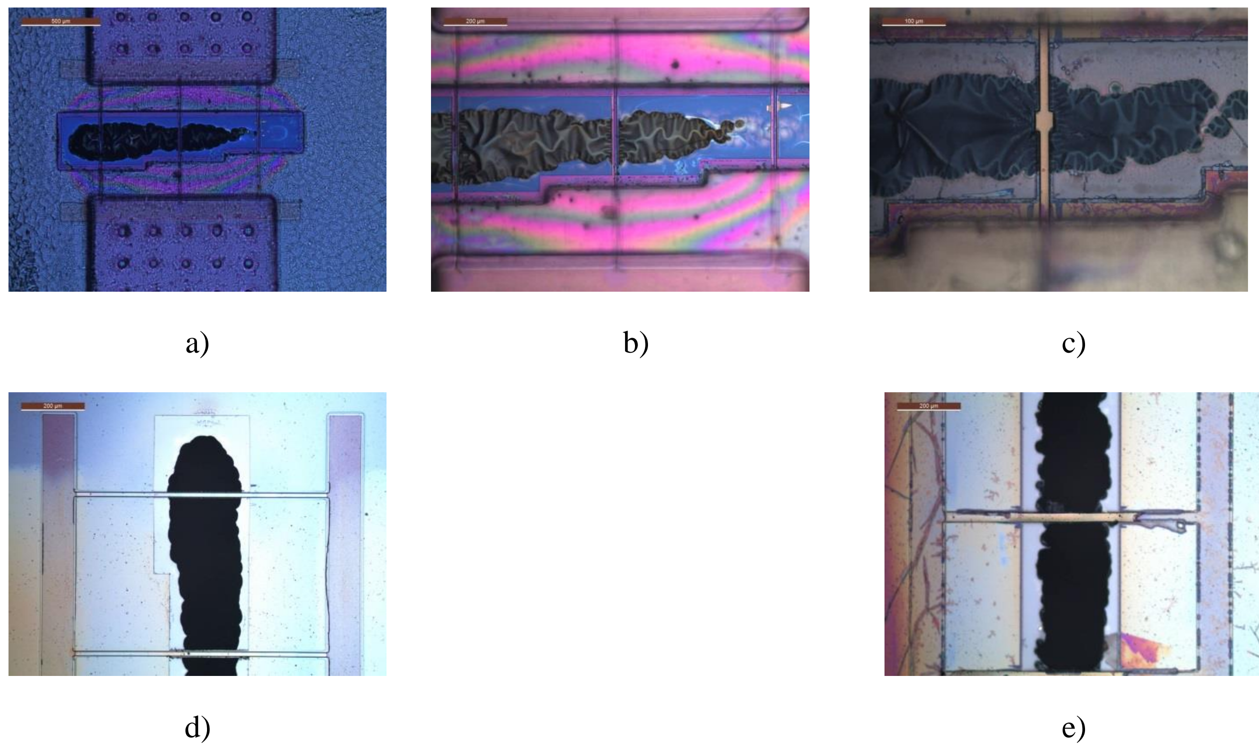
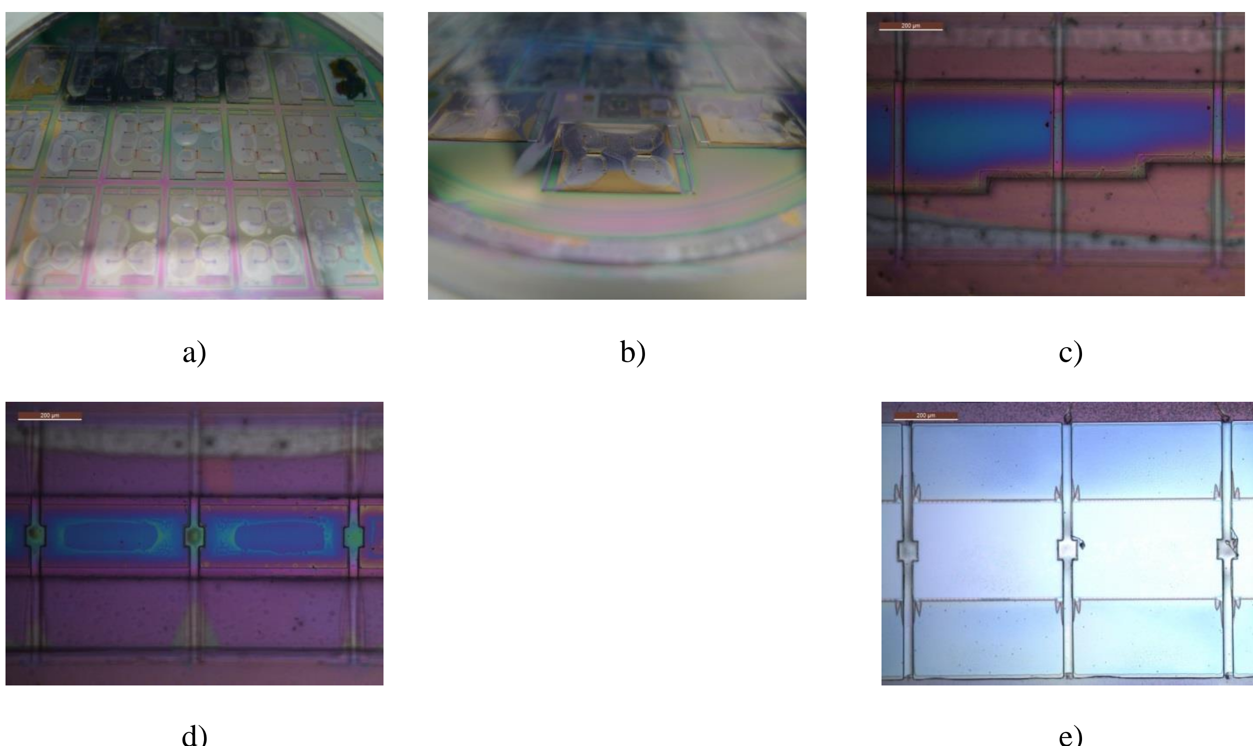


Fig. 3–39. Aspect of wafer 2. a) - c) After the silicon wet etching with KOH solution. The silicon material was not completely removed from beneath the structures because the silicon dioxide layer was also etched during this step in some devices. Therefore only a few devices were released from the substrate. d) - e) Etching of the underlying silicon oxide with BHF solution that stripped the polymer microfluidics from the substrate.

Step	Code	Description	Wafer
60	HOLDRESP	Pending decision to continue with wafers 2-3	2 & 3
61	FOTO-ESP	Photolithography of the backside of wafer with mask CNM788 HMB-GRID6	2 & 3
62	QUAD-ESP	Dry etching of 500 nm of aluminium	2 & 3
63	ESPECIAL	Resin stripping on front side of wafer	2 & 3
64	ESPECIAL	Annealing of backside resin at 200°C for 30 min	2 & 3
65	PGIOXXXX	Dry etching of silicon dioxide from backside of wafer	2 & 3
66	DEC-RESI	Resin stripping on both sides of the wafer	2 & 3
67	ASEM-ING	SEM inspection of wafers	2 & 3
68	CMOS-ING	The RUN is transferred to MNC support	2 & 3
69	FOTO-ING	Patterning of 25 µm of SU-8 resin on the front side of wafer using mask CNM788 HMB-SU8A	2 & 3
70	FOTO-ING	Patterning of 100 µm of laminated SU-8 resin (SUEX) on the front side of wafer using mask CNM788 HMB-SU8B	2 & 3
71	PAMS-ING	Deep dry etching of silicon	2 & 3
72	GHUM-ESP	Wet etching of 500 nm of aluminium from the backside of wafer.	2 & 3
73	MSTMHXXX	Wet etching of silicon with KOH 40% @ 80°C	2
74	DOXF-ING	PECVD deposition of 400 nm of SiO_2 at 120°C	3
75	MST-ESP	Wet etching of silicon with KOH 40% solution @ 80°C using the holder support	3
76	FIN-OBL	Wafer is withdrawn from the RUN process	2 & 3



a) b) c)

d) e)

Fig. 3–40. a) - b) Photos that show the 400 nm of silicon dioxide deposited by PEVCD on wafer 3. The SUEX epoxy was severely damaged to the point that it could easily be removed from the substrate. c) - d) Aspect of the microchannels after the 400 nm coating of silicon dioxide. The colouration indicates the varying thickness of the oxide. e) The resonators were not released from the substrate after the silicon wet etching, instead the polymer layer was removed and the structural layer was partially etched.

3.3.5 General overview and evaluation of the fabrication process

After finishing the fabrication process flow only nine devices from wafer 4 were obtained. The major challenge in this approach was to preserve the integrated polymer microfluidics during the release of the resonators. The main highlights and drawbacks of this manufacturing approach are discussing in the following:

- Adhesion of both polycrystalline silicon layers was notably affected while etching the sacrificial layer with HF 49% acid. The etchant solution diffuse into the interface of both layers causing the top layer to be slightly detached from the substrate. This created small rounded projections along the edges of the microfluidic inlets for the case of higher etching times (67 min).

- Polycrystalline silicon has a high reflectance ratio (0.35 at 633 nm), which makes this material non-transparent within the visual spectrum of light. Therefore, to verify the wet etching of the embedded sacrificial layer, we use test marks located throughout the wafer. However, it was necessary to scratch the middle part of some microbeams using fine tweezers until uncovering the inner cavities for ensuring the complete removal of the sacrificial layer. In addition, we noticed that the etching time was strongly influenced by the doping of the BPSG material, the etchant solution aging and the cross-sectional dimensions of the microchannels.

- The wafers were oxidized to improve the hydrophilic properties of the inner channel walls, similar to the oxidation process of devices from the second generation of HMB devices, using polycrystalline silicon as base material. The oxidation was carried out at a lower temperature (at 950°C) in order to decrease the deformation rate of the structures. The resulted oxide layer was about 270 nm thick, which corresponded to a red-violet colour according to the colour oxidation chart. However, the thermal process expanded the size of the projections along the microfluidic inlets yielding a higher stress over the structural layers.

- During the definition of the effective length of the resonators two important aspects decrease the dry etching selectivity along the walls of the microchannels. First, the lack of surface planarization over these areas modified their etching conditions with respect to rest of the wafer. Second, after the first dry etching of the top silicon dioxide, traces of this material remained along the edges of the microchannels. This further caused that the polycrystalline silicon was not completely removed to correctly define the resonators. By changing the recipe to perform a DRIE process the selectivity of the polycrystalline silicon increased but the already uncovered underlying silicon dioxide layer became thinner for the following bulk micromachining steps. Performing an over-etching of the silicon oxide layer (with a DRIE recipe) until completely revealing the polycrystalline silicon could substantially reduce this effect.

- A good strategy to release the beams from the substrate consisted of a sequential processing of the wafers because the DRIE conditions were not the same for all the wafers. The release of the structures was challenging given the close selectivity of both structural (polycrystalline silicon) and seeding material (silicon dioxide). Furthermore, the selectivity of the DRIE process was non-uniform throughout the surface of the wafers: it strongly depended on the size of the motives, and consequently not all the devices were released. For instance, devices located near the edges of the wafer were etched faster than that located in the center. To overcome this issue in future designs, it can be useful to deposit a thicker oxide layer beneath the beams or a seeding material, such as silicon nitride, with higher selectivity against the DRIE conditions. For example, in some manufacturing process, silicon nitride has been used as masking layer for wet etching of silicon with KOH etchant solution [6]. However, in our approach silicon nitride introduced high stress over the wafers as we already studied on the process flow of the first generation of HMB devices.

- Since the aperture and emptying of the microchannels was done during the first fabrication steps of the RUN, it was necessary to preserve the integrity of the structures for the consecutive surface and bulk micromachining. Therefore, a 6 μm resin was deposited by spin coating over the front side of wafers in different stages of the fabrication process. This action, however, was not quite effective; it introduced two main drawbacks. The long-term adhesion of the resin to the patterned structures made difficult to completely remove it from the substrate, and therefore the wafers had to be over-exposed under plasma treatment. As a result some microchannels broke, cracked and collapsed. On the other hand, some microchannels were partially filled with the protective resin by capillary forces. Thus, it was necessary to do an adequate cleaning of the wafers to avoid the clogging of the cavities. However, in spite of applying this cleaning protocol some devices still had resin traces inside the microchannels.

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