COMPACT MODELING OF THE RF AND NOISE BEHAVIOR OF MULTIPLE-GATE MOSFETS

Bogdan-Mihai Nae

Dipòsit Legal: T-1456-2011

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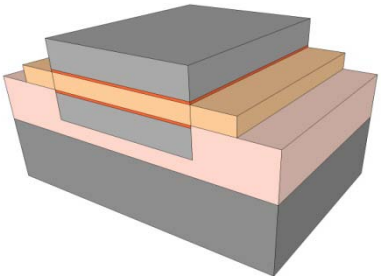
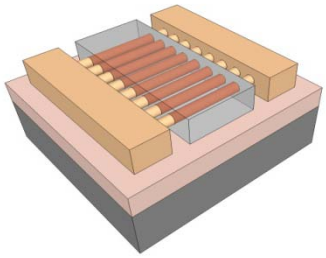
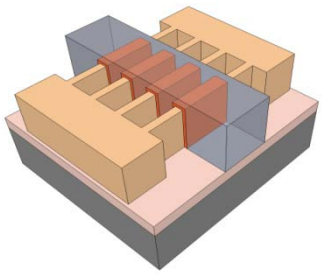

NAE, BOGDAN MIHAI

Doctoral Thesis

2011

Department of Electronic, Electric and Automatic Engineering

Universitat Rovira i Virgili

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DOCTORAL THESIS

Supervised by Dr. Antonio Ramon Lázaro Guillen

Department of Electronic, Electric and Automatic Engineering

UNIVERSITAT ROVIRA I VIRGILI

Tarragona

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I STATE that the present study, entitled “Compact Modeling of the RF and Noise Behavior of Multiple-Gate MOSFETs”, presented by Bogdan Nae for the award of the degree of doctor, has been carried out under my supervision at the Department of Electronic, Electric and Automatic Engineering of this university, and that it fulfills all the requirements to be eligible for the European Doctorate Award.

Tarragona, 9 February 2011

Doctoral Thesis Supervisor

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And to mom and dad…wish you were here to see all this.

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Compact Modeling of the RF and Noise Behavior of Multiple-Gate MOSFETs

In the last decade, the downscaling of the complementary metal-oxide-semiconductor (CMOS) has been the main technological process in the industry. However, we have reached a point where further scaling faces a significant challenge. The main issue arises from the high-channel doping required to control short-channel effects (SCE), which significantly degrades carrier mobility and reduces the drain current. It also increases bond-to-bond tunneling across the junctions, leading to an increase of the parasitic leakage current. In addition, the statistical fluctuation of channel dopants causes variations in the threshold voltage. As a consequence, the implementation of the new structures such as ultra-thin body (UTB) fully depleted (FD) silicon-on-insulator (SOI) and multiple-gate MOSFETs (MUGFETs), which require lower doping levels, appears to be the only viable alternative in silicon-based technologies to replace planar bulk CMOS devices. However, the tremendous challenges faced by the implementation of FD SOI devices (such as a precise control of the silicon film thickness, the reduction of source and drain resistances to tolerable values, etc.) has driven some major integrated circuits (IC) manufacturers - such as Intel or IBM - to directly target the fabrication and production of multiple gate transistors.

The introduction of multiple-gate structures has various advantages. As pointed in the last section, among these advantages is the improved electrostatic control of the charges in the channel, an increase in current gain and a reduction in

the junction capacitances. The existence of the second gate in the buried oxide increases the control in the channel because it reduces the influence of the penetrating lateral electric field which competes for the available depletion charges. This extra second gate or multiple-gate also increases the number of conducting surfaces which in turn increases the total current flow.

With the increase in device complexity come new challenges in modeling these devices. As the channel gets smaller and smaller, new effects appear, which put a strain on the current numerical simulators. In nowadays market, no one can afford to spend huge resources for simulation hardware, or hundreds of hours on numerical software simulations. Here is where the compact modeling of semiconductor devices comes in. It´s main advantage is that it drastically reduces the computation times, while being based on the physical characteristics of the devices, which ensures a remarkable compatibility with numerical simulators. At the same time, these models are perfect for use in circuit simulators, which allows circuit designers endless possibilities for new device architectures.

This research work has been conceived to cover precisely these aspects. The models described here are physical models, with very few adjusting parameters, that are usually replaceable with values extracted from experimental measurements; they are compact models, making use of approximate expressions that have been tweaked to offer a very good fit with numerical simulations and offering in exchange the advantage of computation speed, decreasing the simulation time and thus the productivity. Another major advantage is the fact that these models can be easily incorporated into circuit simulators, which allows designers to unleash the full capabilities of the design software to create new devices and applications.

The most promising SOI devices for the nanoscale range are based on multiple gate structures like the Double-Gate (DG), triple gate or FinFET and Surrounding-Gate (SGT) or Gate-All-Around (GAA). These advanced structures can be scaled more aggressively than the bulk-Si structures, hence, may be adapted for integrated circuit production. Also, these structures are regarded as a near ideal technology, offering a higher drive current than its SG SOI counterpart due to larger control over channel region, and this strongly enhances the immunity towards the short channel effects. With the evolution of MOSFET scaling to shorter gate lengths, the high-frequency capabilities of the transistor have reached the GHz regime so that RF circuit applications have been steadily growing.

In this thesis, the performances of different Multiple-Gate MOSFET (DG, SGT and triple-gate) structures has been evaluated, for the RF mode of operation, and the noise performances of these devices has been studied. The modeling scheme is similar for all these devices and is adapted to each geometry.

The basis for all these models is the fully analytical compact model of the DG transistor described in chapter 2. This model is an extended version of a previously developed compact dc and charge model for doped DG-MOSFET from a unified charge control model derived from Poisson´s equation. A quantum case has been added, using a simple relationship between the inversion centroid and the inversion charge obtained fitting numerical simulation results. Using this compact charge control model, DC drain current models are derived assuming drift-diffusion and hydrodynamic transport mechanisms.

We have proved that the electron heating has an important effect on the performances of the device, especially with scaling, thus the use of a transport model that takes into account this effect (the hydrodynamic transport model) is fully justified.

Several short channel effects have been incorporated into the model, such as the effect of hot carriers, channel length modulation, saturation effect, as well as the shot noise introduced by the tunneling gate current due to the very gate thin oxide (2nm).

The RF and noise performances of DG-MOSFETs have been analyzed using the active transmission line approach from the compact charge control and drain current model. The results we have obtained show important differences in drain current, f_t and f_{max} and noise performances between drift-diffusion and hydrodynamic transport models for short gate lengths. These differences comes from the effect of the velocity overshoot increasing the transconductance, and hence, f_t and f_{max}. The intrinsic noise figure depends on the temperature model used in the simulation. For short-channel devices operated in the saturation region, noise exhibits a strong dependence on the drain bias because the velocity saturation region, where the noise temperature is high, occupies a large portion of the channel. Hydrodynamic models predict higher noise temperatures in this region. In these devices, for typical RF operating bias points, the effect of the shot noise introduced by the gate current is small…however, with further downscaling, this effect will have a bigger importance in the final noise figure.

The same approach has been applied to the SGT structure. In the SGT case, the charge control model comes from 2D device simulations where quantum effects corresponding to the intrinsic transistor parameters are taken into account. The channel current model includes the velocity overshoot and hot carrier effects in the noise temperature. RF and noise are analyzed using the active transmission line method. Furthermore, as an application of the model we have described the RF and noise performance of SGT devices with the gate length being downscaled.

For these two devices (DG and SGT), we have also developed a compact noise model (instead of the channel segmentation method). It includes the channel noise, the induced-gate noise and the cross-correlation noise between drain and gate noises. The expressions are analytical and they depend on the mobile charge at the source and drain ends of the channel. The values of the excess noise factors and correlation coefficients follow the values previously obtained in the DG MOSFET model. Moreover, the compact noise model described does not use adjusting parameters, thus making it ideal for being used in circuit simulators with SGT MOSFETs.

This compact noise model reproduces the measured noise bias behavior for any gate length found for SG MOSFETs in the literature, without the need for additional parameters. Therefore, it is a very promising model for being used in circuit simulators with SG, DG or SGT devices.

As for triple-gate (or FinFET) devices, we have proposed a compact RF model, based on the charge control model obtained for the SGT case, but modified for this specific architecture. The channel current model includes the velocity overshoot and the hot carrier effects in the noise model. The analysis of the RF and noise behavior has been done using the active transmission line method, and the noise performances have been studied with the downscaling of the gate length, to predict the device behavior at future technological nodes.

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Scientific Publications

Published Journals

1. A. Lazaro, B. Nae, O. Moldovan, B. Iniguez, “A compact quantum model of nanoscale double-gate metal-oxide-semiconductor field-effect transistor for high frequency and noise simulations”, Journal of Applied Physics, **100**, 084320 (2006)
2. A. Lazaro, B. Nae, B. Iniguez, F. Garcia, I.M. Tienda-Luna, A. Godoy, “A compact quantum model for fin-shaped field effect transistors valid from dc to high frequency and noise simulations”, Journal of Applied Physics, **103**, 084507 (2008)
3. A. Lazaro, A. Cerdeira, B. Nae, M. Estrada, B. Iniguez, “High-frequency compact analytical noise model for double-gate metal-oxide-semiconductor field-effect transistor”, Journal of Applied Physics, **105**, 034510 (2009)
4. B. Nae, A. Lazaro, B. Iniguez, “High frequency and noise model of gate-all-around metal-oxide-semiconductor field-effect transistors”, Journal of Applied Physics, **105**, 074505 (2009)
5. A. Lazaro, B. Nae, C. Muthupandian, B. Iniguez, “High-frequency compact analytical noise model of gate-all-around MOSFETs”, Semiconductor Science and Technology, **25**, 035015 (2010)

Conference Contributions

1. A. Lazaro, B. Nae, O. Moldovan, B. Iniguez, “A compact quantum model of nanoscale double-gate MOSFET for RF and noise simulations”, Workshop on Electronic Engineering, Jun. 26-27, 2006, Tarragona (Spain)
2. A. Lazaro, B. Nae, B. Iniguez, “Analytical RF and high frequency noise model for undoped multiple-gate SOI MOSFETs”, XXI Conference on Design of Circuits and Integrated Systems (DCIS), Nov. 22-24, 2006, Barcelona (Spain)
3. A. Lazaro, B. Nae, B. Iniguez, “A compact quantum model of nanoscale double-gate MOSFET for RF and noise simulations”, XXI Conference on Design of Circuits and Integrated Systems (DCIS), Nov. 22-24, 2006, Barcelona (Spain)
4. A. Lazaro, B. Nae, O. Moldovan, B. Iniguez, “A CAD model of nanoscale double-gate MOSFET for RF and noise applications including quantum and nonstationary effects”, 6th Conference on Electron Devices (CDE), Jan. 31 – Feb. 2, 2007, El Escorial (Spain)
5. A. Lazaro, B. Nae, O. Moldovan, B. Iniguez, “A compact quantum model of nanoscale double-gate MOSFET for RF and noise simulations”, 6th Conference on Electron Devices (CDE), Jan. 31 – Feb. 2, 2007, El Escorial (Spain)
6. B. Iniguez, A. Lazaro, H.A. Hamid, O. Moldovan, B. Nae, J. Roig, D. Jimenez, “Charge-based compact modelling of multiple-gate MOSFETs”, Custom Integrated Circuits Conference (CICC), Sep. 16-19, 2007, San Jose, CA (USA)

7. B. Nae, A. Lazaro, B. Iniguez, “A FinFET compact model for high frequency and noise analysis”, XII International Conference on Simulations of Semiconductor Processes and Devices (SISPAD), Sep. 25-27, 2007, Viena (Austria)
8. A. Lazaro, B. Nae, B. Iniguez, “A FinFET compact model for high frequency and noise analysis”, XXII Conference on Design of Circuits and Integrated Systems (DCIS), Nov. 21-23, 2007, Sevilla (Spain)
9. B. Iniguez, A. Lazaro, O. Moldovan, B. Nae, A. Cerdeira, “Advanced compact modelling techniques of nanoscale multi-gate MOSFETs”, Lester Eastman Conference on High Performance Devices, Aug. 5-7, 2008, Delaware (USA)
10. B. Iniguez, A. Lazaro, O. Moldovan, B. Nae, H.A. Hamid, “Compact small-signal modelling of multiple-gate MOSFETs up to RF operation”, MOS Modeling and Parameter Extraction Working Group (MOS-AK), Sep. 19, 2008, Edinburgh (UK)
11. A. Lazaro, A. Cerdeira, M. Estrada, B. Nae, B. Iniguez, “Estudio de linealidad para transistores DG MOSFET”, XXIII Symposium Nacional URSI, Sep. 22-24, 2008, Madrid (Spain)
12. B. Nae, A. Lazaro, B. Iniguez, F. Garcia, I.M. Tienda-Luna, A. Godoy, “DC, RF and noise compact model for FinFETs including quantum effects”, XXII Conference on Design of Circuits and Integrated Systems (DCIS), Nov. 12-14, 2008, Grenoble (France)
13. B. Nae, A. Lazaro, B. Iniguez, “High frequency and noise compact model of gate-all-around MOSFETs including quantum effects”, 5th Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits (EUROSOI), Jan. 19-21, 2009, Goteborg (Sweden)

14. B. Nae, A. Lazaro, B. Iniguez, “High frequency and noise model of gate-all-around MOSFETs”, 7th Conference on Electron Devices (CDE), Feb. 11-13, 2009, Santiago de Compostela (Spain)
15. A. Lazaro, A. Cerdeira, M. Estrada, B. Nae, B. Iniguez, “Linearity study of DG MOSFETs”, 7th Conference on Electron Devices (CDE), Feb. 11-13, 2009, Santiago de Compostela (Spain)
16. B. Iniguez, F. Lime, A. Lazaro, O. Moldovan, B. Nae, “Charge-based compact modelling techniques for nanoscale multi-gate MOSFETs”, Workshop on Compact Modelling, Nanotech Conference and Expo, May 3-7, 2009, Houston, TX (USA)
17. A. Lazaro, A. Cerdeira, B. Nae, M. Estrada, B. Iniguez, “A high frequency compact noise model for double-gate MOSFET devices”, 20th International Conference on Noise and Fluctuations, Jun. 14-19, 2009, Pisa (Italy)
18. R. Ritzenthaler, F. Lime, B. Nae, O. Faynot, S. Cristoloveanu, B. Iniguez, “A Short-Channel Analytical Model for Triple-Gate and Planar FDSOI Transistors”, 7th Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits (EUROSOI), Jan. 17-19, 2011, Granada (Spain)
19. B. Nae, A. Lazaro, R. Ritzenthaler, B. Iniguez, “The Effect of Carrier Heating on the Noise Spectral Densities for Double-Gate MOSFET Devices”, 8th Spanish Conference on Electron Devices (CDE), Feb. 8-11, 2011, Palma de Mallorca (Spain)

Table of Contents

Table of Figures

Chapter 3 – Compact Modeling of Double-Gate Transistors

Chapter 4 – Compact Modeling of Surrounding Gate Transistors

Annex I – Numerical Noise Modeling

Annex II – Analytical Noise Modeling

Annex III – The Lambert W Function

List of Abbreviations

ALD	Atomic layer deposition
CAD	Computer aided design
CLM	Channel length modulation
CMOS	Complementary metal-oxide semiconductor
CPW	Coplanar waveguide
DC	Direct current
DELTA	Depleted Lean channel TrAnsistor
DG	Double-gate
DIBL	Drain induced barrier lowering
FD	Fully depleted
FET	Field-Effect transistor
FinFET	Fin-shaped field-effect transistor
GAA	Gate-all-around
GCA	Gradual-channel-approximation
GF	Gain figure
HEMT	High electron mobility transistor
HF	High frecuency

HR	High resistivity
IC	Integrated circuit
IL	Interfacial layer
ITRS	International Technology Roadmap for Semiconductors
LF	Low frequency
MAG	Maximum available gain
MESFET	Metal semiconductor field effect transistor
MOSFET	Metal-oxide semiconductor field-effect transistor
MUGFET	Multiple gate field-effect transistor
NF	Noise figure
nMOS	n-channel metal-oxide-semiconductor
PD	Partially depleted
pMOS	p-channel metal-oxide-semiconductor
R&D	Research & development
RF	Radio frequency
SCE	Short-channel effects
SDDG	Symmetric doped double-gate
SG	Single-gate
SGOI	Silicon-germanium-on-insulator
SGT	Surrounding-gate transistor
SOI	Silicon-on-insulator

sSOI	Strained silicon-on-insulator
TGC	Tunneling gate current
ULG	Unilateral gain
ULSI	Ultra-large-scale-integration
UTB	Ultra-thin body (transistor)
VLSI	Very-large-scale-integration
WKB	Wentzel–Kramers–Brillouin theory

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Chapter 1

Introduction

1.1 A Timeline of Semiconductor Devices

Brilliant inventors from of the 20th century have built on each other´s work to launch a revolution in electronics. We must pay tribute to the predecessors of Bardeen, Brattain and Shockley - the inventors of the transistor –, discoverers of electrons, the vacuum tube, purified crystals and diodes. The transistor opened the road for experimentation with new materials such as silicon and with a host of manufacturing techniques, leading to electronic devices that have altered every aspect of everyday life [ElecTime-2009].

In 1904, Sir John Ambrose Fleming, a professor of electrical engineering, invents the thermionic valve, or diode, a two-electrode rectifier (a rectifier prevents

the flow of current from reversing). Building on the work of Thomas Edison, Fleming devises an “oscillation valve” – a filament and a small plate in a vacuum bulb. He discovers that an electric current passing through the vacuum is always unidirectional.

In 1907, Lee De Forest, an American inventor, files for a patent on a triode, a three-electrode device he calls an Audion. He improves on Fleming’s diode by inserting a gridlike wire between the two elements in the vacuum tube, creating a sensitive receiver and amplifier of radio wave signals. The triode is used to improve sound in long-distance phone service, radios, televisions, sound on film, and eventually in modern applications such as computers and satellite transmitters.

In 1940, Russell Ohl, a researcher at Bell Labs, discovers that small amounts of impurities in semiconductor crystals create photoelectric and other potentially useful properties. When he shines a light on a silicon crystal with a crack running through it, a voltmeter attached to the crystal registers a half-volt jump. The crack, it turns out, is a natural P-N junction, with impurities on one side that create an excess of negative electrons (N) and impurities on the other side that create a deficit (P). The discovery heralds the coming of transistors.

In 1947, John Bardeen, Walter H. Brattain, and William B. Shockley of Bell Labs discover the transistor. Brattain and Bardeen build the first point contact transistor, made of two gold foil contacts sitting on a germanium crystal. When electric current is applied to one contact, the germanium boosts the strength of the current flowing through the other contact. Shockley improves on the idea by building the junction transistor - "sandwiches" of N- and P-type germanium. A weak voltage applied to the middle layer modifies a current traveling across the entire "sandwich."

In 1954, Gordon Teal, a physical chemist formerly with Bell Labs, shows colleagues at Texas Instruments that transistors can be made from pure silicon - demonstrating the first truly consistent mass-produced transistor. By the late 1950s silicon begins to replace germanium as the semiconductor material out of which almost all modern transistors are made.

In 1958-1959, Jack Kilby, an electrical engineer at Texas Instruments and Robert Noyce of Fairchild Semiconductor independently invent the integrated circuit. In September 1958, Kilby builds an integrated circuit that includes multiple components connected with gold wires on a tiny silicon chip, creating a "solid circuit". In January 1959, Noyce develops his integrated circuit using the process of planar technology, developed by a colleague, Jean Hoerni. Instead of connecting individual circuits with gold wires, Noyce uses vapor-deposited metal connections, a method that allows for miniaturization and mass production.

We arrive at 1962, when the metal oxide semiconductor field effect transistor (MOSFET) is invented by engineers Steven Hofstein and Frederic Heiman at RCA's research laboratory in Princeton, New Jersey. Although slower than a bipolar junction transistor, a MOSFET is smaller and cheaper and uses less power, allowing greater numbers of transistors to be crammed together before a heat problem arises. Most microprocessors are made up of MOSFETs, which are also widely used in switching applications.

1.2 Silicon-on-Insulator Technology

In 1965, Gordon Moore, one of the visionaries of the semiconductors field, predicted that the number of components the industry would be able to place on a computer chip would double every year. In 1975, he updated his prediction to once every two years. It has become the guiding principle for the semiconductor industry to deliver ever-more-powerful chips while decreasing the cost of electronics, and over the years and for more than four decades, Moore´s "law" has held true. Figure 1.1 shows the latest update of Moore´s law, which sees the introduction of the world´s first processor with 2 billion transistors.

The extraordinary evolution of microelectronics has thus been made possible by continuously shrinking the size of the transistors and overcoming the challenges encountered at each transistor generation [Lederer-2006]. For a long time, the silicon-based planar bulk CMOS technology has been the choice of the microprocessor manufacturers due to its low cost and excellent scalability. Figure 1.2 shows the evolution of the transistors gate length for the last decades, as well as the predictions made by the International Technology Roadmap for Semiconductors (ITRS) for the next 15 years.

According to the 2009 ITRS Roadmap [ITRS-2009], the downscaling of the complementary metal-oxide-semiconductor (CMOS) has reached a point where further scaling faces a significant challenge. The main issue arises from the high-channel doping required to control short-channel effects (SCE), which significantly degrades carrier mobility and reduces the drain current. It also increases bond-to-bond tunneling across the junctions, leading to an increase of the parasitic leakage

current. In addition, the statistical fluctuation of channel dopants causes variations in the threshold voltage.

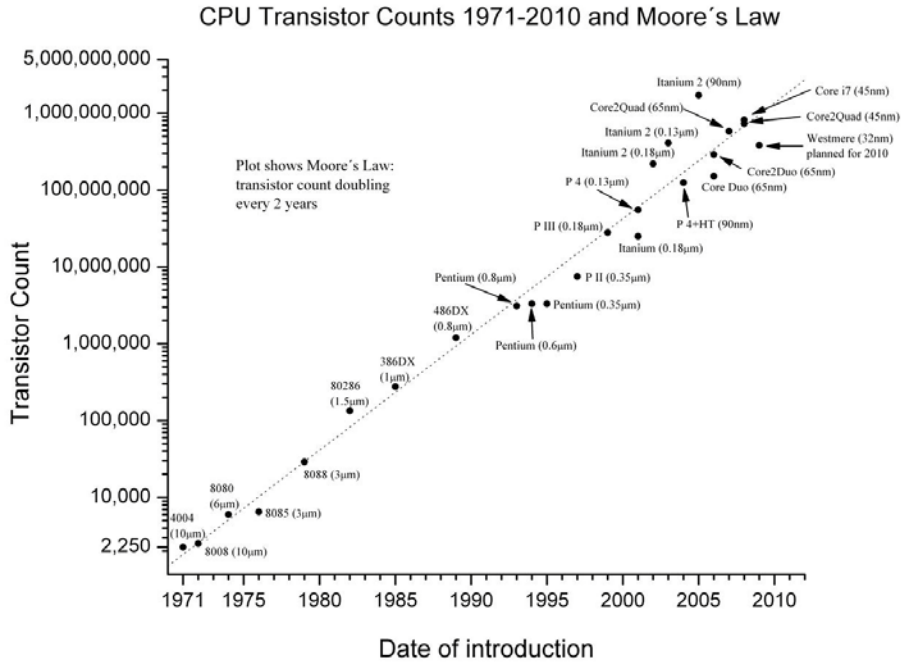


Fig.1.1. Moore´s law – plot of Intel CPU transistor counts against dates of introduction [Intel-2010]

As a consequence, the implementation of the new structures such as ultra-thin body (UTB) fully depleted (FD) silicon-on-insulator (SOI) and multiple-gate MOSFETs (MUGFETs), which require lower doping levels, even though also requires a special gate stack, appears to be the only viable alternative in silicon-based technologies to replace planar bulk CMOS devices.

However, the tremendous challenges faced by the implementation of FD SOI devices (such as a precise control of the silicon film thickness, the reduction of source and drain resistances to tolerable values, etc.) has driven some major integrated circuits (IC) manufacturers - such as Intel [Kavalieros-2006] or IBM [Kedzierski-2003] - to directly target the fabrication and production of multiple gate transistors.

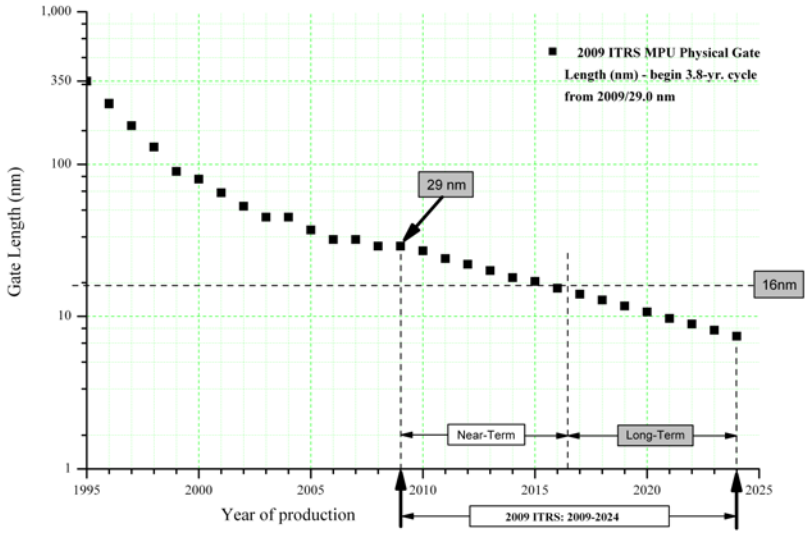


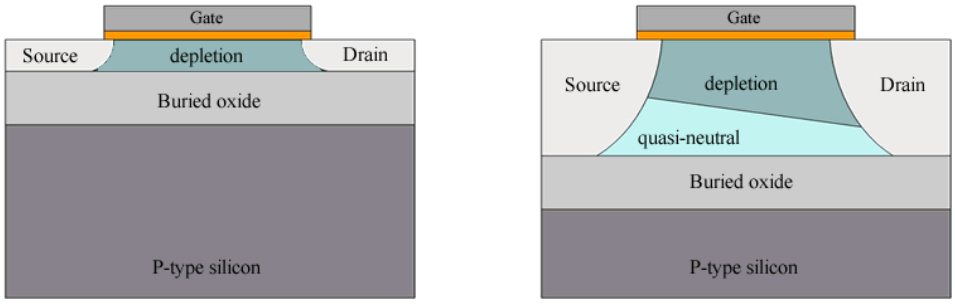
Fig. 1.2. ITRS predictions for the next 15 years [ITRS-2009]

SOI therefore appears as a necessary option for future silicon-based devices. The continuous and long term efforts that have been devoted to

developing and producing SOI by many independent and private research groups have grown SOI into a mature technology.

The use of SOI in the digital microprocessor world is now globally spread. However, as SOI is especially suited for low power applications, the technology has spread to the analog world, being a serious option for low-cost analog/RF products, such as front-end receivers of mobile phones.

Within the SOI planar technology, two distinct families of devices are classically considered, namely fully-depleted (FD) and partially-depleted (PD) MOSFETs (Fig. 1.3).



(a) (b)

Fig.1.3. FD (a) and PD (b) structures

In FD MOSFETs, the thickness of the silicon film is reduced in such a way that the depletion region below the inversion channel extends down to the buried oxide. In this case the entire Si film is depleted from free carriers. When the film is

made thicker the depletion region can stop at a certain depth within the silicon film, leaving an un-depleted region above the buried oxide called the body. For this reason such devices are referred to as partially-depleted MOSFETs. The floating potential of the body region in PD MOSFETs is responsible for the floating body effects, which affect the device´s electrical behavior.

The electrical characteristics of FD and PD MOSFETs are distinct and confer different advantages to both types of devices (see Table 1.1 for more details):

- **FD MOSFETs**: they present nearly ideal subthreshold slopes, enabling the reduction of the threshold voltage and power consumption. Junction capacitances are the lowest and the FD technology is therefore particularly suited for ultra low power analog applications [Vanmackelberg-2002; Ichikawa-2004].

- **PD MOSFETs**: they present a reduced process complexity compared to FD devices [Shahidi-2002]. They also present other advantages such as a dynamic threshold voltage (V_{TH}) (which can boost the drain current and reduces switching times [Cristoloveanu-2001]), an easier processing of multiple V_{TH} circuits, and the possibility of connecting the body (thereby enabling to completely suppress floating body effects under DC conditions [Shahidi-2002]). The characteristics of PD devices make them very attracting for high speed, high performance digital applications.

Type	PD	FD
Structural Differences	• Doped channel • Top silicon 50 to 90 nm thick (or more, for "thick SOI" applications) • Insulating BOX layer is typically 100 to 200 nm thick	• Often uses undoped or slightly doped channel • Top silicon 5 to 20 nm thick • Insulating BOX layer may also be ultra-thin – 5 to 50 nm
Target Applications	• High performance microprocessors • Most others (embedded, analog, RF, automotive, power, military, aero-space, etc.)	• High performance microprocessors • Low-power electronics • Ultra-low power
Advantages	• Well understood • Industrially proven • Easy to fabricate • Can leverage floating body for performance gain or memory applications	• Leakage and power consumption are drastically reduced • For undoped channels, random fluctuations in V_T are minimized • No floating body effect: easier to control short-channel effects
Challenges	• Physical limits to scalability are approaching for high- performance	• New metrology needed for defect detection in very thin layers • V_T defined by gate work function and intrinsic body • Very thin body can be challenging to manufacture and implement
Nodes	• 180 nm to 22 nm	• 22nm and beyond for high performance microprocessors and low power electronics • Ultra-low power now at 150nm

Table 1.1. Comparison between FD and PD MOSFETs

1.3 Advantages of SOI over bulk

At a device or circuit level, the advantages of SOI over bulk CMOS technologies are well known [Cristoloveanu-2001; Colinge-2004; Flandre-2001], and can be summarized as follows:

- **Substrate isolation:** as the BOX insulates the source/drain extensions from the substrate (Fig. 1.4b), junction capacitances and leakage current are reduced. This yields increased speed and reduced power consumption compared to the bulk technology. The isolation from the substrate also provides immunity to latchup.

- **Reliability:** SOI are insensitive to radiation effects, since electron-hole pairs are generated in the thick silicon substrate instead of the thin active film

- **Top material:** since the smart-cut process can be adapted to transfer any semiconductor material on top of the buried oxides, strained SOI (sSOI) and SiGe-on-insulator (SGOI) wafers can be easily fabricated.

- **High-Resistivity (HR) substrates:** the use of HR substrates is hardly compatible with bulk CMOS when digital circuitry is required (due to latchup issues [Huang-1982; Yamaguchi-1984]) unless patterned implants of deep boron doses are used to locally reduce the substrate resistivity [Benaissa-2003]. In SOI, low loss HR substrates can be easily fabricated and boost the performance of Si-based radio-frequency (RF) circuits.

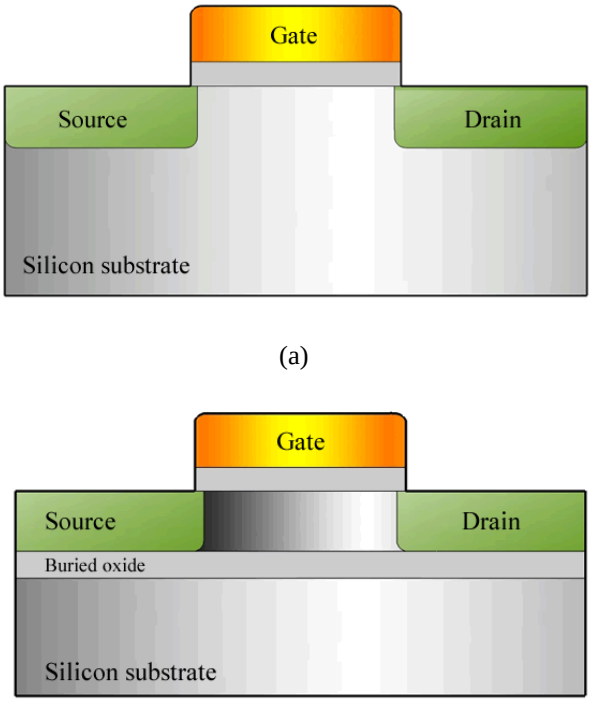


Fig. 1.4. Cross-section of a bulk (a) and SOI (b) MOSFET

- **Increased layout density:** unlike bulk, neither wells nor deep trenches are needed to isolate the devices from one another, allowing flexibility for more compact designs and offering a simplified technology.

- **New device architectures:** the use of SOI substrates facilitates the fabrication of SCE-free multiple gate devices at nanoscale dimensions, which form the future of the CMOS Roadmap.

There are also some disadvantages in using SOI technology, such as:

- **Self-heating:** due to the presence of the insulator which is not able to conduct heat away from the device fast enough, the effect of self-heating occurs. This can lead to a degradation of the current in the device at high current dissipation.

- **High cost of the wafer:** the cost of the wafer is about 2-3 times the cost of the bulk wafer, however after the completion of the process, the overall increase in cost is only about 20-30%.

It is quite clear that the advantages of using SOI technology for CMOS devices outweigh the disadvantages. For that reason, major companies, such as IBM, AMD, Sony, Freescale and many others are already implementing SOI based transistors in their products.

However, even within this SOI technology, devices are already reaching limitations. The main drive to move from classical devices such as Single-Gate (SG) MOSFETs is due to the demanding microelectronics industry and particularly the demand of the industry to shrink devices in the nanometer dimensions. Nowadays, electronic devices are not only getting smaller, but they also need to be multi-functional, with ever increasing demands and requirements. In order to meet them, the core of these electronic devices must be the first to be reinvented and redesigned [Ming-2007].

In the last decade, we have seen some remarkable technology at work, from just a few devices on a single silicon wafer, to Very-Large-Scale-Integration (VLSI) and in the last few years, this has moved to what is known as Ultra-Large-Scale-Integration (ULSI), in keeping with Moore's Law. This constant shrinking, however, has its limits, and we have reached the point where materials and device issues are starting to arise, opening the door for alternative device structures. The

most promising SOI devices for the nanoscale range are based on multiple gate structures, such as the double-gate (DG), the triple gate or fin-shaped field-effect transistor (FinFET), and the surrounding gate (SGT) or gate-all-around (GAA). We will describe in detail these novel devices in the next section.

1.4 Multiple-Gate Devices

1.4.1 Introduction

Multiple-gate transistors are devices with more than one gate operating simultaneously on the channel of a MOSFET. The idea of the multiple-gate device was first introduced in early 1980s. Sekigawa [Sekigawa-1984] exhibited his dual-gate device which was named XMOS in 1984. However, the first fabricated device was only made in 1989, where the DELTA (DEpleted Lean channel TrAnsistor) device was introduced by Hisamoto [Hisamoto-1989]. In 1987, Balestra proposed the GAA structure [Balestra-1987]. He simulated and experimented with the GAA device on a SIMOX wafer and showed that there was a big improvement in the subthreshold slope, current drive, transconductance. From these first devices, it was shown that the multiple-gate architecture has some interesting characteristics. One of the most important ones is the gate control over the electrostatic charges. This increased charge control in the channel translates into improved short channel effects. Another distinct characteristic of multiple-gate devices is the increased current.

Multiple-gate devices can also be grouped into various categories based on the conduction characteristics. The planar DG structure exhibits conduction in the planar horizontal direction. This means that the current flows parallel to the top substrate surface and along the <100> crystalline plane. The FinFET and other similar architectures also exhibits flow in the horizontal direction but it is different compared to the DG devices because the current flows in the <110> crystalline plane. However, for the triple-gate and the quadruple-gate devices, the current flow is a combination of flow in both the <100> and <110> planes, but still in a horizontal direction. Vertical MOS will have a conduction flow in the vertical direction.

The definition of the various multiple-gate structures can be easily mistaken if not defined properly based on their physical gate dimensions. The DG architecture can be characterized into two different types, planar or non-planar. The FinFET can be seen as a non-planar DG MOS if the two side gates are more prominent in dimension compared to the top (third) gate. If all three gates of the FinFET become more comparable in dimensions, this changes the structure into the triple-gate MOS structure. A quadruple-gate or GAA device can also be seen as a 3-dimensional DG if the two side gates are so far apart that they become ineffective compared to the two top and bottom gates. Figure 1.5 shows the various multiple-gate structures described above, which are the focus of this current research work.

1.4.2 Advantages of the multiple-gate structure

The introduction of multiple-gate structures has various advantages. As pointed in the last section, among these advantages is the improved electrostatic control of the

charges in the channel, an increase in current gain and a reduction in the junction capacitances. The existence of the second gate in the buried oxide increases the control in the channel because it reduces the influence of the penetrating lateral electric field which competes for the available depletion charges. This extra second gate or multiple-gate also increases the number of conducting surfaces which in turn increases the total current flow. An interesting characteristic of the multiple-gate devices is the so called volume inversion phenomenon. This phenomenon has

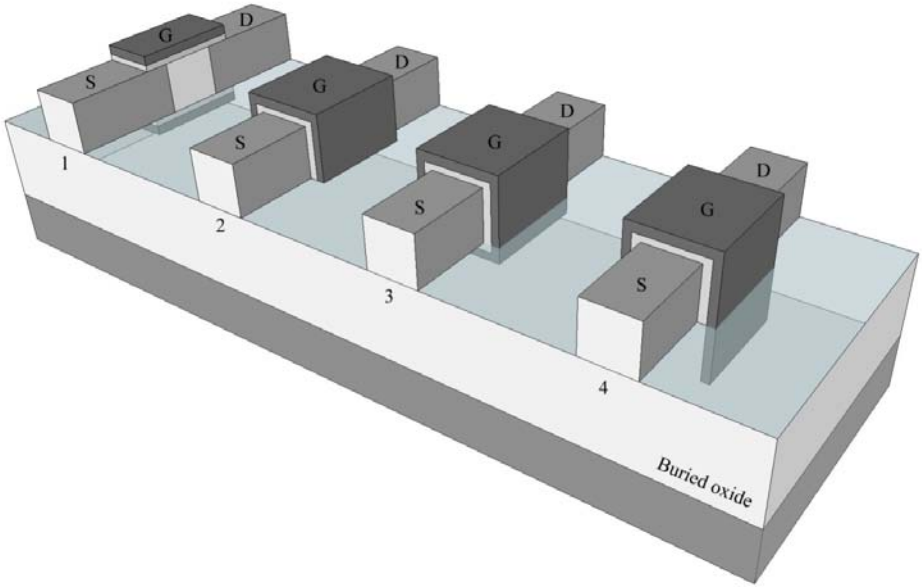


Fig.1.5. Multiple Gate MOSFET devices: 1-DG; 2-Triple-gate; 3-quadruple-gate; 4-PI-gate

many advantages in the functioning of the device. However, it is only limited to certain operation conditions. The mobility in multiple-gate devices is increased compared to the normal single-gate MOS transistor due to the reduced transverse

electric field and during the operation in the volume inversion mode, as well as the usual use of undoped materials. In the next paragraphs, some of the advantages are presented in more detail.

1.4.2.1 Subthreshold regime

One of the main advantages of using multiple-gate devices is the highly improved electrical characteristic in the subthreshold regime. This characteristic is further enhanced when the multiple-gate architecture is combined with the use of a thin silicon film. The threshold roll-off of FD SOI multiple-gate devices is much improved compared to the SG MOSFET, which is related to the reduction of the body effect. The body effect (γ) is already lowered due to the use of a SOI wafer, but in combination with extra gates, this body effect is decreased further. Equation (1.1) shows the correlation between the body effect and the threshold voltage for a FD device [Colinge-2004].

$$dV_{TH} = \gamma \times dV_{G2} \tag{1.1}$$

where V_{G2} is the back gate voltage and V_{TH} is the threshold voltage.

The drain induced barrier lowering (DIBL) characteristic of a FD multiple-gate transistor is much improved over a normal SG MOS transistor [Colinge-2002]. DIBL is the effect of the drain on the source barrier. This means that as the channel length is reduced, the threshold voltage will be influenced by the drain voltage leading to a drastic reduction as the drain voltage increases. This change is caused by the increased control of the drain towards the charges in the channel as the gate

length is reduced. The improved DIBL characteristic of FD multiple-gate MOS devices comes from the increased control of the gate on the charges in the channel, which allows for further downscaling of the device compared to the SG technology.

The subthreshold slope (*S*) is the inverse of the drain current to gate bias derivative in the subthreshold regime. The behavior of the device in the subthreshold regime is reflected by the subthreshold slope, as it shows the change of the subthreshold current with respect to the change in gate voltage. In an ideal transistor, the subthreshold current (drain current) is zero when the gate-to-source bias is less than the threshold voltage. However, such an ideal behavior is never obtained in practice. The idea value of the subthreshold slope is 60mV/dec at room temperature. A sharp subthreshold slope is desired because, as mentioned, it reflects on the subthreshold current with respect to the change in gate bias. Equation (1.2) shows the relation between the subthreshold current (I_{DSsub}) and the gate-to-source bias (V_{GS}) [Neaman-1997].

$$I_{DSsub} \propto \exp\left[\frac{V_{GS}}{S}\times\ln(10)\right]\times\left[1-\exp\left(-\frac{eV_{DS}}{kT}\right)\right] \tag{1.2}$$

where *e* is the electronic charge, *k* is Boltzman´s constant and *T* the temperature.

Another figure of merit to measure or predict the short-channel effect for devices is what is known as the natural (or characteristic) length, λ. This characteristic length determines how far the electric field lines will penetrate the device and affect the depletion zone, and it depends on the gate oxide and silicon thickness. This characteristic length was first introduced by R.-H. Yan et al. [Yan-1992] as a guide for scaling the devices. It is desirable to have λ as short as possible. The λ concept is used to estimate the silicon film thickness and width of

the device in order to reduce as much as possible thee short-channel effects in the device, as described by J.P. Colinge [Colinge-2003].

1.4.2.2 Increased drain current

One of the main advantages of the multiple-gate architecture is the increase of the total current generated by in the device. The current in a multiple-gate SOI MOSFET is proportional to the total gate width. The increase of the drain current per channel is related to the increase in the number of gates. For example, the current drive in a planar DG SOI MOSFET is twice that of a SG SOI MOSFET if the width and gate length are the same. Thus, the drive current would simply be $I_{DSDG} = 2 \cdot I_{DSSG}$.

In order to increase the current density (I_{DS} /occupied die area), we will have to expand the design of the devices. Among the factors that can increase the current density would be to modify the architecture of the device, increasing the number of devices on each die, introducing spacing between the fins creating multi-fingered devices, etc. Figure 1.6 shows a schematic cross-section of a multi-fingered triple-gate transistor.

The current in multi-fingered devices such as the FinFET and triple-gate devices can be expressed in general as Eq. (1.3) [Colinge-2003]. The FinFET is also known as a vertical DG device.

$$I_{DS} = I_{D0} \cdot \left(W_{fin} + 2H_{fin} \right) \cdot n \tag{1.3}$$

where I_{d0} is the current of a unit-width, planar, SG device, W_{fin} is the width of each individual fin, H_{fin} is the silicon film thickness and n is the number of fins. From Eq. (1.3), for the FinFET, the drain current per device unit is reduced to:

$$I_{DS} = I_{D0} \cdot 2H_{fin} \tag{1.4}$$

due to the fact that the top gate would not be effective in generating current, thus it can be omitted.

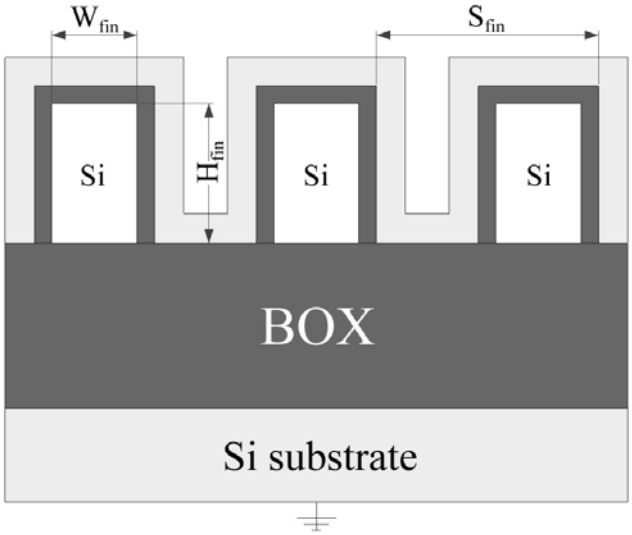


Fig. 1.6. Schematic cross-section of a multi-fin triple-gate transistor

For a triple-gate device, since the width of the device is equal to the thickness of the silicon film, the current drive can be expressed as:

$$I_{DS} = I_{D0} \cdot 3H_{fin} \tag{1.5}$$

One other great advantage of multiple-gate devices compared to SG is the volume inversion regime, described in detail in the next section. When the multiple-gate transistor is biased in weak inversion regime, we can benefit from the volume inversion phenomenon, which further increases the drive current.

1.4.2.3 Volume inversion

The volume inversion is a phenomenon found only in multiple-gate architectures. A device is said to be operating in volume inversion if there is a strong coupling between two conducting channels [Balestra-1987]. This happens only in a certain region of operation, usually around the threshold voltage for certain film thickness and doping concentration in the channel. When a device operates in volume inversion, the whole silicon film is inverted and there is an increase in the minority carriers leading to an increase in current and a reduction of the scattering effects. Because of this reduction in the scattering effects, there is an increase in the carrier mobility, especially in the center of the silicon film (due to the increase in electron concentration), which leads to an overall increase of the transconductance characteristic of the device.

However, as mentioned before, in order to achieve this volume inversion mode of operation, certain criteria have to be met. For example, if we have a thin silicon film, but the doping of the film is too high, it does not necessarily mean that a few hundred milivolts above threshold the volume inversion mode would be achieved. This is because the Fermi level of such a device cannot be overcome due

to the high doping. The same can be said if we have an intrinsic doping but the silicon film is thicker than a certain value.

1.4.2.4 Speed superiority

Results have shown that the DG architecture exhibits excellent unloaded-circuit speed superiority compared to the SG device (SOI or bulk) [Fossum-2002]. The increase of the parasitic capacitances of the DG architecture compared to SG devices does not seem to deteriorate the overall speed. The operation of the DG architecture in lower supply voltage shows that it is a very promising candidate for future nodes. The increase in overall speed of the DG device is attributed to the much improved subthreshold slope and the on-state currents of more than a factor of 2. It was also shown that at low gate voltage and in saturation region the gate capacitance is relatively low [Fossum-2002]. This happens because in the DG devices, at low V_{GS}, it does not need to support the dynamic charge as compared to the SG device. The dynamic charge is related to the common speed metric, which tends to overestimate the intrinsic delay of the DG MOSFET relative to the SG counterpart at low V_{GS}.

It is clear that the multiple-gate architecture is one of the most promising novel devices that will be able to move forward with the ITRS demands. The multiple-gate architecture has been proven to have good electrical characteristics even when the gate length is reduced to the nano regime, thus making it very suitable for deep submicron devices. One of the reasons to the good electrical characteristics of the multiple-gate architecture is the excellent control of the charges in the channel. They have also been shown to reduce the short-channel

effects even further compared to the technologically advanced SG devices, making them very suitable for radio-frequency applications, one of the most important markets for these devices.

1.5 Compact modeling

Compact models of devices are used in circuit simulators, in order to predict the functionality of circuits [Moldovan-2009]. These multiple-gate devices will be preferred in nanoscale circuits, thus calling for accurate and reliable compact models, including new device specific effects. These compact models that accurately describe the novel devices, and are computationally efficient are an important prerequisite for successful circuit design. The currently available compact models are facing enormous challenges in modeling the observed physical phenomena in the sub-90-nm technologies [Saha-2006]. The demands for advanced models, which can describe nanoscale silicon devices in analog and mixed-signal applications and can account for the physical effects on small geometry devices, have led to enormous research & development (R&D) efforts in the development of advanced physics-based compact models.

For multiple-gate MOSFETs the principles of modeling will change as compared to the traditional SG MOSFET, firstly because they will have to introduce the volume inversion effect, secondly, contrary to bulk MOSFETs, depletion charges in multiple-gate devices are negligible because the silicon film is undoped (or lightly doped). Thus, only the mobile charge term needs to be included in Poisson's equation. Therefore, the exact analytic solutions to 1D Poisson's and

current continuity equations based on the gradual-channel-approximation (GCA), which assumes that the quasi Fermi potential stays constant along the direction perpendicular to the channel) can be derived, without the charge-sheet approximation. It is considered that the electrostatic control of the gates is good enough to neglect SCEs associated to 2D effects. Most models presented so far are for undoped devices with a long enough channel to assume that the transport is due to the drift-diffusion transport mechanism [Iniguez-2006; Taur-2004; Ortiz-Conde-2005; Jimenez-2004].

Using the above principles, some models for undoped DG [Taur-2004; Xiong-2005; Ortiz-Conde-2005; Jimenez-2004] and SGT [Iniguez-2006; Jimenez-2003] have been published, showing good agreement with three dimensional numerical simulations.

A very promising modeling approach presented recently is based on the solution of Laplace's equation for the extended body (including the gate insulators) of the short-channel nanoscale DG MOSFETs using conformal mapping techniques [Kolberg-2006; Fjeldly-2006; Kolberg2-2006]. This technique was first explored for the long-channel bulk MOSFETs [Klos-1996] and later for sub-0.1-μm MOSFETs [Osthaug-2004], and finally for DG MOSFETs.

However, for devices with channel lengths shorter than 50nm, the transport mechanism will probably not be drift-diffusion; ballistic or quasi-ballistic transport may appear. We cannot define a continuous quasi- Fermi potential that varies from the source to the drain and controls the mobile-charge distribution. What will happen is that carriers injected from the source will depend on the Fermi potential at the source, and carriers injected from the drain will depend on the Fermi potential at the drain.

For this, accurate models that will include the ballistic or quasi-ballistic regime are needed [Toriumi-1988; Natori-1994; Ren-2000; Chang-2000; Ge-2001]. On the other hand, for films smaller than 10 nm, quantum confinement in the film may not be negligible. Thus, accurate MOSFET models that include these new physical behaviours are crucial to design and optimize advanced VLSI circuits for nanoscale CMOS technology.

In addition to the high levels of integration for digital circuit design offered by advanced CMOS processes, the high-frequency capabilities of the MOSFETs have reached well into the gigahertz range [Shaeffer-1977], opening new opportunities for RF circuit applications and creating new markets in the microwave and millimeter wave region. These MOSFETs are also capable of operating in the GHz regime because of their very high unit-gain frequencies of tens of GHz. The use of low power, low noise devices for future electronic applications is becoming more and more important. Especially, SOI devices are excellent candidates to become an alternative to conventional bulk CMOS for RF operation. High-resistivity SOI substrates have demonstrated a higher performance over standard-resistivity SOI and bulk silicon with regard to crosstalk at frequencies up to 10 GHz [Raskin-1997]. Also, SOI technologies are preferred for RF applications due their lower losses in passive devices [Lederer-2004]. However, when working at high frequencies, the noise generated within the device itself will play an increasingly important role in the overall RF IC performance, for example in the noise performance of a front-end receiver in a RF IC. Therefore, a physics-based noise model which can accurately predict the noise characteristics of multiple-gate MOSFETs is crucial for the low noise, RF IC design. Accurate noise modeling is a prerequisite for the application of multiple-gate MOSFET technologies to low noise RF design.

1.6 Purpose of this work

The main purpose of this research is to study in detail the various novel transistor architectures built on SOI MOSFET technology and their application to RF operation. Numerical characterization methods are very time consuming, thus an alternative is offered by compact models based on the physical characteristics of the transistors, models that are successful in reproducing the behavior of real devices and predict with certain accuracy the next performances of next generation devices.

After the brief introduction in the world of semiconductors done in **Chapter 1**, we dedicate **Chapter 2** to presenting the most important aspects of noise in transistors operating and RF. The noise parameters calculations is based on the equivalent circuit method, which is presented in detail, from the DC equivalent circuit theory to introducing the noise sources and finally solving the transistor equations for RF.

Chapter 3 presents a compact model for DG MOSFETs, detailing the charge control model, the DC equations and finally analyzing the device at RF. A study of the drain and gate noise spectrums is carried on, and novel fully analytical equations for these figures of merit are obtained. Results of the main figures of merit for RF operation (cut-off frequency - f_T -, maximum frequency of oscillation - f_{max} -, minimum noise figure - F_{min}) are presented, which are consistent with numerical simulations, and provide a good insight into what the next technological nodes will bring.

Chapter 4 presents a compact model for SGT, based on the DG transistor model presented before, and the same analysis that was done previously for DG is carried out for SGT, proving the validity of these kinds of devices for future downscaling.

Chapter 5 presents a compact model for FinFET, also based on the DG transistor model, and it´s noise and RF analysis is carried out. The analysis proves that FinFET devices are a possible replacement for planar MOSFET transistors.

Finally, some conclusions are drawn in **Chapter 6**, as well as some recommendations for future developments of these models according to the next ITRS steps.

1.7 References

[Balestra-1987] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion: a new device with greatly enhanced performance", *IEEE Electron Device Letters*, **8**, 410-412 (1987)

[Benaissa-2003] K. Benaissa, J.-T. Yuan, D. Crenshaw, B. Williams, S. Sridhar, J. Ai et al, "RF CMOS high-resistivity substrates for systems-on-chip applications", *IEEE Transactions on Electron Devices*, **50**, 567-576 (2003)

[Chang-2000] L. Chang, C. Hu, "MOSFET scaling into the 10 nm regime", *Superlattices Microstructures*, **28**, 351–355 (2000)

[Colinge-2002] J.-P. Colinge, C.A. Colinge, "Physics of Semiconductor Devices", USA: Springer (2002)

[Colinge-2003] 2003 Spring Meetings Proceedings, editor, "Evolution of SOI MOSFETs: From single-gate to multiple-gates", *MRS Proceedings*, **765**, D1.6 (2003)

[Colinge-2004] J.-P. Colinge, "Silicon-on-insulator technology: Material to VLSI", USA: Springer (2004)

[Cristoloveanu-2001] S. Cristoloveanu, "Silicon-on-insulator technologies and devices: from present to the future", *Solid State Electronics*, **45**, 1403-1411 (2001)

[ElecTime-2009] "Electronics Timeline" [online], available at: http://www.greatachievements.org/?id=3956

[Fjeldly-2006] T.A. Fjeldly, S. Kolberg, B. Iniguez, "Precise 2-D compact modeling of nanoscale DG MOSFETs based on conformal mapping techniques", *Tech. Proc. NSTI-Nanotechnology, Boston, MA*, **3**, 668-673 (2006)

[Flandre-2001] D. Flandre, J.-P. Raskin, D. Vanhoenacker, "SOI CMOS transistors for RF and microwave applications", *International Journal of High Speed Electronics and Systems*, **11**, 1159-1248 (2001)

[Fossum-2002] J.G. Fossum, G. Lixin, C.Meng-Hsueh, "Speed superiority of scaled double-gate CMOS", *IEEE Transactions on Electron Devices*, **49**, 808-811 (2002)

[Ge-2001] L. Ge, J. Fossum, "Physical compact modeling and analysis of velocity overshoot in extremely scaled CMOS devices and circuits", *IEEE Transactions on Electron Devices*, **48**, 2074–2080 (2001)

[Hisamoto-1989] D. Hisamoto, T. Kaga, Y. Kawamoto, E. Takeda, "A fully depleted lean-channel transistor (DELTA) – a novel vertical ultrathin SOI MOSFET", *Technical Digest of IEDM*, 833-836 (1989)

[Huang-1982] C.C. Huang, M.D. Hartranftand, N.F. Pu, C. Yue, C. Rahnand, J. Schrankler et al, "Characterization of CMOS latch-up", *Digest of International Electron Device Meeting*, 454-457 (1982)

[Ichikawa-2004] F. Ichikawa, Y. Nagamoto, Y. Katakura, M. Itoh, S. Itoh, H. Matsuhashi et al, "Fully depleted SOI process and device technology for digital and RF applications", *Solid State Electronics*, **48**, 999-1006 (2004)

[Iniguez-2006] B. Iniguez, T.A. Fjeldly, A. Lazaro, F. Danneville, M.J. Deen, "Compact-modeling solutions for nanoscale double-gate and gate-all-around MOSFETs", *IEEE Transactions on Electron Devices*, **53**, 2128-2142 (2006)

[Intel-2010] "Intel – Microprocessor Quick Reference Guide" [online], available at: http://www.intel.com/pressroom/kits/quirckrefyr.htm

[ITRS-2009] "Executive Summary 2009 Edition" [online], available at: http://www.itrs.net/Links/2009ITRS/2009Chapters_2009Tables/2009_ExecSum.pdf

[Jimenez-2003] D. Jimenez, J.J. Saenz, B. Iniguez, J. Sune, L.F. Marsal, J. Pallares, "Unified compact model for the ballistic quantum wire and quantum well metal oxide semiconductor field effect transistor", *Journal of Applied Physics*, **94**, 1061-1068 (2003)

[Jimenez-2004] D. Jimenez, B. Iniguez, J. Sune, L.F. Marsal, J. Pallares, J. Roig et al, "Continuous analytic current-voltage model for surrounding gate MOSFETs", *IEEE Electron Device Letters*, **25**, 571-573 (2004)

[Kavalieros-2006] J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin et al, "Tri-gate transistor architecture with high-k dielectrics, metal gates and strain engineering", *VLSI Symposium* (2006)

[Kedzierski-2003] J. Kedzierski, M. Ieong, E.J. Nowak, T.S. Kanarsky, Y. Zhang, R. Roy et al, "Extensions and source/drain design for high performance FinFET devices", *IEEE Transactions on Electron Devices*, **50**, 942-957 (2003)

[Klos-1996] A. Klos, A. Kostka, "A new analytical method of solving 2D Poisson´s equation in MOS devices applied to threshold voltage and subthreshold modeling", *Solid State Electronics*, **39**, 1761-1775 (1996)

[Kolberg-2006] S. Kolberg, T.A. Fjeldly, "2-D modeling of nanoscale DG SOI MOSFETs in the subthreshold regime", *Journal of Computational Electronics*, **5**, 217-222 (2006)

[Kolberg2-2006] S. Kolberg, T.A. Fjeldly, B. Iniguez, "Self-consistent 2-D compact model for nanoscale double gate MOSFETs", *Proc. ICCS, Reading, U.K.*, Germany: Springer-Verlag, vol. **3994**, pp. 607-614 (2006)

[Lederer-2004] D. Lederer, R. Lobet, J.-P. Raskin, "Enhanced high resistivuty SOI wafers for RF applications", *Proceedings of IEEE International SOI Conference*, 46 (2004)

[Lederer-2006] D. Lederer, "Wideband characterization of advanced SOI material and MOS devices for high frequency applications", PhD Thesis, UCL (Belgium) (Oct. 2006)

[Ming-2007] C.T. Ming, "Graded Channel and Multiple-Gate Devices in SOI Technology for Analog and RF Applications", PhD Thesis, UCL (Belgium) (Apr. 2007)

[Moldovan-2009] O. Moldovan, B. Iniguez, "Compact modeling for MOSFET devices: small-signal models for multiple-gate transistors", Germany: VDM Verlag (2009)

[Natori-1994] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor", *Journal of Applied Physics*, **76**, 4879-4890 (1994)

[Neaman-1997] D.A. Neaman, "Semiconductor Physics and Devices: Basic Principles", USA: McGraw-Hill Companies Inc., 2nd edition (1997)

[Ortiz-Conde-2005] A. Ortiz-Conde, F.J. Garcia Sanchez, J. Muci, "Rigorous analytic solution for the drain current of undoped symmetric dual-gate MOSFETs", *Solid State Electronics*, **49**, 640-647 (2005)

[Osthaug-2004] J. Osthaug, T.A. Fjeldly, B. Iniguez, "Closed-form 2D modeling of sub-100 nm MOSFETs in the subthreshold regime", *J. Telecom. Inform. Techn.*, 1, 70-79 (2004)

[Raskin-1997] J.-P. Raskin, A. Viviani, D. Flandre, J.-P. Colinge, "Substrate crosstalk reduction using SOI technology", *IEEE Transactions on Electron Devices*, **44**, 2252 (1997)

[Ren-2000] Z. Ren, R. Venugopal, S. Datta, M. Lundstrom, D. Jovanovic, J. Fossum, "The ballistic nanotransistor: a simulation study", *IEDM Tech Digest*, 715–718 (2000)

[Saha-2006] S.K. Saha, N.D. Arora, M.J. Deen, M. Miura-Mattausch, "Foreword special issue on advanced compact models and 45-nm modeling challenges", *IEEE Transaction on Electron Devices*, **53**, 1957-1959 (2006)

[Sekigawa-1984] T. Sekigawa, H. Hayashi, "Calculated threshold voltage characteristics of an XMOS transistor having an additional bottom gate", *Solid State Electronics*, **27**, 827-828 (1984)

[Shaeffer-1977] D.K. Shaeffer, T.H. Lee, "A 1.5 V 1.5 GHz CMOS low noise amplifier", *IEEE Journal of Solid-State Circuits*, **32**, 745 (1977)

[Shahidi-2002] G.G. Shahidi, "SOI technology for the GHz era", *IBM Journal of Research and Development*, **46**, 121-131 (2002)

[Taur-2004] Y. Taur, X. Liang, W. Wang, H. Lu, "A continuous, analytic drain current model for DG-MOSFETs", *IEEE Electron Device Letters*, **25**, 107-109 (2004)

[Toriumi-1988] A. Toriumi, M. Iwase, M. Yoshimi, "On the performance limit for Si MOSFET: experimental study", *IEEE Transactions on Electron Devices*, 35, 999-1003 (1988)

[Vanmackelberg-2002] M. Vanmackelberg, C. Raynaud, O. Faynot, J.-L. Pelloie, C. Tabone, A. Grouilet et al, "0.25 μm fully depleted SOI MOSFETs for RF mixed analog-digital circuits, including a comparison with partially depleted devices with relation to high frequency noise parameters", *Solid State Electronics*, **46**, 379-382 (2002)

[Xiong-2005] S. Xiong, T.J. King, J. Bokor, "A comparison study of symmetric ultrathin body double gate devices with metal source/drain and doped source/drain", *IEEE Transaction on Electron Devices*, **52**, 1859-1867 (2005)

[Yamaguchi-1984] T. Yamaguchi, S. Morimoto, G.H. Kawamoto, J.C.D. Lacy, "Process and device performance of 1 µm-channel n-well CMOS technology", *IEEE Transactions on Electron Devices*, **31**, 205-214 (1984)

[Yan-1992] R.-H. Yan, A. Ourmazd, K.F. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk", *IEEE Transactions on Electron Devices*, **39**, 1704-1710 (1992)

Chapter 2

RF and Noise Theory

2.1 Introduction

The evolution of CMOS technologies in the microwave domain has required the development of specific characterization techniques. Methods have been developed to determine a correct model of transistors, based on the measurements of their true S-parameters. The models for high frequency transistors are basically of two kinds:

- **Polynomial models**: they are obtained easily from measurements. They describe the behavior of the devices, as black boxes. They can be easily

introduced in circuit simulators, but no information about the device physics can be deduced from the model.

- **Physical small signal equivalent circuits**: these circuits are usually close to the device physics. The circuit elements have a known origin, but they are not easily extracted from the S-parameters.

The knowledge of the equivalent circuit is useful in developing circuit design methodologies, or to determine which parameters have strong influences on the performance of MOSFETs.

In the following sections, a general equivalent circuit of MOSFET transistors is presented. It is created based in the device physics and its structure. Also, one of the most important parameters in high frequency transistor operation, namely the noise performance, is discussed.

2.2 Small-Signal Modeling of SOI MOSFETs

One of the advantages of SOI transistors compared to bulk devices is that at microwave frequency, the substrate does not influence significantly the behavior of the transistor. Thanks to the thickness of the buried oxide, the body effect can be neglected at high frequency [Gaffioul-2000]. There are no significant parasitic effects related to the substrate occurring at microwave frequency. Thus, it is not necessary to develop a four terminal model for the SOI transistor used at microwave frequency. Over the next sections, a general equivalent circuit of SOI MOSFETs is presented, which takes into account its intrinsic behavior and physical structure.

2.2.1 Useful effect

The useful effect of a MOSFET is its ability to control its output current (I_D) when a voltage is applied to the gate (V_G). This behavior can be easily modeled using a voltage controlled current source connected between the device source and drain. The gate voltage will be applied between the gate and the source. A preliminary equivalent circuit, modeling the useful effect of the device, can then be drawn (Fig. 2.1). The transconductance (g_{mi}) is qualified as an intrinsic element, because it is a simple representation of the physical phenomenon that occurs inside of the transistor channel. The transconductance is defined as:

$$g_{mi} = \left.\frac{\partial i_{ds}}{\partial v_{gs}}\right|_{v_{ds}=0} \tag{2.1}$$

where i_{ds} is the small variation of the drain current when a small variation of potential (v_{gs}) is applied to the gate.

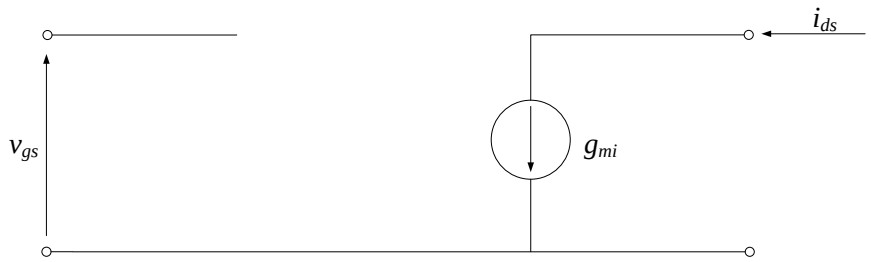


Fig. 2.1. Modeling of the useful effect of a MOSFET

Even if it denotes the useful effect of the MOSFET, the equivalent circuit (Fig. 2.1) is not efficient enough to describe the behavior of the device if the operating frequency is raised, as no parasitic elements are taken into account.

2.2.2 Quasi-static model

Due to transistor physics, there are influences from each device terminals on the others. These influences can be modeled by capacitances added in the equivalent circuit (Fig. 2.2). As explained in [Tsividis-1987], all these capacitances added in the equivalent circuit are bias depended and are related to variations of charges or currents when a small signal is applied around equilibrium on a terminal. The capacitances between the source, drain and gate are defined by:

$$C_{gd} = -\left.\frac{\partial q_g}{\partial v_d}\right|_{v_s = v_g = 0} \tag{2.2}$$

$$C_{gs} = -\left.\frac{\partial q_g}{\partial v_s}\right|_{v_d = v_g = 0} \tag{2.3}$$

$$C_{ds} = -\left.\frac{\partial q_d}{\partial v_s}\right|_{v_d = v_g = 0} \tag{2.4}$$

These relations can be used only in quasi-static operation. The applied small signal is varying sufficiently slowly so that the charges respond instantaneously to the applied signal.

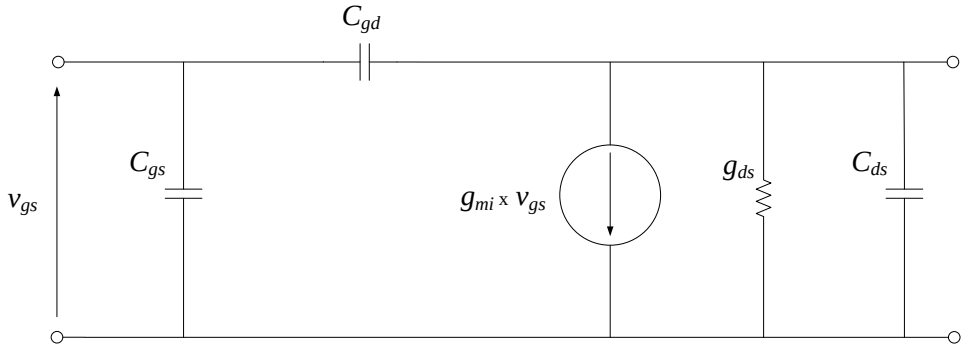


Fig. 2.2. Intrinsic quasi-static model of a MOSFET

However, MOSFETs being imperfect current sources, an output conductance must be added in the model. It is defined by:

$$g_{ds} = \left.\frac{\partial i_{ds}}{\partial v_{ds}}\right|_{v_{gs}=0} \tag{2.5}$$

The capacitances are not linked to any physical capacitor-like structure. They are representations of the influence of a voltage applied on a terminal on the charges being at another terminal, with regards to the MOSFET physics, and are called intrinsic capacitances.

These intrinsic capacitances may not be reciprocal. Considering an ideal MOSFET in saturation, any variation of the drain voltage will not introduce any variation of the output current and of the gate charges because of pinch-off. Hence the drain to gate capacitance must be equal to zero. But if the gate voltage is changed, a variation of the current will occur, inducing a variation of drain charges. The gate to drain capacitance will then be higher than zero, and will be different from the drain to gate capacitance.

This non-reciprocal effect can be modeled by adding a parasitic element to the transconductance, defining a new one. The new "effective" transconductance ($g_{mi}^{'}$) can be defined as:

$$g_{mi}^{'} = g_{mi} - j\omega C_m = \left| g_{mi} \right| \cdot e^{-j\omega\tau} \tag{2.6}$$

where

$$C_m = C_{dg} - C_{gd} \tag{2.7}$$

2.2.3 Non-quasi-static model

In the previous section, an equivalent circuit of MOSFETs has been presented, considering that charges respond without delay to the applied signal. But when the frequency becomes higher, the charges are not able to follow the signal instantaneously. This phenomenon can be observed more easily for long devices. According to Tsividis [Tsividis-1987], the upper frequency limit of the quasi-static model is proportional the cut-off frequency (f_T), which is approximately proportional to $1/L^2$, L being the channel length of the transistor (Fig. 2.3).

To model the non-quasi-static effects, the MOSFET channel can be divided into several small transistors connected together, as presented in (Fig 2.3). Then, quasi-static models are used for all sub-transistors. This solution is used when the values of different intrinsic elements are obtained using formulae from the physical model. If they must be extracted from measurements, this method cannot be used, as the number of unknowns increases drastically.

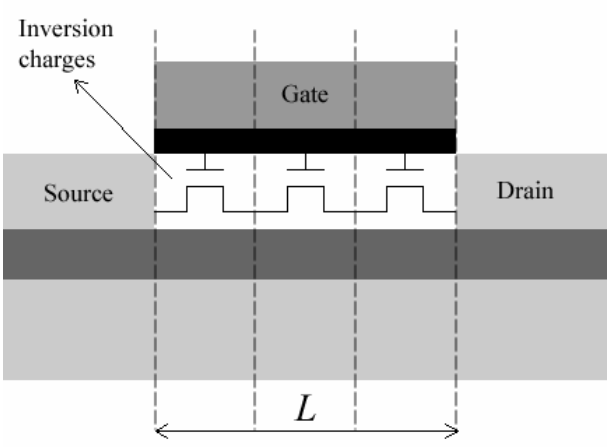


Fig. 2.3. Non-quasi-static modeling of a MOSFET using several quasi-static transistors connected together

Instead of dividing the MOSFET into several small transistors, the non-quasi-static effects can be modeled by introducing new elements in the equivalent circuit (Fig 2.4).

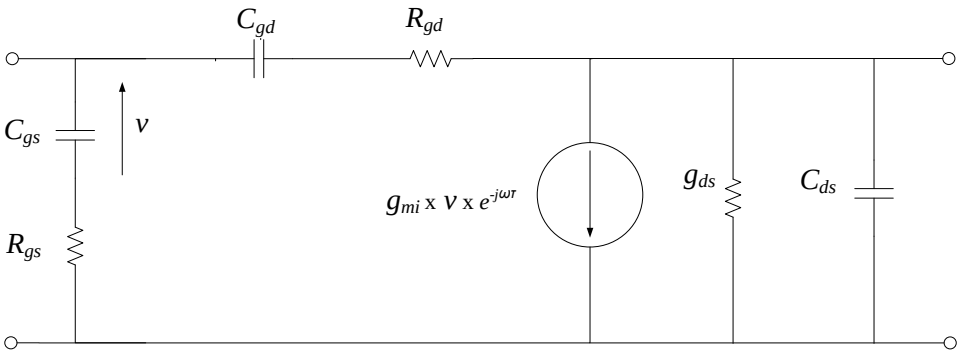


Fig. 2.4. Intrinsic non-quasi-static model of a MOSFET

These elements introduce a delay between the signal and its effects. There are two kinds of elements: intrinsic resistances (R_{gd}, R_{gs}) that are in series with the intrinsic capacitances, and a time delay (τ) affecting the transconductance. The command of the voltage controlled current source is still the potential "v" applied to the intrinsic capacitance C_{gs}.

The Y-matrix of the new equivalent circuit of Fig. 2.4 is given by:

$$Y = \begin{bmatrix} j\omega\left(\frac{C_{gs}}{1+j\omega R_{gs}C_{gs}} + \frac{C_{gd}}{1+j\omega R_{gd}C_{gd}}\right) & -j\omega\frac{C_{gd}}{1+j\omega R_{gd}C_{gd}} \\ \frac{g_{mi}e^{j\omega\tau}}{1+j\omega R_{gs}C_{gs}} - j\omega\frac{C_{gd}}{1+j\omega R_{gd}C_{gd}} & g_{ds} + j\omega\left(C_{sd} + \frac{C_{gd}}{1+j\omega R_{gd}C_{gd}}\right) \end{bmatrix} \quad (2.8)$$

2.2.4 The extrinsic model

In the previous sections, equivalent circuits have been defined considering the physical properties of the MOSFET channel. They are composed of several intrinsic elements, which depend on the device dimensions and on the applied bias. However, the physical structure of the MOSFET is more complex, and due to its geometry, some parasitic elements are surrounding the active part of the device, which are mainly bias independent.

In the following sections, these parasitic elements are described. They will be defined from the closest to the intrinsic region to the furthest, filling the gap between the intrinsic part of the device and the reference planes defined by the calibration (the pads).

2.2.4.1 Extrinsic capacitances

Several parasitic capacitances are located around the channel of the transistor, as presented in Fig. 2.5. They are bias independent and proportional to the transistor width. They are named *extrinsic* capacitances and noted with an index "*e*".

The extrinsic gate-to-source (C_{gse}) and gate-to-drain (C_{gde}) capacitances are composed of two different elements. They include overlap capacitances, located between the gate oxide and the diffusion of the source and the drain under the gate, and fringing capacitances from the gate sides to the source and drain implants.

The capacitance C_{dse} is different from the other extrinsic capacitances. It is the expression of the coupling between source and drain through the silicon film, the buried oxide and the substrate. The capacitance C_{dse} is the simplest high frequency model of a complex capacitive network.

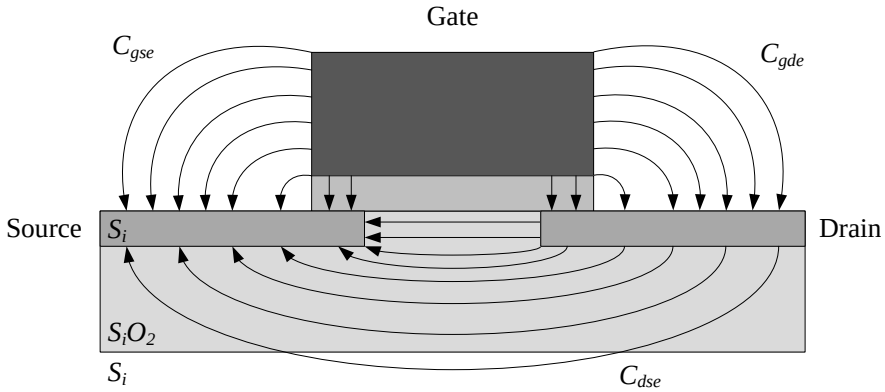


Fig. 2.5. Location of the extrinsic capacitances in the physical structure of the MOSFET

The extrinsic capacitances are added to the previous equivalent circuit. A new one is obtained (Fig. 2.6). Its Y-matrix is given by:

$$Y_{\Pi} = Y_i + Y_e \tag{2.9}$$

where

$$Y_e = \begin{bmatrix} j\omega\left(C_{gde} + C_{gse}\right) & -j\omega C_{gde} \\ -j\omega C_{gde} & j\omega\left(C_{dse} + C_{gse}\right) \end{bmatrix} \tag{2.10}$$

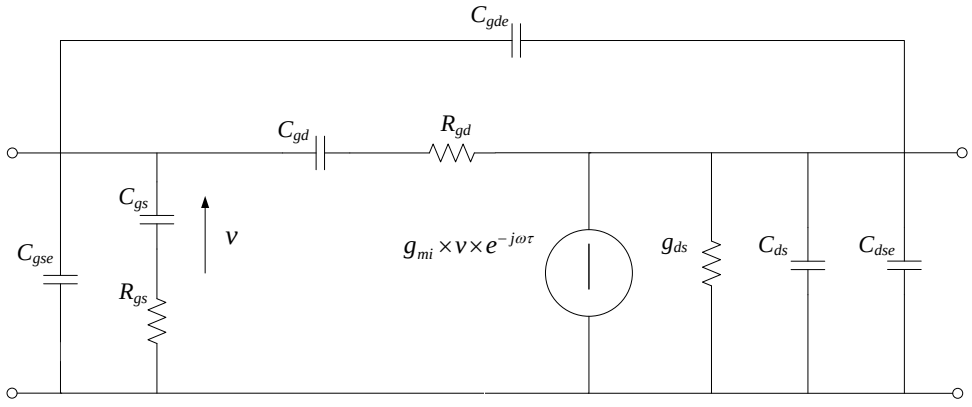


Fig. 2.6. Intrinsic model of a MOSFET with extrinsic capacitances

2.2.4.2 Extrinsic resistances and inductances

The intrinsic gate, source and drain are connected to the “outside world” by gate, source and drain fingers. These fingers having a given resistivity, they are distributed resistances (Fig 2.7.).

These distributed elements are modeled using lumped resistances called R_g, R_s and R_d, since the transistor is generally small compared to the wave length. They are connected to the gate, source and drain respectively.

The resistances R_d and R_s include the metallic losses and the contact resistances between the metal and the source and drain implants. They are proportional to the inverse of the transistor width. The resistance R_g includes the resistance of the gate fingers, which is proportional to the transistor width, and the resistance of some metallic lines. These lines connect the gate fingers together and to the reference plane, in most of the cases, the resistance of the gate finger is much higher than the others. It is usually considered as the only contribution to the extrinsic gate resistance R_g.

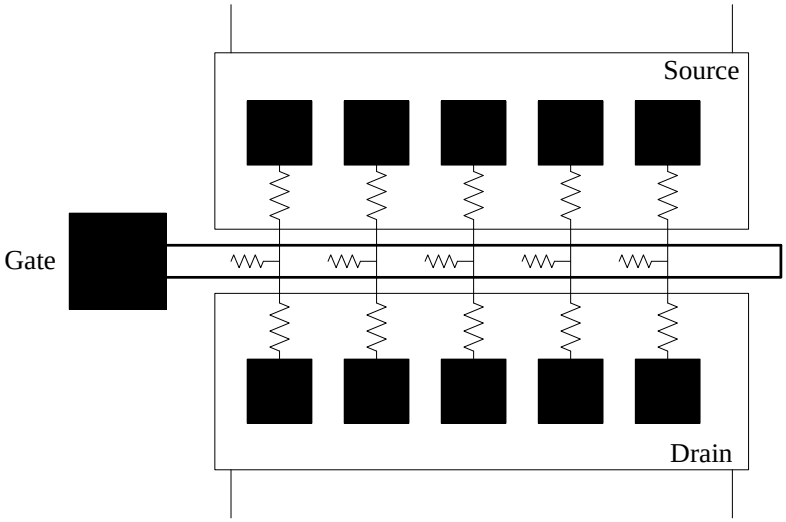


Fig. 2.7. Distributed resistances along the fingers in the physical structure of a MOSFET

Using the same approach, parasitic inductances can be defined; they are called L_g, L_d and L_s. But nowadays, for sub-micron MOSFETs, these inductances are usually a few pH and cannot be ignored at high frequency.

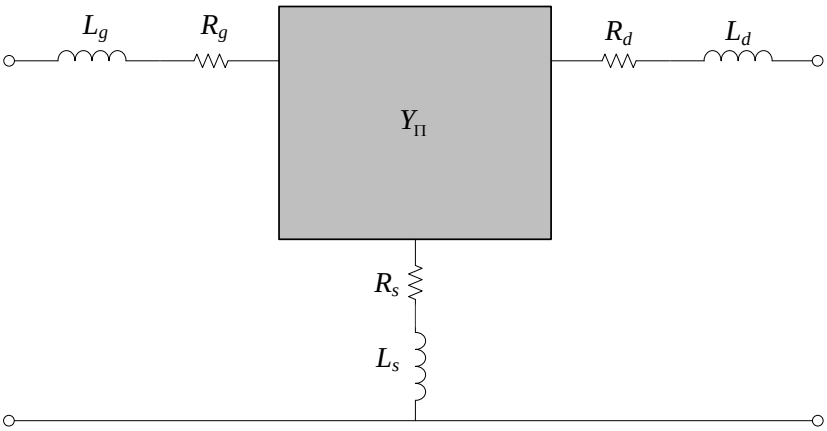


Fig. 2.8. Equivalent circuit of a MOSFET including parasitic extrinsic resistances and inductances

The equivalent circuit including these extrinsic elements is presented in Fig. 2.8. The Z-matrix of this circuit is defined by:

$$Z_\Sigma = Z_e + Y_\pi^{-1} \tag{2.11}$$

where

$$Z_e = \begin{bmatrix} R_g + R_s + j\omega\left(L_g + L_s\right) & R_s + j\omega L_g \\ R_s + j\omega L_g & R_d + R_s + j\omega\left(L_d + L_s\right) \end{bmatrix} \tag{2.12}$$

2.2.4.3 Extrinsic-Extrinsic Capacitances

Since the dimensions of MOSFETs are shrinking, some parasitic couplings, which were negligible for larger devices, cannot longer be neglected. Considering the structure of modern MOSFETs, Gaffioul et al. [Gaffioul-2000] proposed to model the coupling between metal lines outside the active zone by new capacitances. These capacitances (C_{gsee}, C_{gdee}, C_{dsee}) are connected directly between the three terminals of the previous equivalent circuit (Fig. 2.6). Since they are bias independent and proportional to the transistor width, they are called "extrinsic-extrinsic" and are denoted by the index "*ee*" (Fig. 2.9).

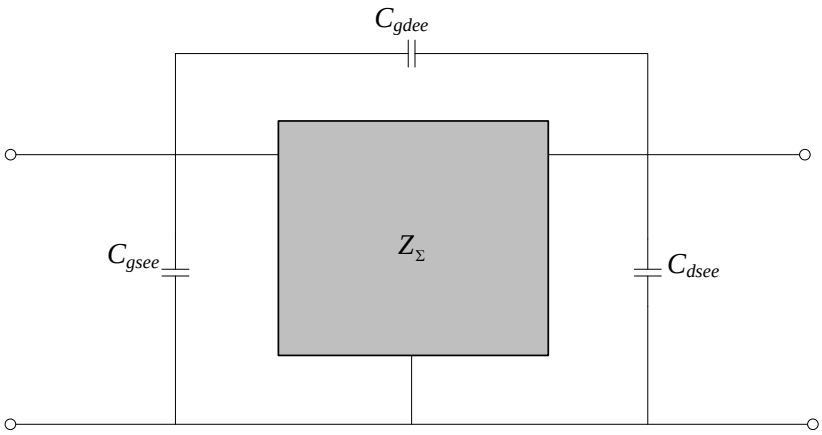


Fig. 2.9. Equivalent circuit of a MOSFET including all extrinsic parasitic elements.

The Y-matrix of the new circuit is defined by:

$$Y_{\Pi} = Z_{\Sigma}^{-1} + Y_{ee} \tag{2.13}$$

where

$$Y_{ee} = \begin{bmatrix} j\omega\left(C_{gdee} + C_{gsee}\right) & -j\omega C_{gdee} \\ -j\omega C_{gdee} & j\omega\left(C_{dsee} + C_{gsee}\right) \end{bmatrix} \tag{2.14}$$

The small signal modeling of a MOSFET transistor is based on the determination of all the components that form the equivalent circuit, which adequately adjust the S parameters of the measured transistor. This equivalent circuit is divided into two parts: the extrinsic part (associated to the parasitic elements assumed constant with respect to the applied voltage), and the intrinsic part (related to the operation principle of a MOSFET, which depends on the applied voltage). The most used circuit is the π equivalent circuit [Liechti-1976; Ladbrooke-1989] (Fig. 2.10).

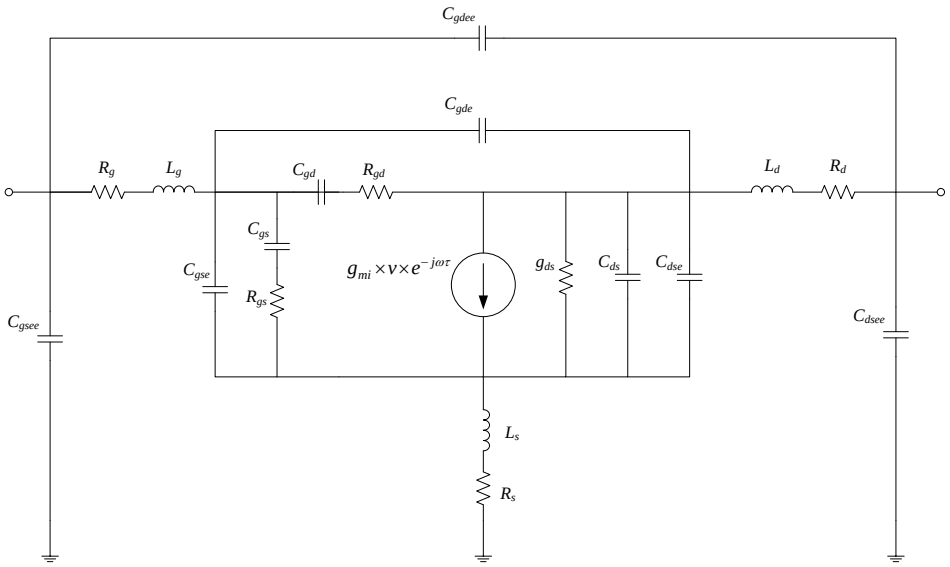


Fig. 2.10. Equivalent circuit for a FET transistor

The components of this equivalent circuit are described in Table. 2.1.

Extrinsic Components	C_{qsee}	Extrinsic-Extrinsic Gate-Source capacitance
	C_{qdee}	Extrinsic-Extrinsic Gate-Drain capacitance
	C_{dsee}	Extrinsic-Extrinsic Drain-Source capacitance
	L_q	Gate inductance
	L_d	Drain inductance
	L_s	Source inductance
	R_g	Gate resistance
	R_d	Drain resistance
	R_s	Source Resistance
	C_{qse}	Extrinsic Gate-Source capacitance
	C_{qde}	Extrinsic Gate-Drain capacitance
	C_{dse}	Extrinsic Drain-Source capacitance
Intrinsic Components	C_{qs}	Gate capacitance
	C_{qd}	Gate-Drain capacitance
	C_{ds}	Gate-Source capacitance
	R_{qs}	Channel resistance
	R_{ds}	Drain-Source resistance
	R_{qd}	Gate-Drain resistance
	g_{mi}	Transconductance
	τ	Delay time

Table 2.1. Basic components of the π equivalent circuit

Figure 2.11 presents the physical interpretation of the main components of the equivalent circuit. Two types of components can be observed: the parasitic components associated to the capacitances and inductances of the transmission lines and *pads*, as well as the intrinsic components. Among the extrinsic elements we can observe the access resistances associated to the ohmic losses between the contacts and the conduction channel. The modulation effect of the electrons in the channel is represented using a controlled current source. The gate capacitances C_{gs} and C_{gd} represent the capacitances associated to the depletion zone present under the gate. The resistance R_{gs} represents the channel resistance. The drain-source resistance models the conduction of the substrate. The delay τ is associated to the

electrons transit time in the channel. Occasionally, the capacitance C_{dc} is included in order to model the dipole generated at the end of the channel, and generally its value is very small. The capacitance C_{ds} is basically parasitic.

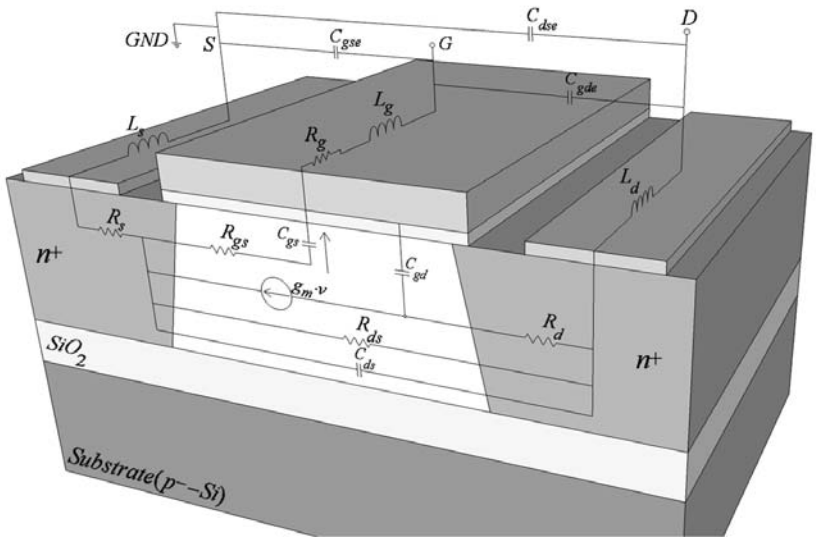


Fig. 2.11. Physical interpretation of the equivalent circuit of a MOSFET transistor

The equivalent circuit is justified using different physical models. In [Ladbrooke-1989] an equivalent circuit is obtained, which is a simplification of a *RC* line in the lineal region of the channel and modeling the saturation region through a controlled source. In [Roblin-1987] we find the expressions of the components starting from the wave equation, resulted from a combination of the charge control in HEMT transistors and the continuity equation, valid in the linear region. In [Danneville-1994] the components of the equivalent circuit are obtained from the analysis of a uniform active line.

Alternatively, in [Yeager-1986; Portilla-1994] a new equivalent circuit is presented (Fig. 2.12) for the intrinsic region, based on the concept of active transmission line in order to model the channel [Lazaro-1994]. The circuit includes two controlled sources to model the charge control in the two channel regions (weak and strong inversion). The main disadvantage of this circuit is the high number of components that make the parameter extraction more difficult [Lazaro-2007]. The main difference between the classical equivalent circuit – valid in the linear region and voltage saturation – and the new circuit is that the latter is valid in all regions of operation.

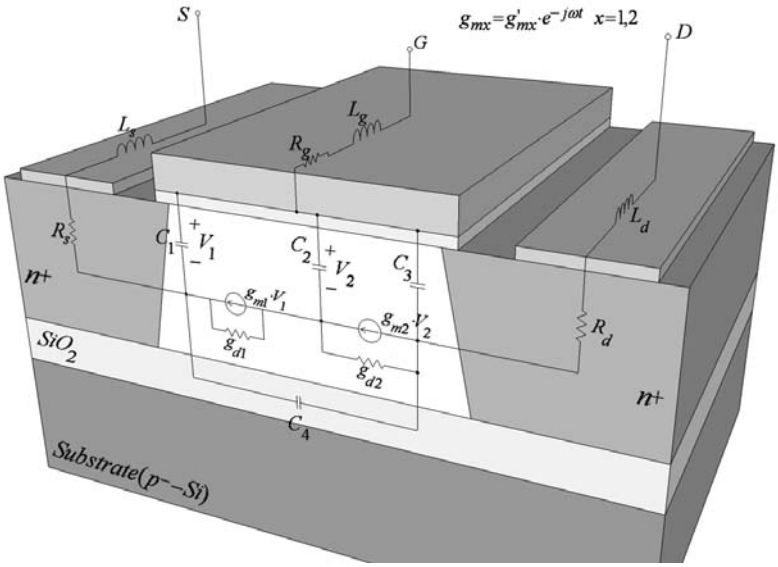


Fig. 2.12. Equivalent circuit of a MOSFET transistor in the active transmission line

Noise temperatures are associated to the transconductances g_{d1} and g_{d2}, which are of the order of the electronic temperature in each channel section, and in

principle, the noise sources can be considered uncorrelated and independent of the frequency, simplifying the noise characterization of the FET.

2.2.4.4 Access parameters

The equivalent circuit would not be complete without defining the access parameters, which add to the parasitic effects on the device. Depending on the device size and the measurement method, the reference planes after the calibration might not be located at the edge of the active zone. Thus metal interconnections remain at the input and at the output of the transistor, which were not canceled by the calibration. Also, when large devices are measured, the ground planes of the coplanar waveguide (CPW) line around the transistor are cut. Several parasitic are then introduced, and are independent of the transistor dimensions.

The parasitic effects of metallic interconnections are usually modeled by inductances and capacitances. These elements are considered lossless because their losses are negligible compared to those introduced by the extrinsic resistances in SOI technologies. Since they are bias dependent and not directly proportional to the device width, these elements are called “access” and are denoted by an index “*a*”. Figure 2.13 presents the final circuit embedded in a CPW line.

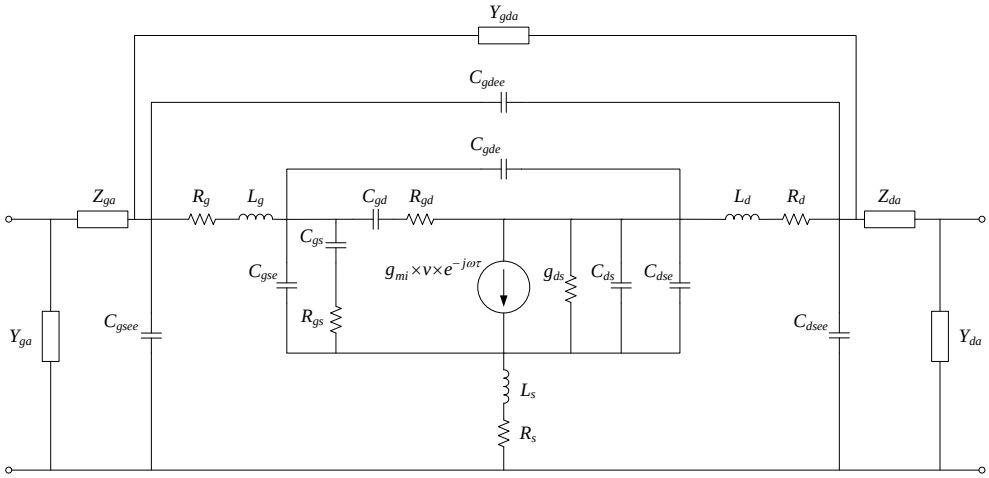


Fig. 2.13. General equivalent circuit of an integrated MOSFET embedded in a CPW line

2.3 Figures of merit for RF applications

Usually, the performances of RF transistors are evaluated using different definitions of gain, ROLLET´s factor, which is the condition of inherent stability, and some characteristic parameters related to the equivalent noise sources of the device.

The transducer gain (G_t) of a transistor is defined as the ratio between the power delivered to the load and the available input power. The transducer gain is equal to $\left|S_{21}^2\right|$ and can be deduced directly from the measurement. This gain is not a relevant figure of merit of a MOSFET transistor. Indeed, the reference impedance of a measured *S-parameters* being usually 50Ω, the transistor is far from conjugate matching condition. Thus, the transducer gain is extremely low.

The current gain, currently used at lower frequencies, is given by:

$$|H_{21}| = \frac{|Y_{21}|}{|Y_{11}|} \tag{2.15}$$

with $Y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0}$ and $Y_{21} = \left.\frac{i_2}{v_1}\right|_{v_2=0}$. It can also be expressed as a function of the scattering parameters:

$$|H_{21}| = \left|\frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}\right| \tag{2.16}$$

This current gain has some interesting properties as it is mainly independent of the extrinsic resistance of the MOSFET. But, as for the transducer gain, it imposes specific conditions at the transistor accesses (a short circuit at the output). These conditions are not optimal to extract the maximum of power from the device.

The voltage gain can also be defined (Y_{21}/Y_{22}), but it is not often used.

A more interesting definition of gain would be the *Gain figure* defined by Bodway in [Bodway-1967]. It is defined as the ratio between the forward (from gate to drain) and reverse (from drain to gate) transducer gain and it is given by:

$$GF = \frac{|S_{21}|^2}{|S_{12}|^2} \tag{2.17}$$

This definition is invariant to changes in generator and load impedances. It gives information on the ability of the device to provide power to a load. Indeed, when the device is not able to provide power, it behaves as a passive, and reciprocal, device. Thus, $S_{21}=S_{12}$ and the *GF* is equal to 1. Unfortunately, this definition of gain does not care about the stability of the device. The inherent stability of transistors is evaluated by the ROLLET´s factor, defined by:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta_s|^2}{2|S_{12}S_{21}|} \tag{2.18}$$

where $\Delta_s = S_{11}S_{22} - S_{12}S_{21}$.

If $|\Delta_s| < 1$, and *K>1* the device is unconditionally stable, which means that whatever the passive load impedance at and access, the real part of the input impedance at the other access will never be negative. If $|\Delta_s| < 1$, and *K<1*, the device is potentially unstable. That means that specific passive load impedances can make the device unstable. It is then useful to determine approximately these impedances, and to avoid using them, in order to ensure stability.

Now that the stability factor has been defined, the maximum available gain for a stable device (*MAG*) can be defined:

$$MAG = \left|\frac{S_{21}}{S_{12}}\right|^2 \left(K - \sqrt{K^2 - 1}\right) \tag{2.19}$$

This relation is very similar to the gain figure defined before, but with the introduction of a correcting factor, related to the stability of the device. When the device is conditionally unstable, this gain does not exist, because *K<1*.

Another definition has been proposed by Mason [Mason-1954]. The unilateral gain (*ULG*) is the maximal available gain of a device when the stability is ensured by using a lossless feedback network to cancel the reverse transmission of the device ($S_{12}=0$). This gain is defined by:

$$ULG = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{K\left|\frac{S_{21}}{S_{12}}\right| - \Re\left(\frac{S_{21}}{S_{12}}\right)} \tag{2.20}$$

2.4 Cut-off frequencies

Based on the different gains, it is possible to define several cut-off frequencies, as the frequency for which a gain becomes equal to unity, or 0 dB. The most used ones are:

f_T: It is defined as cut-off frequency of the current gain H_{21}. It can be approximated for a MOSFET, considering the equivalent circuit from Fig. 2.14, by the following relation:

$$f_T \approx \frac{g_{mi}}{2\pi C_{gg}} \tag{2.21}$$

where C_{gg} is the total gate capacitance of a MOSFET (C_{gg}=C_{gs}+C_{gd}). It is an important coefficient to compare different technologies and devices.

f_c: When the equivalent circuit of a MOSFET is known, another cut-off frequency is sometimes used to describe the intrinsic performances of MOSFETs.

$$f_c = \frac{g_{mi}}{2\pi C_{gs}} \tag{2.22}$$

f_c is equal to the classical cut-off frequency (f_T) when the capacitance C_{gd} is small compared to C_{gs}. It is not the case for deep sub-micron MOSFET [Dambrinne-2003].

f_{max}: It is the highest frequency where the device is able to provide power when it is in a stable state. As for f_T, it is possible to develop a simplified expression of f_{max} based on the equivalent circuit of Fig. 2.14. Sze [Sze-1981] provides the following relation:

$$f_{\max} = \frac{f_T}{2\sqrt{2\pi f_T R_g C_{gd} + g_d\left(R_g + R_s + R_{gs_i}\right)}} \tag{2.23}$$

f_{max} is sensitive to the width of the gate, and to all the parasitic which surround the transistor.

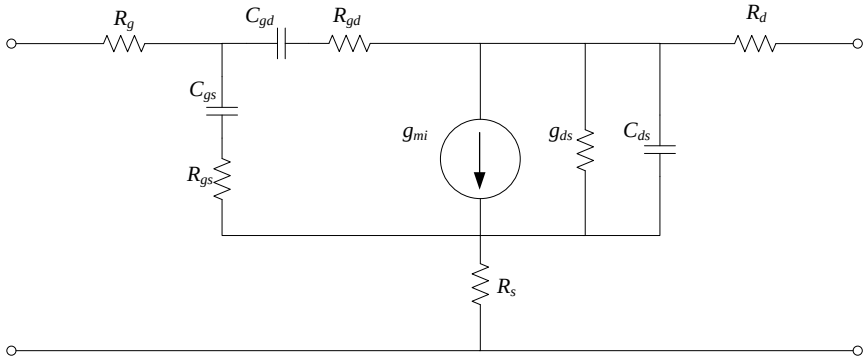


Fig. 2.14. Simple small signal equivalent circuit of a MOSFET

The frequencies f_T and f_{max} are directly extracted from S-parameter measurements as the cut-off frequencies of H_{21} and *MAG* respectively. For transistors having a cut-off frequency higher than the measurements frequency band, f_T and f_{max} can be evaluated by (2.21) and (2.23).

2.5 Noise Modeling

2.5.1 Noise in two-ports

The noise is an unwanted fluctuation that, when added to a signal, reduces its information content. In a communication system, noise can be classified into two broad categories, depending on its source. Noise generated by components within a communication system, such as resistors, solid-state active devices etc. is referred to as *internal noise* (or *electronic noise*). The second category, *the external noise*, results from sources outside a communication system, including atmospheric, man-made and extraterrestrial sources [Chen-1997]. The focus of this research is the electronic noise, which defines the performances of the MOSFET devices under scrutiny.

The electronic noise in a communication system defines the lowest limit of a signal that can be detected. Below this limit, the signal would be “drowned” by the background noise. Therefore, the electronic noise directly affects the accuracy of measurements and the minimum power of a signal that can be used in a circuit to transmit information.

When working at high frequencies, the effect of the noise generated within the device itself plays an increasingly important role in the overall system sensitivity characteristics, dynamic range and signal-to-noise ratio. Due to the rather long turnaround time and expensive cost of actual fabrication of analog circuits, noise simulation of an analog circuit using Computer Aided Design (CAD) tools is a realistic alternative to determine whether the overall noise performance of a circuit would be good enough to allow that circuit to function properly. In order to perform accurate noise simulations, an appropriate physically-based noise model that can predict accurately the noise performance of MOSFET transistors over a wide range of operating conditions of frequencies, currents and device geometries is needed. To this end, this research presents a noise model that includes all the high-frequency noise sources and their correlations and applies this model on several Multiple-Gates MOSFET transistors architectures.

The circuit theory of linear noisy networks shows that any noisy two-port can be replaced by a noise equivalent circuit which consists of the original two-port (now assumed to be noiseless) and two additional noise sources [Hillbrand-1976; Dobrowolski-1991] (Fig. 2.15). In general, six different representations or forms of noise equivalent circuits exists depending upon the type of the additional noise source and their arrangement relative to the noise-less two-port. The most used representations are the admittance, impedance and chain representations. The admittance representation uses two current noise sources i_1, i_2. The impedance is the dual case and it uses two voltage noise sources, u_1 and u_2. Finally, the chain representation uses a input series voltage source u and a parallel current source, i (Fig. 2.15).

A physically significant description of these sources is given by the self- and cross-power spectral densities which are defined as the Fourier transform of

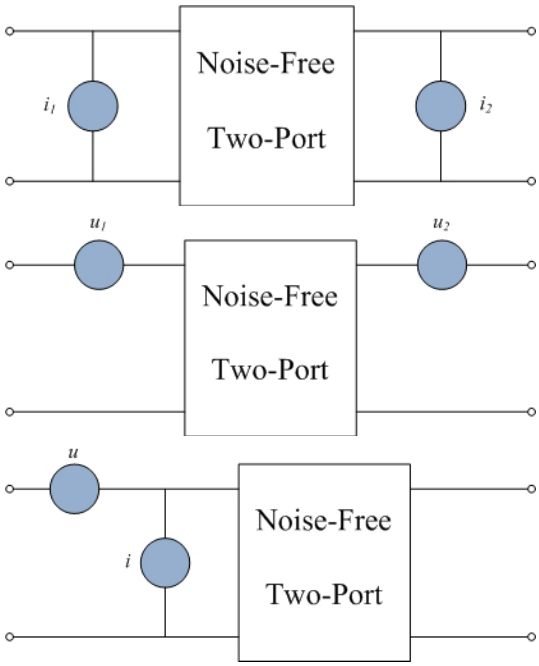


Fig. 2.15. Different representations of noisy two-port networks: admittance representation (a), impedance representation (b) and chain representation (c)

their autocorrelation and cross correlation functions. Arranging these spectral densities in matrix form leads to the so-called correlation matrices. For two noise source s_1 and s_2, the correlation matrix C belonging to the noise source s_1 and s_2 can be written as:

$$C = \overline{\begin{bmatrix} s_1 \\ s_2 \end{bmatrix} \cdot \begin{bmatrix} s_1 \\ s_2 \end{bmatrix}^{\dagger}} = \begin{bmatrix} \overline{s_1^2} & \overline{s_1 s_2^*} \\ \overline{s_2^* s_1} & \overline{s_2^2} \end{bmatrix} \tag{2.24}$$

where † denotes the transpose conjugate operator. It is easy to transform the noise correlation matrix given by a representation to other noise source representation

using the concept of transformation matrix. If two noise source s_1 and s_2 are linearly transformed to other noise sources s_1', and s_2',

$$\begin{bmatrix} s_1' \\ s_2' \end{bmatrix} = T \begin{bmatrix} s_1 \\ s_2 \end{bmatrix} \tag{2.25}$$

then the associated correlation matrix is given by:

$$C' = T \cdot C \cdot T^{\dagger} \tag{2.26}$$

A set of transformation matrices covering all possible transformations between the impedance, admittance, and chain representations is given in Table 2.2.

	Original representation		
Resulting representation	Admittance	Impedance	Chain
Admittance	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$	$\begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix}$
Impedance	$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & -Z_{11} \\ 0 & -Z_{21} \end{bmatrix}$
Chain	$\begin{bmatrix} 0 & A_{12} \\ 1 & A_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & -A_{11} \\ 0 & -A_{21} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$

Table 2.2. Transformation matrix between correlation matrix representations

The interconnection of noisy two-ports is also formulated by means of operations with correlation matrices. The resulting correlation matrices for series, shunt or cascade interconnections are given by:

$$C_Z = C_{Z_1} + C_{Z_2} \quad \textit{(series)} \tag{2.27}$$

$$C_Y = C_{Y_1} + C_{Y_2} \quad \textit{(shunt)} \tag{2.28}$$

$$C_A = C_{A_1} + A_1 \cdot C_{A_2} \cdot A_2^{\dagger} \quad \textit{(cascade)} \tag{2.29}$$

where the subscripts *1* and *2* refer to the two-ports to be connected.

An important case is the passive two-port with thermal noise. In this case, the admittance and impedance correlation matrices could be obtained from admittance and impedance matrices and the physical temperature *T*.

$$C_Z = 4kT\,\mathrm{Re}\left(Z\right) \tag{2.30}$$

$$C_Y = 4kT\,\mathrm{Re}\left(Y\right) \tag{2.31}$$

where *k* is the Boltzmann constant ($k \approx 1.38 \cdot 10^{-23}$ *J/K*).

However, RF designers use the noise figure to characterize noisy circuits. The noise factor is a figure of merit for the performance of a device or a circuit with respect to noise. The noise factor of a two-port is defined as:

$$F = \frac{N_o}{N_{o,ideal}} = \left.\frac{\left(S/N\right)_{input}}{\left(S/N\right)_{output}}\right|_{T=T_0} \tag{2.32}$$

where N_o is the actual noise power at the output of the two-port and $N_{o,ideal}$ is the expected noise power at the output of the ideal (noiseless) two-port at reference temperature ($T=T_0$=290K). The noise factor could also be interpreted as a degradation of the signal to noise ratio (*S/N*) at T_0. The noise figure is the noise

factor expressed in decibels (*NF=10log F*). One more related figure of merit is the equivalent noise temperature, often used by antenna designers:

$$T_e = T_0 \left(F - 1 \right) \tag{2.33}$$

The total noise power at the output is highly dependent on the source impedance of the two-port. A unique optimum source impedance (Z_{opt}) exists, that leads to the best noise performance. The noise factor measured with the source set to Z_{opt} is called F_{min} (or NF_{min} when converted to decibels). Z_{opt} is frequently converted to the optimum noise reflection coefficient, called Γ_{opt}. A third noise parameter called equivalent noise resistance, R_n, is the sensitivity factor; it shows how fast *NF* increases as the source termination changes from Γ_{opt}. At a specific set of operating conditions, the three noise parameters (F_{min}, Γ_{opt}, and R_n) can fully characterize the noise performance of a given two-port. Changing the temperature, frequency, and the dc bias conditions of the active device also change the noise parameters. The noise figure of a two-port network is given by:

$$F\left(\Gamma_s\right) = F_{\min} + \frac{4R_n}{Z_0} \frac{\left|\Gamma_s - \Gamma_{opt}\right|^2}{\left|1+\Gamma_{opt}\right|^2 \left(1-\left|\Gamma_s\right|^2\right)} \tag{2.34}$$

where Z_0 is the reference impedance (often Z_0=50Ω) and Γ_s is the source reflection coefficient.

Having the noise chain correlation matrix C_A, one can easily compute the noise parameters [Hillbrand-1976]:

$$F_{\min} = 1 + \frac{C_{A21} + C_{A11} Y_{opt}^*}{2kT_0\Delta f} \tag{2.35}$$

$$R_n = \frac{C_{A11}}{4kT_0\Delta f} \tag{2.36}$$

$$Y_{opt} = \sqrt{\frac{C_{A22}}{C_{A11}} - \left(\mathrm{Im}\left(\frac{C_{A21}}{C_{A11}} \right) \right)^2} - j\,\mathrm{Im}\left(\frac{C_{A21}}{C_{A11}} \right) \tag{2.37}$$

where Δf is the frequency bandwidth centered on frequency f.

The optimum reflection coefficient Γ_{opt} is not a function of the small-signal S-parameters. For optimum noise performance, the source reflection coefficient is not matched to the input - it is transformed to Γ_{opt}. Since the input port is not conjugate-matched, in low-noise amplifiers we do not get the maximum gain of the two-port. Reactively matching or mismatching the output port does not have any effect on the signal-to-noise ratio and noise figure. Output matching, of course, provides more gain, which helps to reduce the noise contribution of the next stage. In multistage low-noise amplifiers, the goal is to minimize the overall noise performance. Ideally, all stages should see their optimum noise sources at their inputs, but that may not lead to minimum overall noise. Constant noise figure circles and available power gain circles are often used in low noise amplifier design [Gonzales-1984]. Circuit optimization is very helpful here to target minimum noise, flat gain response, and good output match simultaneously.

2.5.2 Noise sources modeling

Figure 2.16 shows the small signal equivalent circuit for a FET. Several noise sources must be considered. The first one is the thermal noise due to parasitic access resistances R_g, R_s and R_d. The other noise sources arise from intrinsic transistor. The intrinsic contribution is modeled using two correlated current noise sources, i_g, and i_d (admittance representation [Hillbrand-1976;Dobrowolski-1991]).

They include the effect of the diffusion noise and flicker noise in the channel, induced gate noise and shot noise. In principle, the flicker noise [Celik-Butler-2006; Min-2004; Simoen-2004; Morshed-2008; Ghibaudo-2006] is a low-frequency noise and it mainly affects the low frequency performance of the device, so it can be ignored at very high frequency. However, the contribution of flicker noise should be considered in designing some RF circuits such as mixers, oscillators, or frequency dividers.

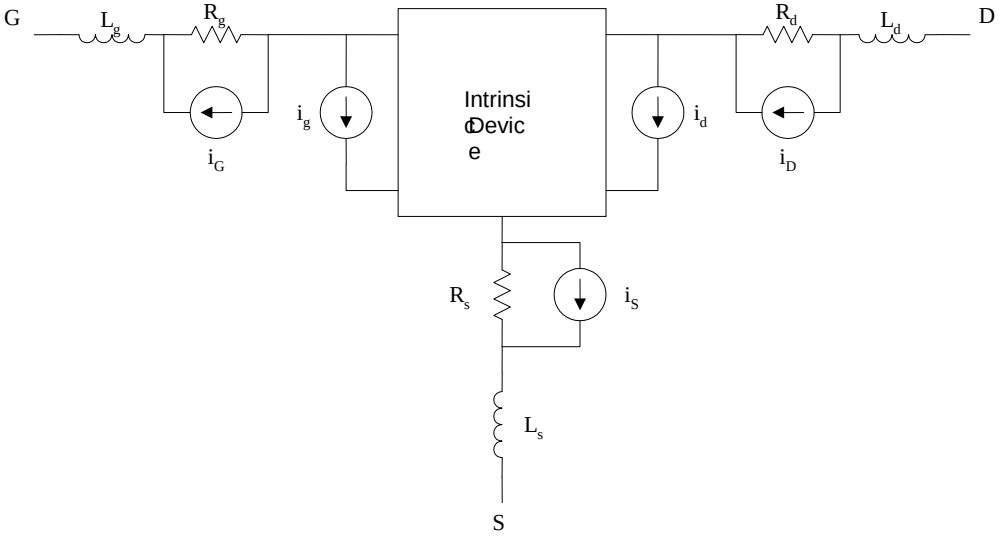


Fig. 2.16. An equivalent circuit to illustrate the noise sources in a SOI MOSFET. i_G, i_S, and i_D are the noise contribution by the terminal resistance at gate, source and drain, i_d is the noise contribution of the channel, including the flicker noise portion, and i_g is the induced gate noise including the shot noise portion. In general i_g and i_d are correlated.

The channel resistance and all terminal resistances contribute to the thermal noise at high frequency (HF), but typically channel resistance dominates in the contributions of the thermal noise from the resistances in the device. Induced gate noise is generated by the capacitive coupling of local noise sources within the channel to the gate, and usually it plays a more important role as the operation frequency goes much higher than the frequency at which channel thermal noise dominates. With the decrease of the oxide thickness due to gate downscaling, the DC tunneling Gate Current (*TGC*) flowing through the oxide in the gate is increasing. This gate current produces an increase of noise due to the shot noise current.

2.5.2.1 Flicker noise

Noise at low frequencies in a MOSFET is dominated by flicker noise. Measurements generally show a spectral density of the input (gate) referred voltage noise, which is roughly inversely proportional to frequency. Therefore, flicker noise is also called *1/f* noise. Much effort has been made in understanding the physical origin of flicker noise. However, the physical mechanism is still not very clear so far.

The exact mechanism is still under discussion; however, basically, there are two different theories to explain the physical origins of the flicker noise. In the carrier number fluctuation theory [Jindal-1978], originally proposed by Mc-Whorter [McWhorter-1957], the flicker noise is due to the random trapping and detrapping processes of charge in the oxide traps near the $Si\text{-}SiO_2$ interface. The charge fluctuation results in fluctuations of the surface potential, which modulates

the channel carrier density. For a uniform oxide trap distribution in the energy gap, the theory predicts an input referred noise density independent of the gate bias voltage and inversely proportional to the square of the gate capacitance, C_{ox}. The mobility fluctuation theory [Jindal-1978; Hooge-1969], considers the flicker noise as a result of the fluctuation in bulk mobility based on Hooge's empirical relation for the spectral density of flicker noise in a homogeneous sample. In the Hooge model [Hooge-1969], the drain current noise results from the fluctuations of the carrier mobility through variations in the scattering cross-section entering the collision probability likely due to phonon number fluctuations [Jindal-1981]. This leads to a flicker noise with amplitude inversely proportional to the total number of carriers in the device. This theory predicts an input referred noise voltage increasing with gate bias voltage and inversely proportional to the gate capacitance. Recently, a new model was presented, namely the *Correlated carrier and mobility fluctuation model* [Hung-1990; Hung2-1990]. It is a unified model proposed by Hung et al. [Hung-1990], with a functional form resembling the number fluctuation model at low bias and the mobility fluctuation model at high bias. The Unified Model shows a better agreement with the experimental data for both the *n* and *p* type devices over a considerable temperature range and thus it has become the most successful theory adopted for low frequency noise modeling and analysis.

According to Ghibaudo et al. [Ghibaudo-1991; Ghibaudo-2002], if the low frequency noise mechanism is correlated number and mobility fluctuations, S_{i_d} / I_D^2 shows a dependence on $\left(g_m / I_D\right)^2$ following the relation:

$$\frac{S_{i_d}}{I_D^2} = \left(1 + \frac{\alpha \mu_{eff} C_{ox} I_D}{g_m}\right)^2 \left(\frac{g_m}{I_D}\right)^2 \frac{K_F}{WLC_{ox}^2 f^{\gamma}} \tag{2.38}$$

where f is the frequency, γ is the characteristic exponent close to 1 [Ziel-1979], g_m is the transconductance (for convenience, and to be in accord with the accepted notation in the literature, we will use g_m instead of g_{mi} from this point on), μ_{eff} is the effective mobility, α is the Coulomb scattering coefficient ($\approx 10^4$ Vs/C for electrons and 10^5 Vs/C for holes), W is the device width, and L is the device length.

The spectral density of the oxide interface charge depends in essence on the physical trapping mechanisms into the oxide. For a tunneling process, the trapping probability decreases exponentially with oxide depth, such that the constant K_F is given by:

$$K_F = q^2 kT \lambda N_t \tag{2.39}$$

where N_t is the volumetric oxide trap density (eV/m^3), λ is the tunnel attenuation distance (about 0.1 nm) given by WKB theory as:

$$\lambda = \frac{h}{4\pi\sqrt{2m^* \Phi_B}} \tag{2.40}$$

where h is Planck's constant, m^* the electron effective mass in the dielectric and $\Phi_B(V)$ the barrier height [Christensson-1968].

For a thermally activated trapping process [Surya-1988], the trapping probability decreases exponentially with the cross-section activation energy E_a, such that the constant K_F is given by:

$$K_F = \frac{kTN_{it}}{\Delta E_a} \tag{2.41}$$

where ΔE_a is the amplitude of the activation energy dispersion and N_{it} is the oxide trap surface state density (eV/m^2).

Whereas, if the dominant mechanism is Hooge's bulk mobility fluctuations model [Jindal-1981], S_{i_d} / I_D^2 shows a dependence on I_D^{-1} following the relation:

$$\frac{S_{i_d}}{I_D^2} = q^2 \alpha_H < \mu_{eff} > \frac{V_D}{L^2 I_D f} \tag{2.42}$$

where α_H is the Hooge parameter (10^{-4}–10^{-6}) and $<\mu_{eff}>$ is the average mobility along the channel.

For low drain voltages, the gate-leakage current is not negligible and is larger than the measured drain current [Morshed-2008]. The low frequency noise parameters have been extracted after correcting the drain current for the gate-leakage current with the simple following expression:

$$I_{D0} = I_D + \alpha_D I_G = I_S - \alpha_G I_G \tag{2.43}$$

where I_{DO} is the intrinsic drain current, I_D the measured drain current, I_S the measured source current, I_G the gate leakage current, α_D the gate-partitioning coefficient at the drain side, and α_S the gate-partitioning coefficient at the source side. The α_D coefficient is evaluated at $V_{DS}=0$ in strong inversion regime and is equal to 25%.

Measurements of devices from many different CMOS processes with oxide thickness between 10 and 80 nm suggest that nMOS transistors behave as predicted by the number fluctuation model [Vandamme-1994; Vandamme-2000]. However, noise measurements of newer deep submicron transistors present a much less consistent picture. For instance, nMOS transistors also may show bias dependence, while pMOS transistors may have a noise corner frequency comparable to nMOS transistors. Also, the experimental results show a $1/f^n$ spectrum and n is not always 1 but in the range of 0.7 to 1.2. Some experimental results even show that n

decreases with increasing gate bias in p-channel MOSFETs. Modified charge density fluctuation theories have been proposed to explain these experimental results. The spatial distribution of the active traps in the oxide is assumed to be nonuniform to explain the technology and the gate-bias dependence of *n* [Hung-1986].

ITRS requirements dictate smaller device dimensions with ever-thinning gate oxide, which in turn leads to high gate leakage current in ultra thin MOSFET devices. In order to minimize this high leakage current, the semiconductor industry is going through an extensive search to investigate the feasibility of using high-dielectric constant (*high-κ*) compounds as the gate dielectric material [Wilk-2001]. However, introduction of these materials in place of conventional SiO_2 affects some of the fundamental device parameters, of which the carrier mobility degradation [Wilk-2001] and the low frequency noise behavior are of particular interest [Celik-Butler-2006; Min-2004; Simoen-2004]. Although the *Unified Model* is the most successful low frequency noise model for the native-oxide MOSFETs, the extracted parameter values using this model show noticeable discrepancies when applied to devices using stacked *high-κ* materials as the gate dielectric. A significant dependence on the interfacial layer thickness (IL) was observed in the extracted trap density values by different research groups, although IL thickness is not a model parameter in the original *Unified Model* [Hung2-1990; Ghibaudo-1991]. Growth process of SiO_2 has matured over decades, resulting in low carrier trap densities and consequently low noise. Unlike SiO_2, *high-κ* material processing is still in research stage, with atomic layer deposition (ALD) being the most promising process technology [Quevedo-Lopez-2005]. The estimated dielectric trap density by different research groups is believed to represent an average value, as they appear to be dependent on the IL thickness as well as the process technology. Moreover, discrepancies in the reported average trap density values have been noted, even for the same *high-κ* material [Celik-Butler-2006]. This

disagreement in trap density extracted using the original *Unified Model*, may be attributed to the fact that the original model accounts for only the noise contribution from a single dielectric layer but not from the *high-κ* layer, as this layer is absent in the conventional native-oxide devices. Figure 2.17 shows contributions from the interfacial layer and the *high-κ* layer in the total drain spectral noise density [Morshed-2008].

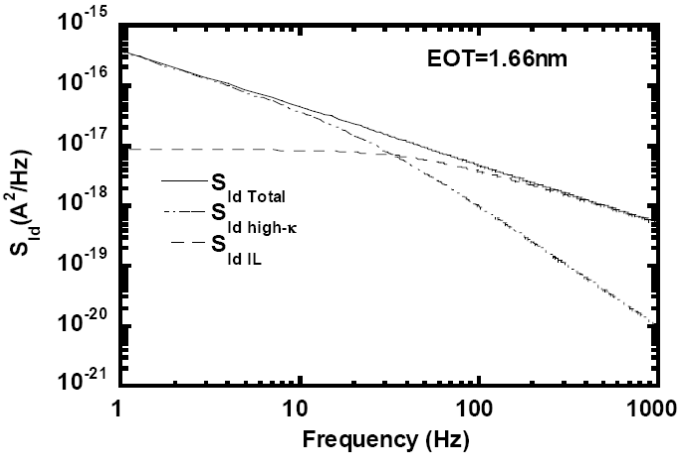


Fig. 2.17. Contributions from the interfacial layer and the *high-κ* layer in the total S_{id} (A2/Hz) for devices with *TIL*=1.8nm [Morshed-2008].

For typical IL trap density (~10^{16} $cm^{-3}eV^{-1}$), the noise contribution from IL falls more than 2 orders of magnitude below the total noise in the 1-100 Hz frequency range. Traps further away from the semiconductor interface contribute noise to the lower end of the frequency spectrum, while traps at the interface are fast-states and contribute fluctuations to the higher frequencies. Consequently, as the IL gets thicker, the noise contribution from the *high-κ* layer increasingly shifts

to the lower frequency range and at the same time higher frequency components get weaker since the noise contribution from the IL is relatively low. In [Ghibaudo-2006], the low frequency noise in both SOI and bulk devices has been investigated. Figure 2.18 shows the normalized drain current noise spectral density S_{id} / I_D^2 of a *W/L*=10/0.05μm DG N-MOSFET at V_{DS}=10mV and *f*=10Hz for different back-gate voltages. In PD, FD and Double-gate SOI MOSFETs the noise source was attributed to carrier number fluctuations, while in advanced bulk CMOS technologies the LF noise stems from carrier and correlated mobility fluctuations [Ghibaudo-2006]. No degradation of gate oxide quality as measured by oxide density of traps N_t was observed despite the ultra thin dielectric used.

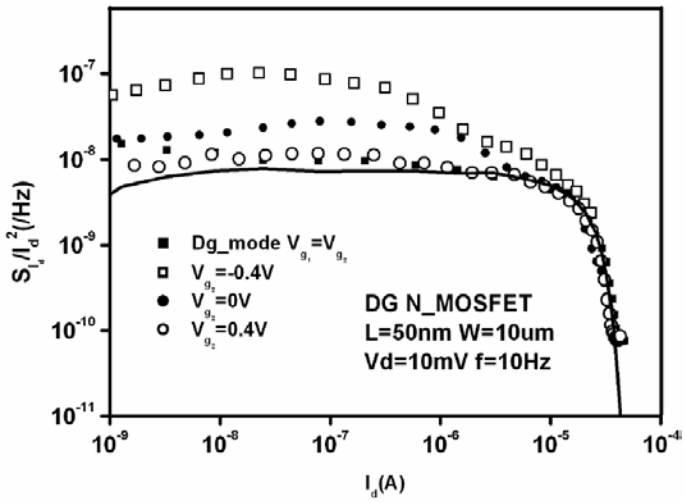


Fig. 2.18. Normalized drain current noise spectral density S_{id} / I_D^2 of a *W/L*=10/0.05μm DG N-MOSFET at V_{DS}=10mV and *f*=10Hz for different back-gate voltages. Solid line: $S_{V_{GS}} \times \left(g_m / I_D \right)^2$ for double-gate mode [Ghibaudo-2006].

2.5.2.2 Thermal noise

At high frequency, the MOS transistor noise is mainly dominated by thermal noise (also called Johnson noise or Nyquist Noise) coming from the channel [Ziel-1986]. The term thermal is due to the origin of this noise, which can be traced to the random thermal motion of carriers in the channel. Accurate noise modeling is a prerequisite for the application of advanced CMOS technologies to low noise RF design.

Let us consider a nonuniform channel as Fig. 2.19. In the segmentation method or active transmission line analysis, the channel is divided in channel sections or slices. The small-signal and noise source for each channel section can be derived from semiconductor equations. This method was used for noise modeling in other devices such as MESFETs [Cappy-1989], HEMTs [Shaeffer-1977; Lazaro-2003], MOSFET and SG SOI [Lazaro-2006; Pailloncy-2004], DG MOSFETs [Lazaro-2006; Lazaro2-2006], GAA [Iniguez-2006; Lazaro-2008] and FinFETs [Lazaro2-2008]. The application of this analysis method will be used to describe small-signal and noise equivalent circuit. Although this analysis could be done using standard circuit analysis techniques implemented in standard microwave circuit simulators, it could be time consuming due the large number of circuit elements to be analyzed. However, compact explicit expressions for the spectral noise densities are preferred for implementation in commercial circuit simulators.

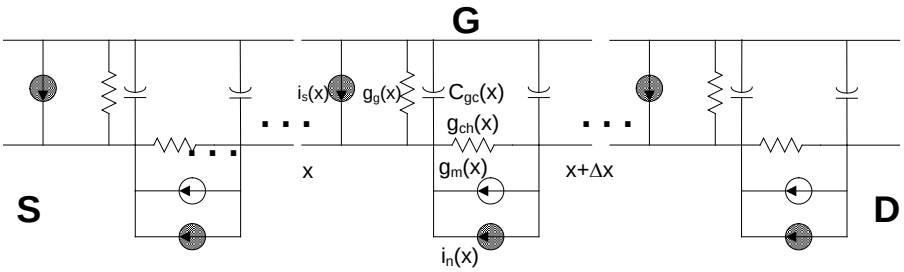


Fig. 2.19. Small-signal and noise equivalent circuit for a channel slice between x and $x+\Delta x$. An equivalent noise source $i_n(x)$ has been introduced to model the channel noise.

For the compact modeling of noise, three methods are usually applied: 1) an equivalent circuit approach, 2) the impedance field method, or 3) the Langevin or Klaasen-Prins method. These three methods have been proven to be equivalent by Roy et al. [Roy-2006], and the same final expression for the spectral densisties and correlation matrix elements were obtained. This research is based on the equivalent circuit approach, which is presented in detail in Annex II.

The local equivalent circuit (Fig. 2.19) is composed of the channel capacitance, the transconductance, and the channel resistance (or conductance). Diffusion noise and gate shot noise can be incorporated to the model. The local equivalent circuit elements could be obtained from linearization of the current at any channel position x and the current continuity equation:

$$I(x) = g\left(V, \frac{dV}{dx}\right) \cdot \frac{dV}{dx} \tag{2.44}$$

where $g=W\mu Q$ is the channel conductance per unit length, and W, μ, Q are the width, mobility and inversion charge density. The mobility depends on the electric field $E=-dV/dx$, so g depends on the channel potential $V(x)$ and the dV/dx.

The local equivalent circuit elements for a channel slice between x and $x+\Delta x$ are:

$$C_{gc}(x) = W\Delta x \frac{dQ}{dV_{GC}} \tag{2.45}$$

$$g_m(x) = W\Delta x \frac{dQ}{dV_{GC}} v(x) \tag{2.46}$$

$$g_{ch}(x) = \frac{g(x) + g'(x)E(x)}{\Delta x} \tag{2.47}$$

where $V_{GC}(x)=V_G-V(x)$ is the gate to channel potential and $g'=dg/dE=WQ\cdot d\mu/dE$.

For high frequency noise analysis, channel diffusion noise source and gate shot noise for each slice are introduced. The modeling of the channel thermal noise of a MOSFET has been an active area of research in recent years [Deen-2006; Chen-2002; Han-2004; Scholten-2003; Roy-2005]. The method to calculate the local noise source due to the carrier fluctuation caused by the diffusion noise in nonequilibrium is to introduce an Einstein's like relationship between the differential mobility and diffusion coefficient [Lazaro2-2006]:

$$D = \frac{kT_n}{q}\mu_d \tag{2.48}$$

where D is the nonequilibrium diffusivity, T_n is the noise temperature and μ_d is the differential mobility ($\mu_d=dv/dE$). For the typical inversion carrier density in the inversion layer, we can consider that the channel is not degenerated, and the velocity distribution is heated Maxwellian [Roy-2005; Nougier-1977; Baker-1980; Seeger-1973]. Under this assumption the noise temperature T_n becomes equal to the carrier temperature T_e, and the spectral current density can be written as [Roy-2005]:

$$S_{i_n} = \overline{i_n^2} = 4qQ(x)D(E)\frac{W}{\Delta x} = 4kT_n g_{ch}(x) = 4kT_e g_{ch}(x) \tag{2.49}$$

Under high channel electric fields, the temperature of electrons in the channel can rise above that of the lattice. This effect can increase the thermal noise of the device [Chen-2002]. However, in the drift-diffusion models an analytical relationship between T_e and the lateral field *E(x)* must be used. One of the more challenging aspects of including the effect of electron temperature in the noise model is finding a good model for the electron temperature. A prevalent model in the literature expresses the electron mobility as a function of the temperature as shown below [Roy-2006]:

$$\mu = \mu_0 \sqrt{\frac{T_L}{T_e}} \tag{2.50}$$

Mobility can also be represented as a function of electric field [Roy-2006]:

$$\mu = \frac{\mu_0}{\left(1 + \left(\frac{E}{E_{sat}}\right)^p\right)^{1/p}} \tag{2.51}$$

Equating (2.50) and (2.51), and solving for T_e/T_L gives:

$$T_e = T_L \left(1 + \left(\frac{E}{E_{sat}}\right)^p\right)^{2/p} \tag{2.52}$$

For p=1 and p=2, eq. (2.52) shows that electronic temperature has a quadratic dependence for high electric fields.

Replacing T_e from (2.49) with the value from (2.52), we obtain a compact expression for the current noise spectral density between x and $x+\Delta x$:

$$S_{in}(x) = \overline{i_n^2} = 4k \frac{\mu_0 T_L}{\left(1 + \left(\frac{E}{E_{sat}}\right)^p\right)^{\frac{p-1}{p}}} \frac{WQ(x)}{\Delta x} \tag{2.53}$$

For p=1, we obtain a constant diffusion coefficient over the channel and that the degradation effect of the mobility by the longitudinal electric field approximately cancels out the enhancing effect of the carrier temperature. This assumption seems to be reasonable due to the very good agreement between measured and simulated data in [Han-2004].

For p=2, we obtain a constant diffusion of type:

$$D = \frac{kT_L}{q} \frac{\mu_0}{\sqrt{1 + \left(\frac{E}{E_{sat}}\right)^2}} \tag{2.54}$$

This longitudinal dependence has been obtained empirically in [Seeger-1973] for bulk devices.

In the model of Chen and Deen [Chen-2002], the electronic temperature is assumed equal to:

$$T_e(x) = T_L \left(1 + \delta \left(\frac{E}{E_{sat}}\right)^2\right) \tag{2.55}$$

where δ is a hot-carrier factor.

Using this model, we obtain:

$$S_{in}(x) = \overline{i_n^2} = 4k \frac{\mu_0 T_L \left(1+\delta\left(\frac{E}{E_{sat}}\right)^2\right)}{\left(1+\left(\frac{E}{E_{sat}}\right)^p\right)^{\frac{p-1}{p}}} \frac{WQ(x)}{\Delta x} \tag{2.56}$$

This model uses a velocity relation with p=1, obtaining for high fields a constant diffusion coefficient equal to δ times the low field diffusion coefficient whereas the diffusion coefficient decreases for fields below saturation field. It was experimentally found in [Chen-2002] that the best agreement with measurement results is obtained when δ is set to zero. Then, the diffusion coefficient decreases with longitudinal electric field. The differences between diffusion models will be studied in the next chapters.

Assuming that the local noise source is spatially uncorrelated and ω is the angular frequency, the drain and gate spectral densities and the correlation matrix are obtained using the following expressions [Lazaro-2009]:

$$S_{i_d^2} = \overline{i_d^2} = \frac{1}{I_D L_c^2} \int_{V_S}^{V_D} \frac{g_c(V)^2}{g(V)} S_{i_n} dV \tag{2.57}$$

$$S_{i_g^2} = \overline{i_g^2} = \frac{\omega^2 W^2}{I_D^5 L_c^2} \int_{V_S}^{V_D} \left(\int_{V_S}^{V_D} g_c(V')(Q(V') - Q(V)) dV' \right)^2 \frac{g_c(V)^2}{g(V)} S_{i_n} dV \tag{2.58}$$

$$S_{i_g i_d^*} = \overline{i_g i_d^*} = \frac{j\omega W}{I_D^3 L_c^2} \int_{V_S}^{V_D} \left(\int_{V_S}^{V_D} g_c(V')(Q(V') - Q(V)) dV' \right) \frac{g_c(V)^2}{g(V)} S_{i_n} dV \tag{2.59}$$

where

$$\frac{g_c(V,E)}{g(V,E)} = \frac{g(V,E)}{g(V,E) + \frac{\partial g(V,E)}{\partial E} E} \tag{2.60}$$

and the corrected length L_c is given by:

$$L_c = \int_0^L \frac{g_c}{g} dx = L \frac{\int_{V_S}^{V_D} g_c(V) dV}{\int_{V_S}^{V_D} g(V) dV} \tag{2.61}$$

The power spectral density for the local noise source is given by:

$$S_{i_n}(x) = 4kT_L \frac{g(x)}{g_c(x)} \frac{T_n(x)}{T_L} \tag{2.62}$$

In order to calculate the integrals with respect to the potential in eqn. (2.57-2.59), we will obtain a relation between the mobile channel charge and the channel potential. The methodology used to obtain all these parameters is detailed over the next chapters, for each device geometry (DG, FinFET, GAA).

2.5.2.3 Shot noise due to the tunneling gate current (TGC)

With gate length downscaling, ultra-thin oxides below 4 nm exhibit a drastic increase of leakage current, called *direct tunneling current* [Schuegraf-1994]. In this regime, the gate oxide capacitor would introduce an extra noise current source, possibly a shot noise current source, besides two classical noise sources: drain and gate current noise. The impact of the direct tunneling current on high frequency noise performance is becoming critical. The gate shot noise current generated in each segment of the MOSFET flows along the channel and subsequently creates drain shot noise current as well, because it is uncorrelated with the origins of the drain and gate current noise. Since the direct tunneling current can be substantial,

the drain shot noise becomes comparable to the drain current noise in MOSFETs with oxides below 2 nm [Danneville-2005; Pailloncy2-2004; Pailloncy3-2004]. The tunneling gate current for each channel slide is given by direct tunneling current theory [Schuegraf-1994; Pailloncy3-2004]. The local gate current expression flowing through the oxide is given by:

$$J_g(x) = AE_{ox}(x)^2 P_{tunnel}(x) \tag{2.63}$$

where the tunnel probability is :

$$P_{tunnel}(x) = \begin{cases} e^{-B/E_{ox}(x)} & , V_{ox}(x) > \Phi_b \\ e^{-\frac{b\left(1-\left(1-\frac{V_{ox}(x)}{\Phi_b}\right)^{3/2}\right)}{E_{ox}(x)}} & , V_{ox} \le \Phi_b \end{cases} \tag{2.64}$$

with the electric field within the oxide $E_{ox}(x)$ equal to:

$$E_{ox}(x) = E(x)\frac{\varepsilon_{si}}{\varepsilon_{ox}} = \left(\frac{V_G - V_{FB} - \phi_s}{t_{ox}}\right)\frac{\varepsilon_{si}}{\varepsilon_{ox}} = \frac{Q(x) + Q_b/2}{\varepsilon_{ox}} \tag{2.65}$$

where ϕ_S is the surface potential, and Q is the sheet mobile charge density, $V_{ox}(x)$ is the voltage across the oxide ($V_{ox}(x)=E_{ox}(x)t_{ox}$), and Φ_b the barrier height equal to 3.1eV [Schuegraf-1994]. The constants A and B are given by:

$$A = \frac{q^3}{8\pi h\Phi_b} \tag{2.66}$$

$$B = \frac{8\pi\sqrt{2m_{ox}}\Phi_b^{3/2}}{3hq} \tag{2.67}$$

where h is the Planck constant, and $m_{ox}=0.4m_0$ (with m_0 equal to electron mass). However, A, B and Φ_b are often considered as adjusting parameters in order to take into account quantification effects.

In order to take into account the shot noise associated to tunneling gate current $i_s(x)=J_n(x)\Delta xW$ in the segmentation method, we need to introduce a gate to channel noise source for each channel slice (see Fig. 2.20) with spectral density equal to:

$$\overline{i_s^2(x)} = 2qi_s(x) \tag{2.68}$$

The small signal conductance $g_g(x)$ associated with the tunneling current is given by:

$$g_g(x) = W\Delta x \frac{\partial J_g(x)}{\partial E_{ox}(x)} \cdot \frac{\partial E_{ox}(x)}{\partial V_G} \tag{2.69}$$

However, for typical bias points its value is small compared with ωC_{gc}, and it can be neglected as first approximation.

The excess noise factors γ, β, or Pucel's parameters R, P [Pucel-1974], and the imaginary part of correlation coefficient C, take into account only the contribution of the diffusion noise. To include the shot noise associated with gate tunneling, two current noise sources must be considered. It was shown in [Pailloncy3-2004], through numerical simulations of SOI MOSFETs using segmentation method, that the microscopic shot noise sources between the gate and the channel can be represented by two correlated macroscopic shot noise sources between the gate and source and between the drain and source, with spectral densities given by:

$$S_{i_{g,shot}} = \overline{i_{g,shot}^2} = 2qI_G \tag{2.70}$$

$$S_{i_{d,shot}} = \overline{i_{d,shot}^2} = 2qI_G\alpha \tag{2.71}$$

$$C_{shot} = \frac{\overline{i_{g,shot} \cdot i^*_{d,shot}}}{\sqrt{\overline{i^2_{g,shot}} \cdot \overline{i^2_{d,shot}}}} \tag{2.72}$$

where the factor α depend on the biasing and has typical values between 0.15 and 0.3, and I_G is the total gate current.

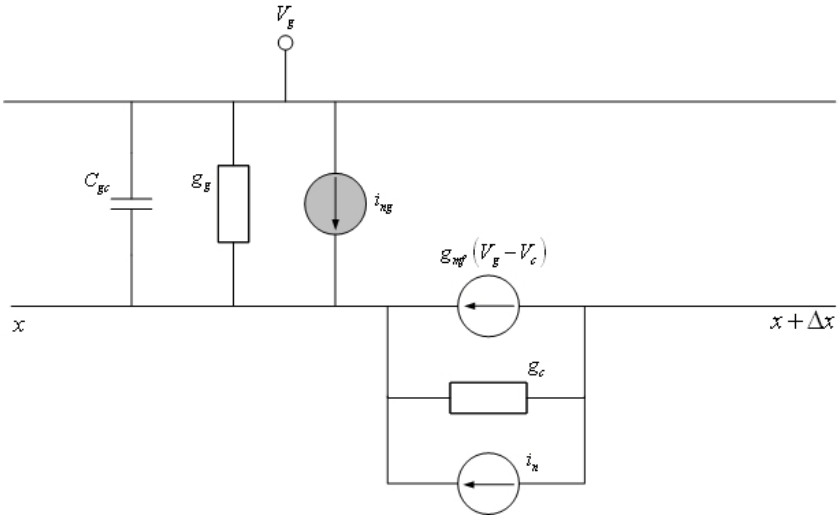


Fig. 2.20. Small-signal and noise equivalent circuit for a channel slice between x and $x+\Delta x$. $i_n(x)$ models the channel noise. The shot noise due to tunneling gate current for each slice is modeled by the noise source $i_s(x)$.

If we consider a fluctuation in the tunneling current flowing from the gate to the channel between x and $x+\Delta x$, it can be shown by solving the current continuity equation in the channel that the fluctuation in is given by:

$$\delta i_{gs}(x) = i_s(x)\left(1-\frac{x}{L}\right) \tag{2.73}$$

The spectral density of the gate to source noise current is found integrating this along the channel [Ranuarez-2005]:

$$S_{i_{gs}} = 2qW\int_0^L J_g(x)\left(1-\frac{x}{L}\right)^2 dx = 2q(I_G - 2I_{GD} + I^*) \tag{2.74}$$

with

$$I^* = W\int_0^L J_g(x)\left(\frac{x}{L}\right)^2 dx \tag{2.75}$$

The noise source fluctuation also produces a fluctuation in the gate to drain current given by [Ranuarez-2005]:

$$\delta i_{gd}(x) = i_s(x) - \delta i_g(x) = i_s(x)\left(\frac{x}{L}\right) \tag{2.76}$$

$$S_{i_{gd}} = 2qI^* \tag{2.77}$$

The cross-spectral density is found:

$$S_{i_{gs},i_{gd}} = 2q(I_{GD} - I^*) \tag{2.78}$$

Finally, the gate to source i_{gs} and gate to drain i_{gd} currents are converted to the equivalent gate $i_{g,shot}$ and drain $i_{d,shot}$ noise sources (see Fig. 2.21).

$$\begin{bmatrix} i_{g,shot} \\ i_{d,shot} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}\cdot\begin{bmatrix} i_{gs} \\ i_{gd} \end{bmatrix} \tag{2.79}$$

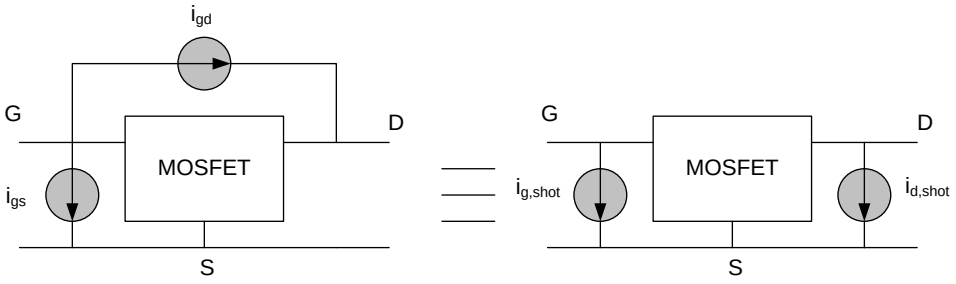


Fig. 2.21. Equivalent gate and drain shot noise source

Then, the correlation matrices are obtained using the transformation matrix (2.79):

$$\begin{bmatrix} \overline{i_{g,shot}^2} & \overline{i_{g,shot} i_{d,shot}^*} \\ \overline{i_{g,shot}^* i_{d,shot}} & \overline{i_{d,shot}^2} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix} \cdot \left(2q \begin{bmatrix} I_G - 2I_{GD} + I^* & I_{GD} - I^* \\ I_{GD} - I^* & I^* \end{bmatrix} \right) \cdot \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}^\dagger = \begin{bmatrix} I_G & I_{GD} \\ I_{GD} & I^* \end{bmatrix} \tag{2.80}$$

Thus, the factor α is given by:

$$\alpha = \frac{I^*}{I_G} \tag{2.81}$$

If we assume a linear variation of the gate current with position, an assumption that has been proposed before in the context of compact modeling and has been justified from numerical simulations [Ngo-2003], and defining the partition ratio as:

$$\alpha_g = \frac{I_{GS}}{I_G} \tag{2.82}$$

then the factor α is given by:

$$\alpha \approx \frac{5}{6} - \alpha_g \tag{2.83}$$

and the correlation between gate and drain shot noise sources is given by:

$$C_{shot} \approx \frac{1-\alpha_g}{\sqrt{5/6-\alpha_g}} \tag{2.84}$$

The expressions (2.82-2.84) are suitable for compact modeling because the only required quantities are I_G and α_g, which are available in most compact models. Also note that while we have assumed only shot noise in the gate current, these equations are still valid if there are other noise components present in the gate current (such as flicker noise). Equations (2.83) and (2.84) only have physically meaningful values when α_g is in the range 0.21–0.79 because it can be shown that if the gate current density depends linearly on the position along the channel, stays well within that range. Moreover, results from numerical solution of the current continuity equation indicate that is limited to values within this range even at relatively high gate and drain biases [Ranuarez-2005]. In this range, it can be shown that the correlation coefficient C_{shot} predicted by (2.84) is close to 0.8, which is the value obtained by A.Van der Ziel in the case of JFETs [Ziel-1969].

Even though the two shot noise sources are correlated, the effect in the final noise is negligible for drain shot noise source because the diffusion drain noise source are predominant, and the spectral drain shot noise current is about 30% lower than gate shot noise source. Analytical expressions for the four noise parameters as function of noise model parameters (R, P, C) can be found in [Danneville-2005].

These expressions are more accurate than the ones given in [Pailloncy3-2004] because they take account the correlation coefficient between noise sources and the gate noise source contribution. In order to obtain simple close form expressions for the noise parameters in presence of a tunneling gate current, we suppose that $1-C^2 \approx 1$ and $P+R-2C(PR)^{1/2} \approx P$. Using these assumptions, approximated expressions for the noise parameters can be obtained [Danneville-2005]:

$$R_n \approx R_g + R_s + \frac{S_{id}}{4kT_0 g_m} + R_g \frac{2qI_G}{4kT_0} \tag{2.85}$$

$$B_{opt} \approx -\left(\frac{f}{f_T}\right)\frac{S_{id}}{4kT_0 g_m R_n} \tag{2.86}$$

$$G_{opt} \approx \frac{\omega(C_{gs}+C_{gd})}{P+(R_g+R_s)g_m}\sqrt{PR+P(R_g+R_s)g_m}\sqrt{1+\left(\frac{f_{cshot}}{f}\right)^2} \tag{2.87}$$

$$F_{\min} \approx 1+2\frac{\omega(C_{gs}+C_{gd})}{g_m}\sqrt{PR+P(R_g+R_s)g_m}\sqrt{1+\left(\frac{f_{cshot}}{f}\right)^2} \tag{2.88}$$

$$f_{cshot} = f_T\sqrt{\frac{2qI_G}{4kT_0 RK_{shot}}};\quad K_{shot} = \frac{P+\frac{P}{R}(R_g+R_s)g_m}{P+(R_g+R_s)g_m} > 1 \tag{2.89}$$

The last expressions show that the tunneling gate current affects basically the F_{min} and G_{opt} parameters. Expression (2.89) differs with the one given in [Pailloncy3-2004] by the factor K_{shot}. This factor takes into account the thermal noise due to R_g and R_s in the shot noise cut-off frequency. The effect is a reduction of this cut-off frequency. Because of the decrease of the oxide thickness along the down-scaling, the DC tunneling gate current (TGC) I_G flowing through the oxide gets more and more important. Thus shot cut-off frequency increase with down-scaling (see 2.89).

2.6 References

[Baker-1980] J.R. Baker, D.K. Ferry, "On the physics of small semiconductors devices-I", *Solid-State Electronics*, **23**, 519 (1980)

[Bodway-1967] G.E. Bodway, "Two port power flow analysis of linear active circuits using the generalized scattering parameters", *The Microwave Journal*, pp. 61-69, (1967)

[Cappy-1989] A. Cappy, W. Heinrich, "High-frequency FET noise performance: a new approach", *IEEE Transactions on Electron Devices*, **36**, 403 (1989)

[Celik-Butler-2006] Z. Çelik-Butler, "Different noise mechanisms in high-k dielectric gate stacks", *Proc. SPIE fluctuations and Noise*, 5844, 177 (2006)

[Chen-1997] C.-H. Chen, "High Frequency Noise Modeling of MOSFETs", Master in Applied Science Thesis, Simon Fraser University (1997)

[Chen-2002] C.H. Chen, M.J. Deen, "Channel noise modeling of deep submicron MOSFETs", *IEEE Transactions on Electron Devices*, **49**, 1484 (2002)

[Christensson-1968] S. Christensson, I. Lundström, C. Svensson, "Low frequency noise in MOS transistors - I Theory", *Solid State Electronics*, **11**, 797-812 (1968)

[Dambrinne-2003] G. Dambrinne, C. Raynaud, D. Lederer, M. Dehan, O. Rozeau, M. Vanmackelberg et al., "What are the limiting parameters of deep-sub-micron mosfets for high frequency applications", *IEEE Electron Device Letters*, **24**, 189-191 (2003)

[Danneville-1994] F. Danneville, H. Happy, G. Dambrine, J. Belquin, A. Cappy, "Microscopic noise modeling and macroscopic noise models: How good a connection?", *IEEE Transactions on Electron Devices*, **41** (1994)

[Danneville-2005] F. Danneville, G. Pailloncy, A. Siligaris, B. Iñiguez, G. Dambrine, "High Frequency Noise of SOI MOSFETs: Performances and Limitations", *Third SPIE International Symp. Fluctuations and Noise*, FaN, 85-199 (2005)

[Deen-2006] M.J. Deen, C-H. Chen, S. Asgaran, G.A. Rezvani, J. Tao, Y. Kiyota, "High-Frequency Noise of Modern MOSFETs: Compact Modeling and Measurement Issues", *IEEE Transactions on Electron Devices*, **53**, 2062-2081 (2006)

[Dobrowolski-1991] J.A. Dobrowolski, "Introduction to Computer Methods for Microwave Circuit Analysis and Design", Ed. Artech House (1991)

[Gaffioul-2000] M. Gaffioul, D. Vanhoenacker, J.-P. Raskin, "Direct extraction techniques of microwave small-signal model and technological parameters for sub-quarter micron SOI MOSFETs", *5th Symposium Diagnostics and Yield, SOI-materials, devices and characterization* (2000)

[Ghibaudo-1991] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, J. Brini, "Improved analysis of low-frequency noise in field-effect MOS transistors", *Physica Status Solidi (a)*, **124**, 571 (1991)

[Ghibaudo-2002] G. Ghibaudo, T. Boutchacha, "Electrical noise and RTS fluctuations in advanced CMOS devices", *Microlectronics Reliability*, **42**, 573-582 (2002)

[Ghibaudo-2006] G. Ghibaudo, J. Jomaah, "Low Frequency Noise and Fluctuations in Sub 0.1 mm Bulk and SOI CMOS Technologies", *25th International Conference on Microelectronics*, 14-17 (2006)

[Gonzales-1984] G. Gonzalez, "Microwave Transistor Amplifiers Analysis and Design", Ed. Prentice Hall (1984)

[Han-2004] K. Han, H. Shin, K. Lee, "Analytical drain thermal noise current model valid for deep submicron MOSFETs", *IEEE Transactions on Electron Devices*, **51**, 261 (2004)

[Hillbrand-1976] H. Hillbrand, P.H. Russer, "An Efficient Method for Computer-Aided Noise Analysis of Linear Amplifier Networks", *IEEE Transactions on Circuits and Systems*, Col.CAS-23, No.4, 235-238 (1976)

[Hooge-1969] F. N. Hooge, "1/f Noise is no surface effect", *Physics Letters A*, **29**, 139–140 (1969)

[Hung-1986] K.K. Hung, Y.C. Cheng, "Characterization of metal-oxide-semiconductor transistors with very thin gate oxide", *Journal of Applied Physics*, **59**, 816-823 (1986)

[Hung-1990] K.K. Hung, P.K. Ko, C. Hu, Y.C. Cheng, "A unified model for the Flicker Noise in Metal-Oxide-Semiconductor Field-Effect Transistors", *IEEE Transactions On Electron Devices*, **37**, 654-665 (1990)

[Hung2-1990] K.K. Hung, P.K. Ko, C. Hu, Y.C. Cheng, "A physics-based MOSFET noise model for circuit simulators", *IEEE Transactions on Electron Devices*, **37**, 1323–33 (1990)

[Iniguez-2006] B. Iñiguez, T. Fjeldly, A. Lazaro, F. Danneville, M. J. Deen, "Compact-modeling solutions for nanoscale double-gate and gate-all-around MOSFETs", *IEEE Transactions on Electron Devices*, **53**, 2128 (2006)

[Jindal-1978] R.P. Jindal, A. Van der Ziel, "Phonon fluctuation model for flicker noise in elemental semiconductor", *Journal of Applied Physics*, **52**, 2884 (1978)

[Jindal-1981] R. Jindal, A. van der Ziel, "Phonon fluctuation model for flicker noise in elemental semiconductors", *Journal of Applied Physics*, **52**, 2884 (1981)

[Ladbrooke-1989] P. Ladbrooke, "MMIC Design: GaAs FETs amd HEMTs", Norwood, MA: Artech House (1989)

[Lazaro-1994] A. Lazaro, "Models de Transistors MESFETs i HEMTs per aplicacions de baix soroll", Proyecto final de Carrera, ETSETB, Universitat Politècnica de Catalunya, UPC (1994)

[Lazaro-2003] A. Lazaro, M.C. Maya, L. Pradell, "Bias-dependence of FET intrinsic noise sources, determined with a quasi-2D model", *Microwave and Optical Technology Letters*, **39**, 317 (2003)

[Lazaro-2006] A. Lazaro , B. Iñiguez, "RF and noise performance of double gate and single gate SOI", *Solid State Electronics*, **50**, 826 (2006)

[Lazaro2-2006] A. Lázaro, B. Nae, O. Moldovan, B. Iñiguez, "A compact quantum model of nanoscale double-gate metal-oxide-semiconductor field-effect transistorfor high frequency and noise simulations", *Journal of Applied Physics*, **100**, 084320 (2006)

[Lazaro-2007] A. Lazaro, B. Nae, O. Moldovan, B. Iniguez, "A CAD model of nanoscale doublé-gate MOSFET for RF and noise applications including quantum and nonstationary effects", *VI Conference of Electronic Devices (CDE)*, Jan. 31 – Feb. 2, El Escorial, Spain (2007)

[Lazaro-2008] A. Lazaro, B. Iñiguez, "RF and noise model of gate-all-around MOSFETs", *Semiconductor Science and Technology*, **23**, 075022 (2008)

[Lazaro2-2008] A. Lázaro, B. Nae, B. Iñiguez, F. Garcia, I.M. Tienda-Luna, A. Godoy, "A compact quantum model for fin-shaped field effect transistors valid from dc to high frequency and noise simulations", *Journal of Applied Physics*, **103**, 084507 (2008)

[Lazaro-2009] A. Lazaro, A. Cerdeira, B. Nae, M. Estrada, B. Iniguez, "High-frequency compact analytical noise model for double-gate metal-oxide-semiconductor field-effect transistor", *Journal of Applied Physics*, **105**, 034510 (2009)

[Liechti-1976] C.A. Liechti, "Microwave Field-Effect Transistors", *IEEE Transactions on Microwave Theory and Technology*, vol. MTT-24, no.6 (1976)

[Mason-1954] S.J. Mason, "Power gain in feedback amplifier", *I.R.E. Transaction on Circuit Theory*, **7**, 20-25 (1954)

[McWhorter-1957] A.L. McWhorter, "1/f Noise and germanium surface properties," *Semiconductor Surface Physics*, Philadelphia, PA, University of Pennsylvania Press (1957)

[Min-2004] B. Min, S.P. Devireddy, Z. Çelik-Butler, F. Wang, A. Zlotnicka, H.H. Tseng, "Low-frequency noise in submicrometer MOSFETs with HfO2, HfO2/Al2O3 and HfAlOx gate stacks", *IEEE Transactions on Electron Devices*, **51**, 1679-1687 (2004)

[Morshed-2008] T.H. Morshed, S.P. Devireddy, Z. Celik-Butler, A. Shanware, K. Green, J.J. Chambers, et al., "Physics-based 1/f noise model for MOSFETs with nitrided high-k gate dielectrics", *Solid State Electronics*, **52**, 711 (2008)

[Ngo-2003] Q. Ngo, D. Navarro, T. Mizoguchi, S. Hosakawa, H. Ueno, M. Miura-Mattausch, et al., "Gate current partitioning in MOSFET models for circuit simulation", *Nanotechnology Conference Trade Show*, 322–325 (2003)

[Nougier-1977] J.P. Nougier, M. Rolland, "Differential relaxation times and diffusivities of hot carriers in isotropic semiconductors", *Journal of Applied Physics*, **48**, 1683 (1977)

[Pailloncy-2004] G. Pailloncy, B. Iñiguez, G. Dambrine, J.-P. Raskin, F. Danneville, "Noise Modeling in Fully Depleted SOI MOSFETs", *Solid State Electronics*, **48**, 813 (2004)

[Pailloncy2-2004] G. Pailloncy, C. Raynaud, M. Vanmackelberg, F. Danneville, S. Lepilliet, J.-P. Raskin et al., "Impact of Downscaling on High-Frequency Noise Performance of Bulk and SOI MOSFETs", *IEEE Transactions on Electron Devices*, **51**, 1605–1612 (2004)

[Pailloncy3-2004] G. Pailloncy, B. Iniguez, G. Dambrine, F. Danneville, "Influence of Tunneling Gate Current on the Noise Performance of SOI MOSFETs", *IEEE International SOI Conference*, 55–57 (2004)

[Portilla-1994] J. Portilla, R. Quere, J. Obregon, "An Improved CAD Oriented FET Model for Large-Signal and Noise Applications", *IEEE MTT-S Digest*, 849-852 (1994)

[Pucel-1974] R.A. Pucel, H. A. Haus, H. Statz, "Signal and noise properties of gallium arsenide field effect transistors", *Advances in Electronics and Electron Physics*, **38**, 195-265 (1974)

[Quevedo-Lopez-2005] M.A. Quevedo-Lopez, S.A. Krishnan, P.D. Kirsch, G. Pant, B.E. Gnade, R.M. Wallace, "Ultrascaled hafnium silicon oxynitride gate dielectrics with excellent carrier mobility and reliability", *Applied Physics Letters*, **87**, 262902 (2005)

[Ranuarez-2005] J.C. Ranuarez, M.J. Deen, C.-H. Chen, "Modeling the partition of noise from the gate-tunneling current in MOSFETs", *IEEE Electron Device Letters*, **26**, 550-552 (2005)

[Roblin-1987] P. Roblin, K. Sungchoon, A. Ketterson, H. Morkoç, "Analysis of MODFET Microwave Characteristics", *IEEE Transactions on Electron Devices*, **ED-34**, 1919-1927 (1987)

[Roy-2005] A.S. Roy, C.C. Enz, "Compact Modeling of Thermal Noise in the MOS Transistor", *IEEE Transactions on Electron Devices*, **52**, 611 (2005)

[Roy-2006] A.S. Roy, C.C. Enz, J.-M. Sallese, "Noise modeling methodologies in the presence of mobility degradation and their equivalence", *IEEE Transactions on Electron Devices*, **53**, 348–355 (2006)

[Scholten-2003] A.J. Scholten, L.F. Tiemeijer, R.V. Langevelde, R.J. Havens, A.T. Duijnhoven, V.C. Venezia, "Noise modeling for RF CMOS circuit simulation", *IEEE Transactions on Electron Devices*, **50**, 618 (2003)

[Schuegraf-1994] K.F. Schuegraf, C. Hu, "Hole Injection SiO2 Breakdown Model for Very Low Voltage Lifetime Extrapolation", *IEEE Transactions on Electron Devices*, **41**, 761–767 (1994)

[Seeger-1973] K. Seeger, "Semiconductor Physics", New York; Springer-Verlag (1973)

[Shaeffer-1977] D.K. Shaeffer and T.H Lee, "A 1.5 V 1.5 GHz CMOS low noise amplifier", *IEEE Journal of Solid–State Circuits*, **32**, 745 (1977)

[Simoen-2004] E. Simoen, A. Mercha, C. Claeys, E. Young, "Correlation between the 1/f noise parameters and the effective low-field mobility in HfO2 gate dielectric n-channel metal-oxide-semiconductor field-effect transistors", *Applied Physics Letters*, **85**, 1057 (2004)

[Surya-1988] C. Surya, T. Hsiang, "A thermal activation model for 1/f noise in Si-MOSFETs", *Solid State Electronics*, **31**, 959-964 (1988)

[Sze-1981] S.M. Sze, "Physics of semiconductor devices", New-York: Wiley (1981)

[Tsividis-1987] Y.P. Tsividis, "Operation of modeling of the MOS transistor", McGraw-Hill Book Company (1987)

[Vandamme-1994] L.K.J. Vandamme, D. Rigaud, "1/f noise in MOS devices, mobility or number fluctuations?", *IEEE Transactions on Electron Devices*, **41**, 1936–1945 (1994)

[Vandamme-2000] E.P. Vandamme, L.K.J. Vandamme, "Critical discussion on unified 1/f noise models for MOSFETs", *IEEE Transactions on Electron Devices*, **47**, 2146–2153 (2000)

[Wilk-2001] G.D. Wilk, R.M. Wallace, J.M. Anthony, "High-κ gate dielectrics: current status and materials properties considerations", *Journal of Applied Physics*, **89**, 5243-5275 (2001)

[Yeager-1986] H.R. Yeager, R.W. Dutton, "Circuit Simulation Models for the High Electron Mobility Transistor", *IEEE Transactions on Electron Devices*, **ED-32**, 682-692, (1986)

[Ziel-1969] A. van Der Ziel, “Noise in Junction- and MOS-FETs at high temperatures”, *Solid State Electronics*, **12**, 861-866 (1969)

[Ziel-1979] A. van der Ziel, “Flicker noise in electronic devices”, *Advances in Electronics and Electron Physics*, **49**, 225 (1979)

[Ziel-1986] A. van der Ziel, “Noise in Solid State Devices and Circuits”, New York: John Wiley & Sons, Inc. (1986)

Chapter 3

Compact Modeling of Double-Gate Transistors

3.1 Introduction

Ultrathin-body MOS transistors, and in particular, DG MOSFETs are considered to be a very attractive option to improve the performance of CMOS devices and overcome some of the difficulties encountered in further downscaling of MOSFET transistors into the sub-50 nm gate length regime [Balestra-1987; Fossum-2002; Fossum-2004; Kim-2001; Taur-2001]. One of the limiting factors in MOSFET downscaling is the static power consumption due to short channel effects (SCEs), including threshold voltage roll-off and subthreshold slope degradation, among

others. These effects increase the off-state leakage current. In DG MOSFETs, the gate control over the channel is stronger than in planar SG MOSFETs, thus these effects can be significantly reduced [Balestra-1987; Fossum-2002; Fossum-2004; Kim-2001; Taur-2001].

Nanoscale DG MOSFETs introduce challenges to compact modeling associated with the enhanced coupling between the electrodes (source and drain gates), quantum confinement, ballistic or quasi-ballistic transport, gate tunnelling current, etc. Most models in literature are for undoped devices with a long enough channel to assume the transport is due to the drift-diffusion mechanism [Taur-2001; Francis-1994; Sallese-2004]. The electrostatics modeling is based on solving the one-dimensional (1D) Poisson equation perpendicular to the gates, thereby neglecting short-channel effects.

These issues justify the need – and relative urgency - for advanced computer-aided-design (CAD) compatible models, based on the physics of the device, which can be used in circuit simulators. Such a model - for short-channel DG MOSFETs - is presented in detail in this chapter.

The starting point is a classical model (without quantification effects) for the doped double gate MOSFET, which is analytical, explicit and continuous. It is based on a previous work by P. Francis et al. [Francis-1994] who presented a current model valid for low V_{DS}. The model works in all operating regimes from weak to strong inversion and from linear regime to saturation. The current expression is based on a unified charge control model, written in terms of charge densities at the source and drain ends [Jimenez-2004; Iniguez-2005], and derived for a doped DG-MOSFET. It uses an accurate explicit expression of the inversion charge densities in terms of the applied bias, and no fitting parameters are used in the charge control model. The model is continuous through all operation regimes

(linear, saturation, sub threshold), up to well above threshold, and since these devices are not operated at high values of V_{GS}, it is considered valid for all regimes of practical interest.

This classical unified charge control model is extended to include quantification effects within the channel. This extension is based on the analytical solution for Schrödinger equation for an infinite potential well presented by Baccarani et al. [Baccarani-1999]. This hypothesis fails for strong inversion region where the wavefunctions differ from the case of infinite potential well [Trivedi-2004; Ge-2000]. Using the concept of inversion layer centroid [Lopez-Villanueva-2000; Ge-2000], a correction in the oxide capacitance is introduced in order to improve the accuracy in the strong inversion bias region. Finally, a compact charge control model is obtained, which includes quantum effects whose explicit formulation is similar to classical charge control. Velocity overshoot is included in the model using a one-dimensional energy-balance model. In contrast with the model presented by G. Baccarani et al. [Baccarani-1999], the effect of saturation region and the channel modulation length effect are considered. The low-field mobility data uses a model that takes into account the mobility degradation due to quantum effects [Ge-2002].

The DC model is extended to RF/microwave frequency range using the active transmission line approach [Iniguez2-2005; Lazaro-2006]. Diffusion and shot noise sources are included in the active line in order to study the noise behaviour of these transistors. Needless to say the carrier temperature has a great influence in the behaviour of the high frequency noise. Whereas in the drift-diffusion models the carrier temperature is considered using empirical relationships with electric field, in the model presented here, the carrier temperature along the channel is obtained from the energy-balance model. In contrast with previous models for DG-MOSFETs [Iniguez2-2005; Iniguez-2006; Pailloncy-2004; Lazaro-

2006], a compact model for RF/noise applications including quantum effects and hydrodynamic transport is presented, as well as a comparison between drift-diffusion and non-stationary models.

3.2 Charge Control Model

3.2.1 A Classical Charge Control Model

Figure 3.1 shows a drawing of a symmetrical DG-MOSFET. Using the Gradual Channel Approximation and neglecting the hole concentration, Poisson's equation in an n-channel DG MOSFET reads as [Lazaro-2006]:

$$\frac{d^2\phi(x,y)}{dy^2} = \frac{q}{\varepsilon_{Si}}\left[N_A + \frac{n_i^2}{N_A} e^{\frac{q}{kT}[\phi(x,y)-V(x)]}\right] \tag{3.1}$$

where ϕ is the surface potential, q is the electron charge, ε_{Si} is the permittivity of the silicon, N_A represents the doping density, n_i is the intrinsic carrier concentration, k is Boltzmann´s constant, T is the temperature and $V(x)$ is the electron quasi-Fermi potential depending on the voltage applied to the channel between source and drain and is assumed to be independent of y [Francis-1994].

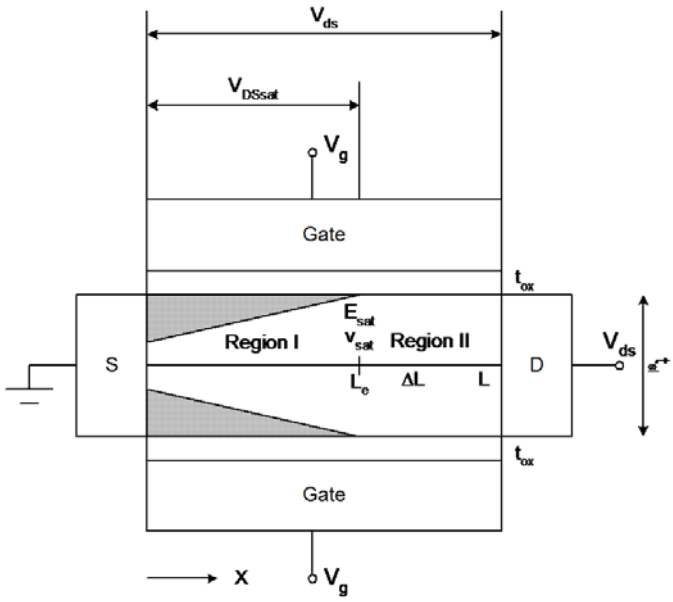


Fig. 3.1. Double-Gate MOSFET structure

The surface electric field $E_S(x)$ can be written in terms of the mobile charge density (in absolute value) per unit area *Q*, and the depletion charge density per unit area (in absolute value) $Q_{Dep} = qN_A t_{si}$ (t_{si} being the silicon film thickness):

$$E_S(x) = \frac{Q + Q_{Dep}}{2\varepsilon_{si}} \tag{3.2}$$

By integrating eq. (3.1) between the centre and the surface of the film we get:

$$E_S(x) = \sqrt{\frac{2qN_A}{\varepsilon_{si}}} \sqrt{(\phi_s - \phi_0) + \frac{kT}{q}\frac{n_i^2}{N_A{}^2} e^{\frac{q}{kT}[\phi_s - V(y)]} \left(1 - e^{-\frac{q}{kT}(\phi_s - \phi_0)}\right)} \tag{3.3}$$

where $\phi_s = \phi(x, -t_{si}/2)$ is the surface potential and $\phi_0 = \phi(x, 0)$ is the potential in the middle of the film. Equation (3.3) cannot be analytically integrated for the potential, but it is observed, from numerical simulations, that the difference $\phi_s - \phi_0$ keeps a constant value from the subthreshold region to well above threshold.

At this point it is useful to define the average penetration of the inversion-charge distribution y_I into the silicon. Following J.A. Lopez-Villanueva et al. [Lopez-Villanueva-2000], due to the symmetry of the inversion-charge distribution in symmetrical DG-MOSFET, we define y_I integrating only half of the silicon film:

$$y_I = \frac{\int_0^{t_{si}/2} yn(y)dy}{\int_0^{t_{si}/2} n(y)dy} = \frac{2q}{Q}\int_0^{t_{si}/2} yn(y)dy \tag{3.4}$$

Integrating the one-dimensional Poisson's equation between $y=0$ and $y=t_{si}/2$ (neglecting the majority-carrier concentration and N_A assumed constant) we obtain the following expression for the difference $\varphi_S - \varphi_0$.

$$\phi_S - \phi_0 = \frac{y_I}{2\varepsilon_{si}}Q + \frac{qN_A t_{si}^2}{8\varepsilon_{si}} = \frac{y_I}{2\varepsilon_{si}}Q + \frac{Q_{Dep}}{8C_{Si}} \tag{3.5}$$

Note that, for weak inversion, the term $y_I Q \ll Q_{Dep}/8C_{si\,i}$ in eq. (3.5) may be simplified to:

$$\phi_S - \phi_0 \approx \frac{qN_A t_{Si}^2}{8\varepsilon_{Si}} = \frac{Q_{Dep}}{8C_{Si}} \tag{3.6}$$

where $C_{si} = \varepsilon_{si}/t_{si}$ represents the silicon film capacitance. Approximation (3.6) is valid from subthreshold to well above threshold, which is demonstrated by the correct agreement with simulations, for low and moderate V_{GS} (~2V). For high V_{GS}

the surface potential increases much more rapidly than the mid-film potential, making the approximation less correct.

Equating (3.2) and (3.3) the following charge control model is obtained:

$$V_{GS} - V_{FB} - V - \left(\frac{Q_{Dep}}{2C_{ox}} + \frac{kT}{q} \log\left[\frac{q^2}{kT} \frac{N_A^{\ 3}}{n_i^{\ 2}} \frac{t_{Si}^{\ 2}}{2\varepsilon_{Si}} \right] \right) = \frac{Q}{C_{ox}} + \frac{kT}{q} \log\left[\frac{Q}{Q_{Dep}} \right] + \frac{kT}{q} \log\left[\frac{Q + Q_{Dep}}{Q_{Dep}} \right] \tag{3.7}$$

Note that V varies from source to drain, being $V=0$ at the source and $V=V_{DS}$ at the drain [Iniguez-2006], V_{FB} is the flat-band voltage and C_{ox} represents the capacitance of the oxide ($C_{ox} = \varepsilon_{ox} / t_{ox}$).

In order to calculate the charge densities from an explicit expression of the applied bias, the following equation is used:

$$Q = 2C_{ox} \left(-\frac{2C_{ox}\beta^2}{Q_{Dep}} + \sqrt{\left(\frac{2C_{ox}\beta^2}{Q_{Dep}} \right)^2 + 4\beta^2 \log^2\left[1 + e^{\frac{V_{GS} - V_{TH} + \Delta V_{TH} - V}{2\beta}} \right]} \right) \tag{3.8}$$

Expression (3.8) is similar to the expression used in surrounding gate MOSFETs [Jimenez-2004; Iniguez-2005], where the charge control model has the same form as eq. (3.6). This expression tends to the desired limits below and above threshold (see [Iniguez-2005] for details).

In eq. (3.8) $\beta = kT / q$ and V_{TH} is defined as:

$$V_{TH} = V_0 + 2\beta \log\left(1 + \frac{Q'}{2Q_{Dep}} \right) \tag{3.9}$$

where *Q'* is actually an initial iteration for *Q*:

$$Q' = 2C_{ox}\left(-\frac{2C_{ox}\beta^2}{Q_{Dep}} + \sqrt{\left(\frac{2C_{ox}\beta^2}{Q_{Dep}}\right)^2 + 4\beta^2 \log^2\left[1+e^{\frac{V_{GS}-V_0-V}{2\beta}}\right]}\right) \tag{3.10}$$

and

$$V_0 = V_{FB} + \left(\frac{Q_{Dep}}{2C_{ox}} + \frac{kT}{q}\log\left[\frac{q^2}{kT}\frac{N_A^{\ 3}}{n_i^{\ 2}}\frac{t_{Si}^{\ 2}}{2\varepsilon_{Si}}\right]\right) \tag{3.11}$$

The term ΔV_{th} ensures the correct behaviour of *Q* above threshold:

$$\Delta V_{TH} = \frac{\left(\frac{C_{ox}\beta^2}{Q_{Dep}}\right)Q'}{Q_{Dep} + Q'/2} \tag{3.12}$$

3.2.2 A Quantum Charge Control Model

Due to the confinement of electron motion normal to the Si–SiO interface, the conduction band within the transistor channel is split into several subbands, each being associated with its corresponding energy eigenvalue. Hence, the channel charge per unit area may be expressed as [Baccarani-1999]:

$$\begin{aligned} Q = qN_i &= q\sum_{n=1}^{N_t}\sum_{k=1}^{N_m} N_k \log\left\{1+e^{-\frac{E_{nk}-E_{Fn}}{kT}}\right\} \\ &= q\sum_{n=1}^{N_t}\sum_{k=1}^{N_m} N_k \log\left\{1+e^{-\frac{E_{nk}-E_{c0}}{kT}}\cdot e^{\frac{q(\phi_c-\phi_{F_n})}{kT}}\right\} \end{aligned} \tag{3.13}$$

where N_k is the density of states in the subband at energy E_{nk} and N_t is the number of subbands generated by each minimum of the silicon conduction band. For a silicon with a <100> crystal orientation, two energy eigenvalues with generacy factor g_1=2 and g_2=4 are considered.

$$N_k = \frac{g_k m_{dk}^* kT}{\pi \hbar^2} \tag{3.14}$$

An initial approximation for the eigenvalues is given using the square potential well:

$$E_{nk} = E_{co} + \frac{\left(n\pi\hbar\right)^2}{2m_{zk}^* t_{si}^2} \tag{3.15}$$

where $m_{d1}^* = m_t^*, m_{d2}^* = \sqrt{m_l^* m_t^*}, m_{z1}^* = m_l^* = 0.916 m_0, m_{z2}^* = m_t^* = 0.19 m_0$.

Using the perturbation theory, a first-order correction to the energy eigenvalues can be computed, as a perturbational potential energy [Baccarani-1999]:

$$\delta H \approx \frac{q\rho}{2\varepsilon_{si}} x^2, \quad \rho = -\left(N_i + N_A t_{si}\right)/t_{si} \tag{3.16}$$

$$\begin{aligned} \delta E_n &= \left\langle w_n \mid \delta H \mid w_n \right\rangle = \frac{q\rho}{\varepsilon_{si} t_{si}} \int_{-t_{si}/2}^{t_{si}/2} \sin^2\left(\frac{n\pi}{t_{si}}\left(x + t_{si}/2\right)\right) x^2 dx \\ &= \frac{q\rho t_{si}^2}{24\varepsilon_{si}}\left(1 - \frac{6}{\left(n\pi\right)^2}\right) \end{aligned} \tag{3.17}$$

where ρ is the average space charge density in the potential well and w_n is the autofunction associated to the eigenvalue E_{nk}.

An approximated channel charge can be obtained using the Boltzmann approximation:

$$Q = 2C_g \frac{kT}{q} \log\left\{1 + e^{\frac{q(V_{GS} - V_{TH} - V)}{kT}}\right\} \tag{3.18}$$

The threshold voltage V_{TH} is defined as:

$$V_{TH} = \Phi_M - \chi + \frac{qN_A t_{si}}{2C_g} + \frac{kT}{q} \log\left(\frac{2C_g kT}{q^2 N_c}\right) \tag{3.19}$$

where N_A is the acceptor channel density, C_g is function of the oxide capacitance per unit area, and C_d is the depletion capacitance per unit area ($C_d \sim 4\varepsilon_{si} / t_{si}$).

$$C_g = \frac{C_{ox} C_d}{C_{ox} + C_d} \tag{3.20}$$

In (3.20) the effective density of states is defined as:

$$N_c = \sum_{n=1}^{N_t} \sum_{k=1}^{N_m} N_k e^{-\frac{E_{nk} - E_{c0}}{kT}} \tag{3.21}$$

To verify the compact quantum-effect model, the predictions where compared with those obtained with SCHRED [Vasileska-2000], which numerically and self-consistently solves the Poisson and Schrödinger equations in arbitrary 1-D MOS structures. Figures 3.2 and 3.3 show the inversion charge as a function of gate bias for a DG-MOSFET (ϕ_M =4.05 eV, t_{ox}=1.5nm) for t_{si}=5 nm, N_A=10^{17} cm^{-3} (Fig. 3.2), and t_{si}=10 nm, N_A=10^{17} cm^{-3} (Fig. 3.3). These figures compare the classical simulation (Poisson equation solved numerically with SCHRED) and the self-consistently Poisson-Schrödinger simulation, with the classical compact model (3.8-3.12) and the new compact model from eq. (3.18).

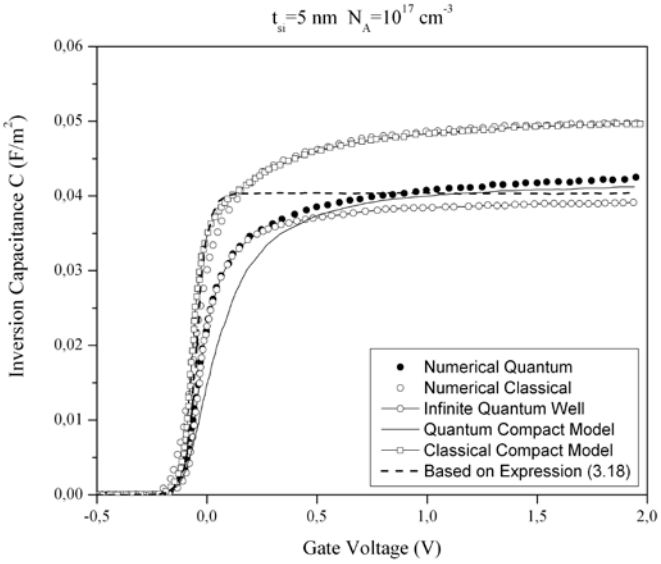


Fig. 3.2. Comparison of the inversion capacitance as a function of gate voltage between the classical and quantum models (t_{si}=5 nm, N_A=10^{17}cm^{-3}).

These figures shows an excellent agreement between the classical simulation and the classical compact model (3.8-3.12), validating the approximation from eq. (3.6). Nevertheless the quantum compact model (3.13-3.17) and the simplified expression (3.18) do not agree with numerical simulations in the strong inversion region, but the agreement is better for low gate bias. These discrepancies arise from the infinite potential well approximation and the uniform

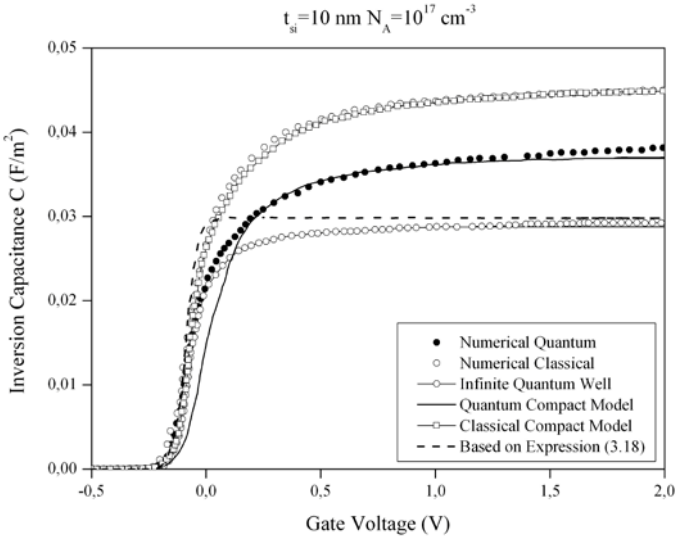


Fig. 3.3. Comparison of the inversion capacitance as a function of gate voltage between the classical and quantum models (t_{si}=10 nm, N_A=10^{17}cm^{-3}).

charge distribution in the well assumed equal to the mean value used in the eigenvalue calculation, in spite of a second order correction performed later in order to improve the initial eigenvalue estimation. Figure 3.4 shows the eigenfunction for a lower subband for different gate bias voltages.

For a higher gate bias voltage the eigenfunctions differs from the eigenfunctions from the infinite potential well formulation. This effect is studied by L. Ge et al. [Ge-2002] where a set of trial eigenfunctions is proposed:

$$\psi_j(y) = \frac{a_j}{2}\sqrt{\frac{2}{t_{si}}}\sin\left(\frac{(j+1)\pi y}{t_{si}}\right)\cdot\left(e^{-b_j y/t_{si}} + e^{-b_j (t_{si}-y)/t_{si}}\right) \qquad (3.22)$$

where a_j are normalisation factors, and b_j are parameters that are found by a variational approach. For the case $b_j=0$, eq. (3.22) reduces to an infinite well eigenfunction.

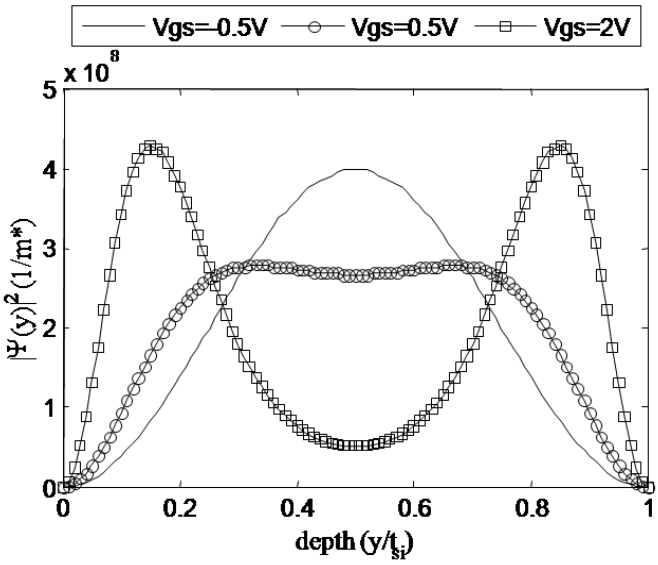


Fig. 3.4. Lowest subband eigenfunction (in 1/m* units) computed numerically as a function of normalised depth for V_{GS}=-0.5V, V_{GS}=0.5V and V_{GS}=2V.

Integrating Poisson's equation over half the Si film yields [Lopez-Villanueva-2000]:

$$Q = 2C_{ox}^{*}\left[V_{GS} - \Phi_{MS} - \phi_0 - \frac{Q_{Dep}}{2C_{ox}}\left(1+\frac{C_{ox}}{4C_{si}}\right)\right] = 2C_{ox}^{*}\left(V_{GS} - V_{TH}\right) \tag{3.23}$$

with

$$C_{ox}^{*} = \frac{C_{ox}}{1 + C_{ox}\dfrac{y_I}{\varepsilon_{si}}} \tag{3.24}$$

Equation (3.23) is accurate in weak, moderate and strong inversion regions due to the fact that no simplified assumptions have been made in its deduction. Note that V_{TH} is a nearly constant threshold voltage for strong-inversion conditions.

Equation (3.23) can be interpreted as a surface potential formulation for DG MOSFET devices. However, the inversion centroid is a function of the inversion charge *Q*. As a result a nonlinear equation that does not have an explicit solution is obtained. In the classical compact model, i.e. $y_I=0$, C_{ox}^{*} reduces to C_{ox}.

A simple relationship between the inversion centroid and the inversion charge obtained fitting numerical simulation results is given by J.A. Lopez-Villanueva et al. [Lopez-Villanueva-2000]:

$$\frac{1}{y_I} = \frac{1}{a + b \cdot t_{si}} + \frac{1}{y_{I0}}\left(\frac{N_I}{N_{I0}}\right)^{n} \tag{3.25}$$

with a=0.35nm, b=0.26, y_{I0}=6 nm, $N_{I0}=7\cdot10^{12}$ cm^{-2} and n=0.8.

Using a variational method and an eigenfunction (3.22), an alternative explicit expression to (3.25) is given by L. Ge et al. [Ge-2002].

Using the results of Figs. 3.2 and 3.3, we propose using the same charge compact model to include quantum effects but using the effective oxide capacitance C_{ox}^{*}, which is calculated using (3.24-3.25) from an initial iteration in the inversion charge given by eq. (3.13). This unified compact model has the same explicit expression for classical and quantum-effect model but using different threshold voltages (see Figs. 3.2 and 3.3) and effective oxide capacitance.

3.3 Drain Current Model

In extremely short channel DG-MOSFET the channel is quasi-ballistic, thus an important overshoot velocity is expected [Fossum-2004; Ge-2001; Baccarani-1999]. Using a simplified energy-balance model, the electron mobility is a function of the electron temperature related to the average energy of the carriers. The electron temperature T_e is governed by the following equation:

$$\frac{dT_e}{dx}+\frac{T_e-T_0}{\lambda_w}=-\frac{q}{2k}E_x(x) \tag{3.26}$$

where the energy-relaxation length is defined as $\lambda_w \approx 2v_{sat}\tau_w$, τ_w being the energy relaxation time and v_{sat} the saturation velocity. Equation (3.26) can be integrated assuming a constant λ_w, under boundary condition $T_e\left(x=0\right)=T_0$, and the x-component of the electric field expressed as function of channel potential, $E_x(x)=-dV(x)/dx$:

$$T_e(x)=T_0+\frac{q}{2k}V(x)-\frac{q}{2k\lambda_w}\int_0^x V(\xi)e^{\frac{\xi-y}{\lambda_w}}d\xi \tag{3.27}$$

The velocity increases along the channel, and for $V_{DS}>V_{DSS}$ (V_{DSS} is called saturation voltage), the velocity reaches a saturation velocity. Assuming that the velocity is saturated, the channel can be divided into two sections (see Fig. 3.1): the first section, $0<x<L_e=L-L_{sat}$, and the saturation region, $x>L_e$. In contrast with classical drift-diffusion models, the saturated velocity in the saturation region due to non-stationary effects can achieve a value several times higher than the stationary saturation velocity, v_{sat}. This phenomenon is known as velocity overshoot.

In the linear region, the carrier velocity can be obtained from the mobility:

$$v(x) = \mu_n(x)E_x(x) = \frac{\mu_{n0}}{1+\alpha(T_e(x)-T_0)}E_x(x) \tag{3.28}$$

where the value of α is determined from eq. (3.26) under static conditions, where $dT_e/dx=0$:

$$\alpha = \frac{2k\mu_{n0}}{q\lambda_w v_{sat}} \tag{3.29}$$

The dependence of the mobility μ_{n0} on the normal electric field is often referred to as mobility reduction, whereas the dependence on the lateral electric field is often referred to as velocity saturation. The effective vertical field E_{eff} reduces the effective mobility given by the model of V.P. Trivedi et al. [Trivedi-2004]:

$$\mu_{n0}(t_{si}, E_{eff}) = \frac{\mu_0}{1+\frac{\mu_0}{\mu_{ph(bulk)}}\left(\frac{\mu_{ph(bulk)}}{\mu_{ph(t_{si(eff)})}}-1\right)+\theta\frac{\mu_0}{\mu_{sr}}} \tag{3.30}$$

where effective μ_0 and θ are fitting parameters, and the effective normal field is given by:

$$E_{eff} \approx \frac{Q+Q_{dep}}{4\varepsilon_{Si}} \tag{3.31}$$

Note that the model from eq. (3.30) takes into account the dependence of mobility with the silicon thickness due to the variation of the distance between the inversion-charge centroid and the surface with respect to t_{si}. It uses the lowest subband associated to the eigenfunction (3.22) to calculate the phonon limited

mobility. Screening mobility is modeled in the same manner as conventional devices, using the effective field ($\mu_{sr}\alpha E_{eff}^{-2}$).

Expression (3.28) differs from the classical drift-diffusion model where the mobility is a function of the lateral electric field.

$$\mu_n = \frac{\mu_{n0}}{1+E_x/E_{sat}}, E_x < E_{sat} \tag{3.32}$$

where E_{sat} is the saturation field when the velocity reaches saturation voltage.

For the calculation of the current that flows from drain to source, the so-called channel current I_{DS}, it is assumed that the hole current as well as recombination/generation can be neglected. The channel current can be described by the drift-diffusion current:

$$I_{DS} = WQv \tag{3.33}$$

where W is the gate width.

Using the charge control models previously presented and the velocity given by eq. (3.28), the drain current in the linear channel region is obtained:

$$I_{DS} = \frac{W\int_0^{V_{Dsat}} \mu_{n0}Q(V)dV}{\int_0^{L_e}\left(1+\alpha(T_e(x)-T_0)\right)dx} = \frac{W\mu_{eff}\int_0^{V_{Dsat}} Q(V)dV}{\int_0^{L_e}\left(1+\alpha(T_e(x)-T_0)\right)dx} \tag{3.34}$$

The numerator integral can be calculated numerically or using the mean value theorem and can be expressed as a function of a mean effective mobility, μ_{eff}, whose value can be obtained by means of a numerical integration of eq. (3.34).

Alternatively, some compact modeling authors propose the use of the following empirical expression for the mean effective mobility:

$$\mu_{eff} = \frac{\mu_0}{1+\theta'(V_{GS}-V_{TH})} \sim \mu_{n0}\left(t_{si}, \frac{E_{eff}(x=0)+E_{eff}(x=L_e)}{2}\right) \tag{3.35}$$

where θ' is an empirical parameter. Another approximation assumes a smoothing change of the mobility along the channel, thus the effective mobility is given by eq. (3.30) but evaluated at the mean effective field between the source and the saturation point.

In the classical case, using the effective mobility, the charge integral from eq. (3.34) can be evaluated and the integration is done analytically in eq. (3.37), being denoted as the function $f(V_{GS},V_{DSsat})$.

From eqs. (3.3-3.4) the following expression is obtained:

$$dV = -\frac{dQ}{C_{ox}} - \frac{kT}{q}\left(\frac{dQ}{Q} + \frac{dQ}{Q+Q_{Dep}}\right) \tag{3.36}$$

Therefore the expression of I_{DS} can be written in terms of carrier charge densities. Integrating the charge density using eq. (3.8), between Q_s and Q_d (Q=Q_s at the source end and Q=Q_d at the saturation point or drain end), we have:

$$f(V_{GS},V_{DSsat}) = 2\left[2\frac{kT}{q}(Q_s-Q_d) + \frac{Q_s^2-Q_d^2}{2C_{ox}} + \frac{kT}{q}Q_{Dep}\log\left[\frac{Q_d+Q_{Dep}}{Q_s+Q_{Dep}}\right]\right] \tag{3.37}$$

In the quantum case, using the effective mobility, the charge integral from eq. (3.34) can be evaluated numerically, and it is denoted as the function $f(V_{GS},V_{DSsat})$.

In order to evaluate the integral of the denominator from eq. (3.34), the temperature profile along the channel is required. As an approximation, in the linear region the lateral field is considered linear from a small value at the source end to the saturation field at $x=Le$ ($E_x=E_{sat}\cdot x/L_e$). Using eq. (3.37), we obtain:

$$I_{DS}=\frac{W\mu_{eff}f(V_{GS},V_{DSS})}{L_e+\frac{q\alpha}{2k}\int_0^{L_e}V(\xi)e^{\frac{\xi-L_e}{\lambda_w}}d\xi}=\frac{W}{L_e}\frac{\mu_{eff}f(V_{GS},V_{DSS})}{1+\gamma_n V_{DSS}} \tag{3.38}$$

where

$$\gamma_n=\frac{\mu_{eff}}{v_{sat}L_e}\frac{1}{\left(1+2\lambda_w/L_e\right)} \tag{3.39}$$

and V_{DSS} is equal to V_{DS} for non saturated channels ($L_e=L$) and $V_{DSS}=V_{DSsat}$ for saturated channels.

Channel length modulation should also be included in the model. For $V_{DS}<V_{DSsat,}$ the device works in the linear region, $L_e=L$ and $V_{DSsat}=V_{DS}$. For $V_{DS}>V_{DSsat}$, the channel is partially saturated, and the saturated channel length is given by:

$$\Delta L=L-L_e=L_c\,\mathrm{arcsin}\,h\left(\frac{V_{DS}-V_{DSsat}}{E_{sat}L_c}\right) \tag{3.40}$$

where $L_c=a\cdot\lambda_c$ is proportional to the characteristic length λ_c [Lazaro-2006], and a is a fitting parameter ($0<a\leq 1$).

The saturation voltage V_{DSsat} is found using the current continuity along the channel. Equating (3.17) with the expression of the current in the saturated channel given by:

$$I_{DS} = WQ(V = V_{DSsat})v_{sat,ns} \tag{3.41}$$

where $v_{sat,ns}$ is the channel velocity in the saturation region ($x>L_e$) taking into account the non-stationary effect from eq. (3.26), we obtain the value of V_{DSsat} by equaling to 0 the derivative of I_{DS} versus V_{DS} [Baccarani-1999]:

$$V_{DSsat} = V_{DSsat}^{(wi)} + \frac{kT}{q}\ln\left\{1+\exp\left[q(V_{DSsat}^{(si)} - V_{DSsat}^{(wi)})/kT\right]\right\} \tag{3.42}$$

where V_{DSsat} in the strong inversion (*si*) and weak inversion bias region is given by:

$$V_{DSsat}^{si} = \begin{cases} \frac{1}{\alpha_n}\left(\sqrt{1+2\alpha_n(V_{GS}-V_{TH})}\right) & ,V_{GS}-V_{TH} > 0 \\ V_{GS}-V_{TH} & ,V_{GS}-V_{TH} \le 0 \end{cases} \tag{3.43}$$

$$V_{DSsat}^{wi} \approx 4kT/q \tag{3.44}$$

where $\alpha_n = \mu_{eff}/\left(v_{sat}\cdot L\right)$.

A smoothing function is used to interpolate V_{DSS}:

$$V_{DSS} = V_{DS} - \frac{kT}{q}\frac{\ln\left\{1+\exp\left[A(V_{DS}-V_{DSsat})/(kT/q)\right]\right\}}{A} \tag{3.45}$$

where A is the parameter that controls the transition between the saturated and the non saturated channel.

Note that the lateral electric field in the saturation region is given by:

$$E_x(x) = E_{sat}\cosh\left(\frac{x-L_e}{L_c}\right) \tag{3.46}$$

where E_{sat} is the field at saturation channel point and is obtained from V_{DSsat}, under the linear field approximation in the linear region. Using eqs. (3.27) and (3.46), the carrier temperature in the saturation region can be calculated.

Note that the conventional drift-diffusion model using the mobility-field relation from eq. (3.32) is recovered if λ_w is set to 0, meaning that $v_{sat,ns}$ is equal to stationary value v_{sat} and $\gamma_n = \alpha_n$.

3.4 RF and Noise Modeling

The existing noise calculation methodologies (namely the Klaassen-Prins approach, equivalent circuit method, and impedance field method) must be adapted to model the noise in short-channel devices. A generalization of the long channel noise calculation methods to incorporate the mobility degradation is described by A.S. Roy et al. [Roy-2006] (see Annex II for a complete study). This reference shows the equivalence between these noise calculation methods in presence of velocity saturation.

In order to take into account the most important effects, such as non quasi stationary effects, the gate and drain correlation between noise sources, the tunneling gate current noise, we use the segmentation method. This method can be considered as an efficient implementation or discretisation to calculate these integrals compatible with RF CAD tools.

An accurate noise model must account for high-field effects. At high electric fields, the carrier velocity saturates, resulting in a corresponding decrease

in effective mobility [Roy-2006; Ziel-1986]. The effective channel length decreases as V_{DS} is increased beyond V_{DSsat} due to the velocity saturation region which has the length L_e [Ziel-1986]. Although channel length modulation (CLM) is also present in long-channel devices, L_e may represent a significant portion of the overall channel length in short-channel devices. All of these effects influence the channel conductance, and the noise.

Recent work has addressed these issues for MOSFETs [Roy-2005]; however, the results are incomplete since the noise model is derived using an equation which does not hold for short-channel devices. Furthermore, hot electrons exist when high electric fields in MOSFET devices cause electrons to have a carrier temperature (T_e) which varies with the electric field and exceeds the lattice temperature (T_L). This alone increases the amount of thermal noise in the device.

Under high channel electric fields, the temperature of electrons in the channel can rise above that of the lattice. This effect can increase the thermal noise of the device [Ziel-1986]. In the hydrodynamic model presented in this chapter, $T_e(x)$ is obtained from eqs. (3.27) and (3.36). As stated in chapter 2, section 2.5.2.2, in the drift-diffusion models an analytical relationship between T_e and the lateral field $E_y(y)$ must be used.

According to K. Seeger [Seeger-1973], the electron mobility is expressed as a function of the temperature:

$$\mu_{eff} = \mu_0 \sqrt{\frac{T_L}{T_e}} \tag{3.47}$$

Mobility can also be represented as a function of electric field [Roy-2005]:

$$\mu_{eff} = \frac{\mu_0}{\sqrt{1+\left(\frac{E_x}{E_c}\right)^2}} \tag{3.48}$$

From eqs. (3.47) and (3.48), we obtain:

$$T_e = T_L\left(1+\left(\frac{E}{E_c}\right)^2\right) \tag{3.49}$$

The channel conductance of each slide is [Roy-2005]:

$$g_c(x) = \frac{WQ}{\Delta x}\mu_d = \frac{WQ\left(\mu_{eff} + \mu_{eff}^{'}\cdot E_x\right)}{\Delta x}, \quad \mu_{eff}^{'} = dv/dE_x \tag{3.50}$$

Using eq. (3.48) and the expression for the differential channel conductance g_c (eq. 3.50), we can obtain a compact expression for the current noise spectral density between x and $x+\Delta x$:

$$S_{in}(x) = \overline{i_n^2} = 4k\frac{\mu_0 T_L}{\sqrt{1+\left(\frac{E}{E_c}\right)^2}}\frac{WQ(x)}{\Delta x} \tag{3.51}$$

However, ultra-thin oxides below 4 nm exhibit drastic increase of leakage current, the so called direct tunneling current [Pailloncy2-2004; Ranuarez-2005; Schuegraf-1994]. In this regime, the gate oxide capacitor introduces a shot noise current source, besides the two classical noise sources: drain and gate current noise. The impact of the direct tunneling current on high frequency noise performance becomes critical. The gate shot noise current generated in each segment of the MOSFET flows along the channel and subsequently creates a drain shot noise current, because it is uncorrelated with the origins of the drain and gate current noise. Since the direct tunneling current can be substantial, the drain shot noise

becomes comparable to the drain current noise in MOSFETs with oxides below 2 nm [Pailloncy2-2004]. The tunneling gate current (TGC) for each channel slide is given by direct tunneling current theory [Ranuarez-2005; Schuegraf-1994]:

$$J_n(y) = AE_{ox}(y)^2 e^{\frac{-B\left(1-\left(1-\frac{V_{ox}(y)}{\Phi_b}\right)^{3/2}\right)}{E_{ox}(y)}} \tag{3.52}$$

with the electric field within the oxide $E_{ox}(y)$ equal to:

$$E_{ox}(y) = E(y)\frac{\varepsilon_{Si}}{\varepsilon_{ox}} = \frac{Q + Q_{dep}}{\varepsilon_{ox}} \tag{3.53}$$

where $V_{ox}(y)$ is the voltage across the oxide ($V_{ox}(y)=E_{ox}(y)t_{ox}$), and Φ_b the barrier height equal to 3.1eV. The constants A and B are given by [Schuegraf-1994] (see chapter 2, section 2.5.2.3).

The small signal conductance $g_g(y)$ associated with the tunneling current is given by:

$$g_g(y) = W\Delta y \frac{\partial J_n(y)}{\partial E_{ox}(x)} \cdot \frac{\partial E_{ox}(y)}{\partial V_{GS}} \tag{3.54}$$

Using the nodal admittance method, the active transmission line can be analyzed [Lazaro-2006]. We start numbering the circuit nodes from source (node 1) to the drain end (node N+1), with the gate numbered as N+2. The current at circuit nodes can be written as:

$$[I_i] = [Y_{ij}] \cdot [V_i] + [i_{n,i}] \tag{3.55}$$

where I_i is the signal input current at each circuit node, V_i is the node voltage, $I_{n,i}$ is the noise current at each node, and Y_{ij} is the admittance matrix.

The current at the internal nodes is equal to zero (I_i,=*0*, for *i*=2…*N*), and the external nodes are connected to voltage bias. To obtain the external admittance and correlation matrix, the nodes are renumbered as internal nodes (i=2…N), and external nodes (nodes 1, *N*+1, *N*+2). Then, the equation system (3.55) can be written as:

$$\begin{bmatrix} \underline{0} \\ \underline{I_e} \end{bmatrix} = \begin{bmatrix} Y_{ii} & Y_{ie} \\ Y_{ei} & Y_{ee} \end{bmatrix} \cdot \begin{bmatrix} \underline{V_i} \\ \underline{V_e} \end{bmatrix} + \begin{bmatrix} \underline{i_{ni}} \\ \underline{i_{ne}} \end{bmatrix} \tag{3.56}$$

The correlation matrix between noise sources at each node can be expressed as:

$$C = \overline{\begin{bmatrix} i_{ni} \\ i_{ne} \end{bmatrix} \cdot \begin{bmatrix} i_{ni} \\ i_{ne} \end{bmatrix}^{\dagger}} = \begin{bmatrix} C_{ii} & C_{ie} \\ C_{ei} & C_{ee} \end{bmatrix} \tag{3.57}$$

The intrinsic transistor admittance matrix, Y_{int}, is given by:

$$\underline{I_e} = Y_{\text{int}} \underline{V_e} + \underline{i_e} \tag{3.58}$$

$$Y_{\text{int}} = Y_{ee} - P \cdot Y_{ie} \tag{3.59}$$

$$\underline{i_e} = \begin{bmatrix} i_g \\ i_d \end{bmatrix} = \underline{i_{ne}} - P \cdot \underline{i_{ni}} \tag{3.60}$$

where

$$P = Y_{ei} Y_{ii}^{-1} \tag{3.61}$$

Using eqs. (3.58-3.61), the admittance equivalent noise sources (i_g, i_d) can be found, and the associated correlation matrix is the intrinsic transistor correlation matrix C_{Yi} given by:

$$C_{Yi} = \begin{bmatrix} \dfrac{\overline{i_g^2}}{i_g i_d^*} & \dfrac{\overline{i_g^* i_d}}{\overline{i_d^2}} \end{bmatrix} = C_{ee} - C_{ei} \cdot P^{\dagger} - P \cdot C_{ie} + P \cdot C_{ii} \cdot P^{\dagger} \tag{3.62}$$

Equation (3.62) expresses the contribution of each channel noise source to the total noise (including the correlation coefficient) affected by a factor that can be interpreted as a generalized impedance field.

The intrinsic small signal equivalent circuit elements (Fig. 3.5) can be obtained from intrinsic *Y* parameters by identification. In order to obtain the transistor *S* parameters and noise parameters, the series parasitic resistances and inductances, and the parallel parasitic capacitance must be included. The extrinsic (including parasitic) parameters are obtained using well known relations described by A. Lazaro et al. [Lazaro-1999] and H. Hillbrand et al. [Hillbrand-1976].

For RF applications the goals are maximizing the intrinsic gain, the cut-off frequency f_T and the maximum frequency of oscillation f_{max}. From the equivalent circuit of Fig. 3.5 these parameters can be easily calculated with the following expressions [Pailloncy2-2004]:

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1 + 2C_{gd}/C_{gs}}} \approx \frac{g_m}{2\pi (C_{gs} + C_{gd})} \tag{3.63}$$

$$f_{\max} \approx \frac{g_m}{2\pi C_{gs}\sqrt{4(R_s + R_i + R_g)\left(g_{ds} + g_m \dfrac{C_{gd}}{C_{gs}}\right)}} \tag{3.64}$$

where C_{gs} and C_{gd}, including fringing and overlap capacitances calculated using expressions given by A. Bansal et al. [Bansal-2005], g_m is the gate transconductance, R_i (in series with C_{gs}) takes into account the distributed nature of the MOSFET and g_{ds} is the drain-to-source conductance. As shown in eq. (3.63-3.64), f_T depends on the ratio g_m and the total gate capacitance while f_{max} also

depends on the source/drain and gate parasitic resistances, as well as the ratio C_{gd}/C_{gs}. The overlap and fringing capacitances increase the intrinsic capacitances, reducing the cut-off frequency f_T and the maximum frequency of oscillation f_{max}.

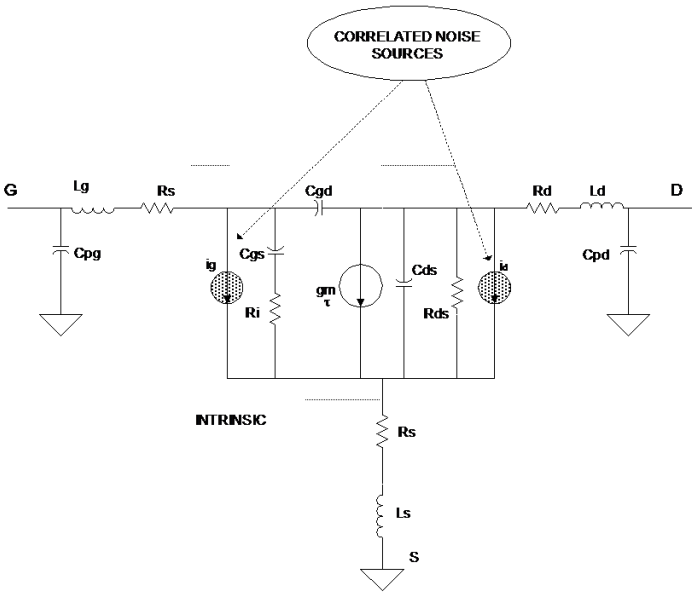


Fig. 3.5. Small-signal equivalent circuit using admittance noise source configuration for an intrinsic MOSFET.

Parasitic resistances reduce f_{max} and increase the transistor noise. The gate resistance consists of two major contributions: one contribution is the well-known silicide sheet resistance [Iniguez2-2005]; the other is the contact resistance between silicide and polysilicon [Pailloncy-2004]. The gate resistance is given by [Shenoy-2003]:

$$R_g = \frac{1}{3}\frac{R_{sheet}W}{L \cdot N_{fingers}^2 N_{contacts}^2} + \frac{\rho_{con}}{WL} \tag{3.65}$$

where R_{sheet} is the silicide gate sheet resistance, $N_{fingers}$ and $N_{contacts}$ are the number of parallel fingers and gate contacts respectively, and ρ_{con} is the silicide-to-polysilicon specific contact resistance. For this DG model, $R_{sheet}=2\ \Omega/sq$ and $\rho_{con}=0$. A distributed contact resistance model is employed for source (drain) access resistance.

3.5 RF and Noise Simulations

In order to analyze the influence of the charge and transport models, in Fig. 3.6 we compare the drain current for DG-MOSFET (N_A=6·10^{17} cm^{-3}, L=50 nm, t_{si}=5 nm, t_{ox}=1.5 nm) obtained using the classical compact model, the quantum charge model and using the drift-diffusion and hydrodynamic models. According to the simulation results from Fig. 3.3, the main differences between classical and quantum charge control models come from the shift in the threshold voltage and capacitance reduction for the quantum case. More important are the differences between the drift-diffusion and hydrodynamic models. Due to overshoot effects, the velocity, the current and transconductance are larger in the hydrodynamic model than in the drift-diffusion model.

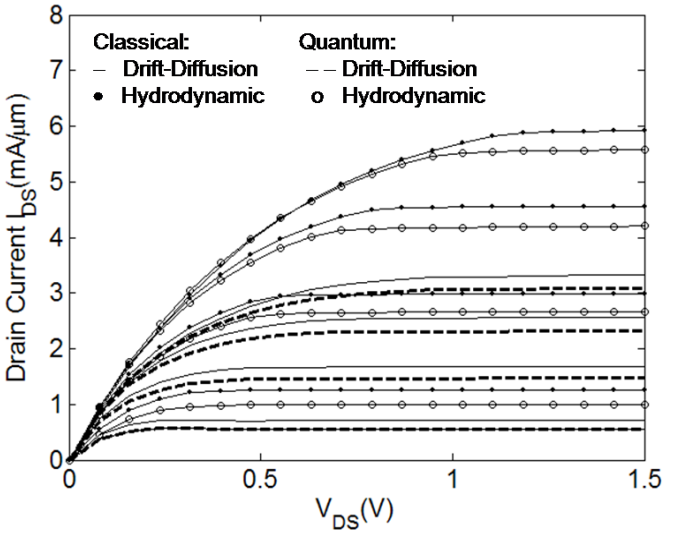


Fig. 3.6. A comparison of drain current for DG-MOSFET (N_A=6·10^{17} cm^{-3}), L=50 nm, t_{si}=5 nm, t_{ox}=1.5 nm for classical charge control (-Drift-Diffusion model, • Hydrodynamic Model) and quantum charge (-- Drift-Diffusion model, o-Hydrodynamic Model). The gate voltages are V_{GS}-V_{TH}=0.5, 1, 1.5 and 2 V.

The f_T and f_{max} computed using eqs. (3.63-3.64) as a function of gate length for a typical RF operating bias point (V_{GS}-V_{TH}=0.5V, V_{DS}=1V) are shown in Figs. 3.7 and 3.8, respectively.

We consider as an upper bound for the silicon thickness the following scaling rule, t_{si}=0.4L. In these results the differences between classical and quantum results arise from the small threshold shift between the two models and the overestimated capacitance in the classical charge control. The differences between transconductances due to the overshoot effect increases with downscaling. In the case of f_{max} the increase in transconductance due to the overshoot compensates the effect of parasitic resistances when gate length decreases.

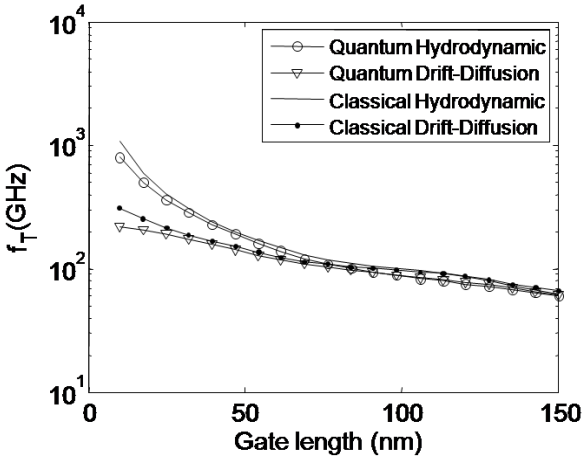


Fig. 3.7. Simulated cut-off frequency f_t versus gate length for DG-MOSFET (N_A=6·10^{17} cm^{-3}, W=10 μm, 10 fingers). V_{DS}=1 V, V_{GS}-V_{TH}=0.5V. A Comparison between the classical and quantum charge controls for the Drift-Diffusion and Hydrodynamic models.

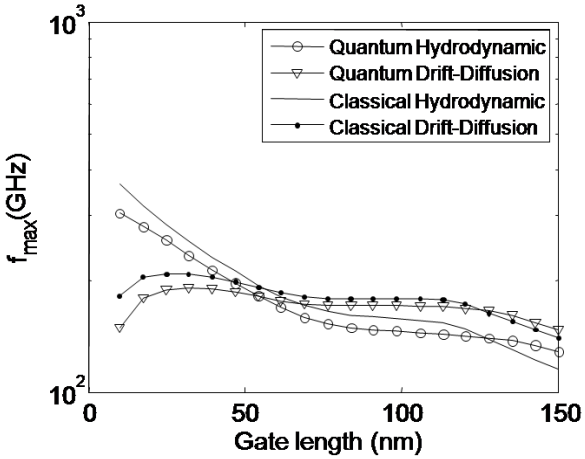


Fig. 3.8. Simulated maximum frequency of oscillation versus gate length for a DG-MOSFET (N_A=6·10^{17} cm^{-3}, W=10 μm, 10 fingers). V_{DS}=1 V, V_{GS}-V_{TH}=0.5V. A comparison between the classical and quantum charge controls for the Drift-Diffusion and Hydrodynamic models.

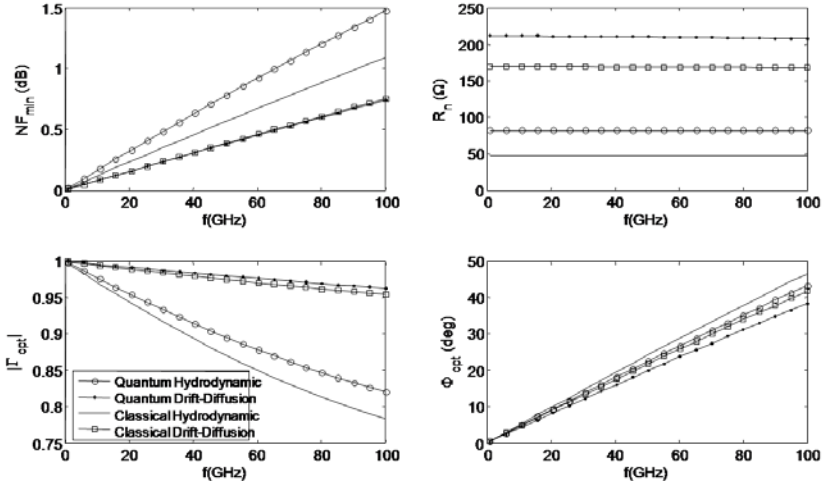


Fig. 3.9. Frequency behaviour of the Intrinsic Noise Parameters including gate current effect for DG-MOSFET (N_A=6·10^{17} cm^{-3}, L=12.5 nm, t_{si}=5nm, 10 fingers, W=10 μm, V_{GS}-V_{TH}=0.5V, V_{DS}=1V). A Comparison between the classical and quantum charge controls for the Drift-Diffusion and Hydrodynamic models.

Figures 3.9 and 3.10 show the frequency behaviour of the intrinsic noise parameters of a DG-MOSFET (N_A=6·10^{17} cm^{-3}, L=12.5 nm, *tsi*=5nm, 10 fingers, W=10 μm) for a V_{GS}-V_{TH}=0.5V, V_{DS}=1V, and V_{GS}-V_{TH}=1V, V_{DS}=1V, respectively. These figures predict important differences between the hydrodynamic and drift-diffusion models due to different carrier temperatures along the channel. Shot noise effect due to TGC is relevant for low frequency range and this effect increases with gate voltage. In Fig. 3.9 hydrodynamic models predict higher noise figure than drift-diffusion, whereas in Fig. 3.10, the behaviour is inverted. This point is justified by the increase of the carrier temperature in the saturated region. In Fig. 3.9, the transistor is in the deep saturation regime, thus the hydrodynamic model

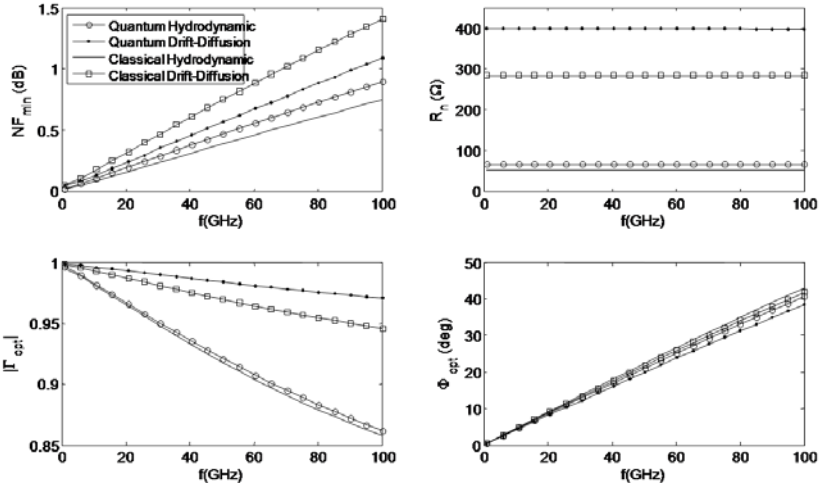


Fig. 3.10. Frequency behaviour of the Intrinsic Noise Parameters including gate current effect for DG MOSFET (N_A=6·10^{17} cm^{-3}, L=12.5 nm, t_{si}=5nm, 10 fingers, W=10 μm, V_{GS}-V_{TH}=1.0V, V_{DS}=1V). A Comparison between the classical and quantum charge controls for the Drift-Diffusion and Hydrodynamic models.

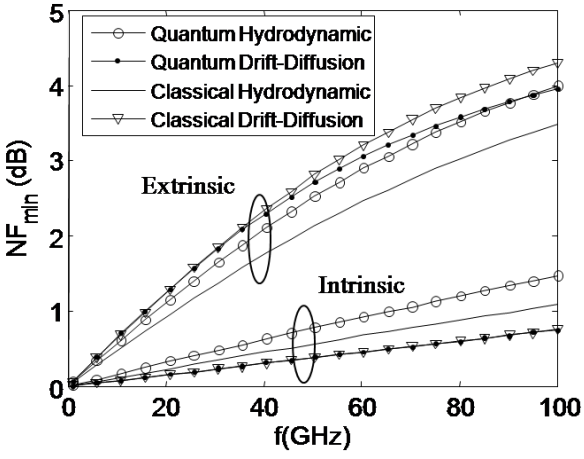


Fig. 3.11. Frequency behaviour of the intrinsic and extrinsic (with parasitics). Minimum Noise Figure for DG-MOSFET (L=12.5 nm, t_{si}=5nm , 10 fingers, W=10 μm, V_{GS}-V_{TH}=0.5V, V_{DS}=1V).

gives higher noise spectral densities in the saturation region than the drift-diffusion using the empirical model given by eq. (3.47).

Figure 3.11 shows the intrinsic and extrinsic minimum noise figures as a function of frequency for a DG-MOSFET (N_A=6·10^{17} cm^{-3}, L=12.5 nm, t_{si}=5nm, 10 fingers, W=10 μm) for a V_{GS}-V_{TH}=0.5V, V_{DS}=1V. This figure shows the need to reduce the parasitic resistances in order to achieve a good noise figure performance at room temperature.

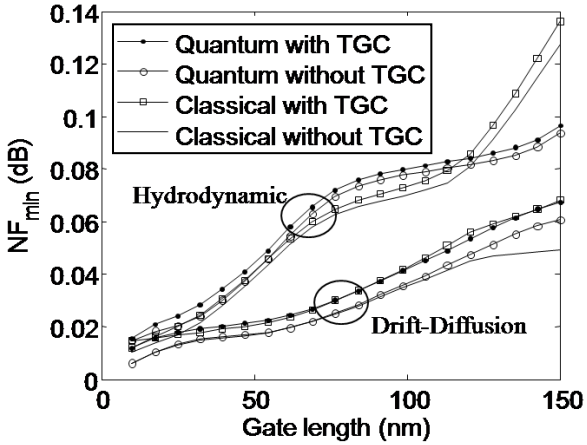


Fig. 3.12. Intrinsic Minimum Noise Figure for DG MOSFET (t_{ox}=1.5nm, t_{si}=0.4L , 10 fingers, W=10 μm, V_{GS}-V_{TH}=0.5V, V_{DS}=1V, f=1GHz) as a function of the gate length including TGC noise contribution and without TGC.

To investigate the downscaling effect in the noise figure, Fig. 3.12 shows the minimum noise figure at 1 GHz as a function of gate length for a DG

(N_A=6·10^{17} cm^{-3}, L=12.5 nm, t_{si}=5nm, 10 fingers, W=10 μm, t_{si}=0.4L, V_{GS}-V_{TH}=0.5V, V_{DS}=1V). This figure shows the small effect in DG-MOSFET of the TGC effect for this typical point. Fig. 3.13 shows the extrinsic minimum noise figure for the same device and bias conditions. This figure shows that the increase in the transconductance due to the velocity overshoot phenomenon taking into account in the hydrodynamic models compensates the higher parasitic resistance caused by downscaling. For this bias point, the hydrodynamic model predicts higher noise figures due to a higher noise temperature along the channel, especially in the saturation region.

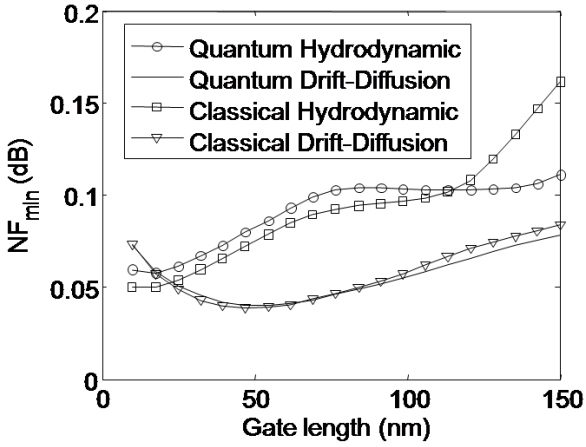


Fig. 3.13. Extrinsic Minimum Noise Figure for DG-MOSFET (t_{ox}=1.5nm, t_{si}=0.4L, 10 fingers, W=10 μm, V_{GS}-V_{TH}=0.5V, V_{DS}=1V, f=1GHz) as a function of the gate length including TGC noise contribution.

3.6 Analytical Determination of Drain and Gate Noise Spectrums

In this section, compact analytical expressions to model the gate and drain current noise spectrum noise densities and their correlation in short channel symmetric DG MOSFETs are developed. These expressions depend on the mobile charge density and the drain current. We use here the Compact Model for Symmetric Doped Double-Gate (SDDG) MOSFETs [Cerdeira-2008] in order to obtain the analytical expressions for charge and current. In this model, the mobile charge density is calculated using analytical expressions obtained from modeling the surface potential and the difference of potentials at the surface and at the center of the Si doped layer without the need to solve any transcendental equations. In addition, this model could be applied to channel doped DG MOSFETs [Cerdeira2-2008] including short channel effects. The compact analytical expressions obtained for different noise magnitudes will be compared with the results obtained with the segmentation method. Finally, using the possibilities of the analytical expressions, the compact noise model will be applied to analyze the high frequency noise performance of these devices and some trends related to their variation with the downscaling will be provided. In this section, the noise properties of the devices are discussed.

3.6.1 Charge and DC Current Models

The DG structure as well as the simpler schematic view of the DG under analysis is shown in Fig. 3.14 ((a) and (b), respectively), where N_A is the uniform acceptor concentration in the silicon layer with thickness equal to t_{si}; t_{ox} is the equivalent

gate dielectric thickness and L is the channel length. The transistor is symmetrical, with both gates connected together at V_G.

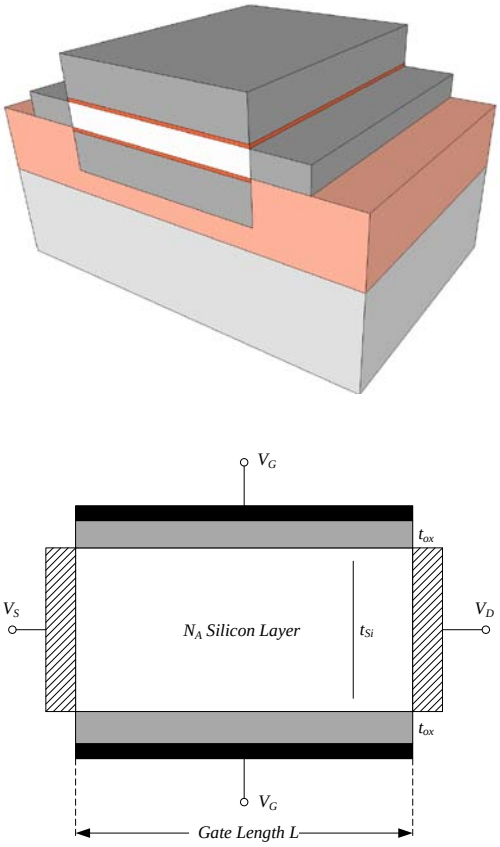


Fig. 3.14. (a) 3D representation of the DG structure; (b) Simplified schematic view of the DG used in simulations

As a reminder (see chapter 2, section 2.5.2.2), the drain and gate spectral densities and the correlation matrix are given by:

$$S_{i_d^2} = \overline{i_d^2} = \frac{1}{I_D L_c^2} \int_{V_S}^{V_D} \frac{g_c(V)^2}{g(V)} S_{i_n} dV \tag{3.66}$$

$$S_{i_g^2} = \overline{i_g^2} = \frac{\omega^2 W^2}{I_D^5 L_c^2} \int_{V_S}^{V_D} \left(\int_{V_S}^{V_D} g_c(V')(Q(V') - Q(V)) dV' \right)^2 \frac{g_c(V)^2}{g(V)} S_{i_n} dV \tag{3.67}$$

$$S_{i_g i_d^*} = \overline{i_g i_d^*} = \frac{j\omega W}{I_D^3 L_c^2} \int_{V_S}^{V_D} \left(\int_{V_S}^{V_D} g_c(V')(Q(V') - Q(V)) dV' \right) \frac{g_c(V)^2}{g(V)} S_{i_n} dV \tag{3.68}$$

where

$$\frac{g_c(V,E)}{g(V,E)} = \frac{g(V,E)}{g(V,E) + \dfrac{\partial g(V,E)}{\partial E} E} \tag{3.69}$$

and the corrected length L_c is given by:

$$L_C = \int_0^L \frac{g_c}{g} dx = L \frac{\int_{V_S}^{V_D} g_c(V) dV}{\int_{V_S}^{V_D} g(V) dV} \tag{3.70}$$

The power spectral density for the local noise source is given by:

$$S_{i_n}(x) = 4kT_L \frac{g_c(x)}{g(x)} \frac{T_n(x)}{T_L} \tag{3.71}$$

In order to calculate the integrals with respect to the potential in eqs. (3.66-3.68), we will obtain a relation between the mobile channel charge Q and the channel potential V at each channel point x. The electric field at the surface of the silicon layer E_s is calculated using Poisson's equation. The following expression is obtained for E_s as a function of the potential at the surface, ϕ_S and at the center of the layer ϕ_0:

$$E_S = \sqrt{\frac{2qN_A\phi_t}{\varepsilon_{Si}}}\sqrt{\left(\frac{\phi_S-\phi_0}{\phi_t}\right)+\left(1-e^{-\left(\frac{\phi_S-\phi_0}{\phi_t}\right)}\right)e^{\frac{\phi_S-2\phi_F-V}{\phi_t}}} \tag{3.72}$$

where $\phi_t = kT/q$ is the thermal potential, k is the Boltzmann constant; q is the electron charge, T is the temperature in K, ε_{Si} is the silicon dielectric permittivity and ϕ_F is the Fermi potential.

A. Cerdeira et al. [Cerdeira-2008], using a detailed numerical calculation, found an empirical expression for the difference of potentials $\phi_S - \phi_0$ as a function of the potential difference $V_{GS} - V$. The surface electric field is analytically calculated using the Lambert function. The charge carrier concentration q_n along the channel Q normalized to $C_{ox}\phi_t$ is determined through the following relation with the surface electric field at each interface:

$$q_n = \frac{\varepsilon_{Si}E_s}{C_{ox}\phi_t} - \frac{q_b}{2} \tag{3.73}$$

with

$$q_b = \frac{qN_A t_{Si}}{C_{ox}\phi_t} \tag{3.74}$$

where t_{si} is the silicon thickness and C_{ox} is the oxide capacitance, $C_{ox}=\varepsilon_{ox}/t_{ox}$.

For the typical operating voltage range in this type of transistors it can be shown that [Cerdeira-2008]:

$$dV = -\phi_t\left[1+\frac{1}{q_n}+\frac{1}{q_n+q_b}\right]dq_n \tag{3.75}$$

Using eq. (3.75), the channel charge can be integrated. Then, the drain current taking into account the velocity saturation and short channel effects is given by (37) in [Cerdeira-2008].

$$I_D = \int_0^{V_{Dsat}} g(V)dV = \frac{2W\mu C_{ox}\phi_t^2}{L_e}\left\{\frac{q_S^2 - q_D^2}{2} + 2(q_S - q_D) - q_b \ln\frac{q_S + q_b}{q_D + q_b}\right\} \tag{3.76}$$

where q_S and q_D represent the normalized charge q_n evaluated at the source $q_n(V=0)$ and at the effective drain voltage $q_n(V=V_{Defs})$ respectively, and $L_e=L-\Delta L$, where ΔL is the channel length modulation in the saturation region given by eq. (36) in [Cerdeira-2008]. The mobility is given by a more generalized form of eq. (3.48), as:

$$\mu = \frac{\mu_0}{\left(1+\left(\frac{E}{E_C}\right)^p\right)^{1/p}} \tag{3.77}$$

3.6.2 Compact Expressions

Conventional compact models use the mobility-longitudinal field relation (see eq. 3.77) with p=1, however, for an accurate description of the velocity saturation we will use p=2, as used in the SDDG model. Using the mobility model from eq. (3.77) with p=2, we obtain the following expression for the channel per unit length conductance:

$$g(V) = \frac{WQ\mu_0}{\sqrt{1+\left(E/E_c\right)^2}} = \frac{g_0}{\sqrt{1+\left(E/E_c\right)^2}} \tag{3.78}$$

with

$$g_0 = WQ(V)\mu_0 = 2WC_{ox}\phi_t\mu_0 q_n(V) \tag{3.79}$$

From (3.69) and (3.71), we obtain:

$$g_c(V) = g(V)\cdot\left(1+\left(E/E_c\right)^2\right) = g_0\sqrt{1+\left(E/E_c\right)^2} \tag{3.80}$$

The heating effect of the electrons plays an important role in the study of the noise in deep nanometric devices. In order to investigate this effect, we start from the case where there is no heating effect, and the noise temperature is equal to the lattice temperature. Thus, we have:

$$\frac{g_c(V)}{g(V)}\frac{T_n}{T_L} = 1+\left(E/E_c\right)^2 \tag{3.81}$$

$$S_{i_d^2} = \frac{4kT_L}{I_D L_c^2}\int_{V_S}^{V_D} g^2\left(\frac{g_c}{g}\frac{T_n}{T_L}\right)dV = \frac{4kT_L}{I_D L_c^2}\int_{V_S}^{V_D} g_0^2 dV = \frac{4kT_L}{I_D L_c^2}(2W\mu_0 C_{ox}\phi_t)^2\int_{V_S}^{V_D} q_n^2 dV \tag{3.82}$$

According to C.H. Chen et al. [Chen-2002], the contribution of the velocity saturation region to the output noise current is negligible as the carriers in that region travel at their saturation velocity v_{sat} and they do not respond to the fluctuations of the electric field caused by the voltage noise in that region. Thus, the integrals (3.66-3.68), and (3.70) must be integrated up to the saturation channel voltage or the effective voltage [Cerdeira-2008] V_{Def} and L in (3.70) must be replaced by L_e in short channel devices to take into account the channel length modulation effect.

Substituting the expression of dV (3.75) in (3.82), the following compact expression for the drain noise spectral density is obtained:

$$S_{i_d^2} = \frac{4kT_L}{I_D L_c^2}(2W\mu_0 C_{ox}\phi_t)^2 F \tag{3.83}$$

where

$$F = -\phi_t\left[\frac{q_n^3}{3} - q_n^2 - q_n q_b + q_b^2 \ln(q_n + q_b)\right]_{q_S}^{q_D} \tag{3.84}$$

Substituting (3.77) in the current equation, we obtain:

$$g = \left[g_0^2 - \left(\frac{I_D}{E_c}\right)^2\right]^{1/2} = (2W\mu_0 C_{ox}\phi_t)\left[q_n^2 - q_a^2\right]^{1/2} \tag{3.85}$$

$$g_c = \frac{g_0^2}{\left[g_0^2 - \left(\frac{I_D}{E_c}\right)^2\right]^{1/2}} = \left(2W\mu_0 C_{ox}\phi_t\right)\frac{q_n^2}{\left[q_n^2 - q_a^2\right]^{1/2}} \tag{3.86}$$

where q_a is defined as:

$$q_a = \frac{I_D}{2W\mu_0 C_{ox}\phi_t E_c} \tag{3.87}$$

Before evaluating the gate spectral density (3.67) and the cross spectral density (3.68), we need to calculate the integral:

$$\begin{aligned}
&\int_{V_S}^{V_D} g_c(V')(Q(V')-Q(V))dV' = \\
&= \int_{V_S}^{V_D} \left(2W\mu_0 C_{ox}\phi_t q_n^2(V')\left[q_n^2(V')-q_a^2\right]^{-1/2}\right) 2C_{ox}\phi_t (q_n(V')-q_n(V))dV' \\
&= 2C_{ox}\phi_t \cdot 2W\mu_0 C_{ox}\phi_t \left[\left(\int_{V_S}^{V_D} q_n^3(V')\left[q_n^2(V')-q_a^2\right]^{-1/2} dV'\right)\right. \\
&\left. - q_n(V)\left(\int_{V_S}^{V_D} q_n^2(V')\left[q_n^2(V')-q_a^2\right]^{-1/2} dV'\right)\right] \\
&= 2C_{ox}\phi_t \cdot 2W\mu_0 C_{ox}\phi_t \left(A + Bq_n(V)\right)
\end{aligned} \tag{3.88}$$

where we have used expression (3.75) to perform a change of variables to integrate with respect to the normalized charge q_n.

A and B are defined using the functions q_S and q_D as:

$$\begin{aligned}
A = -\phi_t \Bigg[&-\frac{q_b^3}{(q_n^2 - q_a^2)^{1/2}} \ln(q_n + q_b) + (q_n^2 - q_a^2)^{1/2}\left(\frac{1}{3}q_n^2 + \frac{2}{3}q_a^2 + q_n - q_b\right) \\
&+ \frac{q_b^3}{(q_n^2 - q_a^2)^{1/2}} \ln\left(\begin{array}{l} 2q_b^2 - 2q_a^2 - 2(q_n + q_b)q_b + 2(q_b^2 - q_a^2)^{1/2}((q_n + q_b)^2 \\ -2(q_n + q_b)q_b + q_b^2 - q_a^2)^{1/2} \end{array}\right) \\
&+ \left(q_a^2 + q_b^2\right)\ln(q_n + (q_n^2 - q_a^2)^{1/2})\Bigg]_{q_S}^{q_D}
\end{aligned} \tag{3.89}$$

$$\begin{aligned}
B = \phi_t \Bigg[&\left(\frac{1}{2}q_n + 2\right)(q_n^2 - q_a^2)^{1/2} + \left(\frac{1}{2}q_a^2 - q_b\right)\ln\left(q_n + (q_n^2 - q_a^2)^{1/2}\right) \\
&+ \frac{q_b^2}{(q_b^2 - q_a^2)^{1/2}}\ln(q_n + q_b) - \frac{q_b^2}{(q_b^2 - q_a^2)^{1/2}}\ln(2q_b^2 - 2q_a^2 - 2(q_n + q_b)q_b + \\
&2(q_b^2 - q_a^2)^{1/2}((q_n + q_n)^2 - 2(q_n + q_b)q_b + q_b^2 - q_a^2)^{1/2})\Bigg]_{q_S}^{q_D}
\end{aligned} \tag{3.90}$$

Using (3.88) the following compact analytical expressions for (3.67) and (3.68) are found:

$$S_{i_g^2} = \frac{\omega^2 W^2}{I_D^5 L_c^2}\left(\int_{V_S}^{V_D}\left(\int_{V_S}^{V_D} g_c(V')(Q(V')-Q(V))dV'\right)^2 \frac{g_c^2(V)}{g(V)} S_{i_n} dV\right)$$

$$= \frac{\omega^2 W^2}{I_D^5 L_c^2} 4kT_L \cdot \left(2W\mu_0 C_{0x}\phi_t\right)^2 \left(2C_{ox}\phi_t\right)^2 \left(\int_{V_S}^{V_D}\left(A+Bq_n(V)\right)^2 g_0^2(V)dV\right)$$

$$= \frac{\omega^2 W^2}{I_D^5 L_c^2} 4kT_L (2W\mu_0 C_{ox}\phi_t)^2 \left(2W\mu_0 C_{0x}\phi_t\right)^2 \left(2C_{ox}\phi_t\right)^2 \tag{3.91}$$

$$\cdot\left(\int_{V_S}^{V_D}\left(A+Bq_n(V)\right)^2 q_n^2(V)dV\right)$$

$$= \frac{\omega^2 W^2}{I_D^5 L_c^2} 4kT_L \cdot (2W\mu_0 C_{ox}\phi_t)^4 \left(2C_{ox}\phi_t\right)^2 \left(\int_{V_S}^{V_D}\left(A+Bq_n(V)\right)^2 q_n^2(V)dV\right)$$

where

$$\int_{V_S}^{V_D}\left(A+Bq_n(V)\right)^2 q_n^2(V)dV = A^2\int_{V_S}^{V_D} q_n^2(V)dV + 2AB\int_{V_S}^{V_D} q_n^3(V)dV + B^2\int_{V_S}^{V_D} q_n^4(V)dV$$
$$= A^2C + 2ABD + B^2E \tag{3.92}$$

and the functions *C*, *D*, *E* are defined as:

$$C = \int_{V_S}^{V_D} q_n^2(V)dV = -\phi_t\left[\frac{q_n^3}{3} + q_n^2 - q_b q_n + q_b^2 \ln\left(q_n + q_b\right)\right]_{q_S}^{q_D} \tag{3.93}$$

$$D = \int_{V_S}^{V_D} q_n^3(V)dV = -\phi_t\left[\frac{q_n^4}{4} + \frac{2q_n^3}{3} - \frac{q_b}{2}q_n^2 + q_b^2 q_n - q_b^3 \ln(q_n + q_b)\right]_{q_S}^{q_D} \tag{3.94}$$

$$E = \int_{V_S}^{V_D} q_n^4(V)dV = -\phi_t\left[\frac{q_n^5}{5} + \frac{q_n^4}{2} - \frac{q_b}{3}q_n^3 + \frac{1}{2}q_b^2 q_n^2 - q_b^3 q_n + q_b^4 \ln(q_n + q_b)\right]_{q_S}^{q_D} \tag{3.95}$$

The cross noise spectral density is calculated by:

$$S_{i_g i_d^*} = \frac{j\omega W}{I_D^3 L_c^2}\left(\int_0^{V_D}\left(\int_0^{V_D} g_c(V')(Q(V')-Q(V))dV'\right)\frac{g_c^2(V)}{g(V)}S_{i_n}dV\right)$$

$$= \frac{j\omega W}{I_D^3 L_c^2} 4kT_L \cdot 2W\mu_S C_{ox}\phi_t \cdot (2C_{ox}\phi_t)\int_0^{V_D}(A+Bq_n(V))\,g_0^2(V)dV \qquad (3.96)$$

$$= \frac{j\omega W}{I_D^3 L_c^2} 4kT_L \cdot (2W\mu_S C_{ox}\phi_t)^3 \cdot (2C_{ox}\phi_t)\int_0^{V_D}(A+Bq_n(V))\,q_n^2(V)dV$$

where

$$\int_{V_S}^{V_D}(A+Bq_n(V))\,q_n^2(V)dV = A\int_{V_S}^{V_D} q_n^2(V)dV + B\int_{V_S}^{V_D} q_n^3(V)dV = AC+BD \qquad (3.97)$$

Finally, the gate and cross spectral densities are given by:

$$S_{i_g^2} = \frac{\omega^2 W^2}{I_D^5 L_c^2} 4kT_L \cdot (2W\mu_0 C_{ox}\phi_t)^4 (2C_{ox}\phi_t)^2 (A^2C + 2ABD + B^2E) \qquad (3.98)$$

$$S_{i_g i_d^*} = \frac{j\omega W}{I_D^3 L_c^2} 4kT_L \cdot (2W\mu_0 C_{ox}\phi_t)^3 (2C_{ox}\phi_t)(AC+BD) \qquad (3.99)$$

These expressions depend on the drain current I_D, and expressions A, B, C, D, E which are functions of q_S and q_D. The length L_c is given by expression (3.70). Using (3.78) and (3.85-3.86), L_c is given by:

$$L_c = L\frac{B}{G} \qquad (3.100)$$

where

$$
\begin{aligned}
G &= \phi_t \int_{q_S}^{q_D} \left(q_n^2 - q_a^2\right)^{1/2} \left(1 + \frac{1}{q_n} + \frac{1}{q_n + q_b}\right) dq_n = \\
&\phi_t \left[\left(\frac{1}{2} q_n + 1\right)(q_n^2 - q_a^2)^{1/2} - \frac{1}{2} q_a^2 \ln(q_n + (q_n^2 - q_a^2)^{1/2}) \right. \\
&+ \frac{q_a^2}{(-q_a^2)^{1/2}} \left(\ln(-2q_a^2 + 2(-q_a^2)^{1/2}(q_n^2 - q_a^2)^{1/2}) - \ln q_n \right) + G_1^{1/2} - q_b \ln(q_n + G_1^2) \\
&-(q_b^2 - q_a^2)^{1/2} \\
&\left. \cdot \left(\ln(2q_b^2 - 2q_a^2 - 2(q_n + q_b)q_b + 2(q_b^2 - q_a^2)^{1/2} G_1^{1/2}) - \ln(q_n + q_b) \right) \right]_{q_S}^{q_D}
\end{aligned}
\tag{3.101}
$$

and

$$
G_1 = (q_n + q_b)^2 - 2(q_n + q_b)q_b + q_b^2 - q_a^2 \tag{3.102}
$$

However, if we consider the heating effect of electrons, then the noise temperature is no longer equal to the lattice temperature, but to the electron temperature (T_n=T_e). In this case, eq. (3.81) must be replaced by:

$$
\frac{g_c(V)}{g(V)} \frac{T_n}{T_L} = \left(1 + \left(E / E_c\right)^2\right)^2 \tag{3.103}
$$

where the electric field can be expressed as a function of the normalized charge q_n:

$$
(E / E_c)^2 = \frac{\left(q_a / q_n\right)^2}{1 - \left(q_a / q_n\right)^2} \tag{3.104}
$$

Using eq. (3.194-new), the drain, gate and cross noise spectral densities can be analytically obtained, following the same procedure as the non-heated case. The new expressions for *A*, *B*, *C*, *D*, *E* and *F* when the heating effects are considered are:

$$A = -\phi_t[-q_0^3 / (q_n^2 - q_a^2)^{1/2} \ln(q_n + q_0) + (q_n^2 - q_a^2)^{1/2} (q_n^2 / 3 + 2q_a^2 / 3 + q_n - q_0) + q_0^3 / (q_n^2 - q_a^2)^{1/2} \ln(2q_0^2 - 2q_a^2 - 2(q_n + q_0)q_0 + 2(q_0^2 - q_a^2)^{1/2}((q_n + q_0)^2 - 2(q_n + q_0)q_0 + q_0^2 - q_a^2)^{1/2}) + (q_a^2 + q_0^2) \ln(q_n + (q_n^2 - q_a^2)^{1/2})]_{q_S}^{q_D} \quad (3.105)$$

$$B = \phi_t \left[(q_n / 2 + 2)(q_n^2 - q_a^2)^{1/2} + \left(q_a^2 / 2 - q_0\right) \ln\left(q_n + (q_n^2 - q_a^2)^{1/2}\right) + q_0^2 / (q_0^2 - q_a^2)^{1/2} \ln(q_n + q_0) - q_0^2 / (q_0^2 - q_a^2)^{1/2} \ln(2q_0^2 - 2q_a^2 - 2(q_n + q_0)q_0 + 2(q_0^2 - q_a^2)^{1/2}((q_n + q_n)^2 - 2(q_n + q_0)q_0 + q_0^2 - q_a^2)^{1/2}) \right]_{q_S}^{q_D} \quad (3.106)$$

$$C = -\phi_t \left[1/3q_n^3 + q_n^2 - q_n q_0 + q_a^2 q_n - q_a^3 / (2q_0 - 2q_a) \ln(q_n + q_a) q_0 + q_a^2 / (2q_0 - 2q_a) \ln(q_n + q_a) q_0 - 2q_a^3 / (2q_0 - 2q_a) \ln(q_n + q_a) + q_a^4 / (2q_0 - 2q_a) \ln(q_n + q_a) + 1/(q_0^2 - q_a^2) q_0^4 \ln(q_n + q_0) + q_a^3 / (2q_a + 2q_0) \ln(q_n - q_a) q_0 + q_a^2 / (2q_a + 2q_0) \ln(q_n - q_a) q_0 + 2q_a^3 / (2q_a + 2q_0) \ln(q_n - q_a) + q_a^4 / (2q_a + 2q_0) \ln(q_n - q_a) \right]_{q_S}^{q_D} \quad (3.107)$$

$$D = -\phi_t \left[1/4q_n^4 + 2/3q_n^3 - 1/2q_n^2 q_0 + 1/2q_n^2 q_a^2 + q_0^2 q_n + 2q_a^2 q_n + q_a^4 / (2q_0 - 2q_a) \ln(q_n + q_a) q_0 - q_a^3 / (2q_0 - 2q_a) \ln(q_n + q_a) q_0 + q_a^4 / (q_0 - q_a) \ln(q_n + q_a) - q_a^5 / (2q_0 - 2q_a) \ln(q_n + q_a) - 1/(q_0^2 - q_a^2) q_0^5 \ln(q_n + q_0) + q_a^4 / (2q_a + 2q_0) \ln(q_n - q_a) q_0 + q_a^3 / (2q_a + 2q_0) \ln(q_n - q_a) q_0 + 2q_a^4 / (2q_a + 2q_0) \ln(q_n - q_a) + q_a^5 / (2q_a + 2q_0) \ln(q_n - q_a) \right]_{q_S}^{q_D} \quad (3.108)$$

$$E = -\phi_t[1/5q_n^5 + 1/2q_n^4 - 1/3q_n^3 q_0 + 1/3q_a^2 q_n^3 + q_n^2 q_a^2 + 1/2q_n^2 q_0^2 - q_a^2 q_n q_0 + q_a^4 q_n - q_0^3 q_n - q_a^5 / (2q_0 - 2q_a) \ln(q_n + q_a) q_0 + q_a^4 / (2q_0 - 2q_a) \ln(q_n + q_a) q_0 - 2q_a^5 / (2q_0 - 2q_a) \ln(q_n + q_a) + q_a^6 / (2q_0 - 2q_a) \ln(q_n + q_a) + q_0^6 / (q_0^2 - q_a^2) \ln(q_n + q_0) + q_a^5 / (2q_a + 2q_0) \ln(q_n - q_a) q_0 + q_a^4 / (2q_a + 2q_0) \ln(q_n - q_a) q_0 + 2q_a^5 / (2q_a + 2q_0) \ln(q_n - q_a) + q_a^6 / (2q_a + 2q_0) \ln(q_n - q_a)]_{q_S}^{q_D} \quad (3.109)$$

$$
\begin{aligned}
F = -\phi_t[&1/3q_n^3 + q_n^2 - q_n q_0 + q_a^2 q_n - q_a^4/(-2q_0 + 2q_a)\ln(q_n + q_a) + \\
&2q_a^3/(-2q_0 + 2q_a)\ln(q_n + q_a) - q_a^3/(-2q_a + 2q_0)\ln(q_n + q_a)q_0 \\
&-q_a^2/(-2q_0 + 2q_a)\ln(q_n + q_a)q_0 + q_a^4/(2q_a + 2q_0)\ln(q_n - q_a) + \\
&q_a^3/(2q_a + 2q_0)\ln(q_n - q_a)q_0 + 2q_a^3/(2q_a + 2q_0)\ln(q_n - q_a) \\
&q_a^2/(2q_a + 2q_0)\ln(q_n - q_a)q_0 - q_0^4/(-q_0^2 + q_a^2)\ln(q_n + q_0)]_{q_S}^{q_D}
\end{aligned}
\tag{3.110}
$$

According to several authors [Deen-2006], the velocity saturation effect only contributes to the total noise in the linear part of the channel. It was successfully shown by M.J. Deen et al. [Deen-2006] that the contribution of the velocity saturation region to the output noise current is negligible as the carriers in that region travel at their saturation velocity v_{sat} and they do not respond to the fluctuations of the electric field caused by voltage noise in that region. This argument has been the basis of most of the channel noise models published. In the saturation region of the channel, we can expect that T_n will be higher than the electronic temperature (T_e), but these noise fluctuations are not collected at the terminals. For this reason, for the integrals involved in eqs. (4.35-4.37), the upper limit V_D must be replaced by V_{Dsat} (see eq. 4.49) in the saturation region ($V_{DS} > V_{DSsat}$).

3.6.3 Results and Discussion

Although the spectral densities (3.83, 3.98 and 3.99) allow circuit simulators to analyze noise performances, in order to compare different devices, some noise models have been proposed in the literature for MOSFETs. Following Van der Ziel notation [Ziel-1986], the drain current noise spectrum density is expressed as:

$$S_{i_d^2} = 4kT_L g_{ds0}\gamma \tag{3.111}$$

where $4kT_L g_{ds0}$ is the current noise spectrum associated to a conductance g_{ds0} at temperature T_L. In the case of a MOSFET, however, since a channel conductance g_{ds} depends on a bias voltage, g_{ds} is fixed to the value obtained when V_{DS}=0 (g_{ds0}=g_{ds}(V_{DS}=0)). The noise excess factor γ is used to evaluate the characteristics of the thermal noise. For V_{DS}=0, γ=*1* due to the fact that the channel acts like a conductance of value g_{ds0}. In the case of long channel, it has been found experimentally and theoretically that $2/3 \leq \gamma \leq 1$ in a linear region and γ converges to 2/3 in the saturation region.

As mentioned above, the physical origin of the induced-gate noise (S_{ig}^2) is the capacitive coupling of the channel conductance to the gate capacitance. Based on this assumption, van der Ziel derived a simple expression:

$$S_{i_g^2} = 4kT_L g_g \beta, \quad g_g = \frac{\left(\omega C_{gs}\right)^2}{5g_{ds0}} \tag{3.112}$$

where C_{gs} is the gate-source capacitance. The expression is valid in the saturation region for frequencies below 1/3 of the cut-off frequency f_T and this frequency range is sufficient for most real applications of the device. Theoretically, the gate excess noise factor, β, tends to 4/3 and the imaginary part of coefficient *Im(C)* tends to 0.4 in saturation for the case of long channel.

In order to verify the compact expressions presented in the previous section, we have compared the drain and gate current noise spectral densities, and the imaginary part of correlation coefficient calculated using the segmentation method and the compact model SDDG. Figures 3.15 and 3.16 show the results as a function of gate voltage and drain voltage, respectively, for a long channel (*L*=1

μm) case using a constant mobility without transversal degradation. A good agreement between the two methods is obtained in all the range of interest.

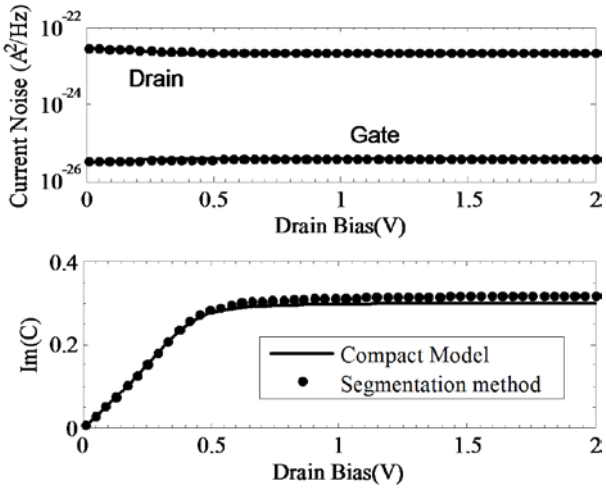


Fig. 3.15. Comparison of current noise densities and imaginary part of correlation coefficient as function of drain voltage calculated with the segmentation method (●) and compact model SDDG (—) for long channel case (L=1 μm, t_{ox}=2 nm, t_{si}=34 nm, V_{GS}=1V, f=1 GHz).

For this case, Fig. 3.17 shows the drain and gate excess noise factors for the case of Fig. 3.15 using the constant mobility model. These figures show that excess noise parameters and correlation coefficient tend to classical van der Ziel MOSFET theory when constant mobility model is used.

In a conventional Klaassen-Prins noise determination method, the drain spectrum density is calculated as (3.82) with g_c=g and L_c=L (or the effective length L_e in short channel case):

$$S_{i_d^2} = \frac{4kT_L}{I_D L^2}\int_{V_S}^{V_D} g^2(V)dV = \frac{4kT_L}{I_D L^2}\int_{V_S}^{V_D}\left(g_0^2(V) - \left(I_D / E_c\right)^2\right)dV \tag{3.113}$$

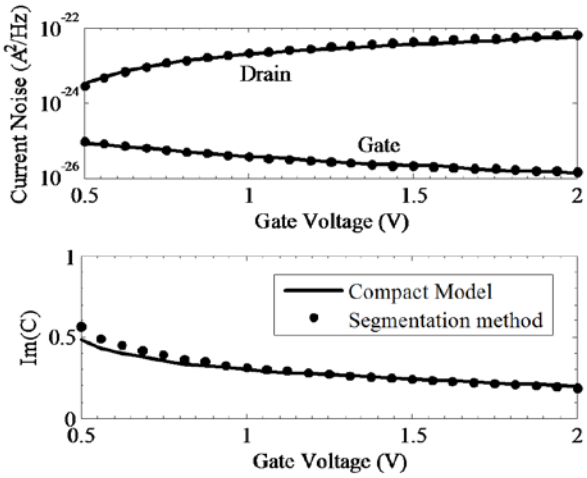


Fig. 3.16. Comparison of current noise densities and imaginary part of correlation coefficient as function of gate voltage calculated with the segmentation method (●) and compact model SDDG (—) for long channel case (L=1 μm, t_{ox}=2 nm, t_{si}=34 nm, V_{DS}=2V, f=1 GHz).

Following a similar procedure, integral (3.113) could be analytically calculated as function of q_S and q_D using (3.75).

Figure 3.18 compares the results obtained using the segmentation method, the new compact analytical model SDDG and the analytical model using the conventional KP approach (3.113) for a SDDG MOSFET with L=0.5 μm and V_{DS}=2V. A good agreement between the three methods is obtained for low drain currents. When V_{GS} is increased, the difference between g and g_0 is greater, thus

(3.113) and (3.82) produce different results. Moreover, when the gate length L_c decreases, it differs from the effective length L_e.

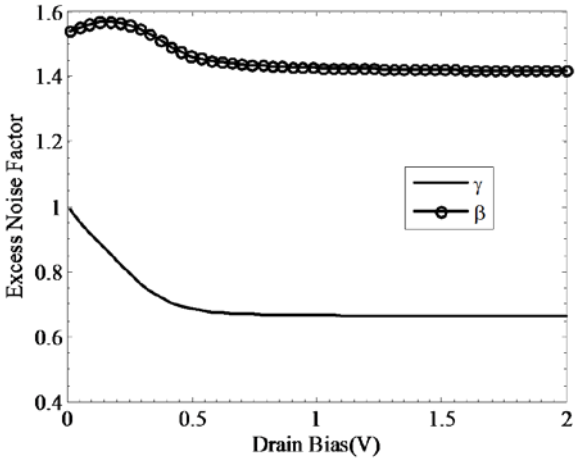


Fig. 3.17. Drain and gate excess noise factors as function of drain voltage for long channel case (L=1 μm, t_{ox}=2 nm, t_{si}=34 nm, V_{GS}=1V).

Figure 3.19 shows the ratio between the corrected length and effective length L_c/L_e in saturation for different gate lengths. The corrected length tends to L for the long channel case, but it can be up to 1.25 times higher than the effective length for short channel cases.

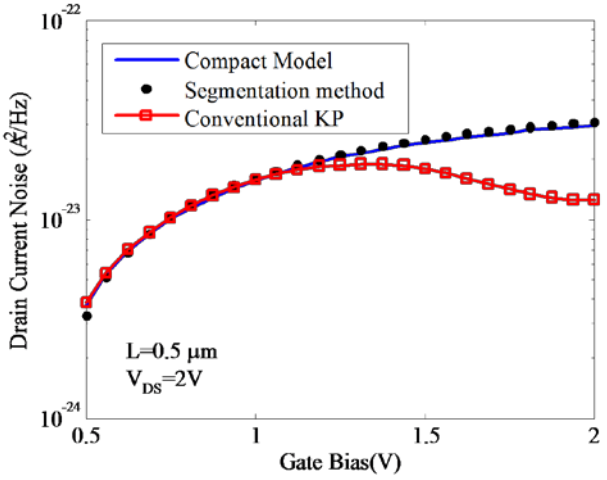


Fig. 3.18. Drain current noise density as function of gate voltage calculated using the segmentation method, the compact model SDDG and the analytical model using conventional Klassen-Prins approach (L=0.5 µm, t_{ox}=2 nm, t_{si}=34 nm, V_{DS}=2V).

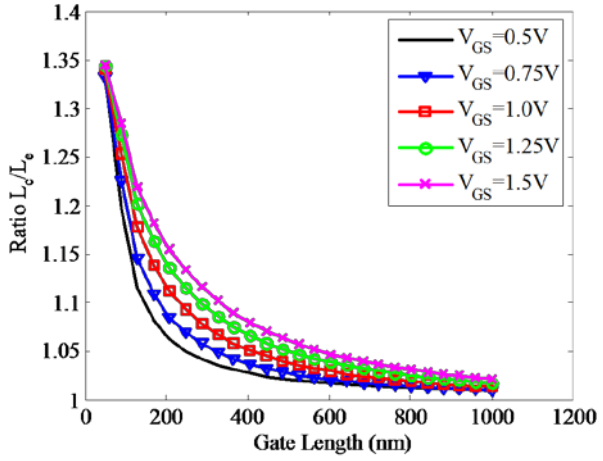


Fig. 3.19. Normalised corrected length L_c/L as function of gate length (t_{ox}=2 nm, t_{si}=34 nm, V_{DS}=2V).

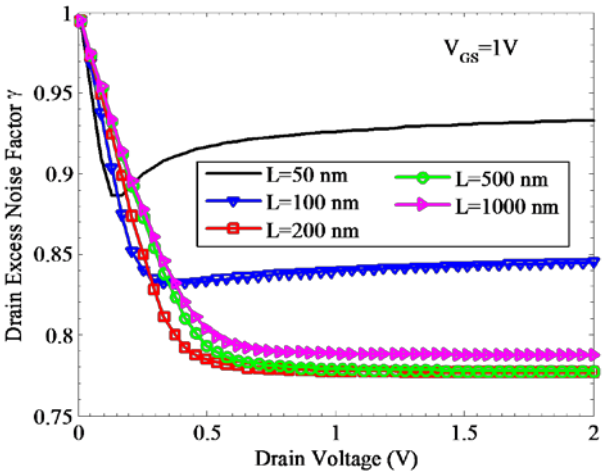


Fig. 3.20. Drain excess noise factor γ as function of drain voltage (t_{ox}=2 nm, t_{si}=34 nm, V_{GS}=1V).

The bias behavior of excess noise factors and correlation coefficient for different channel lengths are shown in the next figures. Now, we consider transversal field mobility degradation and velocity saturation. Figures 3.20, 3.21 and 3.22 show the drain and gate excess noise factors, and the imaginary part of the correlation coefficient as a function of drain voltage (t_{Si}=34 nm, t_{ox}=2 nm, V_{GS}=1V), respectively (calculated by eqs. 3.83, 3.98 and 3.99). These effects introduce some changes with respect to the classical van der Ziel long channel MOSFET model. Due to the velocity saturation effect, V_{DSsat} is smaller as channel length scales down at high gate voltages, which results in the slight increase of thermal noise compared to that of long channel as shown in Fig. 3.20.

This result is in good agreement with the trend determined experimentally in single gate MOSFET [Scholten-2003]. The γ factor tends to 1 for V_{DS}=0 and its value increases steadily with the drain bias in the saturation regime, which is attributed to the channel length modulation effect [Chen-2002; Han-2004] through

the corrected length L_c ,the potential distribution and the related mobility distribution along the channel [Warabino-2006]. Such increase becomes more critical for devices with smaller channel lengths, because the channel length modulation has larger effects for the short-channel devices.

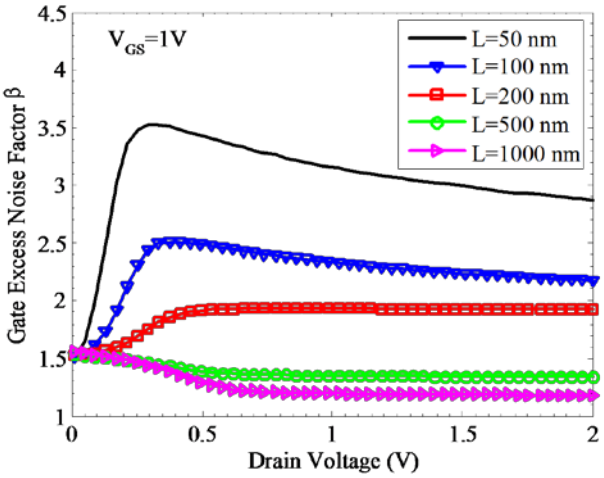


Fig. 3.21. Gate excess noise factor β as function of drain length (t_{ox}=2 nm, t_{si}=34 nm, V_{GS}=1V).

This bias behavior has been found in experimental results for single gate MOSFETs [Han-2004; Warabino-2006]. In Fig. 3.21, the β factor tends to 4/3 for the long channel case and increases with the reduction of L. Figure 3.22 shows our simulation results of the imaginary part of the correlation coefficient. They are slightly smaller than the value 0.4 for the long channel case, and reduce to zero at V_{DS}=0. This coefficient decreases with channel length reduction.

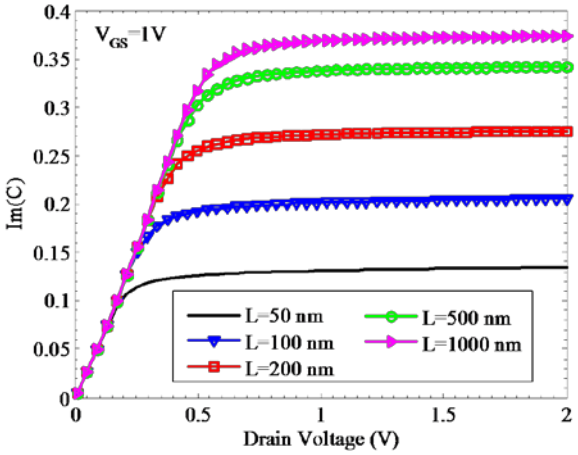


Fig. 3.22. Imaginary part of correlation coefficient *Im(C)* as function of drain voltage (t_{ox}=2 nm, t_{si}=34 nm, V_{GS}=1V).

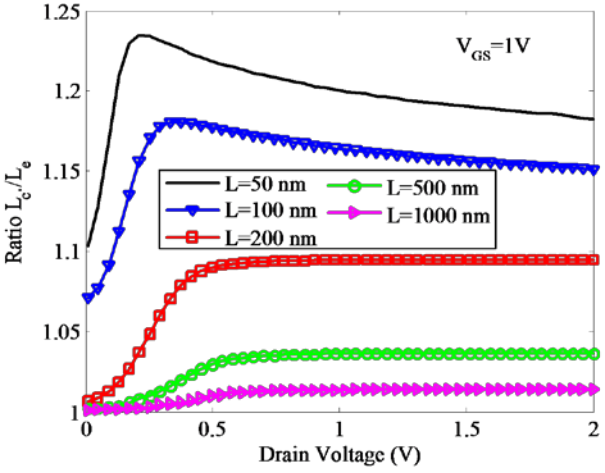


Fig. 3.23. Normalized corrected length *Lc/L* as function of drain voltage (t_{ox}=2 nm, t_{si}=34 nm, V_{GS}=1V).

Figure 3.23 shows the normalized corrected length L_c/L_e, which tends to 1 in linear region and increases with channel length reduction.

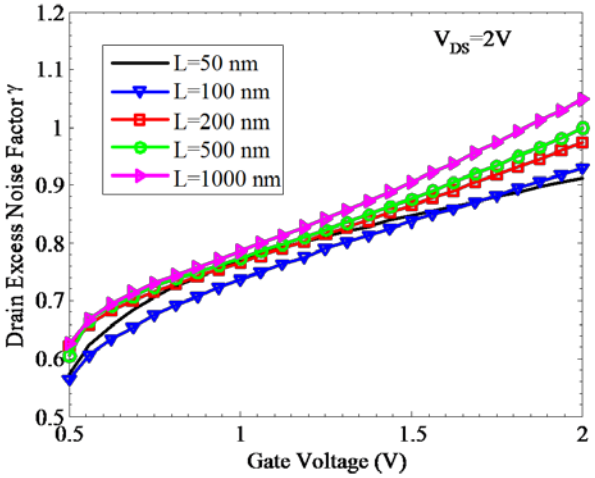


Fig. 3.24. Drain excess noise factor γ as function of gate voltage (t_{ox}=2 nm, t_{si}=34 nm, V_{DS}=2V).

For DG transistors with t_{Si}=34 nm and t_{ox}=2 nm, Figs. 3.24, 3.25 and 3.26 give the drain and gate excess noise factors and the imaginary part of the correlation coefficient as a function of gate voltage, at a fixed drain voltage of 2V. The drain excess noise factor γ increases with the gate voltage for all channel lengths (Fig. 3.24).

The gate excess noise factor β (Fig. 3.25) is found to depend strongly on the gate voltage for short channel devices and it can exceed the value of the long-channel case considerably.

The behavior of the imaginary part of the correlation coefficient as a function of gate voltage is the same for all channel lengths (Fig. 3.26). However it decreases with the reduction of the channel length.

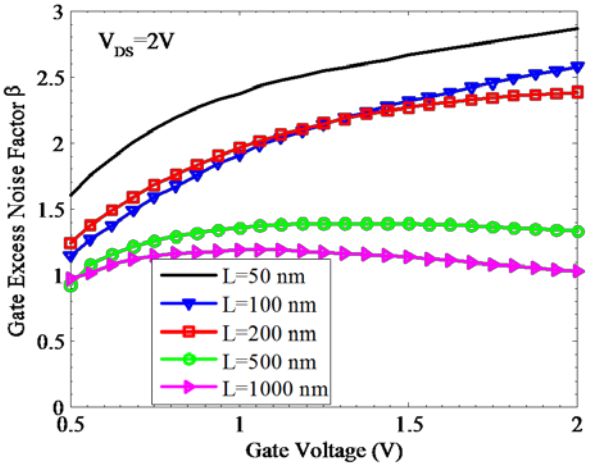


Fig. 3.25. Gate excess noise factor β as function of gate length (t_{ox}=2 nm, t_{si}=34 nm, V_{DS}=2V).

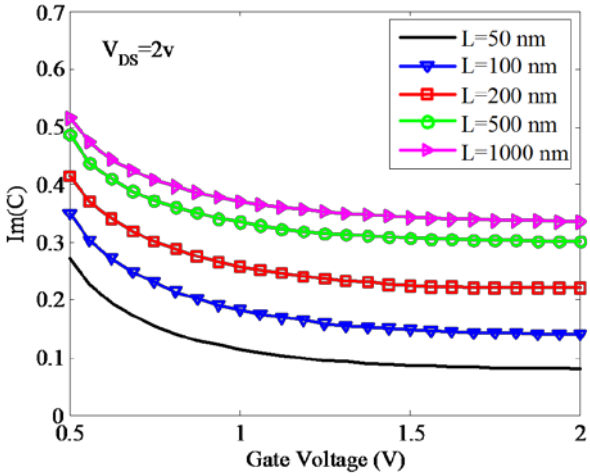


Fig. 3.26. Imaginary part of correlation coefficient *Im(C)* as function of gate voltage (t_{ox}=2 nm, t_{si}=34 nm, V_{DS}=2V).

For the carrier heating case, Fig. 3.27 shows the drain excess noise factor γ as a function of drain voltage, for two channel lengths (100nm, and 45 nm, respectively). As the channel decreases, the drain excess noise factor also decreases. When heating effects are considered, γ increases by ~10-15%.

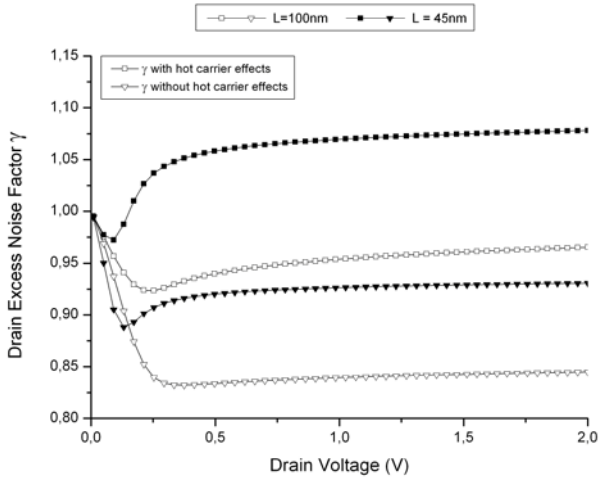


Fig. 3.27. Drain Excess Noise Factor as a function of the drain voltage (t_{ox}=2nm, V_{GS}=1V, V_{TH}=0.3V)

Figure 3.28 shows the gate excess noise factor β for the same DG device and same bias conditions. The factor β shows an important increase with the reduction in the channel length, about 4 times within one order of magnitude (from 1μm to 100 nm). The gate excess noise factor becomes almost constant in the saturation region.

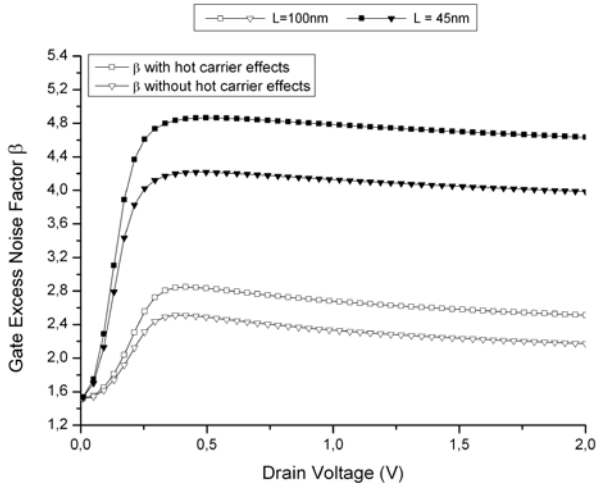


Fig. 3.28. Gate Excess Noise Factor as a function of the drain voltage (t_{ox}=2nm, V_{GS}=1V, V_{TH}=0.3V)

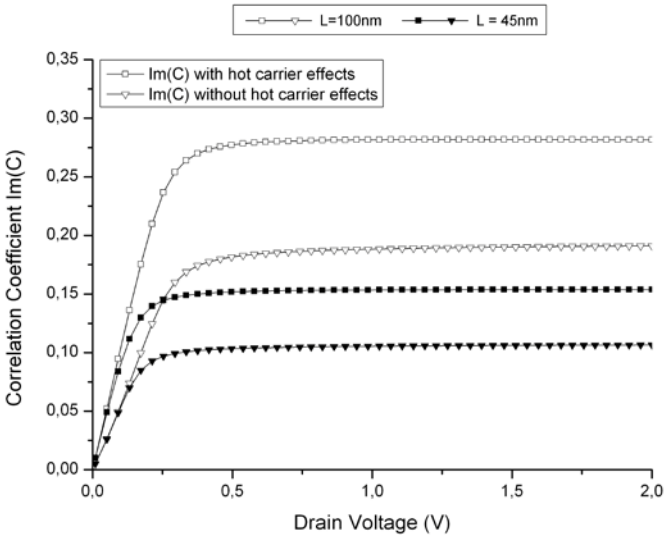


Fig. 3.29. The imaginary part of the correlation coefficient *Im(C)* as a function of the drain voltage (t_{ox}=2nm, V_{GS}=1V, V_{TH}=0.3V)

Figure 3.29 shows the imaginary part of the correlation coefficient *Im(C)* between the gate and drain excess noise factors, as a function of the drain voltage for the same device. In the linear bias region, the correlation coefficient is close to 0, and linearly increases with the drain bias. In the saturation region, it is almost constant, and its value decreases with the channel length, from ~0.4 for 1μm to 0.1 at 45 nm. For V_{DS}=0, the correlation coefficient is 0, as for this bias, the transistor is similar to a resistor.

For a DG transistor with t_{ox}=2nm, and a drain bias V_{DS}=1V, figures 3.30 and 3.31 show the drain and gate excess noise factors as a function of the gate voltage.

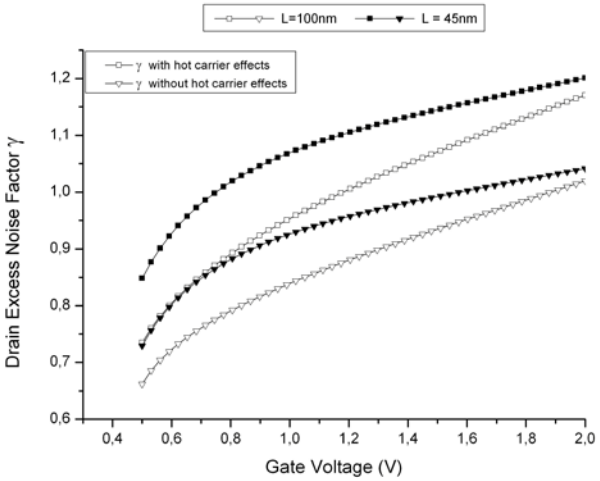


Fig. 3.30. Drain Excess Noise Factor as a function of the gate voltage (t_{ox}=2nm, V_{DS}=1V)

The drain excess noise factor γ increases with the increase in the gate voltage and the decrease in the channel length. On the other hand, the gate excess noise factor β is found to reach a relatively constant value for small channel devices (45 nm), though exceeding the values for longer channels considerably (about 4 times higher than the same DG at 1µm (see Fig. 3.25). The value of the imaginary part of the correlation coefficient *Im(C)* decreases with the gate overvoltage for all channel lengths (fig. 3.32).

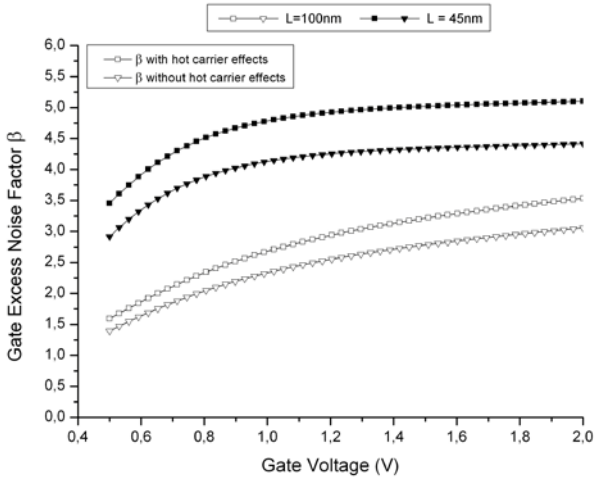


Fig. 3.31. Gate excess noise factor as a function of the gate voltage (tox=2nm, VDS=1V)

In order to estimate the noise performance, the intrinsic noise figure F_{min} is calculated using the following approximated expression [Ziel-1986]:

$$F_{\min} \approx 1 + 2(f / f_T)\sqrt{\gamma\beta(1 - \mathrm{Im}(C)^2)/5} \qquad (3.114)$$

F_{min} was calculated using eq. (3.114) for channel lengths between 50 nm and 1 μm at 10 GHz. The extrinsic parasitic capacitances and resistances were not considered. Figure 3.33 shows the obtained values for the output characteristic at a gate voltage of 1 V, varying the drain voltage. Figure 3.34 shows the calculated values for the transfer characteristic at drain voltage equal to 2V.

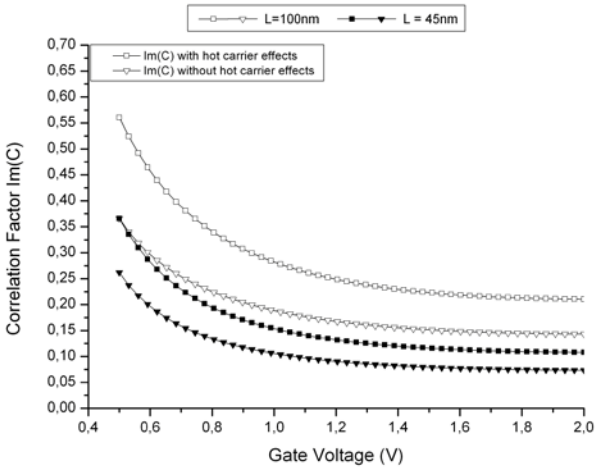


Fig. 3.32. The imaginary part of the correlation coefficient *Im(C)* as a function of gate voltage (t_{ox}=2nm, V_{DS}=1V)

These results justified the interest of DG MOSFETs for low noise RF and microwave application. However, in extrinsic devices (with parasitic elements), an important part of the noise is dominated by extrinsic resistances. Then, the noise factor is proportional to f/f_{max}. The first approach to minimize the noise is by optimizing f_{max} using gate topology engineering with a large number of gate fingers connected in parallel in order to reduce the gate resistance and using a Ti-Co

silicide process to improve the sheet resistance. The second one concerns the optimization of source/drain extensions.

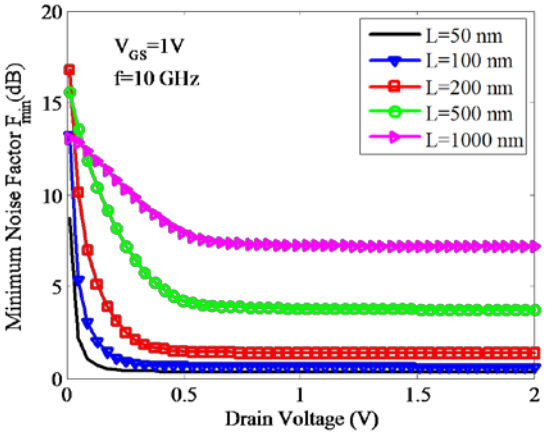


Fig. 3.33. Intrinsic minimum noise factor F_{min}(dB) as function of drain voltage (t_{ox}=2 nm, t_{si}=34 nm, V_{GS}=1V, f=10 GHz).

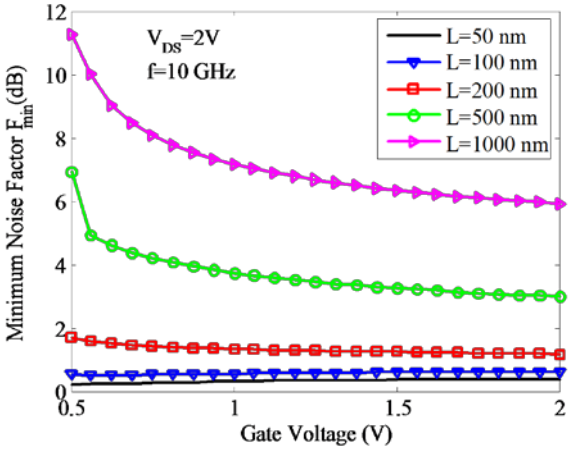


Fig. 3.34. Intrinsic minimum noise factor F_{min}(dB) as function of gate voltage (t_{ox}=2 nm, t_{si}=34 nm, V_{DS}=2V, f=10 GHz).

3.7 Conclusions

Sections 3.2.1 through 3.2.4 present an extended version of a previously developed compact dc and charge model for doped DG-MOSFETs from a unified charge control model derived from Poisson's equation. The quantum case is obtained using a simple relationship between inversion centroid and inversion charge obtained fitting numerical simulation results. This compact quantum model is compared with numerical self-consistent Schrodinger-Poisson simulation with good agreement.

Using this compact charge control model, DC drain current models are derived assuming drift-diffusion and hydrodynamic transport. The RF and noise performance of DG-MOSFETs is analysed using the active transmission line method from the compact charge control and drain current model. The effect of hot carriers, channel length modulation, saturation effect, and shot noise introduced by tunnelling gate current are taken into account.

The obtained results (Figs. 3.7, 3.8) show important differences in drain current, f_T and f_{max}, and noise performances between drift-diffusion and hydrodynamic models for short gate lengths. These differences are due to the velocity overshoot increasing the transconductance, and hence, the f_T and f_{max}. The differences between the classical and quantum charge control models rises from the shift in the threshold voltage and the reduction in the capacitance. These are smaller than the differences obtained using drift-diffusion and hydrodynamic models.

The intrinsic noise figure (Figs. 3.11, 3.12 and 3.13) depends on the temperature model used in simulation. For a short-channel device operated in

saturation region, noise exhibits a strong dependence on the drain bias because the velocity saturation region, where the noise temperature is high, occupies a large portion of the channel. Hydrodynamic models predict higher noise temperature in this region than the classical relation between carrier temperature and electric field, resulting in a higher noise figures. In these devices, for typical RF operating bias points the effect of shot noise introduced by the gate current is small. The simulated results show the limiting effect of parasitics in RF and noise performances.

It is worth noting that experimental results from several authors [Han-2004; Jindal-2006] for single-gate (SG) MOSFETs of various lengths found excess noise factors γ ratios greater than 1 for very short channel devices (under 100nm), as well as important increases of γ with the drain voltage. This trend and values are successfully reported in this work, validating the temperature model employed for these simulations.

Section 3.2.5 presents a gate and drain noise spectrum analysis, which was done based on a new compact analytical noise model using the compact analytical model for Short Channel Symmetric Doped Double-Gate (SDDG) MOSFETs, which considers doped silicon layer in a wide range of doping concentrations and short channel transistors. We have developed a compact model for the channel noise, the induced-gate noise and the cross-correlation noise between drain and gate noises, based on the improved Klassen-Prins approach. This method had been found equivalent to an equivalent circuit approach, and the impedance field method. The expressions obtained are analytical and they depend on the mobile charge at the source and drain ends of the channel.

The noise compact model calculations are compared with the values obtained using the segmentation method, where the active transmission line is

analyzed using circuital nodal analysis. The good agreement obtained between both methods validates the analytical expressions presented. When we do not consider transversal field mobility degradation, the values of the excess noise factors and correlation coefficients predicted in long channel SG MOSFETs by the Van der Ziel model are obtained. Moreover, the compact noise model reproduces the measured noise bias behavior for any gate length found for SG MOSFETs in the literature, without the need of additional parameters. Therefore, the proposed noise model is very promising for being used in circuit simulators with DG MOSFETs.

3.7 References

[Balestra-1987] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini and T. Elewa, "Double-Gate Silicon-on-Insulator Transistor with Volume Inversion - A New Device with Greatly Enhanced Performance", *IEEE Electron Device Letters*, **8** (9), 410-412 (1987)

[Baccarani-1999] G. Baccarani and S. Reggiani, "A compact Double-Gate MOSFET model comprising quantum-mechanical and nonstatic effects", *IEEE Transactions on Electron Devices*, **46**, (8), 1656-1666 (1999)

[Bansal-2005] A. Bansal, B. C. Paul and K. Roy, "Modeling and optimization of fringe capacitance of nanoscale DGMOS devices", *IEEE Transactions on Electron Devices*, **52** (2), 256-262 (2005)

[Cerdeira-2008] A. Cerdeira, B. Iñiguez and M. Estrada, "Compact model for short channel symmetric doped double-gate MOSFETs", *Solid-State Electronics*, **52** (7), 1064-1070 (2008)

[Cerdeira2-2008] A. Cerdeira, O. Moldovan, B. Iniguez and M. Estrada, "Modeling of potentials and threshold voltage for symmetric doped double-gate MOSFETs", *Solid-State Electronics*, **52** (5), 830-837 (2008)

[Chen-2002] C.-H. Chen and M. J. Deen, "Channel noise modeling of deep submicron MOSFETs", *IEEE Transactions on Electron Devices*, **49** (8), 1484-1487 (2002)

[Fossum-2002] J. G. Fossum, L. X. Ge and M. H. Chiang, "Speed superiority of scaled double-gate CMOS", *IEEE Transactions on Electron Devices*, **49** (5), 808-811 (2002)

[Fossum-2004] J. G. Fossum, L. Ge, M. H. Chiang, V. P. Trivedi, M. M. Chowdhury, L. Mathew, et al., "A process/physics-based compact model for nonclassical CMOS device and circuit design", *Solid-State Electronics*, **48**, 919-926 (2004)

[Francis-1994] P. Francis, A. Terao, D. Flandre and F. Vandewiele, "Modeling of Ultrathin Double-Gate NMOS/SOI Transistors", *IEEE Transactions on Electron Devices*, **41**, 715-720 (1994)

[Ge-2000] L. Ge, J.G. Fossum, "A novel compact model of quantum effects in scaled SOI and double-gate MOSFETs", *IEEE International SOI Conference*, 114-115 (2000)

[Ge-2001] L. Ge, J. G. Fossum and B. Liu, "Physical compact modeling and analysis of velocity overshoot in extremely scaled CMOS devices and circuits", *IEEE Transactions on Electron Devices*, **48**, (9), 2074-2080 (2001)

[Ge-2002] L. Ge and J. G. Fossum, "Analytical modeling of quantization and volume inversion in thin Si-film DG MOSFETs", *IEEE Transactions on Electron Devices*, **49**, (2), 287-294 (2002)

[Han-2004] K. Han, H. Shin and K. Lee, "Analytical drain thermal noise current model valid for deep submicron MOSFETs", *IEEE Transactions on Electron Devices*, **51** (2), 261-269 (2004)

[Hillbrand-1976] H. Hillbrand and P. Russer, "An efficient method for computer aided noise analysis of linear amplifier networks", *IEEE Transactions on Circuits and Systems*, **23** (4), 235-238 (1976)

[Iniguez-2005] B. Iniguez, D. Jimenez, J. Roig, H. A. Hamid, L. F. Marsal and J. Pallares, "Explicit continuous model for long-channel undoped surrounding gate MOSFETs", *IEEE Transactions on Electron Devices*, **52**, (8), 1868-1873 (2005)

[Iniguez-2006] B. Iniguez, A. Lazaro, O. Moldovan, A. Cerdeira and T. Fjeldly, "DC to RF Small-Signal Compact DG MOSFET model", *Nanotechnology Conference and Trade Show*, 680-685 (2006)

[Iniguez2-2005] B. Iniguez, A. Lazaro, H. A. Hamid, G. Pailloncy, G. Dambrine and F. Danneville, "Noise in SOI MOSFETs and gate-all around transistors", *Noise and Fluctuations*, **780**, 269-274 (2005)

[Jimenez-2004] D. Jimenez, J. J. Saenz, B. Iniguez, J. Sune, L. F. Marsal and J. Pallares, "Modeling of nanoscale gate-all-around MOSFETs", *IEEE Electron Device Letters*, **25**, (5), 314-316 (2004)

[Jindal-2006] R.P. Jindal, “Compact noise models for MOSFETs”, *IEEE Transactions on Electron Devices*, **53** (9), 2051-2061 (2006)

[Kim-2001] K. Kim and J. G. Fossum, "Double-gate CMOS: Symmetrical-versus asymmetrical-gate devices", *IEEE Transactions on Electron Devices*, **48**, 294-299 (2001)

[Lazaro-1999] A. Lazaro, L. Pradell and J. M. O'Callaghan, "FET noise-parameter determination using a novel technique based on 50-Ω noise-figure measurements", *IEEE Transactions on Microwave Theory and Techniques*, **47** (3), 315-324 (1999)

[Lazaro-2006] A. Lazaro and B. Iniguez, "RF and noise performance of double gate and single gate SOI", *Solid-State Electronics*, **50**, (5), 826-842 (2006)

[Lopez-Villanueva-2000] J. A. Lopez-Villanueva, P. Cartujo-Cassinello, F. Gamiz, J. Banqueri and A. J. Palma, "Effects of the inversion-layer centroid on the performance of double-gate MOSFET's", *IEEE Transactions on Electron Devices*, **47**, (1), 141-146 (2000)

[Pailloncy-2004] G. Pailloncy, B. Iniguez, G. Dambrine, J. P. Raskin and F. Danneville, "Noise modeling in fully depleted SOI MOSFETs", *Solid-State Electronics*, **48** (5), 813-825 (2004)

[Pailloncy2-2004] G. Pailloncy, B. Iniguez, G. Dambrine and F. Danneville, "Influence of a Tunneling Gate Current on the noise performance of SOI MOSFETs", *IEEE International SOI Conference*, 55-57 (2004)

[Ranuarez-2005] J. C. Ranuarez, M. J. Deen and C. Chih-Hung, "Modeling the partition of noise from the gate-tunneling current in MOSFETs", *IEEE Electron Device Letters*, **26** (8), 550-552 (2005)

[Roy-2005] A. S. Roy and C. C. Enz, "Compact modeling of thermal noise in the MOS transistor", *IEEE Transactions on Electron Devices*, **52**, (4), 611-614 (2005)

[Roy-2006] A. S. Roy, C. C. Enz and J. M. Sallese, "Noise modeling methodologies in the presence of mobility degradation and their equivalence", *IEEE Transactions on Electron Devices*, **53**, (2), 348-355 (2006)

[Sallese-2005] J. M. Sallese, F. Krummenacher, F. Pregaldiny, C. Lallement, A. Roy and C. Enz, "A design oriented charge-based current model for symmetric DG MOSFET and its correlation with the EKV formalism", *Solid-State Electronics*, **49**, (3), 485-489 (2005)

[Scholten-2003] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven and V. C. Venezia, "Noise modeling for RF CMOS circuit simulation", *IEEE Transactions on Electron Devices*, **50** (3), 618-632 (2003)

[Schuegraf-1994] K. F. Schuegraf and H. Chenming, "Hole injection SiO_2 breakdown model for very low voltage lifetime extrapolation", *IEEE Transactions on Electron Devices*, **41** (5), 761-767 (1994)

[Seeger-1973] K. Seeger, "Semiconductor Physics", Springer-Verlag: New York (1973)

[Shenoy-2003] R. S. Shenoy and K. C. Saraswat, "Optimization of extrinsic source/drain resistance in ultrathin body double-gate FETs", *IEEE Transactions on Nanotechnology*, **2** (4), 265-270 (2003)

[Taur-2001] Y. Taur, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs", *IEEE Transactions on Electron Devices*, **48**, 2861-2869 (2001)

[Trivedi-2004] V. P. Trivedi, J. G. Fossum and F. Gamiz, "A compact QM-based mobility model for nanoscale ultra-thin-body CMOS devices", *IEEE International Electron Devices Meeting, Technical Digest*, 763-766 (2004)

[Vasileska-2000] D. Vasileska and Z. Ren, SCHRED 2.0 Manual, Arizona State University Press: Tempe (2000)

[Warabino-2006] T. Warabino, M. Miyake, N. Sadachika, D. Navarro, Y. Takeda, G. Suzuki, et al., "Analysis and Compact Modeling of MOSFET High-Frequency Noise", *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 158-161 (2006)

[Ziel-1986] A. van der Ziel, “Noise in Solid State Devices and Circuits”, Wiley-Interscience (1986)

Chapter 4

Compact Modeling of Surrounding Gate Transistors

4.1 Introduction

In the previous chapter, an analytical method for RF and noise modeling applied to DG SOI MOSFET devices was presented. The model was extended to SGT devices and its DC, RF and High Frequency noise behavior was studied by A. Lazaro et al. [Lazaro-2008] In this chapter, the model is improved, taking into account a novel quantum charge control model, and including effects such as velocity overshoot through a one-dimensional (1D) energy-balance model

[Baccarani-1999; Lazaro-2006], the effect of the saturation region, the channel modulation length effect and the mobility degradation produced by quantum effects.

The model is based on the concept of channel segmentation [Lazaro-2006; Lazaro2-2006], and includes the formulation for drift-diffusion and temperature (hydrodynamic) transport models. High frequency performances are analyzed through the use of analytical expressions of the cut-off frequency f_T and maximum frequency of oscillation f_{max}, and noise properties of the devices are discussed. Special attention is paid to figure out how a DC tunneling gate leakage current, due to the decrease of the oxide thickness, might influence the small signal properties and the noise performance of MOSFETs.

4.2 Charge Control Model

A simple diagram showing the structure and the cross-section of the studied SGT is given in Fig. 4.1. It can be observed that the gate surrounds the cylindrical silicon channel. When the diameter of the cylinder decreases, the quantum confinement effects appear, making the self-consistent solution of 2-D Poisson and Schrödinger equations essential in a cross section of the SGT [Roldan-2008].

In order to model quantum confinement effects, an already successful strategy has been employed [Roldan-2001; Lopez-Villanueva-1997; Arora-1995], where the equations for the classical model version were extended in order to take into account these effects. This was carried out by introducing a corrected oxide capacitance and a modified threshold voltage.

The corrected oxide capacitance was computed by determining the inversion layer centroid, which allows accounting for the oxide interface separation of the inversion charge distribution. This leads to a new oxide thickness, which produces more accurate calculations in modeling devices with thin-gate oxide layers [Roldan-2008].

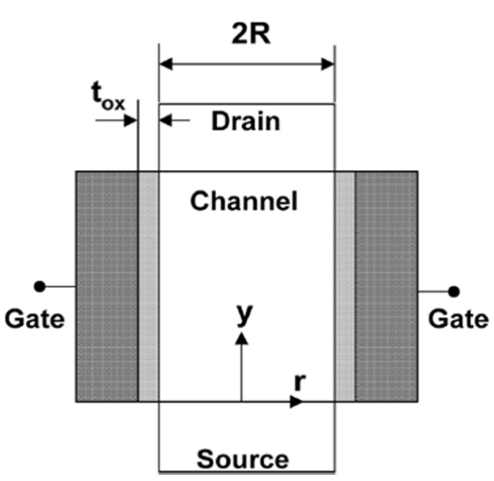
The conventional definition of the inversion layer centroid [Roldan-2001; Lopez-Villanueva-1997] was adapted to the SGT geometry. A parameter Δ is defined as follows [Roldan-2008]:

$$\Delta = \frac{\int_0^R \rho(r) r^2 dr}{\int_0^R \rho(r) r dr} = \frac{\int_0^R \rho(r) r^2 dr}{\frac{Q_I}{2\pi}} = 2\pi \frac{\int_0^R \rho(r) r^2 dr}{Q_I} \tag{4.1}$$

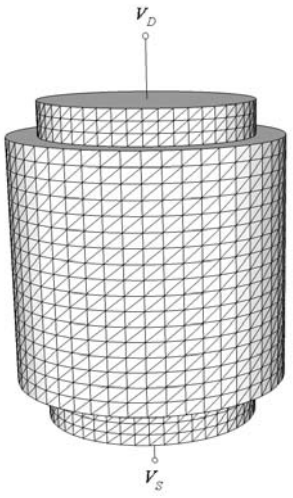
with $\rho(r)$ being the quantum electron density given by:

$$\rho(r) = \frac{q}{\pi}\left(\frac{2mkT}{\hbar^2}\right)^{1/2} \sum_n \psi_n^2(r)\, \Im_{-1/2} \times \left(\frac{E_F - E_n}{kT}\right) \quad C/cm^3 \tag{4.2}$$

where q is the electron charge, k is the Boltzman constant, T is the temperature, E_F is the Fermi level, ψ_n is the wave function belonging to energy level E_n, $\Im_{-1/2}$ is the complete Fermi-Dirac integral of order -1/2, while the other symbols have their usual meaning.



(a)



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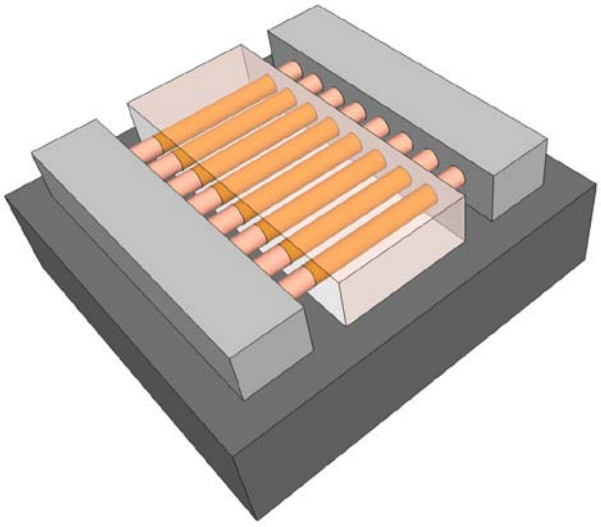


(c)

Fig. 4.1. a) Cross section of the surrounding gate MOSFET; b) Simulated surrounding gate MOSFET structure; c) a 3D schematic of a device with multiple fingers, each of them being a SGT

The inversion charge per unit gate length Q_I is calculated in cylindrical coordinates, assuming that the inversion charge density is not dependent on the rotation angle:

$$Q_I = 2\pi \int_0^R \rho(r)\, r dr \tag{4.3}$$

The inversion charge centroid z_I is calculated as:

$$z_I = R - \Delta \tag{4.4}$$

where R is the radius of the cylinder.

In order to model the centroid data, the following empirical equation is used [Roldan-2008]:

$$\frac{1}{z_I} = \frac{1}{a + 2bR} + \frac{1}{z_{I0}} \left(\frac{N_I}{N_{I0}(R)} \right)^n \tag{4.5}$$

where a, b, z_{I0} and n are constants not dependent on the bias, and N_I is the electron density per unit area, calculated as:

$$N_I = \frac{Q_I}{2\pi R q} \tag{4.6}$$

According to J.B. Roldan et al. [Roldan-2008], the fitting parameters were chosen as: a=0.55 nm, b=0.198, z_{I0}=5.1 nm, n=0.75 and

$$N_{I0}(cm^{-2}) = 8.26 \times 10^{12} cm^{-2} - 4.9 \times 10^{18} cm^{-3} \times R\,(cm) \tag{4.7}$$

Using this centroid model, a classical inversion charge model [Iniguez-2005] has been improved, in order to include quantum effects. In the new model,

the classical oxide capacitance was replaced by one where the capacitance of the oxide layer is in series with the capacitance of the silicon layer, its thickness corresponding to the value of the inversion charge centroid. The new total capacitance is calculated as [Lazaro-2006]:

$$\frac{1}{C_{TOTAL}} = \frac{1}{C_{Oxide}} + \frac{1}{C_{Semiconductor}} \tag{4.8}$$

where C_{Oxide} is the value of a cylindrical capacitor with the external radius equal to $R + t_{ox}$ (t_{ox} is the oxide thickness) and the internal radius equal to R.

$$C_{Oxide} = \frac{\varepsilon_{ox}}{R \cdot \ln\left(1 + \frac{t_{ox}}{R}\right)} \tag{4.9}$$

where ε_{ox} is the oxide permittivity. $C_{Semiconductor}$ is calculated as:

$$C_{Semiconductor} = \frac{\varepsilon_{Si}}{\left(R - z_I\right)\ln\left(1 + \frac{z_I}{R - z_I}\right)} \tag{4.10}$$

where ε_{Si} is the silicon permittivity.

The starting point for the calculation is an initial guess of the inversion charge, called Q' [Iniguez-2005], and defined as:

$$Q' = C_{Oxide}\left(-\frac{2C_{Oxide}V_T^2}{Q_o} + \sqrt{\left(\frac{2C_{Oxide}V_T^2}{Q_o}\right)^2 + 4V_T^2 \ln^2\left(1 + \exp\left(\frac{V_{GS} - V_0 - V}{2V_T}\right)\right)}\right) \tag{4.11}$$

where $V_T = kT/q$, V_{GS} is the gate-source voltage, and V is the channel potential (V=0 at the source).

The expressions for V_0 and Q_o are the following:

$$Q_o = \frac{4\varepsilon_{Si}}{R}\frac{kT}{q} \tag{4.12}$$

$$V_0 = \phi_{MS} + \frac{kT}{q}\ln\left(\frac{8}{\delta R^2}\right), \text{ and } \delta = \frac{q^2 n_i}{kT\varepsilon_{Si}} \tag{4.13}$$

where n_i is the intrinsic carrier concentration, ϕ_{MS} is the metal-semiconductor work-function difference.

The threshold voltage V_{TH} and ΔV_{TH} are calculated, noting that a quantum threshold voltage shift is introduced in the V_{TH} calculation:

$$V_{TH} = V_0 + 2V_T \ln\left(1 + \frac{Q'}{Q_0}\right) + \Delta V_{TQM} \tag{4.14}$$

and

$$\Delta V_{TH} = \frac{\left(\frac{2C_{TOTAL}V_T^2}{Q_0}\right)Q'}{\left(Q_0 + Q'\right)} \tag{4.15}$$

where

$$\Delta V_{TQM} = 0.011V + \frac{1.3\times10^{-15}V\times cm^2}{R^2} \tag{4.16}$$

It is interesting to highlight that if C_{TOTAL} it substituted for C_{Oxide} in (4.15) and (4.16), the classical charge control model is recovered.

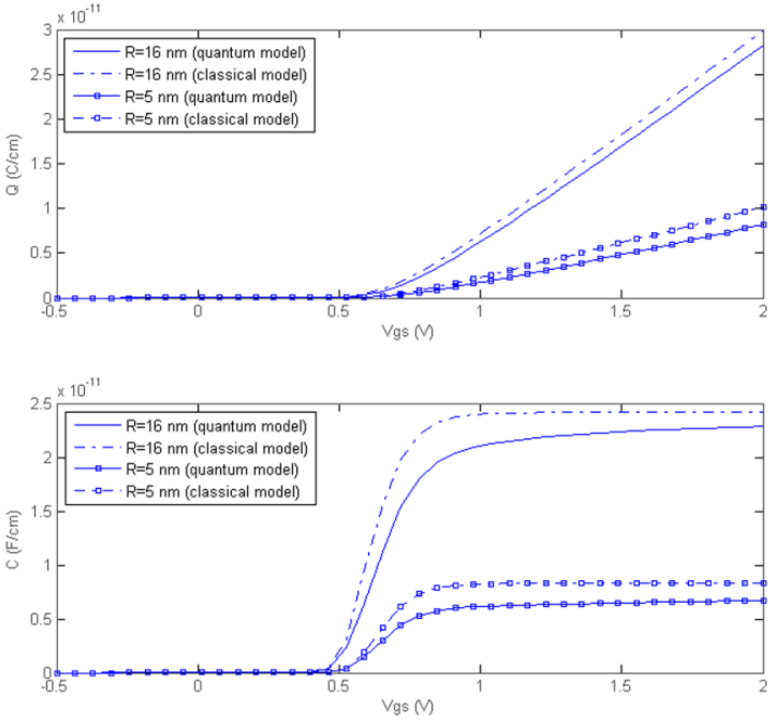


Fig. 4.2. a) Normalized channel charge ($Q/2\pi R$) of an SGT for several values of R, at room temperature ($N_A = 10^{10}\,cm^{-3}$ and $t_{ox} = 1.5nm$); b) Normalized channel capacitance ($C/2\pi R$) of an SGT for several values of R, at room temperature ($N_A = 10^{10}\,cm^{-3}$ and $t_{ox} = 1.5nm$)

Finally, the total charge Q is obtained:

$$Q = C_{TOTAL}\left(-\frac{2C_{TOTAL}V_T^2}{Q_o} + \sqrt{\left(\frac{2C_{TOTAL}V_T^2}{Q_o}\right)^2 + 4V_T^2 \cdot \ln^2\left(1+\exp\left(\frac{V_{GS}-V_{TH}+\Delta V_{TH}-V}{2V_T}\right)\right)}\right) \tag{4.17}$$

Using this model, some simulated results for the normalized channel charge ($Q/2\pi R$) and normalized channel capacitance ($C/2\pi R$) are presented in Fig. 4.2., using the following technological parameters: $N_A = 10^{10} cm^{-3}$ and $t_{ox} = 1.5nm$.

4.3 Drain Current Model

In extremely short SGTs, the channel is quasi-ballistic, thus an important velocity overshoot is expected [Baccarani-1999]. Using a simplified energy-balance model, the electron mobility is a function of the electron temperature related to the average energy of the carriers.

In this section we extend the transport model previously developed for DG-MOSFETs [Lazaro-2006] to the SGT case. Following G. Baccarani [Baccarani-1999], and A. Lazaro [Lazaro-2006], the drain current in the linear channel region ($x<L_e$) can be obtained as:

$$I_{DS} = \frac{W \int_0^{V_{Dsat}} \mu_{n0} Q(V)\, dV}{\int_0^{L} \left(1 + \left(\frac{2k\mu_{n0}}{q\lambda_w v_{sat}}\right)\left(T_e(x) - T_0\right)\right) dx} \tag{4.18}$$

where L_e is the effective channel length, μ_{n0} is the electron mobility as a function of voltage, k is the Boltzmann constant, T_e is the electronic temperature and the energy-relaxation length is defined as $\lambda_w \approx 2v_{sat}\tau_w$, τ_w being the energy relaxation time, and v_{sat} the saturation velocity. In the case of SGTs, for scaling purposes and

for comparison with other MOSFET structures, W can be assumed equal to $W = n_{fingers} \cdot 2\pi R$, $n_{fingers}$ being the number or cylinders (fingers) in the structure.

In order to evaluate eq. (4.18), we first integrate the charge density from eq. (4.17) between Q_s and Q_d (Q=Q_s at the source end and Q=Q_d at the saturation point or drain end), and obtain [Moldovan-2007]:

$$\begin{aligned} f(V_{GS,}V_{DSsat}) &= \int_0^{V_{DSsat}} \mu_{n0} Q(V) dV \\ &\approx \mu_{eff} \left[2\frac{kT}{q}\left(Q_s - Q_d\right) + \frac{Q_s^2 - Q_d^2}{2C_{ox}} + \frac{kT}{q} Q_0 \log\left[\frac{Q_d + Q_0}{Q_s + Q_0} \right] \right] \end{aligned} \tag{4.19}$$

At large inversion densities the ultra-thin film mobility can be higher than heavily doped bulk MOS devices due to a lower effective field, and it is largely insensitive to the silicon thickness (t_{si}). Thus, the common expression for bulk devices is not longer valid. However, at small inversion densities the mobility is reduced for decreasing t_{si} [Esseni-2003]. This reduction in the mobility is caused by the increase of the surface roughness scattering (the two interfaces are closer) as well as phonon scattering due to the reduction of the quantum well formed by the thin Si layer between the oxide layers. We suggest using the method given by V.P. Trivedi et al. [Trivedi-2004] and S. Reggiani et al. [Reggiani-2007], originally proposed for DG MOSFET devices. The effective vertical field E_{eff} reduces the effective mobility given by Trivedi [Trivedi-2004]:

$$E_{eff} \approx \frac{Q}{4\varepsilon_{Si}} \tag{4.20}$$

and

$$\mu_{n0}(t_{si,}E_{eff}) = \frac{\mu_0}{1+\frac{\mu_0}{\mu_{ph(bulk)}}\left(\frac{\mu_{ph(bulk)}}{\mu_{ph(t_{si,eff})}}-1\right)+\theta\frac{\mu_0}{\mu_{sr}}} \tag{4.21}$$

where effective μ_0 and θ are fitting parameters, and the effective normal field is given by (4.20).

Note that eq. (4.21) takes into account the dependence of mobility with silicon thickness due to the variation with t_{si} of the distance between the inversion-charge centroid and the surface. The model (4.21) uses the lowest subband of the Schrödinger-Poisson equation to calculate the phonon limited mobility. The screening mobility is modelled as in conventional devices using the effective field ($\mu_{sr}\alpha E_{eff}^{-2}$). Although the model is derived for DG MOSFET, we expect that it could be used for SGT because the type of confinement in SGT and the shape of the first eigenfunction are qualitatively similar to DG devices. In order to use eq. (4.21) for SGT MOSFETs, we use $t_{si}=2R$ and replace the effective thickness $t_{si,eff}$ with $2R_{eff}$, obtained from the centroid z_I (4.5).

In order to evaluate the integral in the denominator of eq. (4.18), we need to know the temperature profile along the channel. The electron temperature T_e is governed by the following equation [Baccarani-1999]:

$$\frac{dT_e}{dx}+\frac{T_e-T_0}{\lambda_w}=-\frac{q}{2k}E_x(x) \tag{4.22}$$

Equation (4.19) can be integrated assuming a constant λ_w, under boundary condition $T_e\left(x=0\right)=T_0$, and the *x*-component of the electric field expressed as a function of the channel potential, $E_x\left(x\right)=-dV\left(x\right)/dx$. As an approximation, in the linear channel region we can assume that the lateral field is linear from a small

value at the source end to the saturation field at $x=L_e$ ($E_x = E_{sat} \cdot x / L_e$). Using eqs. (4.19) and (4.22), we obtain:

$$I_{DS} = \frac{Wf(V_{GS}, V_{DSS})}{L_e + \frac{q\alpha}{2k}\int_0^{L_e} V(\xi) e^{\frac{\xi - L_e}{\lambda_w}} d\xi} = \frac{W}{L_e} \frac{f(V_{GS}, V_{DSS})}{1 + \gamma_n V_{DSS}} \tag{4.23}$$

where

$$\gamma_n = \frac{\mu_{eff}}{v_{sat} L_e} \frac{1}{\left(1 + 2\lambda_w / L_e\right)} \tag{4.24}$$

with V_{DSS} equal to V_{DS} for non saturated channels ($L_e=L$) and $V_{DSS}=V_{DSsat}$ for saturated channels. A smoothing function is used to interpolate V_{DSS}:

$$V_{DSS} = V_{DS} - \frac{kT}{q} \frac{\ln\left\{1 + \exp\left[A(V_{DS} - V_{DSsat}) / (kT / q)\right]\right\}}{A} \tag{4.25}$$

where A is the adjusting parameter that controls the transition between saturated and non saturated channel ($A=1$ for a smooth transition).

The value of V_{DSsat} can be found by equaling the drain current given by eq. (4.23) with the current in the channel saturation point:

$$I_{DS} = WQ(V_{DSsat}) v_{sat,ns} \tag{4.26}$$

where the overshoot channel velocity $v_{sat,ns}$ is calculated from the expression:

$$v_{sat,ns} = \frac{\mu_{eff}}{1 + \alpha(T(L) - T_0)} E_x(x = L) \tag{4.27}$$

with

$$\alpha = \frac{2k\mu_{n0}}{q l_w v_{sat}} \tag{4.28}$$

Note that the conventional drift-diffusion model is recovered if λ_w is set to 0, then non-stationary saturation velocity $v_{sat,ns}$. is equal to stationary value v_{sat}.

Channel length modulation should also be included. For $V_{DS}<V_{DSsat}$, the device works in the linear region, with $L_e=L$ and $V_{DSsat}=V_{DS}$. For $V_{DS}>V_{DSsat}$, the device operates in the saturation regime, and the channel is partially saturated, and the saturated channel length is given by:

$$\Delta L = L - L_e = L_c \operatorname{arcsin} h\left(\frac{V_{DS} - V_{DSsat}}{E_{sat} L_c}\right) \tag{4.29}$$

where $L_c=a\cdot\lambda_c$ is proportional to the characteristic length λ_c given by J.P. Colinge [Colinge-2004]:

$$\lambda_c = \sqrt{\frac{\varepsilon_{si} t_{ox} R}{\varepsilon_{ox}} + \frac{R^2}{2}} \tag{4.30}$$

4.4 RF and Noise Modeling

In order to model the noise in the SGT structure presented in Fig. 4.1, several noise sources must be considered. The first one is the thermal noise due to parasitic access resistances R_G, R_S and R_D. which is easily modeled using the Nyquist theorem. The other noise sources come from the intrinsic transistor. The intrinsic contribution is modeled using two correlated current noise sources, i_g and i_d (admittance representation). They include the effect of the diffusion noise and flicker noise in the channel, induced-gate noise and shot noise.

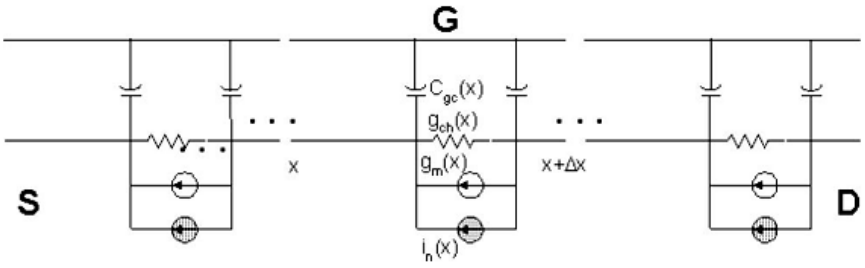


Fig. 4.3. Small-signal and noise equivalent circuit for a channel slice between x and $x+\Delta x$. An equivalent noise source $i_n(x)$ has been introduced to model the channel noise.

Let us consider a nonuniform channel as shown in Fig. 4.3. According to the segmentation method, the channel is split into several slices, and the small-signal and noise sources can be derived from the basic semiconductor equations. The local equivalent circuit for each channel slice is composed of the gate-to-channel capacitance, the transconductance and the channel resistance (or conductance). Diffusion noise and gate shot noise can be incorporated into the model by adding two more noise sources for each slice. The local equivalent circuit elements can be obtained from linearizing the current at any channel position x, resulting in and the following current continuity equation:

$$I(x) = g\left(V, \frac{dV}{dx}\right) \cdot \frac{dV}{dx} \tag{4.31}$$

where $g = W\mu Q$ is the channel conductance per unit length, and W, μ, Q, are the channel width ($W=2\pi R$), mobility and inversion charge density respectively. The mobility depends on the electric field $E=-dV/dx$ and g depends on the channel potential $V(x)$ and the dV/dx.

We consider here a drift-diffusion model, where an analytical relationship between T_e and the lateral field $E(x)$ must be used. A prevalent model in literature [Moldovan-2007] describes the electron mobility as a function of the temperature as:

$$\mu_{eff} = \mu_0 \sqrt{\frac{T_L}{T_e}} \tag{4.32}$$

The mobility can also be expressed as:

$$\mu_{eff} = \frac{\mu_0}{\left(1+\left(\frac{E}{E_c}\right)^2\right)^{1/2}} \tag{4.33}$$

Equating (4.32) and (4.33) and solving for T_e / T_L we obtain:

$$T_e = T_L\left(1+\left(\frac{E}{E_c}\right)^2\right) \tag{4.34}$$

For the typical values of the inversion carrier density in the inversion layer, we can consider that the channel is not degenerated, and the velocity distribution is heated Maxwellian. Under this assumption, following J.P. Nougier et al. [Nougier-1977], the noise temperature T_n becomes equal to the carrier temperature T_e.

The analysis of the active transmission line (Fig. 4.3) using the admittance method gives the small-signal admittance matrix and its noise correlation matrix [Lazaro2-2006]. For the compact modeling of the noise, three methods are usually applied: (1) and equivalent circuit approach, (2) the impedance field method or (3) the Langevin or Klaasen-Prins (KP) method. A.S. Roy et al. [Roy-2006] show that these three methods are equivalent and the same final expression for the current noise densities and correlation coefficient is obtained. Thus, the compact modeling

methods could be considered as an analytic analysis technique of the active transmission line.

Assuming that the local noise source is spatially uncorrelated and ω is the angular frequency, the drain and gate spectral densities and the correlation matrix are obtained using the following expressions [Roy-2006]:

$$S_{i_d^2} = \overline{i_d^2} = \frac{1}{I_D L_c^2} \int_{V_S}^{V_D} \frac{g_c(V)^2}{g(V)} S_{i_n} dV \tag{4.35}$$

$$S_{i_g^2} = \overline{i_g^2} = \frac{\omega^2 W^2}{I_D^5 L_c^2} \int_{V_S}^{V_D} \left(\int_{V_S}^{V_D} g_c(V')(Q(V') - Q(V)) dV' \right)^2 \frac{g_c(V)^2}{g(V)} S_{i_n} dV \tag{4.36}$$

$$S_{i_g i_d^*} = \overline{i_g i_d^*} = \frac{j\omega W}{I_D^3 L_c^2} \int_{V_S}^{V_D} \left(\int_{V_S}^{V_D} g_c(V')(Q(V') - Q(V)) dV' \right) \frac{g_c(V)^2}{g(V)} S_{i_n} dV \tag{4.37}$$

where

$$\frac{g_c(V,E)}{g(V,E)} = \frac{g(V,E)}{g(V,E) + \frac{\partial g(V,E)}{\partial E} E} \tag{4.38}$$

and the corrected length L_c is given by:

$$L_c = \int_0^L \frac{g_c}{g} dx = L \frac{\int_{V_S}^{V_D} g_c(V) dV}{\int_{V_S}^{V_D} g(V) dV} \tag{4.39}$$

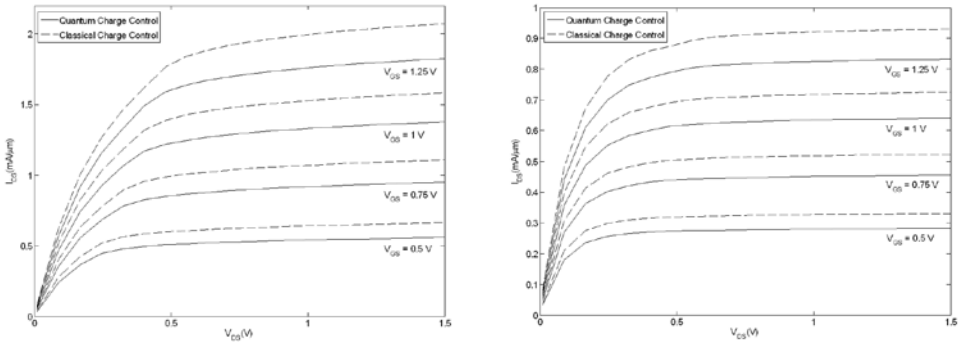
From eq. (4.39), L_c can be considered as effective or corrected length of the channel in order to take into account the degradation of mobility along the channel due to velocity saturation.

The power spectral density for the local noise source is given by:

$$S_{i_n}(x) = 4kT_L \frac{g(x)}{g_c(x)} \frac{T_n(x)}{T_L} \tag{4.40}$$

4.5 RF and Noise Simulations

In this section some simulated results will be obtained using the previously presented model. First, the DC drain characteristics are obtained. Figure 4.4a and 4.4b shows the drain current characteristics for a 50 nm gate length SGT (R=5 nm, t_{ox}=1.5 nm, V_{GS}-V_{TH}=0.5V, 0.75V, 1V, 1.25V) calculated with the above described model. In Fig. 4.4a the temperature model is used, whereas Fig. 4.4b presents results obtained using the drift-diffusion transport model.



(a) (b)

Fig. 4.4. Drain current characteristics for the temperature model (a) and Drift-Diffusion model (b). Quantum charge control (solid line) and Classical charge control (dashed line). Gate length L=50 nm, V_{GS}-V_{TH}=0.5V, 0.75V, 1V, 1.25V

The effect of velocity overshoot translates into an increase (about 25% higher for this gate length) in the drain current and transconductance.

Figure 4.5 presents a comparison between measured data from S. D. Suk et al. [Suk-2005] and simulated normalized drain current (I_{DS}) versus the diameter of the cylinder (V_{GS}=0.8V, 1V, 1.2V, 1.4V). The device is a SGT MOSFET with R=5 nm, t_{ox}=3 nm and gate length L=30 nm. A good agreement has been obtained adjusting the constant μ_0 in eq. (4.38), by using μ_0=*847 cm^2/V*s*.

Figures 4.6 and 4.7 compare the f_T and f_{max} calculated with drift-diffusion and hydrodynamic models for a SGT (R=5nm, V_{GS}–V_{TH}=0.5V, V_{DS}=1V).

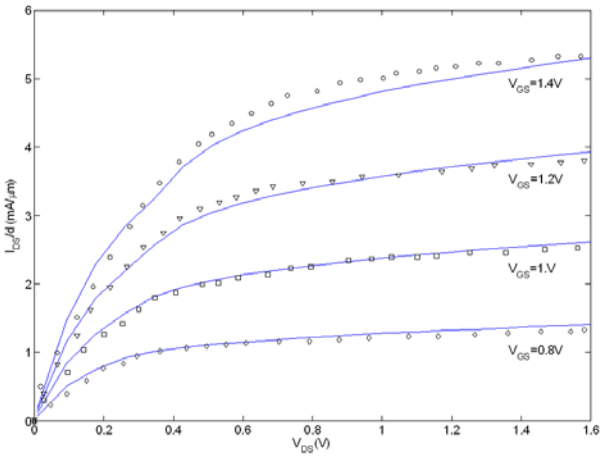


Fig. 4.5. Comparison between measured and simulated normalized drain current versus diameter, using the temperature model (solid line)

Due to the overshoot effect the values of f_T and f_{max} are considerably higher in the temperature transport model. Small differences have been shown in f_T

between classical and quantum charge control models. This is due to the fact that f_T depends on the ratio g_m/C_{gs}, where the numerator and denominator are affected in the same magnitude for the channel capacitance. Thus, except for the threshold voltage shift, the channel capacitance reduction due to quantum effect is not appreciable in f_T. However, the differences in f_{max} between the classical and quantum case are more important due to the differences in the intrinsic resistance and channel conductances. For shorter gate length the overshoot velocity effect, taken into account in the temperature transport model, increases the transconductance and, as a consequence, the value of f_{max}.

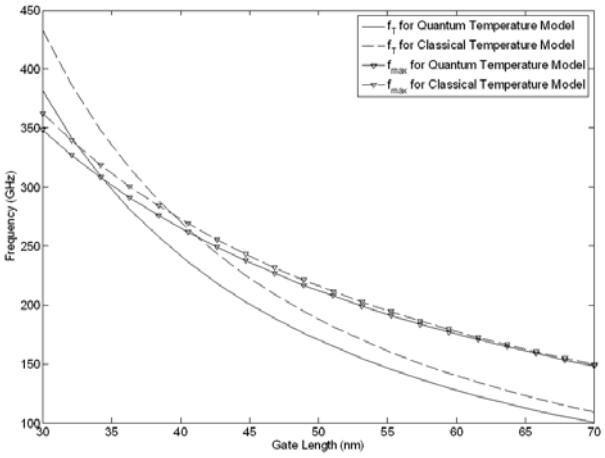


Fig. 4.6. Transition frequency f_T and Maximum Oscillation frequency f_{max} as a function of gate length, for temperature model. Radius R=5 nm, V_{GS}-V_{TH}=0.5V, V_{DS}=1V

Changing to a current-current representation, the noise sources, and their correlation are written as a function of parameters independent of the frequency *R*,

P, *C*, the intrinsic gate-to-source capacitance of the device, C_{gs}, and the room temperature T_a:

$$< i_g^2 >= 4kT_a RC_{gs}^2 \omega^2 \Delta f \; / \; g_m \tag{4.41}$$

$$< i_d^2 >= 4kT_a P g_m \Delta f \tag{4.42}$$

$$C = \frac{\mathrm{Im} < i_g i_d^* >}{\sqrt{< i_g^2 > \cdot < i_d^2 >}} \tag{4.43}$$

An accurate knowledge of *P* is important because it characterizes the channel noise. The correlation is essentially imaginary because of the capacitive coupling between the channel and the gate. Here *C* is the correlation parameter.

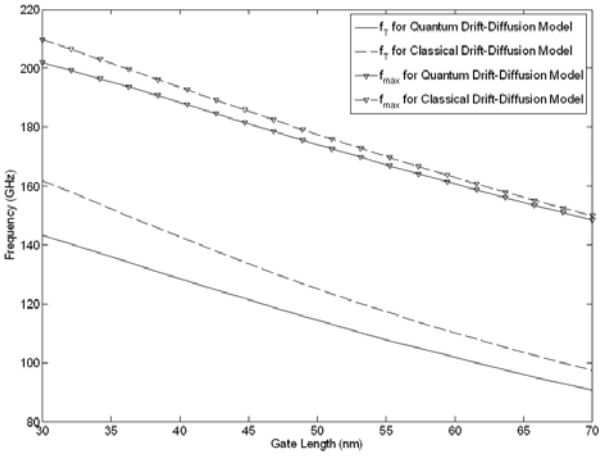


Fig. 4.7. Transition frequency f_T and Maximum Oscillation frequency f_{max} as a function of gate length, for drift-diffusion model. Radius R=5 nm, V_{GS}-V_{TH}=0.5V, V_{DS}=1V

For a typical low noise bias point, the shot noise due to the gate tunneling effect can be neglected compared to diffusion noise [Pailloncy-2004]. Then, the

minimum noise temperature including parasitics can be written as a function of correlation matrix elements [Danneville-2005]:

$$T_{\min} = 2T_0 \frac{f}{f_T} \sqrt{PR(1-C^2) + (P + R - 2C\sqrt{PR})(R_g + R_s) g_m} \tag{4.44}$$

Figure 4.8 shows the intrinsic and extrinsic noise figure for SGT (R=5 nm, t_{ox}=1.5 nm, V_{ds}=1V, V_{gs}-V_{TH}=0.5V) at 10 GHz calculated using the drift-diffusion and temperature models.

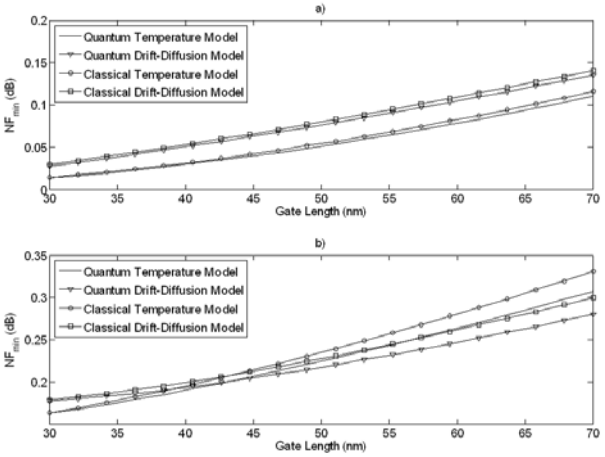


Fig. 4.8. Intrinsic (a) and extrinsic (b) Minimum Noise Figure NF_{min}(dB) as function of gate length. Radius R=5 nm, V_{GS}-V_{TH}=0.5V, V_{DS}=1V

From this figure some conclusions can be drawn. First, a lower noise figure is always achieved when quantum effects are taken into account. Second, for gate lengths smaller than 45 nm, lower noise figure values are obtained using the

temperature model. This fact is a consequence of higher f_T and f_{max} since around these gate lengths velocity overshoot compensates the higher intrinsic noise due to larger *P* values obtained using the temperature model.

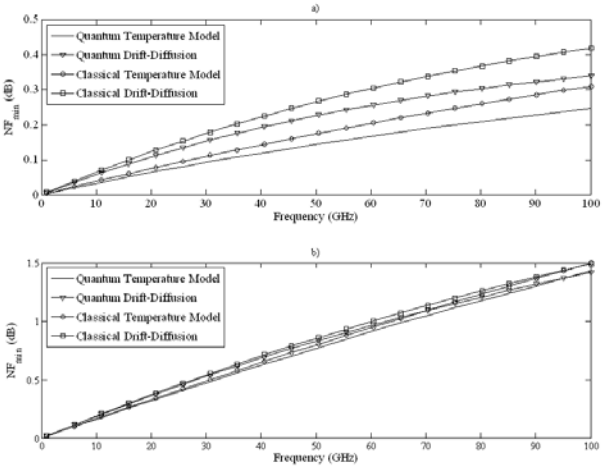


Fig. 4.9. Intrinsic (a) and extrinsic (b) Minimum Noise Figure NF_{min}(dB) as function of frequency. Gate length L=50 nm, Radius R=5 nm, V_{GS}-V_{TH}=0.5V, V_{DS}=1V

The frequency dependence of the noise performance is also studied, as shown in Fig. 4.9. For a 50 nm gate length the intrinsic minimum noise figure is better for the temperature model than for the drift-diffusion model. Following eq. (4.44), the frequency slope of the minimum noise temperature depends on the parasitic resistance and the f_T, resulting in an important contribution of parasitics in the high frequency extrinsic noise. The difference between drift-diffusion and temperature transport model increases when the extrinsic (with parasitics) noise figure is considered, due to the difference in f_T between the two models.

4.6 Analytical Determination of Drain and Gate Noise Spectrums

In this section compact expressions to model the drain and gate current noise spectrum densities and their correlation for SGT MOSFETs are presented. We apply the model previously developed for DG MOSFET devices [Lazaro-2006] to the SGT case and obtain the charge and current expressions. The compact noise model will be applied to analyze the noise performance of SGT devices and some trends related to the downscaling variations will be provided. Also, the noise properties of the devices will be discussed.

4.6.1 Charge and Drain Current Models

In order to compute the drain current, we need to determine the charge carrier concentration along the channel. To this end, we define the charge q_n, as the charge Q given by eq. (4.17) and normalized to $C_{ox}\phi_t$:

$$q_n = \frac{Q}{C_{ox}\phi_t} \tag{4.45}$$

For the typical operating voltage range in this type of transistors it can be shown that [Iniguez-2005]:

$$dV = -\phi_t \left[1 + \frac{1}{q_n} + \frac{1}{q_n + q_0} \right] dq_n \tag{4.46}$$

where q_0 is the normalized charge Q_0 given by eq. (4.12):

$$q_0 = \frac{Q_0}{C_{ox}\phi_t} \tag{4.47}$$

Using eq. (4.46), the channel charge can be integrated. Following the procedure given in [Nae-2009], the drain current taking into account the velocity saturation and short channel effects is given by:

$$I_D = \frac{W\mu_{eff}C_{ox}\phi_t^2}{2L_e}\left\{(q_S^2 - q_D^2) + 4(q_S - q_D) + q_0 \ln\frac{q_S + q_0}{q_D + q_0}\right\} \tag{4.48}$$

where q_S and q_D represent the normalized charge q_n evaluated at the source $q_n(V=0)$ and at the effective drain voltage $q_n(V=V_{Defs})$ respectively, and $L_e=L-\Delta L$, where ΔL is the channel length modulation in the saturation region given by eq. (25) in [Nae-2009].

The saturation voltage is obtained in eq. (4.48) to the current at saturation point, $I_{DSAT} = WC_{ox}\phi_t q_{sat} v_{sat}$, solving for the charge at saturation point $q_{sat}=q_n(V=V_{DSsat})$. From q_{sat}, the saturation voltage V_{DSsat} is easily obtained from:

$$V_{DSsat} = V_{GS} - V_0 - \phi_t q_{sat} - \phi_t \ln\left(q_{sat}/q_0\right) - \phi_t \ln(1 + q_{sat}/q_0) \tag{4.49}$$

The same function that was introduced by B. Nae et al [Nae-2009] to interpolate V_{DSef} is used in this model. The effective mobility is given by:

$$\mu_{eff} = \frac{\mu_0}{\sqrt{1 + \left(\frac{\mu_0 V_{DSef}}{L v_{sat}}\right)^2}} \tag{4.50}$$

where μ_0 is evaluated at the source end of the channel using eq. (4.21).

4.6.2 Compact Noise Expressions

Following the procedure proposed by A. Lazaro et al. [Lazaro-2009] for DG MOSFETs, in this section we will derive the compact expressions for the drain and gate current noise spectrum densities and their correlation of SGT MOSFETs. In order to have an accurate description of the velocity saturation, we used the relationship between the mobility and the longitudinal electric field given by eq. (4.33), obtaining the following expression for the channel per unit length conductance:

$$g(V) = \frac{WQ\mu_0}{\sqrt{1+\left(E/E_c\right)^2}} = \frac{g_0}{\sqrt{1+\left(E/E_c\right)^2}} \tag{4.51}$$

with

$$g_0 = WQ(V)\mu_0 = WC_{ox}\phi_t\mu_0 q_n(V) \tag{4.52}$$

From eqs. (4.38) and (4.40), we obtain:

$$g_c(V) = g(V)\cdot\left(1+\left(E/E_c\right)^2\right) = g_0\sqrt{1+\left(E/E_c\right)^2} \tag{4.53}$$

$$S_{i_d^2} = \frac{4kT_L}{I_D L_c^2}\int_{V_S}^{V_D} g^2\left(\frac{g_c}{g}\frac{T_n}{T_L}\right)dV \tag{4.54}$$

In order to investigate the heating effect of electrons in the gradual region of the channel, we will consider first the case where we have no heating. If we ignore the heating effect of electrons in the gradual channel region, namely we assume the thermal equilibrium prevails in gradual channel region, the noise temperature is equal to the lattice temperature, T_n=T_L. From eqs. (4.51) and (4.53), the following expression to evaluate the power spectral density for the local noise source (see eq. 4.54) is obtained:

$$\frac{g_c(V)}{g(V)}\frac{T_n}{T_L} = 1 + \left(E / E_c\right)^2 \tag{4.55}$$

$$S_{i_d^2} = \frac{4kT_L}{I_D L_c^2}\int_{V_S}^{V_D} g_0^2 dV = \frac{4kT_L}{I_D L_c^2}(W\mu_0 C_{ox}\phi_t)^2 \int_{V_S}^{V_D} q_n^2 dV \tag{4.56}$$

Substituting the expression of *dV* from eq. (4.46) in eq. (4.56), the following compact expression for the drain noise spectral density is obtained:

$$S_{i_d^2} = \frac{4kT_L}{I_D L_c^2}(W\mu_0 C_{ox}\phi_t)^2 F \tag{4.57}$$

where

$$F = -\phi_t\left[\frac{q_n^3}{3} - q_n^2 - q_n q_0 + q_0^2 \ln(q_n + q_0)\right]_{q_S}^{q_D} \tag{4.58}$$

Substituting eq. (4.33) in eq. (4.31), the following relations for the conductance and corrected conductance are found:

$$g = \left[g_0^2 - \left(\frac{I_D}{E_c}\right)^2\right]^{1/2} = (W\mu_0 C_{ox}\phi_t)\left[q_n^2 - q_a^2\right]^{1/2} \tag{4.59}$$

$$g_c = \frac{g_0^2}{\left[g_0^2 - \left(\frac{I_D}{E_c}\right)^2\right]^{1/2}} = \left(W\mu_0 C_{ox}\phi_t\right)\frac{q_n^2}{\left[q_n^2 - q_a^2\right]^{1/2}} \tag{4.60}$$

where q_a is defined as:

$$q_a = \frac{I_D}{W\mu_0 C_{ox}\phi_t E_c} \tag{4.61}$$

Before evaluating the gate spectral density (see eq. 4.36) and the cross spectral density (see eq. 4.37), we need to calculate the integral:

$$\begin{aligned}
&\int_{V_S}^{V_D} g_c(V')(Q(V')-Q(V))dV' = \\
&= \int_{V_S}^{V_D} \left(W\mu_0 C_{ox}\phi_t q_n^2(V')\left[q_n^2(V')-q_a^2\right]^{-1/2}\right) C_{ox}\phi_t (q_n(V')-q_n(V))dV' \\
&= C_{ox}\phi_t \cdot W\mu_0 C_{ox}\phi_t \left[\left(\int_{V_S}^{V_D} q_n^3(V')\left[q_n^2(V')-q_a^2\right]^{-1/2} dV' \right) \right. \\
&\left. - q_n(V)\left(\int_{V_S}^{V_D} q_n^2(V')\left[q_n^2(V')-q_a^2\right]^{-1/2} dV' \right) \right] = C_{0x}\phi_t \cdot W\mu_0 C_{ox}\phi_t \left(A + Bq_n(V)\right)
\end{aligned} \tag{4.62}$$

where A and B are functions of the normalized charges, q_S and q_D:

$$\begin{aligned}
A = -\phi_t \Bigg[& -\frac{q_0^3}{(q_n^2 - q_a^2)^{1/2}} \ln(q_n + q_0) + (q_n^2 - q_a^2)^{1/2}\left(\frac{1}{3}q_n^2 + \frac{2}{3}q_a^2 + q_n - q_0\right) \\
& + \frac{q_0^3}{(q_n^2 - q_a^2)^{1/2}} \ln\left(\begin{array}{l} 2q_0^2 - 2q_a^2 - 2(q_n + q_0)q_0 + 2(q_0^2 - q_a^2)^{1/2} \\ \cdot((q_n + q_0)^2 - 2(q_n + q_0)q_0 + q_0^2 - q_a^2)^{1/2} \end{array}\right) \\
& + \left(q_a^2 + q_0^2\right)\ln(q_n + (q_n^2 - q_a^2)^{1/2})\Bigg]_{q_S}^{q_D}
\end{aligned} \tag{4.63}$$

$$\begin{aligned}
B = \phi_t \Bigg[& \left(\frac{1}{2}q_n + 2\right)(q_n^2 - q_a^2)^{1/2} + \left(\frac{1}{2}q_a^2 - q_0\right)\ln\left(q_n + (q_n^2 - q_a^2)^{1/2}\right) \\
& + \frac{q_0^2}{(q_0^2 - q_a^2)^{1/2}}\ln(q_n + q_0) - \frac{q_0^2}{(q_0^2 - q_a^2)^{1/2}}\ln(2q_0^2 - 2q_a^2 - 2(q_n + q_0)q_0 + \\
& 2(q_0^2 - q_a^2)^{1/2}((q_n + q_n)^2 - 2(q_n + q_0)q_0 + q_0^2 - q_a^2)^{1/2})\Bigg]_{q_S}^{q_D}
\end{aligned} \tag{4.64}$$

Using eq. (4.61), the following compact analytical expressions for eqs. (4.36) and (4.37) are found:

$$S_{i_g^2} = \frac{\omega^2 W^2}{I_D^5 L_c^2}\left(\int_{V_S}^{V_D}\left(\int_{V_S}^{V_D} g_c(V')(Q(V')-Q(V))dV'\right)^2 \frac{g_c^2(V)}{g(V)} S_{i_n} dV\right)$$

$$= \frac{\omega^2 W^2}{I_D^5 L_c^2} 4kT_L \cdot (W\mu_0 C_{ox}\phi_t)^2 (C_{ox}\phi_t)^2 \left(\int_{V_S}^{V_D} (A+Bq_n(V))^2 g_0^2(V)dV\right)$$

$$= \frac{\omega^2 W^2}{I_D^5 L_c^2} 4kT_L (W\mu_0 C_{ox}\phi_t)^2 (W\mu_0 C_{ox}\phi_t)^2 (C_{ox}\phi_t)^2 \cdot \qquad (4.65)$$

$$\cdot \left(\int_{V_S}^{V_D} (A+Bq_n(V))^2 q_n^2(V)dV\right)$$

$$= \frac{\omega^2 W^2}{I_D^5 L_c^2} 4kT_L \cdot (W\mu_0 C_{ox}\phi_t)^4 (C_{ox}\phi_t)^2 \left(\int_{V_S}^{V_D} (A+Bq_n(V))^2 q_n^2(V)dV\right)$$

where

$$\int_{V_S}^{V_D} (A+Bq_n(V))^2 q_n^2(V)dV = A^2\int_{V_S}^{V_D} q_n^2(V)dV + 2AB\int_{V_S}^{V_D} q_n^3(V)dV + B^2\int_{V_S}^{V_D} q_n^4(V)dV \qquad (4.66)$$
$$= A^2C + 2ABD + B^2E$$

and the functions *C*, *D*, *E* are defined as:

$$C = \int_{V_S}^{V_D} q_n^2(V)dV = -\phi_t\left[\frac{q_n^3}{3} + q_n^2 - q_0 q_n + q_0^2 \ln(q_n + q_0)\right]_{q_S}^{q_D} \qquad (4.67)$$

$$D = \int_{V_S}^{V_D} q_n^3(V)dV = -\phi_t\left[\frac{q_n^4}{4} + \frac{2q_n^3}{3} - \frac{q_0}{2}q_n^2 + q_0^2 q_n - q_0^3 \ln(q_n + q_0)\right]_{q_S}^{q_D} \qquad (4.68)$$

$$E = \int_{V_S}^{V_D} q_n^4(V)dV = -\phi_t\left[\frac{q_n^5}{5} + \frac{q_n^4}{2} - \frac{q_0}{3}q_n^3 + \frac{1}{2}q_0^2 q_n^2 - q_0^3 q_n + q_0^4 \ln(q_n + q_0)\right]_{q_S}^{q_D} \qquad (4.69)$$

The cross noise spectral density is calculated by:

$$S_{i_g i_d^*} = \frac{j\omega W}{I_D^3 L_c^2}\left(\int_{V_S}^{V_D}\left(\int_{V_S}^{V_D} g_c(V')(Q(V')-Q(V))dV'\right)\frac{g_c^2(V)}{g(V)}S_{i_n}dV\right)$$
$$= \frac{j\omega W}{I_D^3 L_c^2} 4kT_L \cdot W\mu_0 C_{0x}\phi_t \cdot \left(C_{ox}\phi_t\right)\int_{V_S}^{V_D}\left(A+Bq_n(V)\right)g_0^2(V)dV \qquad (4.70)$$
$$= \frac{j\omega W}{I_D^3 L_c^2} 4kT_L \cdot \left(W\mu_0 C_{0x}\phi_t\right)^3 \cdot \left(C_{ox}\phi_t\right)\int_{V_S}^{V_D}\left(A+Bq_n(V)\right)q_n^2(V)dV$$

where

$$\int_{V_S}^{V_D}\left(A+Bq_n(V)\right)q_n^2(V)dV = A\int_{V_S}^{V_D} q_n^2(V)dV + B\int_{V_S}^{V_D} q_n^3(V)dV = AC+BD \qquad (4.71)$$

Finally, the gate and cross spectral densities are given by:

$$S_{i_g^2} = \frac{\omega^2 W^2}{I_D^5 L_c^2} 4kT_L \cdot (W\mu_0 C_{ox}\phi_t)^4 \left(C_{ox}\phi_t\right)^2 \left(A^2C + 2ABD + B^2E\right) \qquad (4.72)$$

$$S_{i_g i_d^*} = \frac{j\omega W}{I_D^3 L_c^2} 4kT_L \cdot \left(W\mu_0 C_{0x}\phi_t\right)^3 \left(C_{ox}\phi_t\right)\left(AC+BD\right) \qquad (4.73)$$

These expressions depend on the drain current I_D, and expressions A, B, C, D, E which are functions of q_S and q_D. The length L_c is given by eq. (4.39). Using eqs. (4.51) and (4.59-4.60), L_c is given by:

$$L_c = L\frac{B}{G} \qquad (4.74)$$

where G is given by:

$$G = \phi_t\left[\left(\frac{1}{2}q_n+1\right)(q_n^2-q_a^2)^{1/2} - \frac{1}{2}q_a^2\ln(q_n+(q_n^2-q_a^2)^{1/2})\right.$$
$$+\frac{q_a^2}{(-q_a^2)^{1/2}}\left(\ln(-2q_a^2+2(-q_a^2)^{1/2}(q_n^2-q_a^2)^{1/2}) - \ln q_n\right) + G_1^{1/2} - q_0\ln(q_n+G_1^2) \qquad (4.75)$$
$$\left.-(q_0^2-q_a^2)^{1/2}\left(\ln(2q_0^2-2q_a^2-2(q_n+q_0)q_0+2(q_0^2-q_a^2)^{1/2}G_1^{1/2}) - \ln(q_n+q_0)\right)\right]_{q_S}^{q_D}$$

If we consider the heating effect of electrons in the gradual channel region, and use the approximation that the noise temperature is equal to carrier temperature given by eq. (4.34) (T_n=T_e), then eq. (4.55) must be replaced by:

$$\frac{g_c(V)}{g(V)}\frac{T_n}{T_L}=\left(1+\left(E/E_c\right)^2\right)^2 \tag{4.76}$$

From eqs. (4.51) and (4.59) a useful relationship can be obtained:

$$(E/E_c)^2=\frac{\left(q_a/q_n\right)^2}{1-\left(q_a/q_n\right)^2} \tag{4.77}$$

Using eq. (4.77), the drain, gate and cross noise spectral densities can be analytically obtained following the same steps as the case without carrier heating. The new expressions for *C*, *D*, *E* and *F* when the heating effect is considered are:

$$\begin{aligned}
C=&\int_{V_S}^{V_D}\frac{q_n^2(V)}{1-(q_a/q_n)^2}dV=-\phi_t[1/3q_n^3+q_n^2-q_nq_0+q_a^2q_n-q_a^3/(2q_0-2q_a)\cdot\\
&\ln(q_n+q_a)q_0+q_a^2/(2q_0-2q_a)\ln(q_n+q_a)q_0-2q_a^3/(2q_0-2q_a)\ln(q_n+q_a)\\
&+q_a^4/(2q_0-2q_a)\ln(q_n+q_a)+1/(q_0^2-q_a^2)q_0^4\ln(q_n+q_0)\\
&+q_a^3/(2q_a+2q_0)\ln(q_n-q_a)q_0+q_a^2/(2q_a+2q_0)\ln(q_n-q_a)q_0\\
&+2q_a^3/(2q_a+2q_0)\ln(q_n-q_a)+q_a^4/(2q_a+2q_0)\ln(q_n-q_a)\Big]_{q_S}^{q_D}
\end{aligned} \tag{4.78}$$

$$\begin{aligned}
D=&\int_{V_S}^{V_D}q_n^3(V)\frac{1}{1-(q_a/q_n)^2}dV=-\phi_t\Big[1/4q_n^4+2/3q_n^3-1/2q_n^2q_0+1/2q_n^2q_a^2\\
&+q_0^2q_n+2q_a^2q_n+q_a^4/(2q_0-2q_a)\ln(q_n+q_a)q_0-q_a^3/(2q_0-2q_a)\ln(q_n+q_a)q_0\\
&+q_a^4/(q_0-q_a)\ln(q_n+q_a)-q_a^5/(2q_0-2q_a)\ln(q_n+q_a)-1/(q_0^2-q_a^2)q_0^5\ln(q_n+q_0)\\
&+q_a^4/(2q_a+2q_0)\ln(q_n-q_a)q_0+q_a^3/(2q_a+2q_0)\ln(q_n-q_a)q_0\\
&+2q_a^4/(2q_a+2q_0)\ln(q_n-q_a)+q_a^5/(2q_a+2q_0)\ln(q_n-q_a)\Big]_{q_S}^{q_D}
\end{aligned} \tag{4.79}$$

$$E=\int_{V_s}^{V_D} q_n^4(V)\frac{1}{1-(q_a/q_n)^2}dV=-\phi_t\cdot$$
$$[1/5q_n^5+1/2q_n^4-1/3q_n^3q_0+1/3q_a^2q_n^3+q_n^2q_a^2+1/2q_n^2q_0^2-q_a^2q_nq_0+q_a^4q_n$$
$$-q_0^3q_n-q_a^5/(2q_0-2q_a)\ln(q_n+q_a)q_0+q_a^4/(2q_0-2q_a)\ln(q_n+q_a)q_0$$
$$-2q_a^5/(2q_0-2q_a)\ln(q_n+q_a)+q_a^6/(2q_0-2q_a)\ln(q_n+q_a) \quad (4.80)$$
$$+q_0^6/(q_0^2-q_a^2)\ln(q_n+q_0)+q_a^5/(2q_a+2q_0)\ln(q_n-q_a)q_0$$
$$+q_a^4/(2q_a+2q_0)\ln(q_n-q_a)q_0$$
$$+2q_a^5/(2q_a+2q_0)\ln(q_n-q_a)+q_a^6/(2q_a+2q_0)\ln(q_n-q_a)]_{q_s}^{q_D}$$

$$F=-\phi_t\left[1/3q_n^3+q_n^2-q_nq_0+q_a^2q_n-q_a^3/(2q_0-2q_a)\log(q_n+q_a)q_0\right.$$
$$+q_a^2/(2q_0-2q_a)\log(q_n+q_a)q_0$$
$$-2q_a^3/(2q_0-2q_a)\log(q_n+q_a)+q_a^4/(2q_0-2q_a)\log(q_n+q_a) \quad (4.81)$$
$$+1/(q_0^2-q_a^2)q_0^4\log(q_n+q_0)+q_a^3/(2q_a+2q_0)\log(q_n-q_a)q_0$$
$$+q_a^2/(2q_a+2q_0)\log(q_n-q_a)q_0+2q_a^3/(2q_a+2q_0)\log(q_n-q_a)$$
$$\left.+q_a^4/(2q_a+2q_0)\log(q_n-q_a)\right]_{q_S}^{q_D}$$

According to several authors [Deen-2006], the velocity saturation effect only contributes to the total noise in the linear part of the channel. It was successfully shown by M.J. Deen et al. [Deen-2006] that the contribution of the velocity saturation region to the output noise current is negligible as the carriers in that region travel at their saturation velocity v_{sat} and they do not respond to the fluctuations of the electric field caused by voltage noise in that region. This argument has been the basis of most of the channel noise models published. In the saturation region of the channel, we can expect that T_n will be higher than the electronic temperature (T_e), but these noise fluctuations are not collected at the terminals. For this reason, for the integrals involved in eqs. (4.35-4.37), the upper limit V_D must be replaced by V_{Dsat} (see eq. 4.49) in the saturation region ($V_{DS}>V_{DSsat}$).

4.6.3 Results and Discussion

Some noise models have been proposed in the literature for MOSFETs. Following the Van der Ziel notation [Ziel-1986], the drain current noise spectrum density is expressed as:

$$S_{i_d^2} = 4kT_L g_{ds0}\gamma \tag{4.82}$$

where $4kT_Lg_{ds0}$ is the current noise spectrum associated to a conductance g_{ds0} at temperature T_L. In the case of a MOSFET, however, since a channel conductance g_{ds} depends on a bias voltage, g_{ds} is fixed to the value obtained when V_{DS}=0 (g_{ds0}=g_{ds}(V_{DS}=0)). The noise excess factor γ is used to evaluate the characteristics of the thermal noise. For V_{DS}=0, γ=*1* because the channel is like a conductance of value g_{ds0}. In the case of long channel, it has been found experimentally and theoretically that 2/3 ≤ γ ≤1 in a linear region and γ converges to 2/3 in the saturation region.

As mentioned above, the physical origin of the induced-gate noise (S_{ig}^2) is the capacitive coupling of the channel conductance to the gate capacitance. Based on this assumption, van der Ziel derived a simple expression:

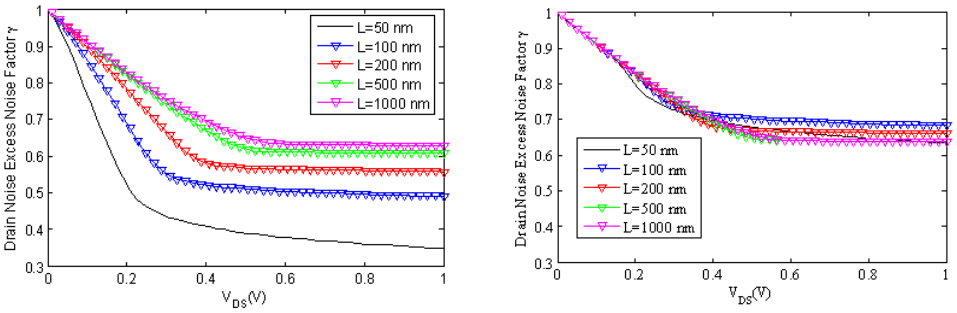
$$S_{i_g^2} = 4kT_L g_g \beta \tag{4.83}$$

with

$$g_g = \frac{\left(\omega C_{gs}\right)^2}{5g_{ds0}} \tag{4.84}$$

where C_{gs} is the gate-source capacitance. The expression is valid in the saturation region for frequencies below 1/3 of the cut-off frequency f_T and this frequency

range is sufficient for most real applications of the device. Theoretically, the gate excess noise factor, β, tends to 4/3 and the imaginary part of coefficient *Im(C)* tends to 0.4 in saturation for the case of long channel. The bias behavior of the excess noise factors and correlation coefficients for SGT with different channel lengths are shown in the next figures.

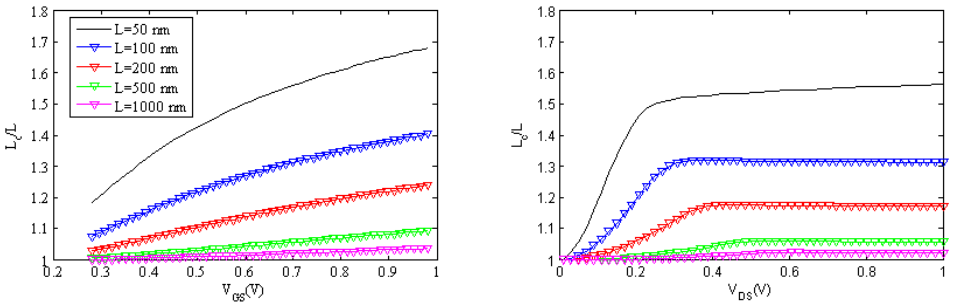


(a) (b)

Fig. 4.10. The drain excess noise factor γ as function of drain voltage (R=5nm, t_{ox}=3 nm and V_{GS}-V_{TH}=0.5 V): (a) considering T_n=T_L, (b) including carrier heating

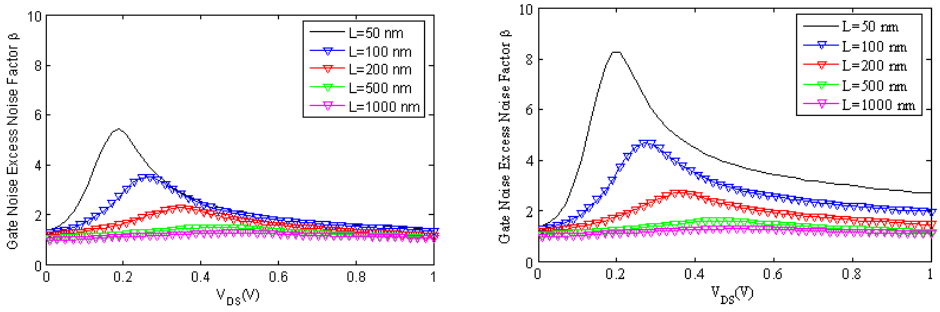
Figure 4.10 shows the drain excess noise factor γ as function of drain voltage for a SGT with R=*5nm*, t_{ox}=*3 nm* and V_{GS}-V_{TH}=*0.5 V*. As the channel decreases, the drain noise factor also decreases. It can be observed that for the long-channel case in saturation, the drain excess noise factor γ tends to 2/3, and for V_{DS}=*0* it tends to 1. The values decrease steadily with the drain bias in saturation regime, which is attributed to the channel length modulation effect through the corrected length L_c and the potential distribution and the related mobility distribution along the channel. Such decrease of γ with the drain bias

becomes more critical for devices with smaller channel lengths, because the channel length modulation has larger effects for the short-channel devices. Moreover, when the gate length decreases, L_c differs from the channel length L. Figure 4.11 shows the ratio between the corrected length and channel length L_c/L for different gate lengths as function of gate voltage and drain voltage. The corrected length tends to L for the long channel case. In the long channel case we can consider that the critical field E_c tends to infinite and velocity saturation will not occur, thus from eqs. (4.51) and (4.53), g_c is equal to g and $L_c=L$. When the channel length decreases, g_c differs from g and the corrected length can be up to 1.5 times higher than the effective length for short channel cases. As a conclusion the noise model based on the conventional Klassen-Prins [Lazaro-2009; Klaassen-1967] which considers $g_c=g$ and $L_c=L$ is not useful to model the channel noise for the short channel case.



(a) (b)

Fig. 4.11. (a) Normalized corrected length L_c/L as function of gate voltage (R=5nm, t_{ox}=3nm, V_{DS}=1V). (b) Normalized corrected length L_c/L as function of drain voltage (R=5nm, t_{ox}=3nm and V_{GS}-V_{TH}=0.5V.



(a) (b)

Fig. 4.12. The gate excess noise factor β as a function of drain voltage (R=5nm, t_{ox}=3 nm and V_{GS}-V_{TH}=0.5 V): (a) considering T_n=T_L, (b) including carrier heating

Figure 4.12 shows the gate noise factor β for the same SGT and same bias conditions of Fig. 4.10. The factor β increases with the reduction in the channel length. Also, the factor β is almost constant for the long channel case and close to 4/3. Figure 4.13 shows the imaginary part of the correlation coefficient as a function of drain voltage for the same SGT (R=5nm, t_{ox}=3 nm and V_{GS}-V_{TH}=0.5 V). In the linear bias region, the correlation coefficient is close to zero and linearly increases with drain bias. In the saturation region is almost constant. It is around 0.4 for the long-channel case, and goes to 0 at V_{DS}=0 V, where the transistor is similar to a resistor. This coefficient decreases with channel length reduction.

For a SGT with R=5nm and t_{ox}=3 nm, Fig. 4.14 and 4.15 show the drain and gate excess noise factors as well as the imaginary part of the correlation coefficient as a function of gate voltage, at a fixed drain voltage of 1 V. The drain excess noise factor γ remains relatively constant with the increase of gate voltage for all channel lengths (Fig. 4.14). On the other hand, the gate excess noise factor

β (Fig. 4.15) is found to depend strongly on the gate voltage for short-channel devices and it exceeds the value for long channels considerably. The value of the imaginary part of the correlation coefficient as a function of gate voltage (Fig. 4.16) smoothly decreases with gate overvoltage for all channel lengths.

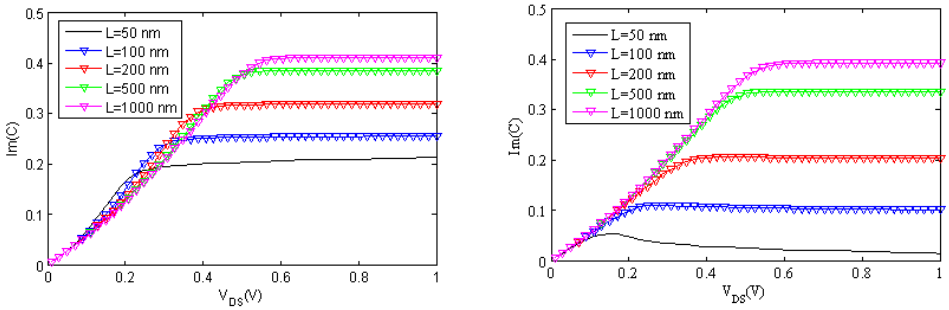


Fig. 4.13. The imaginary part of the correlation coefficient *Im(C)* as a function of drain voltage (R=5nm, t_{ox}=3 nm and V_{GS}-V_{TH}=0.5 V): (a) considering T_n=T_L, (b) including carrier heating

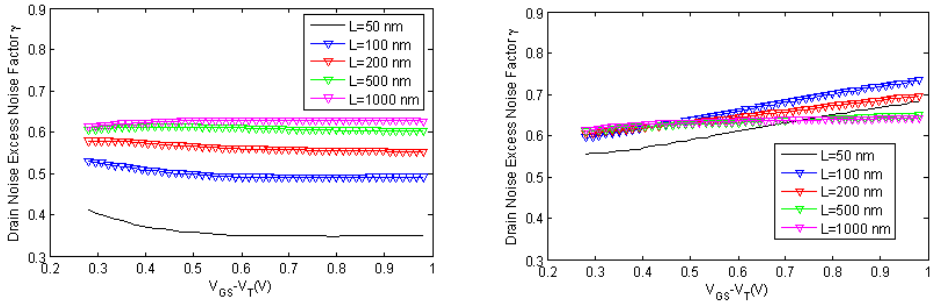


Fig. 4.14. The drain excess noise factor γ as function of gate voltage (R=5nm, t_{ox}=3 nm and V_{DS}=1 V): (a) considering T_n=T_L, (b) including carrier heating

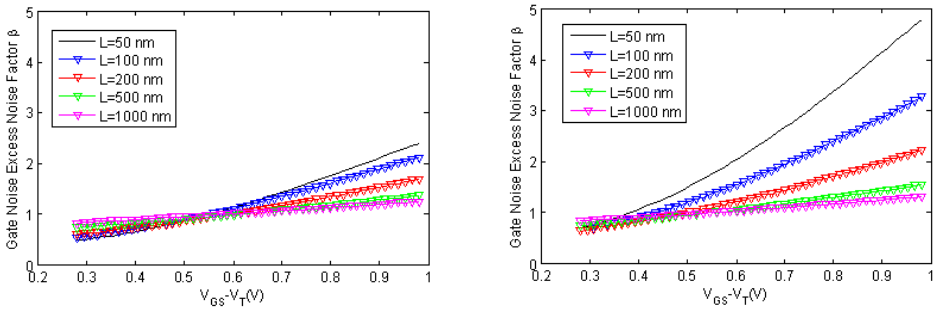


Fig. 4.15. The gate excess noise factor β as a function of gate voltage (R=5nm, t_{ox}=3 nm and V_{DS}=1 V): (a) considering $T_n=T_L$, (b) including carrier heating

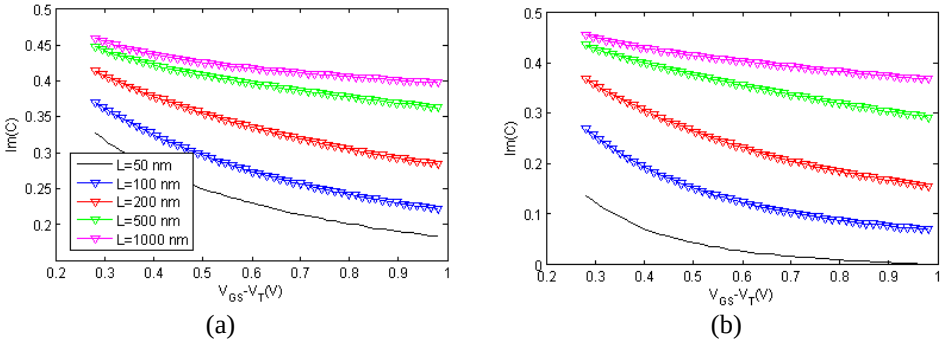


Fig. 4.16. The imaginary part of the correlation coefficient *Im(C)* as a function of gate voltage (R=5nm, t_{ox}=3 nm and V_{DS}=1 V): (a) considering $T_n=T_L$, (b) including carrier heating

Previous figures compare the case where the noise temperature is equal to the lattice temperature and the effects of carrier heating are ignored, and considering that the noise temperature is equal to the carrier temperature given by eq. (4.34). Although this assumption is questionable [Nougier-1977], it can help to understand the effect of heating in the gradual channel region. In addition, this assumption allows obtaining analytical expressions for the noise spectral densities.

Fig. 4.10b and Fig. 4.14b show an important increase in drain excess noise ratio γ when heating is considered. Also important increases in gate excess noise ratio β are caused (Fig. 4.12b and 4.15b) by carrier heating. However, the correlation coefficient (Fig. 4.12b and 4.15b) decreases when carrier heating is incorporated. The bias and scaling behavior predicted for the present SGT MOSFETs noise model agree with other compact models for conventional SG MOSFETs. However, experimental results from different authors [Deen-2006; Mahajan-2009; Klein-1999; Knoblinger-2001] for SG MOSFETs for various lengths found excess noise ratios γ greater than 1 for short channel devices below 100 nm. Also experimental results [Han-2004; Jundal-2006] show an important increase of γ with drain voltage for sub-100 nm gate lengths SG MOSFET devices. Various theories supported by experimental measurements have been developed to explain this channel excess noise. Klein [Klein-1999] and Knoblinger et al. [Knoblinger-2001] attribute the excess channel noise to the carrier heating in the velocity saturated region. However, Deen et al. [Deen-2006] show experimentally that hot carrier effects in the saturation region are negligible, as considered in the present model. They explain the excess noise using channel-length-modulation (CLM) only. R.P. Jindal [Jindal-2006] attributes part of this excess noise to the noise contribution due to a shot noise associated to a diffusion current at the source side of the channel. However, device simulations using drift-diffusion and hydrodynamic models for sub-100 nm MOSFETs report noise less than the noise seen experimentally [Mahajan-2009]. Additional noise mechanisms or noise contributions must be taken into account in simulations in order to explain the experimental results. There is a lack of experimental noise and simulated results using more accurate techniques such as Monte Carlo to validate these statements for sub-100 nm SGT MOSFETs.

4.7 Conclusions

The model presented in this section includes the channel noise, the induced-gate noise and the cross-correlation noise between drain and gate noises. The expressions are analytical and they depend on the mobile charge at the source and drain ends of the channel. The values of the excess noise factors and correlation coefficients follow the values previously obtained in the DG MOSFET model [Klaassen-1967]. Moreover, the compact noise model described does not use adjusting parameters, thus making it ideal for being used in circuit simulators with SGT MOSFETs.

The effect of carrier heating in the gradual channel has been investigated. According to the literature the noise associated with the saturation region has been neglected. Important increases are observed due to gradual channel heating for the drain and gate excess noise ratio when the gate length decreases. However, the increases in transition frequency (f_T) with downscaling compensate this effect, and the intrinsic minimum noise figure decreases with downscaling because it is proportional to f/f_T . However, the present model using the noise temperature equal to the carrier temperature does not give drain excess noise ratios higher than unity, as experimentally observed for sub-100 nm conventional MOSFET devices. The lack of noise experimental results in the literature for SGT devices does not permit to clarify the importance of excess noise in these devices. An improved channel noise temperature that takes into account more accurately the channel heating needs to be investigated further in order to explain possible discrepancies in nanoscale devices. Small dependence of excess noise parameters γ, β and correlation coefficient on the silicon radius is found using the noise model presented here. However, quantum effects must be incorporated in the charge control when the silicon radius decreases. These effects can be taken into account

by modifying the charge model proposed by B. Nae et al. [Nae-2009]. The compact model used here for the drain current is based on a drift diffusion formulation that could be questioned for nanoscale devices. A more sophisticated transport model should be used for nanoscale devices [Lazaro-2008].

4.8 References

[Arora-1995] N. D. Arora, R. Rios and D. A. Antoniadis, "Capacitance Modeling for Deep Submicron Thin Gate Oxide MOSFETs", *25th European Solid State Device Research Conference (ESSDERC)*, 569-572 (1995)

[Baccarani-1999] G. Baccarani and S. Reggiani, "A compact Double-Gate MOSFET model comprising quantum-mechanical and nonstatic effects", *IEEE Transactions on Electron Devices*, **46** (8), 1656-1666 (1999)

[Colinge-2004] J.-P. Colinge, "Multiple-gate SOI MOSFETs", *Solid-State Electronics*, **48** (6), 897-905 (2004)

[Danneville-2005] F. Danneville, G. Paillocny, A. Siligaris, B. Iniguez and G. Dambrine, "High frequency noise of SOI MOSFETs: Performances and limitations", *SPIE - Noise in Devices and Circuits III*, Austin, TX, 185-199 (2005)

[Deen-2006] M. J. Deen, C.-H. Chen, S. Asgaran, G. A. Rezvani, J. Tao and Y. Kiyota, "High-Frequency Noise of Modern MOSFETs: Compact Modeling and Measurement Issues", *IEEE Transactions on Electron Devices*, **53** (9), 2062-2081 (2006)

[Esseni-2003] D. Esseni, M. Mastrapasqua, G. K. Celler, C. Fiegna, L. Selmi and E. Sangiorgi, "An experimental study of mobility enhancement in ultrathin SOI transistors operated in double-gate mode", *IEEE Transactions on Electron Devices*, **50** (3), 802-808 (2003)

[Han-2004] K. Han, H. Shin and K. Lee, "Analytical drain thermal noise current model valid for deep submicron MOSFETs", *IEEE Transactions on Electron Devices*, **51** (2), 261-269 (2004)

[Iniguez-2005] B. Iniguez, D. Jimenez, J. Roig, H. A. Hamid, L. F. Marsal and J. Pallares, "Explicit continuous model for long-channel undoped surrounding gate MOSFETs", *IEEE Transactions on Electron Devices*, **52** (8), 1868-1873 (2005)

[Jindal-2006] R. P. Jindal, "Compact Noise Models for MOSFETs", *IEEE Transactions on Electron Devices*, **53** (9), 2051-2061 (2006)

[Klaassen-1967] F. M. Klaassen and J. Prins, "Thermal noise of MOS transistors", *Philips Results Reports*, 505-514 (1967)

[Klien-1999] P. Klein, "An analytical thermal noise model of deep submicron MOSFET's", *IEEE Electron Device Letters*, **20** (8), 399-401 (1999)

[Knoblinger-2001] G. Knoblinger, P. Klein and H. Tiebout, "A new model for thermal channel noise of deep-submicron MOSFETs and its application in RF-CMOS design", *IEEE Journal of Solid-State Circuits*, **36** (5), 831-837 (2001)

[Lazaro-2006] A. Lazaro, B. Nae, O. Moldovan and B. Iniguez, "A compact quantum model of nanoscale double-gate metal-oxide-semiconductor field-effect transistor for high frequency and noise simulations", *Journal of Applied Physics*, **100** (8), 084320 (2006)

[Lazaro-2008] A. Lazaro and B. Iniguez, "RF and noise model of gate-all-around MOSFETs", *Semiconductor Science and Technology*, **23** (7), 075022 (2008)

[Lazaro-2009] A. Lazaro, A. Cerdeira, B. Nae, M. Estrada and B. Iniguez, "A High Frequency Compact Noise Model for Double-Gate MOSFET Devices", *Noise and Fluctuations*, **1129**, 577-580 (2009)

[Lazaro2-2006] A. Lazaro and B. Iniguez, "RF and noise performance of double gate and single gate SOI", *Solid-State Electronics*, **50** (5), 826-842 (2006)

[Lopez-Villanueva-1997] J. A. Lopez-Villanueva, P. Cartujo-Casinello, J. Banqueri, F. Gamiz and S. Rodriguez, "Effects of the inversion layer centroid on MOSFET behavior", *IEEE Transactions on Electron Devices*, **44** (11), 1915-1922 (1997)

[Mahajan-2009] V. M. Mahajan, R. P. Jindal, H. Shichijo, S. Martin, H. Fan-Chi and D. Trombley, "Numerical investigation of excess RF channel noise in sub-100 nm MOSFETs", *2nd International Workshop on Electron Devices and Semiconductor Technology (IEDST)*, 1-4 (2009)

[Moldovan-2007] O. Moldovan, B. Iniguez, D. Jimenez and J. Roig, "Analytical charge and capacitance models of undoped cylindrical surrounding-gate MOSFETs", *IEEE Transactions on Electron Devices*, **54** (1), 162-165 (2007)

[Nae-2009] B. Nae, A. Lazaro and B. Iniguez, "High frequency and noise model of gate-all-around metal-oxide-semiconductor field-effect transistors", *Journal of Applied Physics*, **105** (7), 074505 (2009)

[Nougier-1977] J. P. Nougier and M. Rolland, "Differential relaxation times and diffusivities of hot carriers in isotropic semiconductors", *Journal of Applied Physics*, **48** (4), 1683-1687 (1977)

[Pailloncy-2004] G. Pailloncy, B. Iniguez, G. Dambrine, J. P. Raskin and F. Danneville, "Noise modeling in fully depleted SOI MOSFETs", *Solid-State Electronics*, **48** (5), 813-825 (2004)

[Reggiani-2007] S. Reggiani, E. Gnani, A. Gnudi, M. Rudan and G. Baccarani, "Low-Field Electron Mobility Model for Ultrathin-Body SOI and Double-Gate MOSFETs With Extremely Small Silicon Thicknesses", *IEEE Transactions on Electron Devices*, **54** (9), 2204-2212 (2007)

[Roldan-2001] J. B. Roldan, F. Gamiz, J. A. Lopez-Villanueva, P. Cartujo and A. Godoy, "Strained-Si on Si_{1-x}Ge_x MOSFET inversion layer centroid modeling", *IEEE Transactions on Electron Devices*, **48** (10), 2447-2449 (2001)

[Roldan-2008] J. B. Roldan, A. Godoy, F. Gamiz and M. Balaguer, "Modeling the centroid and the inversion charge in cylindrical surrounding gate MOSFETs, including quantum effects", *IEEE Transactions on Electron Devices*, **55** (1), 411-416 (2008)

[Roy-2006] A. S. Roy, C. C. Enz and J. M. Sallese, "Noise modeling methodologies in the presence of mobility degradation and their equivalence", *IEEE Transactions on Electron Devices*, **53** (2), 348-355 (2006)

[Seeger-1973] K. Seeger, "Semiconductor Physics", Springer-Verlag: New York (1973)

[Suk-2005] S. D. Suk, S.-Y. Lee, S.-M. Kim, E.-J. Yoon, M.-S. Kim, M. Li, et al., "High performance 5nm radius Twin Silicon Nanowire MOSFET (TSNWFET) : fabrication on bulk si wafer, characteristics, and reliability", *IEEE International Electron Devices Meeting (IEDM)*, 717-720 (2005)

[Trivedi-2004] V. P. Trivedi, J. G. Fossum and F. Gamiz, "A compact QM-based mobility model for nanoscale ultra-thin-body CMOS devices", *IEEE International Electron Devices Meeting*, 763-766 (2004)

[Ziel-1986] A. van der Ziel, "Noise in Solid State Devices and Circuits", Wiley-Interscience (1986)

Chapter 5

Compact Modeling of Triple-Gate Transistors

5.1 Introduction

The Triple-Gate (or FinFET) transistors were born from the need to overcome technological limitations of current MOS technology, and improve the performances of CMOS devices. They are three dimensional FET devices which are compatible with existing CMOS fabrication, and do not require any special technology processes, like, for example, the bottom gate alignment on DG devices.

The purpose of this study is to examine the performance capabilities of Triple-gate devices in the RF regime using a simulation study of their small-signal

behavior in order to compare their performance with state of-the-art planar RF MOSFETs.

The inclusion of the quantum confinement effects in these models becomes mandatory due to the use of ultra-thin silicon oxides. Hence, a self consistent solution of the two-dimensional (2D) Schrödinger and Poisson equations is needed. The three dimensional structure of FinFETs makes it difficult to obtain an analytical classical and quantum charge control expression. In this chapter, an empirical charge control expression derived from a DG structure will be proposed. This expression depends on adjustable parameters that must be derived from numerical simulations or experimental measurements and will allow us the calculation of the channel current.

This model includes velocity overshoot through a one-dimensional energy-balance model [Baccarani-1999; Lazaro-2006], the effect of saturation region and the channel modulation length effect and the mobility degradation produced by quantum effects [Ge-2002].

The DC model is extended to the RF/microwave frequency range using the active transmission line approach [Pailloncy-2004; Lazaro2-2006]. Diffusion and shot noise sources are included in the active line in order to study the noise behaviour of these transistors. Needless to say the carrier temperature has a great influence in high frequency noise behaviour. In the drift-diffusion models the carrier temperature is calculated using empirical relationships with electric field, while in the model presented here, the carrier temperature along the channel is obtained from the energy-balance model. This study will present a comparison between the drift-diffusion and non-stationary models, applied to RF operation.

5.2 Charge Control Model

We consider a Triple-Gate device which, from the geometrical point of view, is similar to a FinFET device, in the sense that its height is much higher than its width. For that reason, from this point on, we will call the device used in the simulations a FinFET. A simple diagram showing the FinFET structure is given in Fig 5.1. The FinFET uses a single poly-Si layer deposited over a silicon fin patterned to form perfectly aligned gates straddling the fin structure. The other side of the channel ends at the buried oxide. The Si fin acts as the device channel and terminates on both sides at the source and drain. The fin is raised above the usual manufacturing plane. The polysilicon gate straddles the Si fin and thus the gate is on both sides of the channel. This leads to a very good electrostatic control of the channel charge by the gate compared to conventional MOSFETs.

The inversion charge associated to lateral and top gates can be calculated using 2D ATLAS device simulation of FinFET cross section from the electrical field integral along the gates (Fig. 5.2a). Figure 5.2b shows these charges as a function of the applied gate voltage for a FinFET with W_{fin}=10nm, H_{fin}=50nm, t_{ox}=1.5nm, t_{box}=50nm. This figure shows that the threshold voltage for the lateral and top gates has a small shift. The charge contribution associated to the top gate is small compared to the charge controlled by lateral gates. This effect is observed in devices with small aspect *W/H* ratios. This result suggests a charge control model similar to that employed for DG SOI devices.

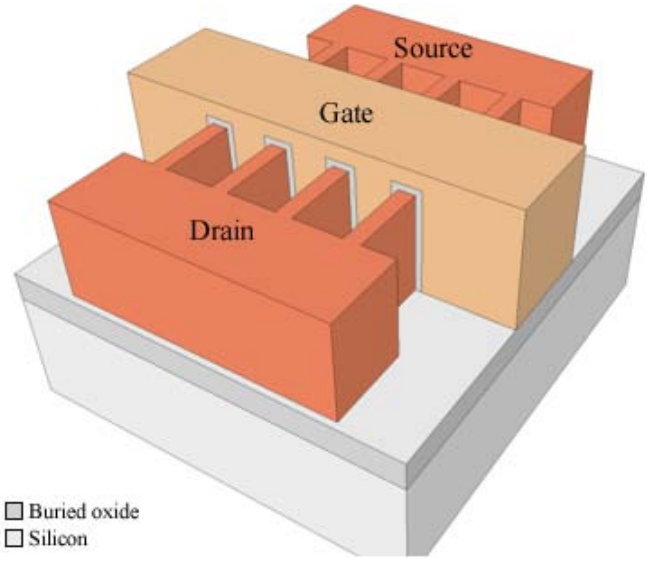
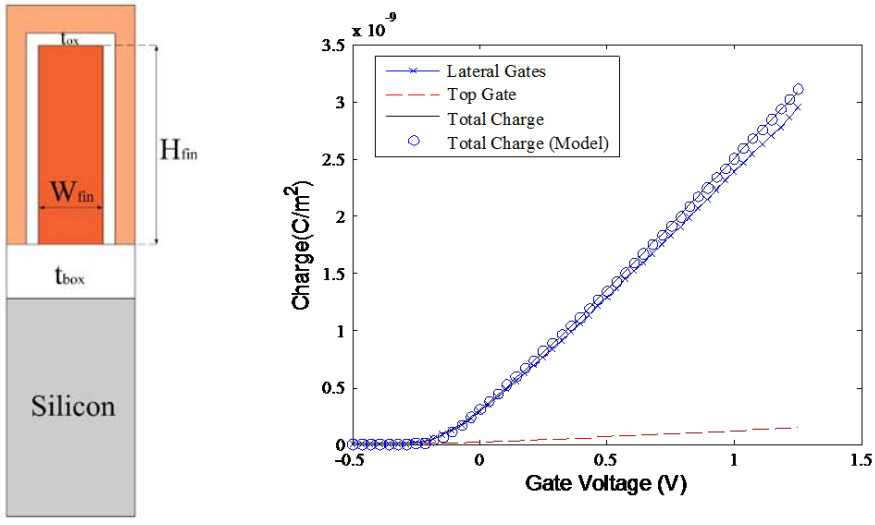


Fig. 5.1. The FinFET structure used in the simulations



(a) (b)

Fig. 5.2. A cross-section of the FinFET device used in the simulations (a); Charge associated to top and lateral gates and total charge calculated with SILVACO ATLAS and with the compact model W_{fin}=10 nm, H_{fin}=50 nm, t_{ox}=1.5 nm, t_{box}=50 nm. (b)

Three cases will be discussed in this study: a classical charge control model and quantum correction for both undoped and doped devices. For the undoped case, an exact solution for the surface potential can be obtained following the method proposed by Taur [Taur-2004]. The solution is expressed as a function of a parameter β that depends on the surface potential. This parameter is found solving a nonlinear equation resulting from the boundary conditions for the electric field at the surface. Following J.-M. Sallese et al. [Sallese-2005], the charge control model can be linearised, resulting in:

$$V_{GS} - V - V_{TH} = \frac{Q_G}{C_{ox}} + V_T \ln\frac{Q_G}{Q_0} + V_T \ln\frac{Q_G + Q_0}{Q_0} \tag{5.1}$$

where V_{GS} is the gate voltage, V is the channel potential, C_{ox} is the oxide capacitance, $V_T=kT/q$ is the thermal potential, $Q_0=2C_{ox}V_T$ (for the undoped DG MOSFET case) is a process dependent parameter, and V_{TH} is the threshold voltage. Note that the inversion charge density Q is $Q=2Q_G$.

For the doped case, numerical simulations have shown that the difference between the surface potential and central potential, $\phi_s - \phi_0$, keeps a constant value from the subthreshold region to well above threshold [Francis-1994]. Thus, the same charge control model given in eq. (5.1) can be obtained [Iniguez-2006; Iniguez2-2006; Moldovan-2007], but replacing Q_0 with the depletion charge $Q_{dep}=qN_At_{si}$.

By means of Lambert-function (defined as the solution to the equation $W(x)e^{W(x)}=x$), we can write:

$$Q_G = Q_n W\left(\exp\left(\frac{V_{GS} - V - V_{TH}}{nV_T}\right)\right) \tag{5.2}$$

where $Q_n=nC_{ox}V_T$, and $n=2$ for $Q_G>>Q_0$, i.e., well above threshold, when eq. (5.2) is an infinitely continuous solution of eq. (5.1). Then n can be interpreted as a fitting parameter with values between 1 and 2.

However, the Lambert-function does not have an explicit form. This function is implemented in several common mathematical codes (MATLAB, Maple, Mathematica) using a series expansion or iterative methods (see Annex III for details on the Lambert function). For compact modeling a good explicit approximation (a relative error less than 10^{-2}) of the Lambert-function, based on a Hermite-Padé rational approximation, is given by [Winitzki-2003]:

$$W(x) \approx \ln(1+x)\left(1-\frac{\ln(1+\ln(1+x))}{2+\ln(1+x)}\right) \tag{5.3}$$

Note that eq. (5.1) is the same expression used by A. Lazaro et al. [Lazaro-2006] considering quantum confinement, and assuming that the eigenvalues of the Schrödinger equation can be derived from the case of an infinite rectangular quantum well. A numerical self-consistent solution of Poisson-Schrödinger equations shows that the main difference between the classical and quantum charge control is a shift in the threshold voltage and a reduction in the gate capacitance [Baccarani-1999; Lazaro-2006].

Also, the same charge control given in (5.1) can be obtained for other types of multiple gate transistors such as Gate-All-Around (GAA) or Surrounding-Gate Transistor (SGT) [Iniguez-2006].

In the case of FinFETs, due to their 3D structure, the charge control given by eq. (5.2) may be used considering Q_n, V_{TH} and n as unknowns to be extracted from capacitance measurements or numerical simulations. To improve the agreement we propose a new explicit function:

$$Q = Q_{dep} + Q_n W \left(\exp\left(\frac{V_{GS} - V - V_{TH}}{n_{ef} V_T} \right) \right) \tag{5.4}$$

where Q_{dep} is the depletion charge, and n is replaced by the following smoothing function:

$$n_{ef} = \frac{n_{\min} + n_{\max}}{2} + \left(\frac{n_{\max} - n_{\min}}{2} \right) \tanh\left(\frac{V_{GS} - V - V_{TH} + \Delta V_{TH}}{n V_T} \right) \tag{5.5}$$

where n_{min} is the minimum slope (n_{min}=1) and n_{max} is the maximun slope (n_{max} is set to 3 in order to include the top gate charge contributions). In eq. (5.5) a small shift ΔV_{TH} is introduced in order to take into account the voltage shift for the top gate charge contributions, n is a smoothing parameter that controls the abruptness of the slope transition between n_{min} and n_{max} typically takes values close to 15. The new charge expression (5.4) has four adjustment parameters (V_{TH}, ΔV_{TH}, Q_n and n). In eq. (5.5), in the subthreshold regime, we get $n_{ef} \cong 1$, and obtain the subthreshold slope. As V_{GS} increases, n_{ef} approaches n_{max} which means that eq. (5.5) extends expression (5.2) into the subthreshold regime.

Figure 5.2b compares the charge per unit area extracted from Silvaco ATLAS simulations and the one obtained using eq. (5.2) for an undoped FinFET (in fact a very light doping of 10^{11} cm^{-3}). The good agreement obtained with both approximations proves that the charge control model presented here can also be used for FinFETs for typical RF bias points. However, the agreement using eq. (5.2) is not good in the subthreshold region. The reason is that in this region Q is comparable to Q_0 and the subthreshold slope n tends to 1. Figure 5.2b shows a good agreement between ATLAS simulations and the new charge expression (5.4) in all bias regions.

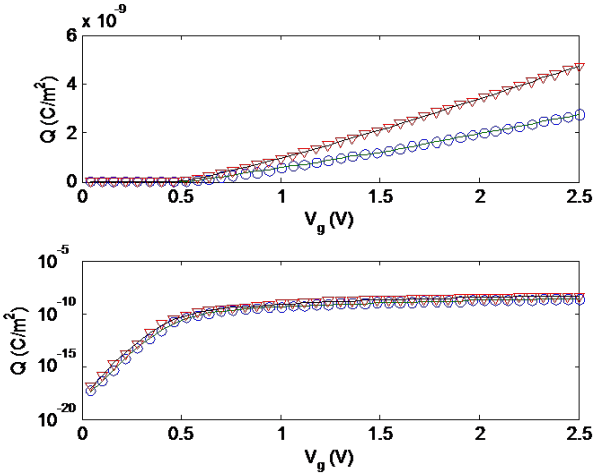


Fig. 5.3. Total charge sheet density numerically calculated (∇ classic and o quantum) and the charge control model (solid-line) for a FinFET with (W_{fin}=10 nm, H_{fin}=30 nm, t_{ox}=1.5 nm, t_{box}=50 nm).

As previously mentioned, new MOSFET architectures, such as ultrathin-body single- or multi-gate FETs, can in fact be scaled down more aggressively than the bulk-CMOS ones, and may become good candidates for future technology nodes. For such reduced dimensions quantum effects must be taken into account. Hence, the channel charge must be obtained from the self-consistent solution of the 2D Schrödinger–Poisson equations. A home-made simulation tool has been developed using partial differential equations toolbox in MATLAB [Ruiz-2007]. The same charge control equation (5.4) could be applied for the quantum case changing the adjustment parameters. In Fig. 5.3 the total charge sheet density is numerically computed for a FinFET (W_{fin}=10 nm, H_{fin}=30nm, t_{ox}=1.5 nm, t_{box}=50 nm). This figure compares the classical and quantum simulations with the compact charge control model proposed here.

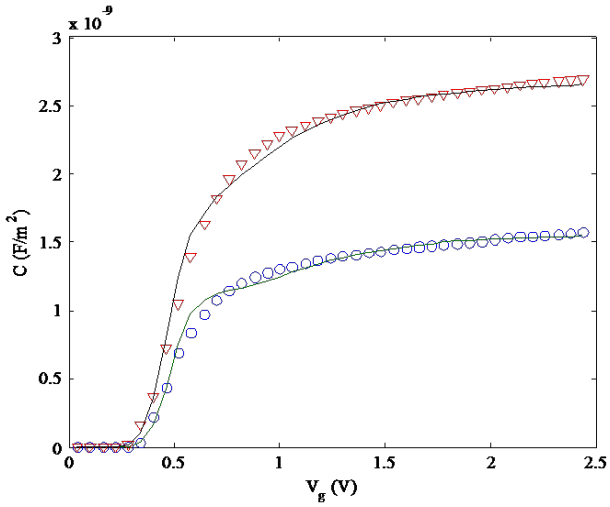


Fig. 5.4. Capacitance simulated (∇ classic and o quantum) and calculated with charge control model (solid-line) for a FinFET with (Wfin=10 nm, Hfin=50 nm, tox=1.5 nm, tbox=50 nm).

Figure 5.4 shows the capacitance for the same FinFET. A good agreement between numerical simulations and the compact charge control has been found in the classical and quantum cases in the whole range of applied bias. The two main effects observed in this figure are an increase in the threshold voltage and an important reduction of channel capacitance for the quantum simulations.

5.3 Drain Current Model

In extremely short channel DG MOSFETs and FinFETs the channel is quasi-ballistic, and as a consequence an important velocity overshoot is expected

[Baccarani-1999]. Using a simplified energy-balance model, the electron mobility is a function of the electron temperature related to the average energy of the carriers.

The transport model previously developed for DG-MOSFETs [Lazaro-2006] is extended to the FinFET case. Following G. Baccarani et al. [Baccarani-1999] and A. Lazaro et al. [Lazaro-2006] , the drain current in the linear channel region ($x<L_e$) can be obtained as:

$$I_{DS} = \frac{W \int_0^{V_{Dsat}} \mu_{n0} Q(V) dV}{\int_0^{L_e} \left(1 + \left(\frac{2k\mu_{n0}}{q\lambda_w v_{sat}} \right) (T_e(x) - T_0) \right) dx} \tag{5.6}$$

where the energy-relaxation length is defined as $\lambda_w \approx 2v_{sat}\tau_w$, τ_w being the energy relaxation time, and v_{sat} the saturation velocity. In case of FinFETs, for scaling purposes and for comparison with other MOSFET structures, W can be assumed equal to $W=n_{fingers}(W_{fin}+2H_{fin})$, W_{fin} and H_{fin} being the fin width and height, respectively, and $n_{fingers}$ the device number of fingers.

Therefore, the expression of I_{DS} can be written in terms of carrier charge densities. The above integrals (5.6) can be numerically computed using quadrature integral formulas. In order to obtain explicit expressions we linearize the charge around half saturation voltage: $V_m=V_{DSsat}/2$. Then the charge can be expressed as:

$$Q(V) \approx Q(V_m) + \left. \frac{dQ}{dV} \right|_{V_m} (V - V_m) = Q_m + \alpha \cdot \Delta V \tag{5.7}$$

Integrating the charge density between Q_s and Q_d ($Q=Q_s$ at the source end and $Q=Q_d$ at the saturation point or drain end), we obtain:

$$f(V_{GS},V_{DSsat}) = \int_0^{V_{DSsat}} \mu_{n0} Q(V) dV \approx \mu_{eff}\left(Q_m V_{DSsat} + \alpha \frac{V_{DSsat}^2}{8}\right) \tag{5.8}$$

The dependence of the mobility μ on the normal electric field is often referred to as mobility reduction, whereas the dependence on lateral electric field is often referred to as velocity saturation. We use the semiempirical model presented by V.P. Trivedi et al. [Trivedi-2004] but considering an effective DG-MOSFET thickness $t_{si}=W_{fin}$. The effective mobility is approximated by the mobility at the midpoint, $\mu_{eff}=\mu(V_m)$.

In order to evaluate the integral in the denominator of eq. (5.6), we need to know the temperature profile along the channel. The electron temperature T_e is governed by the following equation [Baccarani-1999]:

$$\frac{dT_e}{dx} + \frac{T_e - T_0}{\lambda_w} = -\frac{q}{2k} E_x(x) \tag{5.9}$$

Equation (5.8) can be integrated assuming a constant λ_w, under boundary condition $T_e(x=0)=T_0$, and the x-component of the electric field expressed as a function of the channel potential, $E_x(x)=-dV(x)/dx$:

$$T_e(x) = T_0 + \frac{q}{2k}V(x) - \frac{q}{2k\lambda_w}\int_0^x V(\xi) e^{\frac{\xi - y}{\lambda_w}} d\xi \tag{5.10}$$

As an approximation, in the channel linear region we can assume that the lateral field is linear from a small value at the source end to the saturation field at $x=L_e$ ($E_x=E_{sat}\cdot x/L_e$). Using eqs. (5.8) and (5.10), we obtain:

$$I_{DS} = \frac{Wf(V_{GS},V_{DSS})}{L_e + \frac{q\alpha}{2k}\int_0^{L_e} V(\xi) e^{\frac{\xi - L_e}{\lambda_w}} d\xi} = \frac{W}{L_e}\frac{f(V_{GS},V_{DSS})}{1+\gamma_n V_{DSS}} \tag{5.11}$$

where

$$\gamma_n = \frac{\mu_{eff}}{v_{sat} L_e} \frac{1}{\left(1 + 2\lambda_w / L_e\right)} \tag{5.12}$$

and V_{DSS} is equal to V_{DS} for non saturated channels *(L_e=L)* and V_{DSS}=V_{DSsat} for saturated channels. A smoothing function is used to interpolate V_{DSS}:

$$V_{DSS} = V_{DS} - \frac{kT}{q} \frac{\ln\left\{1 + \exp\left[A(V_{DS} - V_{DSsat}) / (kT/q)\right]\right\}}{A} \tag{5.13}$$

where A is the parameter that controls the transition between saturated and non saturated channel (in this model A=1 is chosen for smooth transition).

The value of V_{DSsat} can be found by equalling the drain current given by eq. (5.11) with the current in the channel saturation point:

$$I_{DS} = WQ(V_{DSsat}) v_{sat,ns} \tag{5.14}$$

where the overshoot channel velocity $v_{sat,ns}$ is calculated from the expression:

$$v_{sat,ns} = \frac{\mu_{n0}}{1 + \alpha(T(L) - T_0)} E_x(x = L) \tag{5.15}$$

with

$$\alpha = \frac{2k\mu_{n0}}{q l_w v_{sat}} \tag{5.16}$$

Note that the conventional drift-diffusion model is recovered if λ_w is set to 0, then the non-stationary saturation velocity $v_{sat,ns}$ is equal to the stationary value v_{sat}.

Channel length modulation should also be included. For V_{DS}<$V_{DSsat,}$ the device works in the linear region, with L_e=L and V_{DSsat}=V_{DS}. For V_{DS}>V_{DSsat}, the device operates in the saturation regime, and the channel is partially saturated, and the saturated channel length is given by:

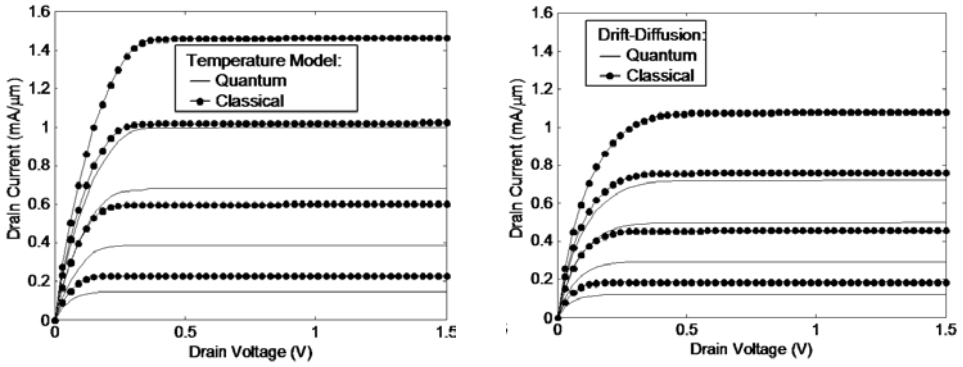
$$\Delta L = L - L_e = L_c \operatorname{arcsin} h\left(\frac{V_{DS} - V_{DSsat}}{E_{sat} L_c}\right) \tag{5.17}$$

where $L_c = a \cdot \lambda_c$ is proportional to the characteristic length λ_c (using the same expression for DG transistors given by J.P. Colinge [Colinge-2004]), and a is a fitting parameter ($0 < a \leq 1$).

5.4 Results and Discussion

In this section some simulated results will be obtained using the previously presented model. First, the DC drain characteristics are obtained. Figure 5.5 shows the drain current characteristics for a 50 nm gate length FinFET (W_{fin}=10 nm, H_{fin}=50 nm, t_{ox}=1.5 nm) calculated with the above described model. In Fig. 5.5a the temperature model is used, whereas in Fig. 5.5b the drift-diffusion transport model is used. The effect of velocity overshoot translates into an increase (about 25% higher for this gate length) in the drain current and transconductance. Due to the reduction in the channel capacitance (see Fig. 5.4) an important reduction in the drain level is observed in the quantum case for the same gate voltage overdrive.

In order to take into account the most important effects, such as non quasi stationary effects, the gate and drain correlation between noise sources, and the tunnelling gate current noise, we use the segmentation method [Lazaro-2006; Lazaro2-2006]. This method is based on splitting the channel in several channel slides. For each channel slide a local small-signal equivalent circuit (see Fig. 5.6a) is derived from the charge control and drain current. This circuit is composed by the gate to channel capacitance, C_{gc}, the channel conductance g_c and the transconductance g_m.



(a) (b)

Fig. 5.5. A comparison of drain current for FinFET (W_{fin}=10 nm, H_{fin}=30 nm, t_{ox}=1.5 nm, t_{box}=50 nm)), L=100 nm, for classical charge control (•) and quantum charge (–) using a) Temperature model b) Drift-Diffusion model. The gate voltages are V_{GS}-V_{TH}=0.5, 0.75, 1 and 1.25 V.

These components are calculated using the following expressions:

$$C_{gc}(x) = W\Delta x \frac{\partial Q}{\partial V_{gc}} \tag{5.18}$$

$$g_m(x) = Wv(x)\frac{\partial Q}{\partial \mathrm{V_{gc}}} \tag{5.19}$$

$$g_c(x) = \left.\frac{\partial I_{DS}}{\partial V}\right|_{V_{g=cte}} \approx \frac{I_{DS}}{E_x(x)\Delta x} \tag{5.20}$$

where $V_{gc}(y) = V_{GS} - V(y)$.

The derivative *dQ/dVgc* in eqs. (5.18-5.19) can be obtained analytically from eq. (5.4), and the electric field is supposed to change linearly with the channel distance in the linear region, and it is given by eq. (5.21) in the saturation region:

$$E_x(x) = E_{sat}\cosh\left(\frac{x - L_e}{L_c}\right) \tag{5.21}$$

where E_{sat} is the electric field at the saturation channel point and is obtained from V_{DSsat}, under the linear field approximation in the linear region.

The local noise sources are taken into account in order to simulate the noise parameters. Thus, we include a channel noise source due to diffusion noise (i_n) and a shot noise source associated with the tunneling gate current (i_{ng}). Also the tunneling gate conductance may be taken into account. Using the nodal analysis the *Y* parameters and admittance correlation matrix of the intrinsic circuit are calculated [Lazaro-2006; Lazaro2-2006]. By using common matrix correlation relations, the extrinsic small-signal and noise parameters are calculated (Fig. 5.6b). From intrinsic Y parameters the typical FET admittance small-signal model can be obtained by means of real and imaginary part identification. Finally, the parasitic resistances (R_s, R_d, R_g) and inductances (L_s, L_d, L_g) are added.

The cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) are the most important RF figure merit parameters [Raskin-2006; Pailloncy-2004]. These parameters can be calculated from the small signal equivalent circuit extracted from the *Y* parameters computed using the active transmission line analysis identifying each branch of the *Pi* equivalent circuit.

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1 + 2C_{gd}/C_{gs}}} \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{5.22}$$

$$f_{\max} \approx \frac{g_m}{2\pi C_{gs}\sqrt{4(R_s + R_i + R_g)\left(g_{ds} + g_m\dfrac{C_{gd}}{C_{gs}}\right)}} \tag{5.23}$$

where C_{gs} and C_{gd}, are the gate to source and gate to drain small signal capacitance respectively, including fringing and overlap capacitances, g_m is the gate

transconductance, R_i (in series with C_{gs}) takes into account the distributed nature of the MOSFET and g_{ds} is the drain-to-source conductance.

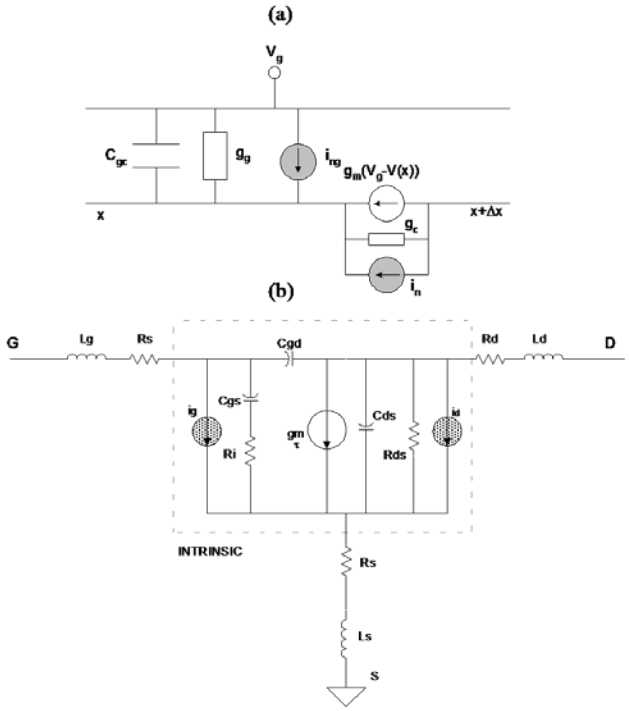


Fig. 5.6. (a) Local equivalent circuit for a channel slide, and (b) FinFET small signal equivalent circuit

As shown in eqs. (5.22-5.23), f_T depends on the ratio between g_m and the total gate capacitance while f_{max} also depends on the source/drain and gate parasitic resistances, and the ratio C_{gd}/C_{gs}. In this model the fringing and overlap capacitance are estimated using the analytical model proposed by W. Wu et al. [Wu-2006], whereas the gate resistance and source and drain resistances are calculated using

the formulas given by W. Wu et al.[Wu-2007] and A. Dixit et al. [Dixit-2005], respectively.

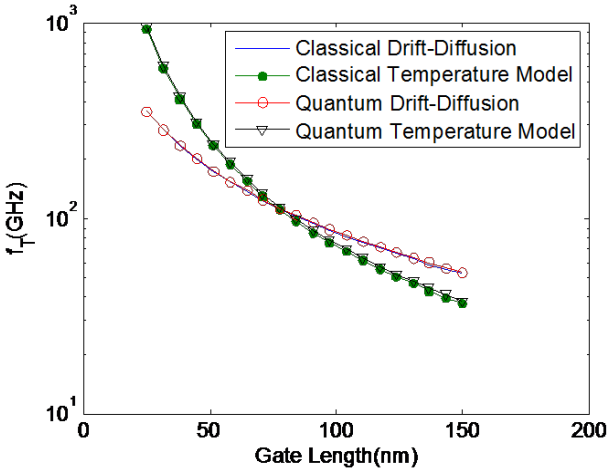


Fig. 5.7. Simulated cut-off frequency f_t versus gate length for FinFET (W_{fin}=10 nm, H_{fin}=30 nm, t_{ox}=1.5 nm, t_{box}=50 nm, V_{DS}=1 V, V_{GS}-V_{TH}=0.5V). A Comparison between the classical and quantum charge controls for the Drift-Diffusion and temperature or temperature models are shown.

Figures 5.7 and 5.8 compare the f_T and f_{max} calculated with drift-diffusion and hydrodynamic (or electron temperature) model for a FinFET (W_{fin}=10 nm, H_{fin}=50 nm, 100 fingers, V_{GS}–V_{TH}=0.5V, V_{DS}=1V). Due to the overshoot effect the values of f_T and f_{max} are considerably higher in the temperature transport model. Small differences have been shown in f_T between classical and quantum charge control models. This is due to the fact that f_T depends on the ratio g_m/C_{gs}, where the numerator and denominator are affected in the same magnitude for the channel

capacitance. Then, except for the threshold voltage shift, the channel capacitance reduction due to quantum effect is not appreciable in f_T. However, the differences in f_{max} between classical and quantum case are more important due to the differences in intrinsic resistance and channel conductances. For shorter gate length the overshoot velocity effect, taken into account in the temperature transport model, increases the transconductance and, as a consequence, the value of f_{max}.

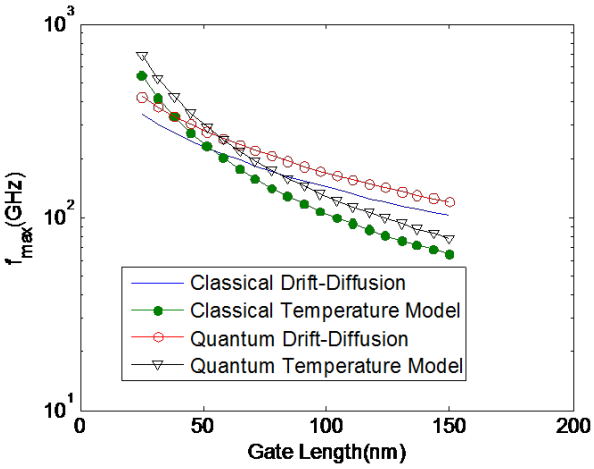


Fig. 5.8. Simulated f_{max} versus gate length for FinFET (W_{fin}=10 nm, H_{fin}=30 nm, t_{ox}=1.5 nm, t_{box}=50 nm, V_{DS}ds=1 V, $V_{GS}gs$-V_{TH}=0.5V). A Comparison between the classical and quantum charge controls for the Drift-Diffusion and temperature or temperature models are shown.

Changing to a current-current representation, we define a set of dimensionless noise coefficients which are convenient for noise figure calculations, the so-called Pucel´s parameters *P*, *R* and the correlation coefficient *C*:

$$P = \frac{\left|\overline{i_d^2}\right|}{4kT_0\Delta f g_m} \tag{5.24}$$

$$R = \frac{\left|\overline{i_g^2}\right|}{4kT_0\Delta f C_{gs}^2 / g_m} \tag{5.25}$$

$$C = \mathrm{Im}\left(\frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\cdot\overline{i_d^2}}}\right) \tag{5.26}$$

where T_0=290 K and Δf is the frequency bandwidth. An accurate knowledge of P is important because it characterizes channel noise. The correlation is essentially imaginary because of the capacitive coupling between the channel and the gate.

For a typical low noise bias point, the shot noise due to the gate tunneling effect can be neglected compared to diffusion noise [Pailloncy-2004]. Then, the minimum noise temperature including parasitics can be written as a function of correlation matrix elements [Danneville-2005]:

$$T_{\min} = 2T_0\frac{f}{f_T}\sqrt{PR(1-C^2)+(P+R-2C\sqrt{PR})(R_g+R_s)g_m} \tag{5.27}$$

Figure 5.9 shows the admittance noise parameters R, P, C previously defined in eqs. (5.24-5.26) as a function of gate length for a FinFET (W_{fin}=10 nm, H_{fin}=30 nm, t_{ox}=1.5 nm, t_{box}=50 nm, 100 fingers, V_{DS}=1V, V_{GS}–V_{TH}=0.5V). The value of parameter R is found to be almost constant, equal to 0.2 for classical transport and around 0.15 for temperature transport, which makes the induced gate noise current source only dependent on C_{gs} and g_m. The parameter P is the most affected by both short-channel and hot-carrier effect increasing with downscaling. The values of P are larger in the temperature model, because the intrinsic noise source in the local equivalent circuit is higher than the drift-diffusion case due to the hot carrier effect. The correlation coefficient C decreases with downscaling in

the drift-diffusion model whereas in the temperature model remains almost constant with a small increase. From eq. (5.27) the higher value of *C* compensates the effect of larger *P* resulting in a lower noise figure for shorter gate lengths in the temperature model. The range of values of *R*, *P* and *C* parameters obtained here are quite comparable with the experimental ones obtained for 110 nm gate length SG MOSFET devices [Pailloncy-2004].

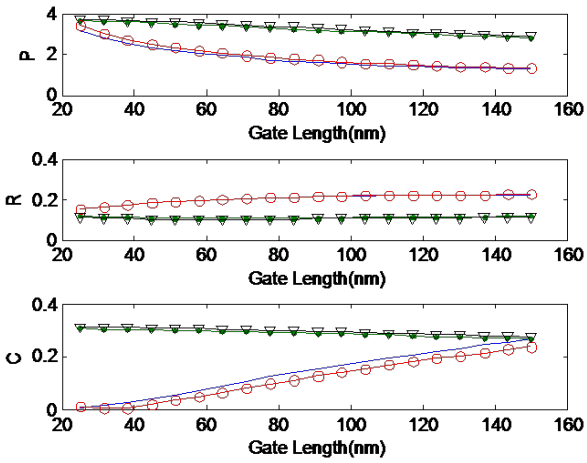


Fig. 5.9. Intrinsic noise model R, P, C for FinFET (W_{fin}=10 nm, H_{fin}=30 nm, t_{ox}=1.5 nm, t_{box}=50 nm, 100 fingers, V_{GS}-V_{TH}=0.5V, V_{DS}=1V) . ˜() Classical Drift-Diffusion, (•) classical Temperature model, (o), Quantum Drift-Diffusion, (∇) Quantum temperature model.

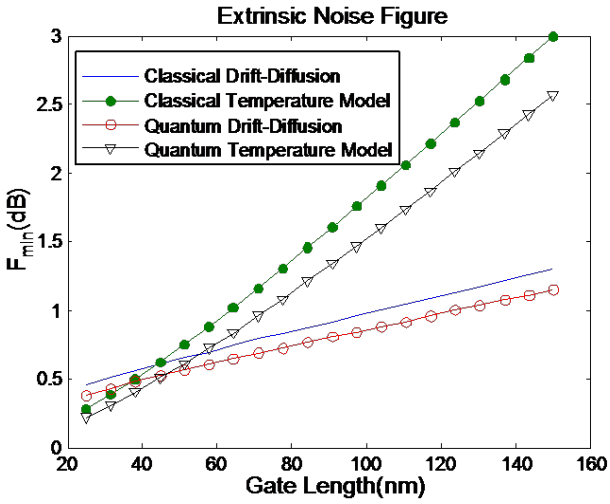


Fig. 5.10. Extrinsic Noise Parameters as function of gate length for FinFET (W_{fin}=10 nm, H_{fin}=30 nm, t_{ox}=1.5 nm, t_{box}=50 nm, 100 fingers, V_{GS}-V_{TH}=0.5V, V_{DS}=1V) at 10 GHz.

Figure 5.10 shows the extrinsic noise figure for FinFET (W_{fin}=10 nm, H_{fin}=30 nm, t_{ox}=1.5 nm, t_{box}=50 nm, 100 fingers, V_{DS}=1 V, V_{GS}-V_{TH}=0.5V) at 10 GHz calculated using the drift-diffusion and temperature models. From this figure some conclusions can be drawn. First, a lower noise figure is always achieved when quantum effects are taken into account. Second, for gate lengths smaller than 45 nm, lower noise figure values are obtained using the temperature model. This fact is a consequence of higher f_T and f_{max} since around these gate lengths velocity overshoot compensates the higher intrinsic noise due to larger P values obtained using the temperature model.

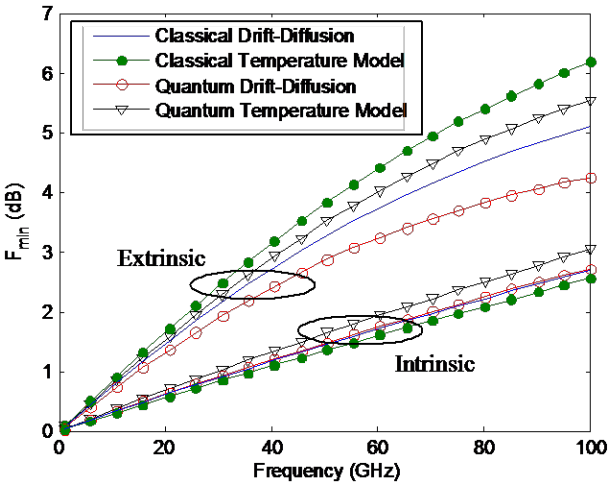


Fig. 5.11. Frequency behaviour of the Extrinsic Noise Parameters including gate current effect for FinFET (W_{fin}=10 nm, H_{fin}=30 nm, t_{ox}=1.5 nm, t_{box}=50 nm, L=50 nm, 100 fingers, V_{GS}-V_{TH}=0.5V, V_{DS}=1V).

The frequency dependence of the noise performance is also studied, as shown in Fig. 5.11. For a 50 nm gate length the intrinsic minimum noise figure is better for the temperature model than for the drift-diffusion model. Following eq. (5.27), the frequency slope of the minimum noise temperature depends on the parasitic resistance and the f_T, resulting in an important contribution of parasitics in the high frequency extrinsic noise. The difference between drift-diffusion and temperature transport model increases when the extrinsic (with parasitics) noise figure is considered, due to the difference in f_T between the two models.

5.5 Conclusions

In this chapter, a compact RF model for FinFETs, is proposed, based on a charge control model obtained from 2D device simulations where quantum effects corresponding to the intrinsic transistor parameters are taken into account. The charge control model can be applied to both the classical or quantum cases.

The channel current model is based on an electronic energy transport model which includes the velocity overshoot and hot carrier effects in the noise temperature. RF and noise are analysed using the active transmission line method. Furthermore, as an application of the model we have described the RF and noise performance of FinFET devices with the downscaling of the gate length.

Comparisons between the two transport models and the influence of quantum effects have been studied. The obtained results show important differences in drain current, f_T, f_{max}, and noise performances between drift-diffusion and hydrodynamic models for short gate lengths. These differences are due to the velocity overshoot that increases the transconductance, and hence, f_T and f_{max} values. Also, significative difference have been observed in f_{max} and F_{min} between classical and quantum models.

The intrinsic noise figure depends on the temperature model used in the simulation. The electronic temperature transport model predicts a higher noise temperature in the saturation bias region than the classical relation between carrier temperature and electric field, resulting in a higher noise figure. However, for gate lengths shorter than 50-60 nm the increase of f_T due to velocity overshoot compensates for the channel temperature increment, finally resulting in a lower noise figure. In these devices, for typical RF operating bias points, the effect of the

shot noise introduced by the gate current is small. The simulated results show the limiting effect of parasitics in FinFETs RF and noise performances.

5.6. References

[Baccarani-1999] G. Baccarani and S. Reggiani, "A compact Double-Gate MOSFET model comprising quantum-mechanical and nonstatic effects", *IEEE Transactions on Electron Devices*, **46** (8), 1656-1666 (1999)

[Colinge-2004] J.-P. Colinge, "Multiple-gate SOI MOSFETs", *Solid-State Electronics*, **48** (6), 897-905 (2004)

[Danneville-2005] F. Danneville, G. Paillocny, A. Siligaris, B. Iniguez and G. Dambrine, "High frequency noise of SOI MOSFETs: Performances and limitations", *SPIE - Noise in Devices and Circuits III*, Austin, TX, 185-199 (2005)

[Dixit-2005] A. Dixit, A. Kottantharayil, N. Collaert, M. Goodwin, M. Jurczak and K. De Meyer, "Analysis of the parasitic S/D resistance in multiple-gate FETs", *IEEE Transactions on Electron Devices*, **52** (6), 1132-1140 (2005)

[Francis-1994] P. Francis, A. Terao, D. Flandre and F. Vandewiele, "Modeling of Ultrathin Double-Gate NMOS/SOI Transistors", *IEEE Transactions on Electron Devices*, **41** (5), 715-720 (1994)

[Ge-2002] L. X. Ge and J. G. Fossum, "Analytical modeling of quantization and volume inversion in thin Si-film DG MOSFETs", *IEEE Transactions on Electron Devices*, **49** (2), 287-294 (2002)

[Iniguez-2006] B. Iniguez, T. A. Fjeldly, A. Lazaro, F. Danneville and M. J. Deen, "Compact-Modeling Solutions For Nanoscale Double-Gate and Gate-All-Around MOSFETs", *IEEE Transactions on Electron Devices*, **53** (9), 2128-2142 (2006)

[Iniguez2-2006] B. Iniguez, A. Lazaro and O. Moldovan, "Compact RF Modeling of multiple-gate MOSFETs", *2006 European Microwave Integrated Circuits Conference*, Manchester, UK, 213-216 (2006)

[Lazaro-2006] A. Lazaro, B. Nae, O. Moldovan and B. Iniguez, "A compact quantum model of nanoscale double-gate metal-oxide-semiconductor field-effect transistor for high frequency and noise simulations", *Journal of Applied Physics*, **100** (8), (2006)

[Lazaro2-2006] A. Lazaro and B. Iniguez, "RF and noise performance of double gate and single gate SOI", *Solid-State Electronics*, **50** (5), 826-842 (2006)

[Moldovan-2007] O. Moldovan, A. Cerdeira, D. Jimenez, J. P. Raskin, V. Kilchytska, D. Flandre, et al., "Compact model for highly-doped double-gate SOI MOSFETs targeting baseband analog applications", *Solid-State Electronics*, **51** (5), 655-661 (2007)

[Pailloncy-2004] G. Pailloncy, B. Iniguez, G. Dambrine, J. P. Raskin and F. Danneville, "Noise modeling in fully depleted SOI MOSFETs", *Solid-State Electronics*, **48** (5), 813-825 (2004)

[Raskin-2006] J. P. Raskin, C. Tsung Ming, V. Kilchytska, D. Lederer and D. Flandre, "Analog/RF performance of multiple gate SOI devices: wideband simulations and characterization", *IEEE Transactions on Electron Devices*, **53** (5), 1088-1095 (2006)

[Ruiz-2007] F. J. Garcia Ruiz, A. Godoy, F. Gamiz, C. Sampedro and L. Donetti, "A Comprehensive Study of the Corner Effects in Pi-Gate MOSFETs Including Quantum Effects", *IEEE Transactions on Electron Devices*, **54** (12), 3369-3377 (2007)

[Sallese-2005] J. M. Sallese, F. Krummenacher, F. Pregaldiny, C. Lallement, A. Roy and C. Enz, "A design oriented charge-based current model for symmetric DG MOSFET and its correlation with the EKV formalism", *Solid-State Electronics*, **49** (3), 485-489 (2005)

[Taur-2004] Y. Taur, X. Liang, W. Wang and H. Lu, "A continuous, analytic drain-current model for DG MOSFETs", *IEEE Electron Device Letters*, **25** (2), 107-109 (2004)

[Trivedi-2004] V. P. Trivedi, J. G. Fossum and F. Gamiz, "A compact QM-based mobility model for nanoscale ultra-thin-body CMOS devices", *IEEE International Electron Devices Meeting, Technical Digest*, 763-766 (2004)

[Winitzki-2003] S. Winitzki, "Uniform approximations for transcendental functions", Springer-Verlag Berlin: Berlin (2003)

[Wu-2006] W. Wu and M. Chan, "Gate resistance modeling of multifin MOS devices", *IEEE Electron Device Letters*, **27** (1), 68-70 (2006)

[Wu-2007] W. Wu and M. Chan, "Analysis of Geometry-Dependent Parasitics in Multifin Double-Gate FinFETs", *IEEE Transactions on Electron Devices*, **54** (4), 692-698 (2007)

Chapter 6

Conclusions

The nanoelectronics world is moving forward at incredible speed, and technology keeps improving overnight. One can no longer afford to spend months or even years evaluating a future technological node, thus the need for a robust evaluation system has arisen. Numerical ways of modeling the new device architectures, apart from precision, offer very little in terms of performance, and are being replaced by new analytical tools, focused on providing exactly that – speed and accuracy. However, many analytical tools these days are in fact a combination of numerical approaches and analytical expressions, and often rely on adjusting parameters that do not give any insight on the internal functioning of the device. What is really needed is a complete analytical modeling tool, based on a physical characterization

of a device, taking into account all the new phenomena that come into play when lowering the dimensions of the devices towards tens of nanometers.

This research work has been conceived to cover precisely these aspects. The models described here are physical models, with very few adjusting parameters, that are usually replaceable with values extracted from experimental measurements; they are compact models, making use of approximate expressions that have been tweaked to offer a very good fit with numerical simulations and offering in exchange the advantage of computation speed, decreasing the simulation time and thus the productivity. Another major advantage is the fact that these models can be easily incorporated into circuit simulators, which allows designers to unleash the full capabilities of the design software to create new devices and applications.

As for the actual devices, the scaling of the planar MOSFET has been the main technology option for the past decade. However, we are at a point where materials and device issues arise, opening the door for alternative device structures. SOI devices are excellent candidates to replace conventional bulk CMOS. The most promising SOI devices for the nanoscale range are based on multiple gate structures like the DG, triple gate or FinFET and SGT or Gate-All-Around (GAA). These advanced structures can be scaled more aggressively than the bulk-Si structures, hence, may be adapted for integrated circuit production. Also, these structures are regarded as a near ideal technology, offering a higher drive current than its SG SOI counterpart due to larger control over channel region, and this strongly enhances the immunity towards the short channel effects. With the evolution of MOSFET scaling to shorter gate lengths, the high-frequency

capabilities of the transistor have reached the GHz regime so that RF circuit applications have been steadily growing.

In this thesis, the performances of different Multiple-Gate MOSFET (DG, SGT and triple-gate) structures has been evaluated, for the RF mode of operation, and the noise performances of these devices has been studied. The modeling scheme is similar for all these devices and is adapted to each geometry.

The basis for all these models is the fully analytical compact model of the DG transistor described in chapter 2. This model is an extended version of a previously developed compact dc and charge model for doped DG-MOSFET from a unified charge control model derived from Poisson´s equation. A quantum case has been added, using a simple relationship between the inversion centroid and the inversion charge obtained fitting numerical simulation results. Using this compact charge control model, DC drain current models are derived assuming drift-diffusion and hydrodynamic transport mechanisms.

We have proved that the electron heating has an important effect on the performances of the device, especially with scaling, thus the use of a transport model that takes into account this effect (the hydrodynamic transport model) is fully justified.

Several short channel effects have been incorporated into the model, such as the effect of hot carriers, channel length modulation, saturation effect, as well as the shot noise introduced by the tunneling gate current due to the very gate thin oxide (2nm).

The RF and noise performances of DG-MOSFETs have been analyzed using the active transmission line approach from the compact charge control and drain current model. The results we have obtained show important differences in drain current, f_t and f_{max} and noise performances between drift-diffusion and hydrodynamic transport models for short gate lengths. These differences comes from the effect of the velocity overshoot increasing the transconductance, and hence, f_t and f_{max}. The intrinsic noise figure depends on the temperature model used in the simulation. For short-channel devices operated in the saturation region, noise exhibits a strong dependence on the drain bias because the velocity saturation region, where the noise temperature is high, occupies a large portion of the channel. Hydrodynamic models predict higher noise temperatures in this region. In these devices, for typical RF operating bias points, the effect of the shot noise introduced by the gate current is small…however, with further downscaling, this effect will have a bigger importance in the final noise figure.

The same approach has been applied to the SGT structure. In the SGT case, the charge control model comes from 2D device simulations where quantum effects corresponding to the intrinsic transistor parameters are taken into account. The channel current model includes the velocity overshoot and hot carrier effects in the noise temperature. RF and noise are analyzed using the active transmission line method. Furthermore, as an application of the model we have described the RF and noise performance of SGT devices with the gate length being downscaled.

For these two devices (DG and SGT), we have also developed a compact noise model (instead of the channel segmentation method). It includes the channel noise, the induced-gate noise and the cross-correlation noise between drain and gate noises. The expressions are analytical and they depend on the mobile charge at

the source and drain ends of the channel. noise between drain and gate noises. The expressions are analytical and they depend on the mobile charge at the source and drain ends of the channel.

The values of the excess noise factors and correlation coefficients follow the values previously obtained in the DG MOSFET model. Moreover, the compact noise model described does not use adjusting parameters, thus making it ideal for being used in circuit simulators with SGT MOSFETs.

This compact noise model reproduces the measured noise bias behavior for any gate length found for SG MOSFETs in the literature, without the need for additional parameters. Therefore, it is a very promising model for being used in circuit simulators with SG, DG or SGT devices.

As for triple-gate (or FinFET) devices, we have proposed a compact RF model, based on the charge control model obtained for the SGT case, but modified for this specific architecture. The channel current model includes the velocity overshoot and the hot carrier effects in the noise model. The analysis of the RF and noise behavior has been done using the active transmission line method, and the noise performances have been studied with the downscaling of the gate length, to predict the device behavior at future technological nodes.

Annex I

Numerical noise modeling

Using the nodal admittance method, the active transmission line can be analyzed (see Fig. A.1.1).

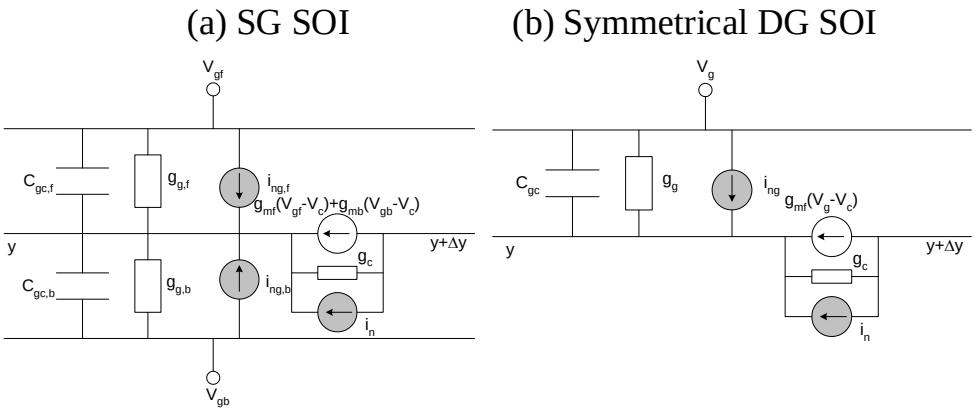


Fig. A1.1. Small-signal and noise model for a channel slide (a) SG SOI MOSFET (b) Symmetrical DG SOI MOSFET

The circuit nodes are numbered from *1* to *N+1* (1 for source end, and *N+1* for drain end), and the front gate and back gate nodes are numbered as *N+2* and *N+3*, respectively. The current at circuit nodes can be written as:

$$[I_i] = [Y_{ij}] \cdot [V_i] + [i_{n,i}] \tag{A1.1}$$

where I_i is the signal input current at each circuit node, V_i is the node voltage, $I_{n,i}$ is the noise current at each node, and Y_{ij} is the admittance matrix. The current at the internal nodes is equal to zero (I_i,*=0, for i=2…N*). And the external nodes are connected to voltage bias.

The admittance matrix and the correlation matrix elements are given by the following expressions:

$$Y_{ii} = \sum_{k=1}^{N} (j\omega C_{gf,k} + j\omega C_{gb,k} - g_{mf,k} - g_{mb,k}) \tag{A1.2}$$

$$Y_{N+2,N+2} = \sum_{k=1}^{N} j\omega C_{gf,k} \tag{A1.3}$$

$$Y_{N+3,N+3} = \sum_{k=1}^{N} j\omega C_{gb,k} \tag{A1.4}$$

$$Y_{i,N+3} = -\sum_{k=1}^{N} (j\omega C_{gb,k} + g_{mb,k}) \tag{A1.5}$$

$$Y_{N+3,i} = -\sum_{k=1}^{N} j\omega C_{gb,k} \tag{A1.6}$$

$$Y_{i,N+2} = -\sum_{k=1}^{N} (j\omega C_{gf,k} + g_{mf,k}) \tag{A1.7}$$

$$Y_{N+2,i} = -\sum_{k=1}^{N} j\omega C_{gf,k} \tag{A1.8}$$

$$Y_{i,i+1} = -\sum_{k=1}^{N} g_{c,k} \tag{A1.9}$$

$$Y_{i+1,i+1} = \sum_{k=1}^{N} g_{c,k} \tag{A1.10}$$

$$Y_{i+1,i} = -\sum_{k=1}^{N} (g_{c,k} + g_{mf,k} + g_{mb,k}) \tag{A1.11}$$

$$Y_{i+1,N+2} = \sum_{k=1}^{N} g_{mf,k} \tag{A1.12}$$

$$Y_{i+1,N+3} = \sum_{k=1}^{N} g_{mb,k} \tag{A1.13}$$

$$C_{i,i} = \sum_{k=1}^{N} (S_{in,k} + S_{igf,k} + S_{igb,k}) \tag{A1.14}$$

$$C_{i+1,i+1} = \sum_{k=1}^{N} S_{in,k} \tag{A1.15}$$

$$C_{i+1,i} = C_{i,i+1} = -\sum_{k=1}^{N} S_{in,k} \tag{A1.16}$$

$$C_{N+2,N+2} = \sum_{k=1}^{N} S_{igf,k} \tag{A1.17}$$

$$C_{N+2,i} = C_{i,N+2} = -\sum_{k=1}^{N} S_{igf,k} \tag{A1.18}$$

$$C_{N+3,N+3} = \sum_{k=1}^{N} S_{igb,k} \tag{A1.19}$$

$$C_{N+3,i} = C_{i,N+3} = -\sum_{k=1}^{N} S_{igb,k} \tag{A1.20}$$

To obtain the external admittance and correlation matrix, first, the nodes are renumbered as internal nodes (*I=2…N*), and external nodes (nodes *1*, *N+1*, *N+2*, *N+3*). Then, the equation system (A1.1) can be written as:

$$\begin{bmatrix} \underline{0} \\ \underline{I_e} \end{bmatrix} = \begin{bmatrix} Y_{ii} & Y_{ie} \\ Y_{ei} & Y_{ee} \end{bmatrix} \cdot \begin{bmatrix} \underline{V_i} \\ \underline{V_e} \end{bmatrix} + \begin{bmatrix} \underline{i_{ni}} \\ \underline{i_{ne}} \end{bmatrix} \tag{A1.21}$$

$$C = \begin{bmatrix} C_{ii} & C_{ie} \\ C_{ei} & C_{ee} \end{bmatrix} \tag{A1.22}$$

Then the internal voltages can be obtained as:

$$\underline{V_i} = -Y_{ii}^{-1} Y_{ie} \underline{V_e} - Y_{ii}^{-1} \underline{i_{ni}} \tag{A1.23}$$

The intrinsic transistor admittance matrix, Y_{int}, is given by:

$$\underline{I_e} = Y_{\text{int}} V_e + \underline{i_e} \tag{A1.24}$$

$$Y_{\text{int}} = Y_{ee} - P \cdot Y_{ie} \tag{A1.25}$$

$$\underline{i_e} = \underline{i_{ne}} - P \cdot \underline{i_{ni}} \tag{A1.26}$$

where

$$P = Y_{ei} Y_{ii}^{-1} \tag{A1.27}$$

Using (A1.26) and (A1.27), the intrinsic transistor correlation matrix C_{Yi} (Fig. A1.2) is given by:

$$C_{Yi} = \begin{bmatrix} \overline{i_g^2} & \overline{i_g^* i_d} \\ \overline{i_g i_d^*} & \overline{i_d^2} \end{bmatrix} = C_{ee} - C_{ei} \cdot P^{\dagger} - P \cdot C_{ie} + P \cdot C_{ii} \cdot P^{\dagger} \tag{A1.28}$$

The intrinsic circuit elements can be obtained from intrinsic *Y* parameters by identification.

A useful intrinsic noise model proposed by [Pospieszalski-1989; Tasker-1993; Lazaro-1999] also known as temperature noise model are commonly used. The noise sources in this model (Fig. A1.3) are arranged as input voltage noise source, e_g, and output current noise source, i_d.

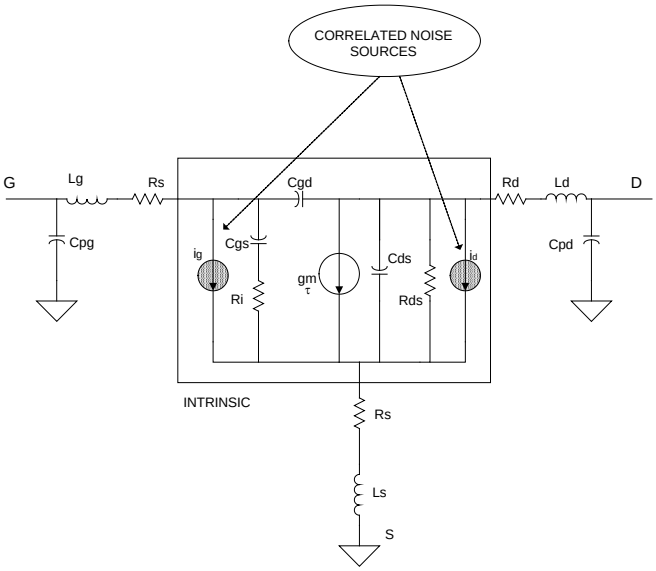


Fig. A.1.2. Small-signal equivalent circuit using admittance noise source configuration for intrinsic MOSFET

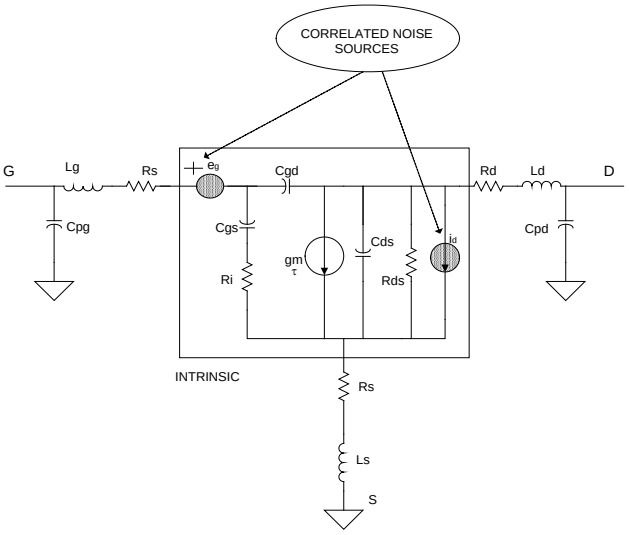


Fig. A1.3. Small-signal equivalent circuit using hybrid noise source configuration for intrinsic MOSFET

$$P = \begin{bmatrix} \dfrac{-1}{Y_{i11}} & 0 \\ \dfrac{-Y_{i21}}{Y_{i11}} & 1 \end{bmatrix} \tag{A1.29}$$

$$C_H = \begin{bmatrix} \overline{e_g^2} & \overline{e_g^* i_d} \\ \overline{e_g i_d^*} & \overline{i_d^2} \end{bmatrix} = P \cdot C_{Y_i} \cdot P^{\dagger} \tag{A1.30}$$

The gate and drain temperature and the hybrid correlation coefficient are defined as:

$$T_g = \frac{\overline{e_g^2}}{4k\Delta f R_i} \tag{A1.31}$$

$$T_d = \frac{\overline{i_d^2}}{4k\Delta f \,/\, R_{ds}} \tag{A1.32}$$

$$\rho_H = \frac{\overline{e_g^* i_d}}{\sqrt{\overline{e_g^2} \cdot \overline{i_d^2}}} \tag{A1.33}$$

The intrinsic admittance parameter, Y_i, and admittance matrix, C_{Yi}, are obtained from (A1.25) and (A1.28), respectively. In order to obtain the transistor *S* parameters and noise parameters the series parasitic resistances and inductance, and the parallel parasitic capacitance must be included [Hillbrand-1976].

$$Z_e = \begin{bmatrix} Z_s + Z_g & Z_s \\ Z_s & Z_d \end{bmatrix} + Y_i^{-1} \tag{A1.34}$$

$$Y = j\omega \begin{bmatrix} C_{pg} + C_{pgd} & -C_{pgd} \\ -C_{pgd} & C_{pd} + C_{pgd} \end{bmatrix} + Z_e^{-1} \tag{A1.35}$$

where

$$Z_x = R_x + j\omega L_x, x = s, g, d \tag{A1.36}$$

$$C_{Z_e} = 4kT\begin{bmatrix} R_s + R_g & R_s \\ R_s & R_s + R_d \end{bmatrix} + \left(Y_i^{-1}\right)\cdot C_{Y_i}\cdot\left(Y_i^{-1}\right)^{\dagger} \tag{A1.37}$$

$$C_Y = \left(Z_e^{-1}\right)\cdot C_{Z_e}\cdot\left(Z_e^{-1}\right)^{\dagger} \tag{A1.38}$$

The total ABCD noise correlation matrix can be obtained using [Hillbrand-1976]:

$$A = \frac{1}{Y_{21}}\begin{bmatrix} -Y_{22} & -1 \\ -\det(Y) & -Y_{11} \end{bmatrix} \tag{A1.39}$$

$$C_A = \begin{bmatrix} 0 & A_{12} \\ 1 & A_{22} \end{bmatrix}\cdot C_Y \cdot \begin{bmatrix} 0 & A_{12} \\ 1 & A_{22} \end{bmatrix}^{\dagger} \tag{A1.40}$$

Then the noise parameters are obtained using [Hillbrand-1976]:

$$R_n = \frac{C_{A11}}{4kT_0\Delta f} \tag{A1.41}$$

$$Y_{opt} = \sqrt{\left(\frac{C_{A22}}{C_{A11}}\right)^2 - \left(\frac{\mathrm{Im}(C_{A21})}{C_{A11}}\right)^2} \tag{A1.42}$$

$$F_{\min} = 1 + 2\left(\mathrm{Re}(C_{A12}) + \mathrm{Re}(Y_{opt})C_{A11}\right)/(4kT_0\Delta f) \tag{A1.43}$$

where k is the Boltzmann constant and T_0 is the reference temperature (T_0=*290K*).

References

[Hillbrand-1976] H. Hillbrand and P. Russer, "An efficient method for computer aided noise analysis of linear amplifier networks", *IEEE Transactions on Circuits and Systems*, **23** (4), 235-238 (1976)

[Lazaro-1999] A. Lazaro, L. Pradell and J. M. O'Callaghan, "FET noise-parameter determination using a novel technique based on 50-Omega noise-figure measurements", *IEEE Transactions on Microwave Theory and Techniques*, **47** (3), 315-324 (1999)

[Pospieszalski-1989] M. W. Pospieszalski, "Modeling of noise parameters of MESFETs and MODFETs and their frequency and temperature dependence", *IEEE Transactions on Microwave Theory and Techniques*, **37** (9), 1340-1350 (1989)

[Tasker-1993] P. J. Tasker, W. Reinert, B. Hughes, J. Braunstein and M. Schlechtweg, "Transistor noise parameter extraction using a 50 Omega measurement system", *IEEE MTT-S International Microwave Symposium Digest*, Atlanta, GA, USA, 1251-1254 (1993)

Annex II

Analytical Noise Modeling

For the compact modeling of noise, three methods are usually applied: 1) an equivalent circuit approach, 2) the impedance field method, or 3) the Langevin or Klaasen-Prins method. A.S.Roy et al. [Roy-2006] demonstrated that the three methods are equivalent and the same final expression for the spectral densities or correlation matrix elements were obtained. Therefore, the compact modeling methods could be considered as an analytic analysis technique of the active transmission line. The method used in this research - the equivalent circuit approach - will be described in more detail below.

Let us consider a non-uniform channel with a distributed noise current source $\delta i_n(x,t)$ [Roy-2006]. The current at any position *x* can be written as:

$$I(x) = g\left(V, \frac{dV}{dx}\right) \cdot \frac{dV}{dx} \tag{A2.1}$$

where $g = W\mu Q_i$ and *W* is the width, μ is the mobility, Q_i is the inversion charge density and *V* is the channel potential. In the presence of velocity saturation, μ starts to depend on the electric field so *g* will be a function of *V* and *(dV/dx)*. Figure A2.1 shows the basics of calculating noise by an equivalent circuit approach [Roy-2006]. An elementary noise source $\delta i_n(x',t)$ between *x'* and *x'+Δx'* sets up a

noise current $\delta i_d(x',t)$ at the drain. Now $\delta i_d(x',t)$ is given by $g_{eq}(x') \cdot \Delta r \cdot \delta i_n(x',t)$ [Roy-2005].

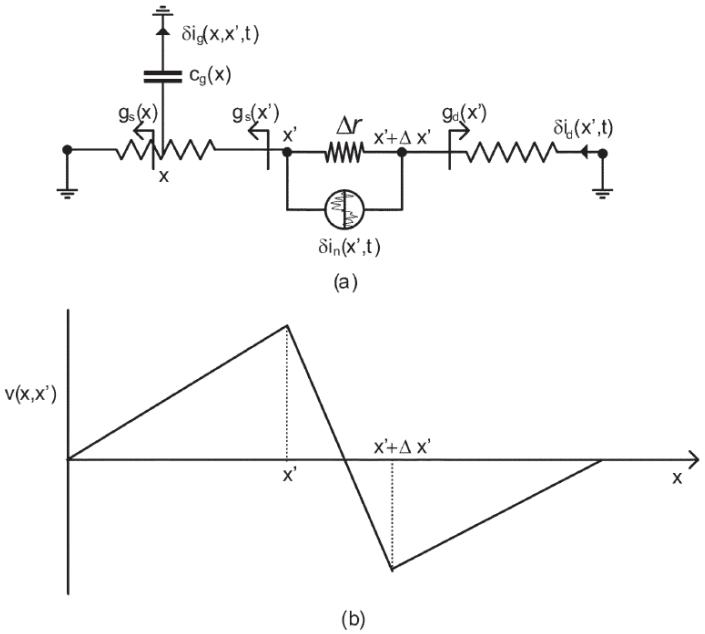


Fig. A2.1. Noise calculation using an equivalent circuit approach. (a) the basic method; (b) typical potential fluctuation *v(x)* due to a current source between *x'* and *x'+dx'* as function of position *x* in the channel. *v(x)* between *x* and *x+Δx* causes a fluctuation in gate current by the coupling through capacitance $c_g(x)$.

From [Roy-2005] and [Roy2-2005] we have the conductance between a fixed point *a* and a variable point *x*, g_{xa} defined as:

$$g_{xa}=\frac{WQ_i(x)\mu}{(x-a)+\int_{V_a}^{V}\frac{\mu'}{\mu+\mu'E}dV}=\frac{WQ_i(x)\mu}{\int_{a}^{x}\frac{\mu}{\mu+\mu'E}dx}$$
$$=\frac{g(V)}{\int_{a}^{x}\frac{g(V,E)}{g(V,E)+\frac{\partial g(V,E)}{\partial E}E}dx}=\frac{g(V,E)}{\int_{a}^{x}\frac{g_c(V,E)}{g(V,E)}dx} \quad \text{(A2.2)}$$

where $E=-(dV/dx)$, $\mu'=(\partial\mu/\partial E)$ and:

$$\frac{g_c(V,E)}{g(V,E)}=\frac{g(V,E)}{g(V,E)+\frac{\partial g(V,E)}{\partial E}E} \quad \text{(A2.3)}$$

A factor L_c is introduced as well, given by:

$$L_c=\int_0^L\frac{g_c(V,E)}{g(V,E)}dx=\frac{1}{I}\int_{V_S}^{V_D}g_c(V,E)\,dV$$
$$=L\cdot\frac{\int_{V_S}^{V_D}g_c(V,E)\,dV}{I\cdot L}=L\cdot\frac{\int_{V_S}^{V_D}g_c(V,E)\,dV}{\int_{V_S}^{V_D}g(V,E)\,dV} \quad \text{(A2.4)}$$

which yields $(1/g_{eq})=(1/g_s)+(1/g_d)$ as:

$$g_{eq}(x)=\frac{g(V,E)}{\int_0^L\frac{g_c(V,E)}{g(V,E)}dx}=\frac{g(V,E)}{L_c} \quad \text{(A2.5)}$$

where $g_s(g_d)$ is the conductance which point x sees looking towards the source (drain). For the sake of simplicity, $g(V)$ and $g_c(V)$ is used instead of $g(V,E)$ and $g_c(V,E)$ from this point on (the field dependence is implied). Δr can be deduced from (A2.2) as [Roy-2006]:

$$\Delta r = \frac{\Delta x}{W\left(Q_i\right)\left(\mu + \mu' E\right)} = \frac{\Delta x}{g\left(V\right)} \frac{g_c\left(V\right)}{g\left(V\right)} \tag{A2.6}$$

Therefore the expression of $\delta i_d\left(x',t\right)$ reads:

$$\begin{aligned} \delta i_d\left(x',t\right) &= \frac{1}{\int_0^L \frac{g_c\left(V\right)}{g\left(V\right)} dx} \cdot \frac{g_c\left(V'\right)}{g\left(V'\right)} \cdot \delta i_n\left(x',t\right) \Delta x' \\ &= \frac{1}{L_c} \cdot \frac{g_c\left(V'\right)}{g\left(V'\right)} \cdot \delta i_n\left(x',t\right) \Delta x' \end{aligned} \tag{A2.7}$$

where *V'* is the channel potential at *x'*. The total drain current fluctuation can be written as a sum (integral) of the contributions from different local noise sources located at *x'*:

$$\Delta i_d\left(t\right) = \int_0^L \delta i_d\left(x',t\right) dx' = \frac{1}{L_c} \int_0^L \frac{g_c\left(V'\right)}{g\left(V'\right)} \cdot \delta i_n\left(x',t\right) dx' \tag{A2.8}$$

In order to calculate the induced gate current, the voltage perturbation induced by this elementary noise source as a function of position needs to be found. A potential fluctuation *v(x)* between *x* and *x+Δx* causes a fluctuation in gate current by capacitive coupling. Therefore, the gate current i_g is given by:

$$i_g = j\omega W \int_0^L C_g\left(x\right) v\left(x\right) dx \tag{A2.9}$$

where $C_g = \left(dQ_g / dV\right)$, Q_g being the charge stored per unit area in the gate.

The voltage perturbation at *x* due to the noise source $\delta i_n\left(x',t\right)$, $v\left(x,x'\right)$, for *x<x'* is given by $\left(\delta i_d\left(x',t\right) / g_s\left(x\right)\right)$ (see Fig. A2.1(b)), where

$$\frac{1}{g_s(x)} = \frac{\int_0^x \frac{g_c(V)}{g(V)}dx}{g(V)} = \frac{\int_{V_S}^{V} \frac{g_c(V)}{g(V)}\frac{g(V)dV}{I}}{g(V)} = \frac{\int_{V_S}^{V} g_c(V)dV}{I \cdot g(V)} \tag{A2.10}$$

and the voltage perturbation *v(x,x')* for *x'*<*x* is given by $-\left(\delta i_d(x',t)/g_d(x)\right)$ where:

$$\frac{1}{g_d(x)} = \frac{\int_{V}^{V_D} g_c(V)dV}{I \cdot g(V)} \tag{A2.11}$$

Then, $\delta i_g(x,x',t)$, the induced gate noise between *x* and *x*+*Δx* caused by the current fluctuation between *x'* and *x'*+*Δx'*, becomes $\delta i_g(x',t)$ due to the fluctuation at *x'* given by (from (A2.9)):

$$\delta i_g(x',t) = j\omega W \left(\begin{array}{l} \int_0^{x'} C_g(x) \cdot \frac{\int_{V_S}^{V} g_c(V)dV}{I \cdot g(V)} dx \\ -\int_{x'}^{L} C_g(x) \cdot \frac{\int_{V}^{V_D} g_c(V)dV}{I \cdot g(V)} dx \end{array} \right) \delta i_d(x',t) \tag{A2.12}$$

Converting (A2.12) to the voltage domain using $I = g(V)(dV/dx)$ we obtain:

$$\delta i_g(x',t) = \frac{j\omega W}{I^2} \left(\begin{array}{l} \int_{V_S}^{V'} \frac{dQ_g}{dV}\left(\int_{V_S}^{V} g_c(V)dV\right)dV - \\ \int_{V'}^{V_D} \frac{dQ_g}{dV}\left(\int_{V}^{V_D} g_c(V)dV\right)dV \end{array} \right) \delta i_d(x',t) \tag{A2.13}$$

Integrating by parts yields:

$$\delta i_g\left(x',t\right)=\frac{j\omega W}{I^2}\begin{pmatrix} Q_g\left(V'\right)\int_{V_S}^{V_D} g_c\left(V\right)dV \\ -\int_{V_S}^{V_D} Q_g\left(V\right)g_c\left(V\right)dV \end{pmatrix}\delta i_d\left(x',t\right) \tag{A2.14}$$

Rearranging and putting the expression of $\delta i_d\left(x',t\right)$ from (A2.7) we obtain $\delta i_g\left(x',t\right)$ (the contribution to the gate current from the noise source between *x'* and *x'+Δx'*) as:

$$\begin{aligned}\delta i_g\left(x',t\right)=&\frac{j\omega W}{I^2L_c}\left(\int_{V_S}^{V_D} g_c\left(V\right)\left(Q_g\left(V'\right)-Q_g\left(V\right)\right)dV\right)\\ &\cdot\frac{g_c\left(V'\right)}{g\left(V'\right)}\cdot\delta i_n\left(x',t\right)\Delta x'\end{aligned} \tag{A2.15}$$

Thus the sum of all elementary contributions to the total induced gate current $\Delta i_g(t)$ becomes;

$$\begin{aligned}&\Delta i_g\left(t\right)=\frac{j\omega W}{I^2L_c}\cdot\\ &\cdot\int_0^L\left(\int_{V_S}^{V_D} g_c\left(V\right)\left(Q_g\left(V'\right)-Q_g\left(V\right)\right)dV\right)\cdot\frac{g_c\left(V'\right)}{g\left(V'\right)}\cdot\delta i_n\left(x',t\right)dx'\end{aligned} \tag{A2.16}$$

Equations (A2.8) and (A2.16) are they key for calculating any noise parameter, and as shown in [Roy-2006], these two expressions are identical to the other two noise calculation methodologies – Klaassen-Prins and the impedance field method.

References

[Roy-2005] A. S. Roy and C. C. Enz, "Compact modeling of thermal noise in the MOS transistor", *IEEE Transactions on Electron Devices*, **52** (4), 611-614 (2005)

[Roy-2006] A. S. Roy, C. C. Enz and J. M. Sallese, "Noise modeling methodologies in the presence of mobility degradation and their equivalence", *IEEE Transactions on Electron Devices*, **53** (2), 348-355 (2006)

[Roy2-2005] A. S. Roy and C. C. Enz, "An analytical thermal noise model of the MOS transistor valid in all modes of operation", *Noise and Fluctuations*, Salamanca, Spain, 741-744 (2005)

Annex III

The Lambert W Function

Many modern engineering processes, including signals, images and communication systems, often have to operate in complex environments dominated by noise. Efficient design, control and performance evaluation in these contexts depend on the capability of the modeling such noise. One tool for modeling is the special function known under the name of the Lambert W function. The Lambert W function is defined as the inverse of the function $f(W)=We^{W}$, or:

$$x = W(x)e^{W(x)} \tag{A3.1}$$

for any complex number x. However, in our application only real values of x will be considered.

This function has progressively been recognized in the solution to many problems in various fields of mathematics, physics, and engineering, up to a point at which many authors convincingly argued to establish the Lambert W function as a special function of mathematics on its own. These elements also motivated the introduction of the Lambert W function in various mathematical software programs, such as Matlab, Mathematica, Maple. However, the main problem of this function is that its implementation is purely numerical, which in the field of

semiconductors, can lead to increasing computation times, as the dimensions of the devices shrink and new quantum mechanical effects come into play.

In order to solve this problem, several approximations have been proposed by mathematicians; however, their uses are many times limited to the negative side of the Lambert W function, or to the very near proximity of the center coordinates. However, a function proposed by Winitzki [Winitzki-2003] can be successfully employed for the simulation of such devices as FinFET (see chapter 5), in the range of interest of the bias for these devices.

$$W(x) \approx \ln(1+x)\left(1-\frac{\ln(1+\ln(1+x))}{2+\ln(1+x)}\right) \tag{A3.2}$$

Figure A3.1 presents a comparison between the numerical calculation of the Lambert W function implemented in Matlab and this approximation, and shows a good agreement, with a very low relative error (Fig. A3.2), which makes it very suitable for compact modeling, due to the speed of computations.

The approximation has been employed in chapter 5 for the computations of the charge in FinFET devices, and can be used for other devices as well, like SGT or DG transistors.

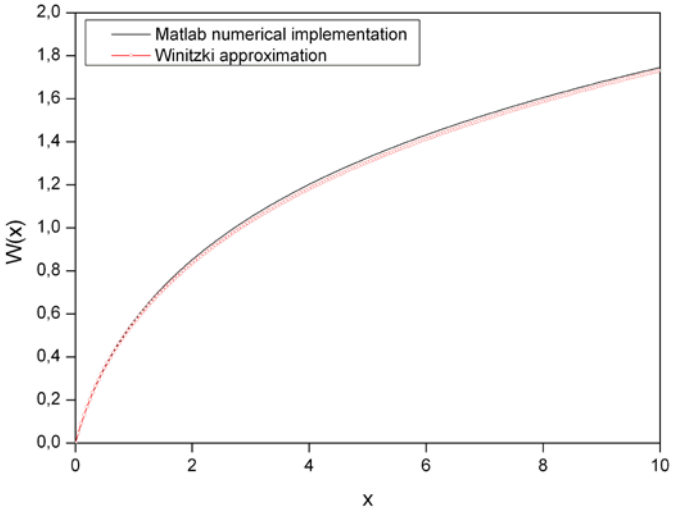


Fig. A3.1. Comparison between the numerical implementation of the Lambert W function in Matlab and the approximation given by Winitzki [Winitzki-2003]

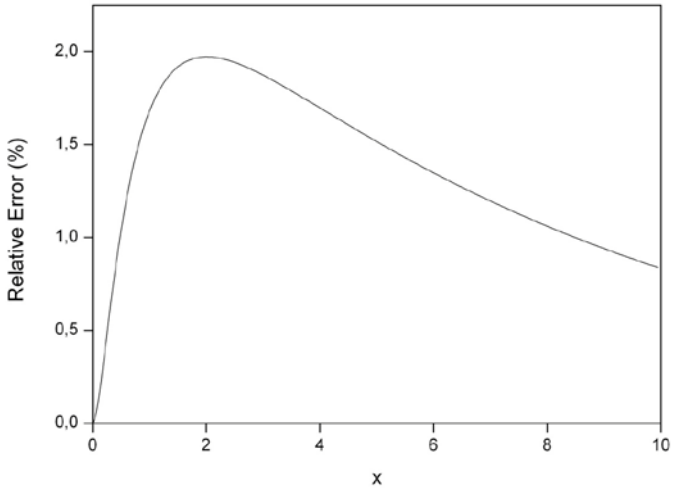


Fig. A3.2. Relative error between the two expressions

References

[Winitzki-2003] S. Winitzki, "Uniform approximations for transcendental functions", Springer-Verlag Berlin: Berlin (2003)

UNIVERSITAT ROVIRA I VIRGILI
COMPACT MODELING OF THE RF AND NOISE BEHAVIOR OF MULTIPLE-GATE MOSFETS
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The nanoelectronics world is moving forward at incredible speed, and technology keeps improving overnight. One can no longer afford to spend months or even years evaluating a future technological node, thus the need for a robust evaluation system has arisen. Numerical ways of modeling the new device architectures, apart from precision, offer very little in terms of performance, and are being replaced by new analytical tools, focused on providing exactly that – speed and accuracy.

This research work has been conceived to cover precisely these aspects. The models described here are physical models, with very few adjusting parameters, that are usually replaceable with values extracted from experimental measurements; they are compact models, making use of approximate expressions that have been tweaked to offer a very good fit with numerical simulations and offering in exchange the advantage of computation speed, decreasing the simulation time and thus the productivity. Another major advantage is the fact that these models can be easily incorporated into circuit simulators, which allows designers to unleash the full capabilities of the design software to create new devices and applications.

In this thesis, the performances of different Multiple-Gate MOSFET (DG, SGT and triple-gate) structures has been evaluated, for the RF mode of operation, and the noise performances of these devices has been studied. The modeling scheme is similar for all these devices and is adapted to each geometry.

The compact noise models presented in this thesis reproduce the measured noise bias behavior for any gate length found for SG MOSFETs in the literature, without the need for additional parameters. Therefore, they are very promising models for being used in circuit simulators for SG, DG, SGT and FinFET devices.