Integration of thin film based micro solid oxide fuel cells in silicon technology

Iñigo Garbayo Senosiain

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Integration of thin film-based micro solid oxide fuel cells in silicon technology

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Thesis submitted to apply for the degree of Doctor, in the *Nanoscience* Program of the University of Barcelona.

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El Dr. Albert Tarancón Rubio, investigador del Institut de Recerca en Energia de Catalunya (IREC) y la Dra. Neus Sabaté Vizcarra, investigadora del Instituto de Microelectrónica de Barcelona (IMB-CNM, CSIC), CERTIFICAN:

Que la memoria titulada *"Integration of thin film-based micro solid oxide fuel cells in silicon technology"* presentada por Íñigo Garbayo Senosiain para optar al grado de Doctor en el Programa de Nanociencias de la Universitat de Barcelona ha sido realizada bajo su dirección en el Instituto de Microelectrónica de Barcelona del Consejo Superior de Investigaciones Científicas.

Barcelona, Septiembre de 2013

Dr. Albert Tarancón Rubio | Dra. Neus Sabaté Vizcarra

Iñigo Garbayo Senosiain

*" Nothing in life is to be feared, it is only
to be understood"*

(Marie Skłodowska-Curie)

ABSTRACT

In the last decades, there has been a huge proliferation of portable devices. Among them, consumer electronics such as mobile phones, music players, e-books, etc. are greatly extended. In order to provide these devices with the required autonomy, a power supply system has to be integrated within the device packaging. This impels the search of integrated power sources that could satisfy the requirements of high power density, long operation lifetime and low cost. Up to now, batteries have been commonly used as power supply for these devices. However, as functionalities increase, the need high off-grid power supply and storage exponentially increases. Just entering on the 4th generation (4G) era on consumer electronics devices, some studies suggest that the already optimized batteries are probably reaching their energy density limit and no longer can be considered for reliably powering high-performance devices.

Therefore, in the last years, many research groups around the world have focused their attention on the development of efficient alternatives to batteries, as power supply for the new high-performance portable devices working on the low power regime ($1 - 20\ W$). Due to their long lifetime, high power density and integrability, probably the most promising alternative is the development of micro fuel cells. Among them, micro solid oxide fuel cells (micro SOFC) present the highest values of specific energy densities (by unit mass and/or volume), mainly due to their higher operating temperature and subsequent capability of operate directly on hydrocarbon fuels. The most extended design for micro SOFC devices is based on the fabrication of accessible free-standing membranes of the functional layers, i.e. a thin electrolyte covered by an anode and a cathode one at each side (electrodes), supported on silicon-based microfabricated platforms. The use of silicon as supporting material has been found to be very convenient as it is the principal material used in microfabrication technology and therefore there exist a wide and well-known series of techniques already developed for its micromachining. This allows the fabrication of functional membranes, while ensuring robustness on the system.

This thesis encompasses the design, fabrication and characterization of thin film-based micro solid oxide fuel cells integrated in silicon. The development of micro SOFC was carried out in three different ways; (i.) presenting new designing strategies for the optimization of the free-standing membranes, (ii.) fabricating thermo-mechanically stable thin film electrolytes and (iii.) suggesting and implementing new more reliable thin film electrode materials.

On one side, two different membrane designs are micro fabricated using silicon micro machining technology. First, the fabrication of a basic square design was firstly addressed, where the main concerns were placed on the adaptation of the fabrication flow to the Clean Room capabilities at IMB-CNM (CSIC). Then, an innovative large-area membrane was designed and fabricated. This second design was based on the use of doped silicon slab grids as robust support for the larger free-standing areas, allowing the fabrication of $x30$ larger membranes than previous basic designs.

Yttria-stabilized zirconia (YSZ), the state-of-the-art electrolyte material in bulk SOFC, was used for the fabrication of thin film free-standing electrolytic membranes. Dense, fully crystalline and homogeneous films were obtained, as required for the fabrication of effective electrolytes, thus avoiding shortcuts between electrodes and/or gas leakages. An exhaustive study on the thermo-mechanical stability of the electrolytic membranes was performed, paying special attention to the evolution of the stress with fabrication conditions. Finally, target values of resistance associated to the electrolyte (Area Specific Resistance, $ASR = 0.15\ \Omega cm^2$) were obtained at temperatures as low as $400°C$ for $250\ nm$-thick YSZ membranes, thus presenting them as suitable electrolyte for micro SOFC operating in the intermediate range of temperatures (IT range, $400 - 800°C$).

Several materials were tested as thin film electrodes for their use in micro SOFC. First, although widely used by other authors in previous reports of micro SOFC systems, thin film metallic electrodes (porous Pt) were found to be thermally instable under micro SOFC operating temperatures. This impelled the search for alternative materials as either cathode or anode. For the cathode side, porous $La_{0.6}Sr_{0.4}CoO_{3-\delta}$ (LSC) thin films were fabricated and implemented in real micro SOFC configurations, i.e. free-standing membranes. Sufficient conductivity for their use as cathode films was measured, and no degradation was observed in the whole operating range. The thermo-mechanical stability of LSC/YSZ/LSC membranes was ensured up to $700℃$. Target values of ASR required for SOFC cathode/electrolyte bi-layers ($0.30\ \Omega cm^2$) were achieved in the IT range ($700℃$). For the anode side, porous Pt-$Ce_{0.8}Gd_{0.2}O_{1.9-\delta}$ (Pt-CGO) thin film cermets were fabricated. Porous CGO films below $1\ \mu m$-thick had to be fabricated due to delamination problems. Percolation of Pt into the porous ceramic network was ensured by thermal treatment and observed by SEM. Anode electrochemical performance was tested on Pt-CGO/YSZ/CGO-Pt symmetrical membranes. Target values for the anode/electrolyte bi-layer were reached again at temperatures of *ca.* $700℃$.

In addition, the fabrication of thermally stable metal-based current collectors was also addressed. A non-conventional lithographic step, i.e. nanosphere lithography was used in order to define a patterned grid on both sides of the functional membranes. Dense Pt grids were fabricated thermo-mechanically stable, and their durability was ensured during real micro SOFC operating conditions.

Finally, a fully ceramic-based micro SOFC was presented here for the first time. The three functional components of the fuel cell, i.e. cathode, electrolyte and anode, were fabricated by using the previously developed thin films. Thus, LSC/YSZ/CGO-Pt free-standing membranes were fabricated, and finally Pt current collectors were implemented on both sides. Thermo-mechanical stability of the micro SOFC membrane was proved till $750℃$, extending the up-to-now reported operating temperatures of micro SOFC and therefore allowing the use of ceramic electrodes. A maximum power density of $100\ mW/cm^2$ was measured at $750℃$ under pure H_2 as fuel and synthetic air as oxidant. These results represented the first report on a second generation of more reliable micro SOFC systems, based on ceramics instead of thermally instable metal-based electrodes.

RESUMEN *(en castellano)*

En las últimas décadas, ha habido una gran proliferación de aparatos portátiles. Entre ellos, cabe destacar los aparatos destinados a electrónica de consumo, como por ejemplo teléfonos móviles, reproductores de música, libros electrónicos, etc, los cuales están actualmente muy extendidos. De cara a proporcionar a estos aparatos con suficiente autonomía, se ha de integrar una fuente de alimentación en el mismo dispositivo. Esto urge a buscar posibles fuentes de alimentación con capacidad de integración, y que a su vez satisfagan los requerimientos básicos de alta densidad de potencia, gran tiempo de vida y bajo coste. Hasta ahora, la principal fuente de alimentación utilizada en este tipo de dispositivos ha sido las baterías. Sin embargo, conforme aumentan las funcionalidades, la necesidad de mayor capacidad de suministro (o almacenamiento) energético aumenta. Es más, justo ahora entrando en la cuarta generación (4G) de la electrónica de consumo, diversos estudios sugieren que las baterías, ya optimizadas, probablemente están alcanzando su límite en densidad energética, con lo que no podrían ya considerarse más para alimentar de manera viable los dispositivos más avanzados.

En este sentido, en los últimos años muchos grupos de investigación han puesto su atención en el desarrollo de alternativas viables que puedan mejorar las prestaciones de las baterías como fuente de alimentación de dispositivos de altas prestaciones que trabajen en el régimen de baja potencia ($1 - 20\ W$). Debido a su alto tiempo de vida, alta densidad energética y capacidad de integración, probablemente la alternativa más prometedora es el desarrollo de micro pilas de combustible. En particular, entre los diferentes tipos, las micro pilas de combustible de óxido sólido (micro SOFC, de sus siglas en inglés), presentan los mayores valores de densidad energética específica (por unidad de masa y/o volumen), mayormente debido a su alta temperatura de operación y la consecuente capacidad de operar directamente con combustibles hidrocarburos. El diseño de micro SOFC más extendido está basado en la fabricación de membranas auto soportadas, las cuales integran ya todas las partes funcionales de la pila, es decir, un electrolito fino cubierto por un ánodo y un cátodo (uno a cada lado). Estas membranas, de grosor muy fino (menos de $1\ \mu m$), normalmente se encuentran soportadas en plataformas de silicio micro mecanizadas, de manera que se facilita un fácil acceso al combustible directamente a ambos lados de la membrana, a la vez que se proporciona robustez al sistema. El uso de silicio como material de soporte es muy conveniente, ya que es el material más utilizado en micro fabricación, por lo que existe una amplia y altamente desarrollada serie de técnicas para su micro mecanizado.

Esta tesis engloba el diseño, la fabricación y la caracterización de micro pilas de combustible de óxido sólido basadas en capas delgadas, e integradas en tecnología de silicio. El desarrollo de las micro SOFC se ha llevado a cabo de tres formas diferentes: (i.) presentando nuevos diseños para la optimización de las membranas auto soportadas, (ii.) fabricando electrolitos en capa delgada estables termo-mecánicamente y (iii.) sugiriendo e implementando en el dispositivo final nuevos materiales de electrodo en capa delgada más efectivos y viables que los actuales.

En primer lugar, se fabricaron dos diseños de membrana diferentes, usando tecnología de micro fabricación de silicio. En el primero de los diseños, se fabricaron membranas cuadradas básicas. En este caso, el trabajo más importante fue el de la adaptación del proceso de fabricación al flujo de fabricación de la Sala Blanca del IMB-CNM (CSIC). Más adelante, se desarrolló un nuevo diseño de membrana de gran superficie, basado en el uso de mallas de nervios de silicio dopado como soporte robusto. Así, se consiguieron fabricar membranas auto soportadas con un área total de hasta 30 veces mayor que las conseguidas en el diseño básico anterior.

Para el electrolito, se usó zirconia estabilizada con ytria (YSZ, de sus siglas en inglés), el material estado del arte en SOFC de gran volumen. Se fabricaron membranas auto soportadas de YSZ con gran reproducibilidad, obteniendo capas delgadas densas, cristalinas y de grosor homogéneo. Estas características son básicas para un buen funcionamiento del electrolito, ya que así se evitan posibles cortocircuitos entre los dos electrodos y/o fugas de gas. Además, se realizó un estudio exhaustivo de la estabilidad termo-mecánica de las membranas de YSZ, ya que las temperaturas de operación de la pila son de varios centenares de ℃. En particular, se prestó atención especial a la evolución de los estreses en función de las condiciones de fabricación de la capa de YSZ, para así evitar posibles fallos en los continuos ciclados térmicos. Finalmente, se realizó un estudio de las propiedades electroquímicas de las membranas de YSZ fabricadas. Normalmente, se establece un valor de resistencia específica por área de $0.15\,\Omega cm^2$ para cada una de las capas funcionales de las pilas. En este caso, este valor objetivo se obtuvo a temperaturas de 400℃ en membranas de YSZ de $250\ nm$ de grosor. De esta forma, se comprobó que estas capas pueden funcionar perfectamente como electrolito en todo el rango de operación de las micro SOFC, que normalmente se establece en $400-800$℃.

A continuación, se probaron diversos materiales como electrodos en capa delgada, para su implementación en micro SOFC. En primer lugar, aunque éstos han sido usados frecuentemente por otros autores en estudios previos de micro SOFC, se comprobó que los electrodos metálicos en capa delgada (capas de Pt poroso) son inestables a las temperaturas de operación de las micro SOFC. Por lo tanto, esto hizo que se probaran materiales alternativos, bien para el ánodo o para el cátodo. En particular, para el cátodo se fabricaron capas delgadas porosas de $La_{0.6}Sr_{0.4}CoO_{3-\delta}$ (LSC) y se integraron en membranas auto soportadas de YSZ (electrolito). La conductividad electrónica que se midió en estas capas es adecuada, y no se observó degradación en todo el rango de temperaturas de operación. Así mismo, se comprobó la estabilidad termo mecánica del sistema fabricando membranas simétricas de LSC/YSZ/LSC y realizándoles ciclados térmicos hasta los 700℃. Por último, se midieron las propiedades electroquímicas de las bi-capas cátodo/electrolito, obteniendo los valores objetivo de resistencia específica por área ($0.30\,\Omega cm^2$) a temperaturas de 700℃.

Para el ánodo, se fabricaron capas delgadas porosas de un cermet de Pt y $Ce_{0.8}Gd_{0.2}O_{1.9-\delta}$ (Pt-CGO). Las capas de CGO se tuvieron que fabricar de grosores por debajo de $1\,\mu m$, debido a problemas de delaminación del sustrato. Se aseguró una buena inter-conexión entre el Pt y el CGO mediante tratamientos térmicos. Las propiedades electroquímicas se midieron nuevamente fabricando membranas simétricas, esta vez Pt-CGO/YSZ/CGO-Pt. Así mismo, el objetivo de $0.30\,\Omega cm^2$ se obtuvo de nuevo a temperaturas alrededor de 700℃.

Además, en esta tesis se llevó a cabo la fabricación de colectores de corriente térmicamente estables y a su vez compatibles con la configuración básica de una micro SOFC (membranas auto soportadas). Para ello, se usó un proceso de litografía no convencional, llamado "nanosphere lithography". De esta forma se fabricaron mallas de Pt denso perfectamente ordenadas en ambos lados de las membranas. La estabilidad térmica y la durabilidad en el tiempo de estas mallas fue igualmente probada mediante medidas en condiciones de trabajo reales de micro SOFC.

Por último, en este trabajo se presentó una micro SOFC completamente basada en cerámicas por primera vez. Las tres capas funcionales de la pila, es decir, tanto el cátodo, como el electrolito y el ánodo, se fabricaron basándose en los estudios previos de cada material. Así, se fabricaron membranas auto soportadas siguiendo la configuración LSC/YSZ/CGO-Pt. Además, se implementaron mallas de Pt en ambos lados para asegurar una buena colección de corriente. La estabilidad termo mecánica de la membrana se midió hasta 750℃, extendiendo así el rango de temperaturas de operación reportado anteriormente en dispositivos finales de micro SOFC y en consecuencia permitiendo el uso de electrodos cerámicos. Se midieron valores de densidad de potencia de $100\ mW/cm^2$ a 750℃, usando H_2 como combustible y aire sintético como oxidante. Estos resultados representan los primeros valores de potencia presentados en micro SOFC basadas en cerámicas, abriendo así la posibilidad de desarrollar una segunda generación de micro SOFC más viables térmicamente.

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I.1. Power sources for portable devices

In the last decades there has been a huge proliferation of portable devices (PD) and wireless sensor networks (WSN). Among these devices, Consumer Electronics (CE) such as mobile phones, music players, e-books, etc, and WSN for health or ambience monitoring are greatly extended. Even a recently published study from Cisco predicts that the number of mobile devices will exceed the number of people on earth by the end of 2013 [1]. In order to provide these PD and WSN with the required autonomy, a power supply system has to be integrated within the device packaging. This impels the search of integrated power sources that could satisfy the requirements of high power density, long operation lifetime and low cost, depending on the device operating power range.

Figure I-1 shows a classification of some of the most common portable/remote devices, as a function of their operating power needs [2]. Depending on the power range, different power supply systems are employed. In this sense, energy harvesting (EH) and button batteries are the most common power supply systems used for the ultra-low power regime ($< 1\ mW$, see blue zone in the figure). On the other hand, the most common option when power needs are incremented (low power regime, $1mW - 10W$, red zone in the figure) is the use of batteries. Largely developed during decades, batteries are nowadays responsible of powering most of the commercial CE devices, including GSM -Global System for Mobile communications-, music players or other small electronic devices including laptops [3,4].

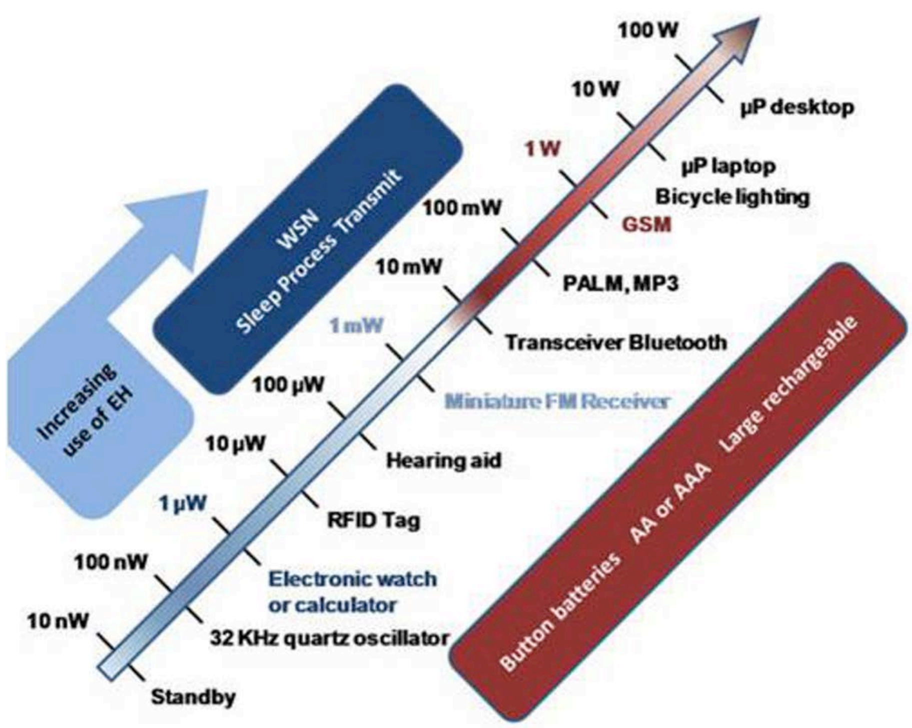

Figure I-1. *Power consumption on remote devices, extracted from [2].*

I.1.1. Limitations of batteries for new energy demands

Up to now, batteries have ensured device autonomy for several days (on less power consuming devices such as standard mobile phones, music players...) or hours (laptops), requiring regular wiring to the electrical grid for recharge. However, as functionalities increase and wireless communication systems or large screens are implemented on these devices, the needs for high off-grid power supply and storage have increased exponentially. With the global explosion in the use of high performance devices such as smartphones or tablets, an important limitation on their autonomy and a gap between device energy needs

and battery energy supply capacity has appeared. Figure I-2 shows the evolution of energy needs for a "heavy" daily use of the outstanding standard mobile phones and smart-phones with time, compared to the energy capacity of batteries (extracted from [5]). The figure clearly illustrates the mismatch lately appeared between power needs (red line) and power supply capacities (blue line). According to this study, the already developed batteries would be reaching their energy density limit (dashed purple line) and no longer could be considered for reliably powering high-performance devices. Therefore, it is appearing a need to consider new technologies with potential of high energy and power density than state-of-the-art battery prototypes, and high storage density to further miniaturize portable electronics for increased device functionality.

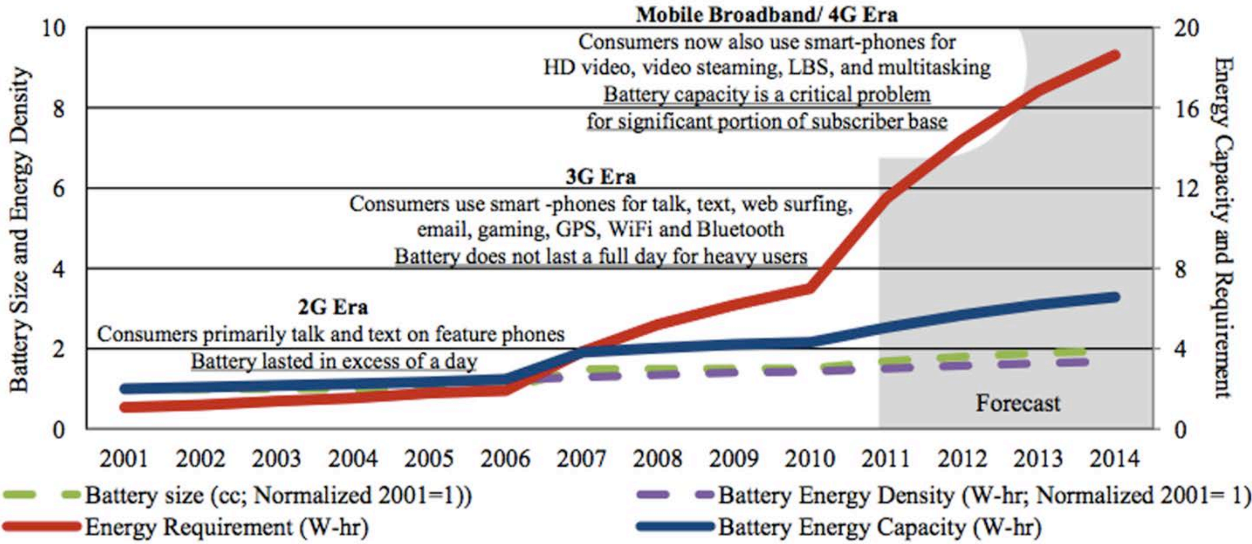

Figure I-2. *Energy needs and capacities of mobile phones and smart-phones vs. time [5].*

I.1.2. Micro fuel cells as battery replacement

According to this scenario, in the last decade there have been several attempts to develop alternative power supplying systems, trying to improve traditional batteries specifications in terms of power density and lifetime. Among the different options appeared, probably the most promising is the development of micro fuel cells (micro FC). Being an electrochemical power source (such as batteries), micro FCs can offer a continuous energy delivering and their high energy density (associated to the capability of using hydrocarbons and their better packaging) and easy and cheap fuel refilling make them really attractive for miniaturization and portable applications. Moreover, since the energy is stored in a fuel reservoir aside from the fuel cell body, these devices offer the additional advantage of allowing an instant recharge, which is very convenient regarding their application to portable devices as it eliminates the grid autonomy (only a cartridge replacement needed).

Although FC principle was proposed more than 100 years ago [6], micro FC technology is a relatively new field (~15 years of research history, [7]). Nevertheless, due to their very promising advantages compared to other power supplying systems, it has received a great interest by the scientific and industrial communities [8-14] and first micro FC prototypes has been already commercialized (see *Section I.2.2* of the present chapter).

I.2. Introduction to micro fuel cells

I.2.1. Fuel cell basics

A Fuel Cell (FC) is an electrochemical device that converts chemical energy into electrical energy. Figure I-3 shows the basic structure of a FC, consisting of an ionic-conductor electrolyte layer that separates two electrode layers (anode and cathode, one at each side). Two redox sub-reactions take place when fuel and oxidant are flowed through the anode and cathode respectively, generating electrical energy by the electrochemical oxidation and reduction of the fuel and oxidant. During operation, the electrolytic barrier layer must be permeable to one of the species (a specific ion depending on the type of FC) generated on one sub-reaction while remaining electrically insulator. Thus, these ions flow through the cell and the electrons go through an external circuit, closing the redox reaction and generating the desired electronic flow [15].

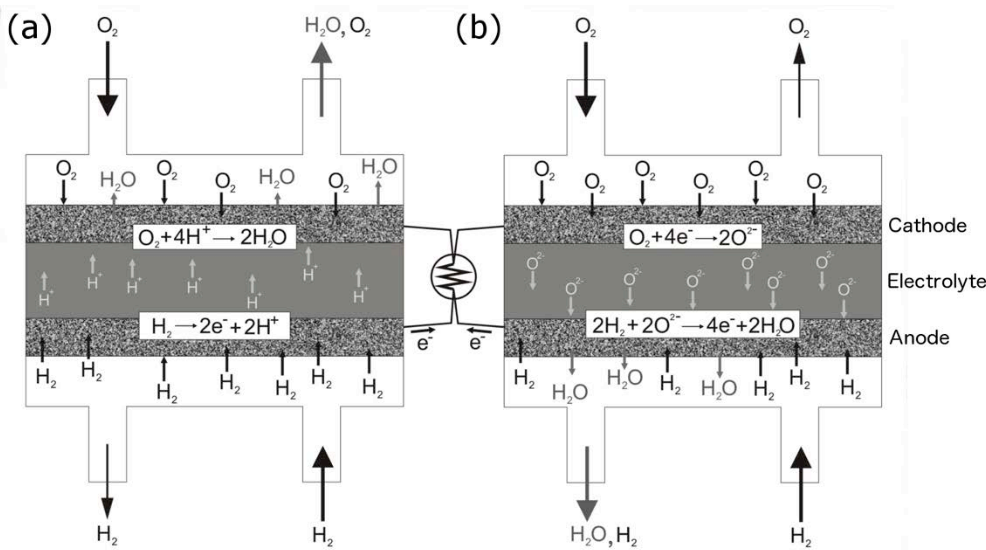

Figure I-3. *Scheme of the two most relevant types of FC. Depending on the movable species through the electrolyte, H^+ (a) or O^{2-} (b), the different electrode sub-reactions are detailed in each case.*

In principle, any substance capable of chemical oxidation/reduction can be used as the fuel/oxidant at the anode/cathode of a fuel cell, as long as the electrochemical potential of the fuel cell (E_{FC}) is positive, i.e. energetically favourable. This potential E_{FC} is a measure of the energy per unit charge that is available from the redox sub-reactions to drive the fuel cell overall reaction, and is given by the Nernst equation *(I.1)*. This equation provides a relationship between the ideal *standard* potential of the cell (E^0_{FC})[1] and the ideal equilibrium potential (E_{FC}) at other partial pressures of reactants and products:

$$E_{FC} = E^0_{FC} - \frac{RT}{nF} lnQ \qquad (I.1)$$

where R is the universal gas constant, T is the temperature, n the number of moles of electrons transferred in the cell reaction, F the Faraday constant and Q the reaction quotient, i.e. a function of the activities of the chemical species involved in the reaction[2].

[1] Potential measured under standard conditions, i.e. 25°C and (i.) concentration of 1 M, (ii.) partial pressure of 1 atm and/or (iii.) metals in their pure state for each ion, gas or element participating in the reaction, respectively.

[2] $Q = \frac{\Pi_j a_j^{v_j}}{\Pi_i a_i^{v_i}}$, where a_j and a_i are the activities of products and reactants respectively, each raised to the power of a stoichiometric coefficient v.

On any electrochemical cell, the cell potential E_{FC} can be also calculated from the specific half-cell potentials. Each sub-reaction has a specific reduction potential (E_{red}), which measures the ability of the reactant (oxidant) to gain electrons, relative to the E_{red} of the reaction $2H^{+} + 2e^{-} \leftrightarrow H_2$ that is arbitrarily set as $+0,00$. Analogously, the oxidation potential E_{oxi} is a measure of the ability of the fuel to lose electrons, and is calculated simply as $E_{oxi} = -E_{red}$. Then, E_{FC} will be defined by,

$$E_{FC} = E_{oxi} + E_{red} \qquad (I.2)$$

Table I-1 shows the electrode and fuel cell reactions for the most common fuel i.e. hydrogen. The corresponding electrode (standard) reduction potentials and subsequent cell potential are also included[3]. Hydrogen has become the fuel of choice for most applications because of its high reactivity when suitable catalysts or enough operating temperature are used. However, nowadays a huge variety of alternative fuels are also under investigation for being used in different types of fuel cells (methanol for low temperature fuel cells, methane or other more complex hydrocarbons for high temperature fuel cells). When using other fuels, either the subsequent electric potential of the cell varies as a function of the specific E_{red} of each fuel (for example, $E_{CH_3OH} = +0,13$) or internal reforming occurs on the anode side thus producing H_2 in-situ (and therefore not affecting the fuel cell electric potential). On the cathode side, the oxidant of choice is always oxygen, due to the easy handling and access (usually directly in air form).

Table I-1. *Electrode and fuel cell reactions, and related electric potentials.*

		Reaction	$E^0(V)$
ANODE	H_2 oxidation	$H_2 \leftrightarrow 2H^{+} + 2e^{-}$	$+0,00$
CATHODE	O_2 reduction	$O_2 + 4e^{-} \leftrightarrow 2O^{2-}$	$+1,229$
CELL	**Formation of H_2O**	$\boldsymbol{O_2 + 2H_2 \leftrightarrow 2H_2O}$	$\boldsymbol{+1,229}$

It is important to notice here that the Nernst expression *(I.1)* only describes the system under equilibrium conditions, i.e. without current flow through the device (open circuit voltage, OCV). In practice, the real voltage (V) measured on a FC is lower than the standard cell potential due to several accumulative irreversible losses associated to different physical-chemical factors appeared under operation. Three major losses have been found on a FC under load, depending on the current flowing through the device: (i.) *activation losses* when low current is flowing through the cell due to activation of the electrochemical reaction (specially significant in low-temperature FCs), (ii.) *ohmic losses*, increasing linearly with the current flow due to ionic and electronic conduction and (iii.) *concentration losses*, appeared when too much current is flowing through the cell, due to mass transport and fuel delivery limitations. This way, the actual voltage V under load would be determined by,

$$V = E_{FC} - \eta_{act} - \eta_{ohm} - \eta_{con} \qquad (I.3)$$

where η_{act}, η_{ohm} and η_{con} correspond to the activation, ohmic and concentration losses respectively. As shown in Figure I-4, the three losses are reflected on different regions when performing an Intensity-Voltage (I-V) curve (voltage variation with increasing current density). Therefore, they and have a direct correlation with the power output of the FC ($P = I \cdot V$) and minimising them is of fundamental importance when optimising any FC device.

[3] The ideal standard potential for a fuel cell in which H_2 and O_2 react is $1.229V$ with liquid water product, but $1.18V$ with gaseous water product. It is important to notice here that E_{FC} also varies with temperature, therefore on high temperature fuel cells the ideal potential is lowered ($\sim 1.0 - 1.1V$ expected at $400 - 800$°C) [15].

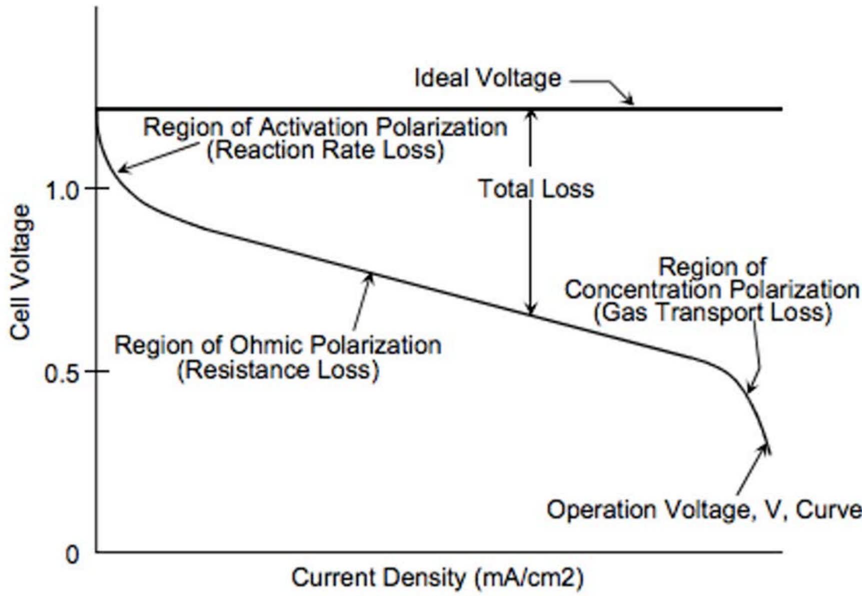

Figure I-4. *Characteristic I-V curve showing the ideal and actual fuel cell voltage (extracted from [15]).*

Fuel cell types

Fuel cells are usually classified according to their specific electrolyte material and/or their associated mobile ions going through it under electrochemical operation. Table I-2 summarizes the main types of fuel cells, listed comparing their main features i.e. electrolyte material, mobile ion, compatible fuels and typical operating temperature. In this sense, it is important to point out the large temperature range of operation, according to the corresponding electrolyte material of each cell, i.e. from almost room temperature for the proton exchange membrane FC (PEMFC) up to $1000℃$ in the case of solid oxide FC (SOFC). The specific operating temperature plays an important role in dictating the type of fuel that can be used in each fuel cell. Thus, for fuel cells requiring high operating temperatures (as it is the case for SOFC and Molten Carbonate FC (MCFC)), it is possible to feed the FC with a wider variety of fuels including many hydrocarbons (internal reforming into hydrogen). On the contrary, fuel cells working at lower temperatures (PEMFC, Alkaline FC (AFC) and Phosphoric Acid FC (PAFC)) are limited to the use of hydrogen as fuel, with the exception of a particular type of PEMFC that allows the use of methanol too (Direct Methanol FC (DMFC)).

Table I-2. *Summary of main features on different fuel cell types.*

FC type	Electrolyte material	Mobile ion	Fuel compatibility	Typical operating temperature (ºC)
PEMFC	Hydrated polymer	H^+	H_2, methanol	$30 - 100$
AFC	KOH solution	OH^-	H_2	$50 - 200$
PAFC	H_3PO_4 soaked in a matrix	H^+	H_2	200
MCFC	$(Li,K)_2CO_3$ in $LiAlO_2$	CO_3^-	H_2, CH_4	650
SOFC	Ceramic	O^{2-}	H_2, hydrocarbons	$700 - 1000$

I.2.2. Miniaturization requirements for portable applications

The following list summarizes the main requirements for a successful and efficient miniaturization of FCs:

- **High energy density per unit mass and volume**. High the energy densities are required if smaller and lighter devices are to be fabricated. Figure I-5 shows a comparison of the specific energy density per volume (Wh/cm^3) and mass (Wh/kg) of different batteries and micro FC [16]. Taking the state-of-the-art Li-ion batteries as a reference, the target values for energy density per unit mass and unit volume are thereby ascribed to $300-500\ Wh/cm^3$ and $200-500\,Wh/kg$.
- **Quick start-up and low power consumption**. In this sense, lower operating temperatures and/or reduced device thermal masses benefit for the overall FC efficiency, as less energy would be devoted to the starting process. Start-up times of seconds and power consumptions of mW are targeted.
- **Easy fuel handling and availability**. The use of pressurized fuels (such as hydrogen) is not recommended due to security reasons. In this sense, liquid fuels such as hydrocarbons or methanol are preferred.
- **Low fabrication costs and scalability**. The possibility of batch mode fabrication is crucial for cost reduction. If the FC fabrication process is silicon-integrated, a huge batch of techniques and processes are available for fabricating hundreds of micro devices in parallel with high reproducibility [17].

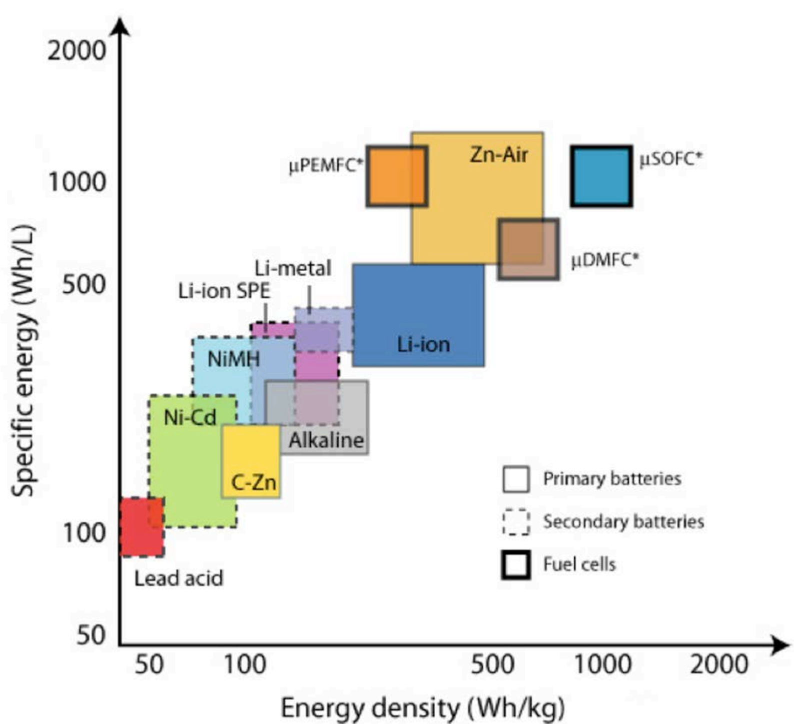

Figure I-5. *Specific energy and energy density of several portable energy sources, extracted from [3,16]. * indicates estimated values as still under development.*

Figure I-5 already shows the potential of micro FC (micro PEMFC, micro DMFC and micro SOFC) in terms of energy density, as presenting higher potential energy densities than state-of-the-art commercial batteries (up to a factor $x5$ compared to Li-ion batteries). In particular, micro SOFC presents the highest values of specific energy densities among micro FC prototypes. This is mainly related to their capability of operating with different types of fuels. Being hydrogen or methanol the only fuels borne by other low temperature FCs, the lower packaging density of such fuels compared to hydrocarbons as propane or butane ($x8$ and $x3$ in energy density by mass [18]) make hydrocarbons-fuelled micro SOFC preferable. In addition, the direct use of hydrocarbons is much more attractive for a rapid implementation of micro SOFC in the real market, as a worldwide distribution net for those liquid fuels already exists (i.e. lighter cartridge, camping gas...), opposite to hydrogen or methanol (not yet established).

On the contrary, major micro SOFC drawbacks are associated to its elevated operating temperature, which could involve slow start-up and high power consumption. On the contrary, micro PEMFC are capable of working at almost room temperature, thus facilitating the start-up process. Probably because of this, first commercial prototypes using micro FC technology (from *Toshiba*, *Medis*, *Horizon*, etc) have been based on PEMFC fuelled with methanol (DMFC). On the other hand, the first system based on micro SOFC technology is not yet commercially available. Indeed, it has been announced for this year by *Nectar Mobile Power* *TM* (INTEL-MIT joint company) [19].

Being still uncertain the acceptance of *Nectar*'s prototype, the micro DMFC-based systems have not been yet a commercial success. This is mainly due to the low specific energy of the whole device after accumulation of different loss sources. Table I-3 shows a comparison of the specific energy density (per mass and volume) of one of these devices taken as a reference (*Toshiba Dynario*) with typical values provided by Li-ion batteries (values of efficiency for micro FCs were extracted from [5]) and expected values for fuels and micro FCs. The table clearly shows that the low efficiency reached by the commercial micro FC, i.e. less than 1% compared to methanol specific energy density [18] and 10% compared to micro DMFC perspectives, drastically lowers the micro FC performance even much below the battery specifications. On the contrary, in the case of micro SOFC-based systems, *Nectar*'s first prototype presents final energy densities comparable to state-of-the-art batteries (values of final energy density are extracted here from reports prior to commercialization [5]). However, there is still a wide range for optimization. Values of final energy density still represents only a 4% compared to propane specific energy density [18] while 25% with respect to micro SOFC perspectives.

Table I-3. *A comparison on specific energy density of micro FC prototypes [5,18].*

	Specific energy density per mass (Wh/kg)	Specific energy density per volume (Wh/L)
Li-ion batteries	$190-220$	$250-700$
Methanol (fuel)	5500	4300
Micro DMFC (perspectives)	500	600
Toshiba Dynario DMFC	30	50
Propane (fuel)	13800	7000
Micro SOFC (perspectives)	1000	1000
Nectar SOFC	240	270

I.3. Micro Solid Oxide Fuel Cells

Despite SOFC technology has been highly investigated and developed since decades ago and bulk SOFC devices are already commercialized and implemented for power supplying big plants like hospitals, industries or other buildings (for example, the Bloom Box from *Bloom Energy* [20]), micro SOFC have recently entered in the research scene. First publications on the topic appeared less than 10 years ago in the US (2004, Tuller and co-workers from MIT [21,22]) and Europe (2005, Gauckler's group at ETH Zurich [10]), mainly focused on the concept, device design and main development strategies.

Apart from MIT [21-26] and ETH [10,16,18,27-37], Stanford University (Prinz's group, [38-43]), IMB-CNM and IREC (Tarancón and co-workers, through this thesis and [44-46]), KIST (Son's group [47]) or Harvard University (Ramanathan and co-workers, [48-63]) have reported very promising results of micro SOFC prototypes working on the IT regime.

I.3.1. Micro SOFC concept

SOFCs are differentiated from other types of FCs by the use of ceramics as electrolyte material. State-of-the-art electrolytes, usually complex-oxide ceramics, present O^{2-} conductivity while remaining electrically isolating. These oxide-ionic conductors usually require high temperatures for reaching high enough ionic conductivity. Standard bulk SOFC systems, which conventionally use components of several mm to $20\ \mu m$ thick, usually work at very high temperatures (> 800°C), in order to keep the overall ohmic resistance of the electrolyte low. In micro SOFC, however, all components (electrode-electrolyte-electrode and current collectors) are fabricated in the form of thin films (tens to hundreds of nm thick), which drastically reduces the electrolyte-associated resistance and permits operate at lower temperatures compared to bulk SOFCs.

The most extended design for micro SOFC devices is shown in Figure I-6, and is based on the fabrication of accessible thin free-standing membranes of the functional layers, i.e. a thin electrolyte film covered by an anode and a cathode one at each side (electrodes), supported on silicon-based microfabricated platforms. This way, by fabricating thin film self-supported membranes, a double purpose is covered:

- Electrolyte thickness is significantly reduced, lowering its associated resistance losses and allowing operating at lower temperatures. When using electrolyte films $< 1\ \mu m$, R can be lowered by a factor of $x10^3$ compared to standard bulk SOFC. Thereby, the operating temperature can be decreased to a Low-to-Intermediate Temperature (LT-IT) regime ($400 - 800$°C).
- Integration of micro SOFCs on Si by Micro Electro-Mechanical Systems (MEMS) technology allows the fabrication of low thermal mass structures. The total active mass of the fuel cell, i.e. the free-standing membrane, is minimized and the thermal response time is consequently reduced. This is extremely important for reaching fast start-up processes with low power consumptions. Micro SOFC based on thin film free-standing membranes can reduce the power consumption by a factor of $x10^6$ compared to standard bulk systems.

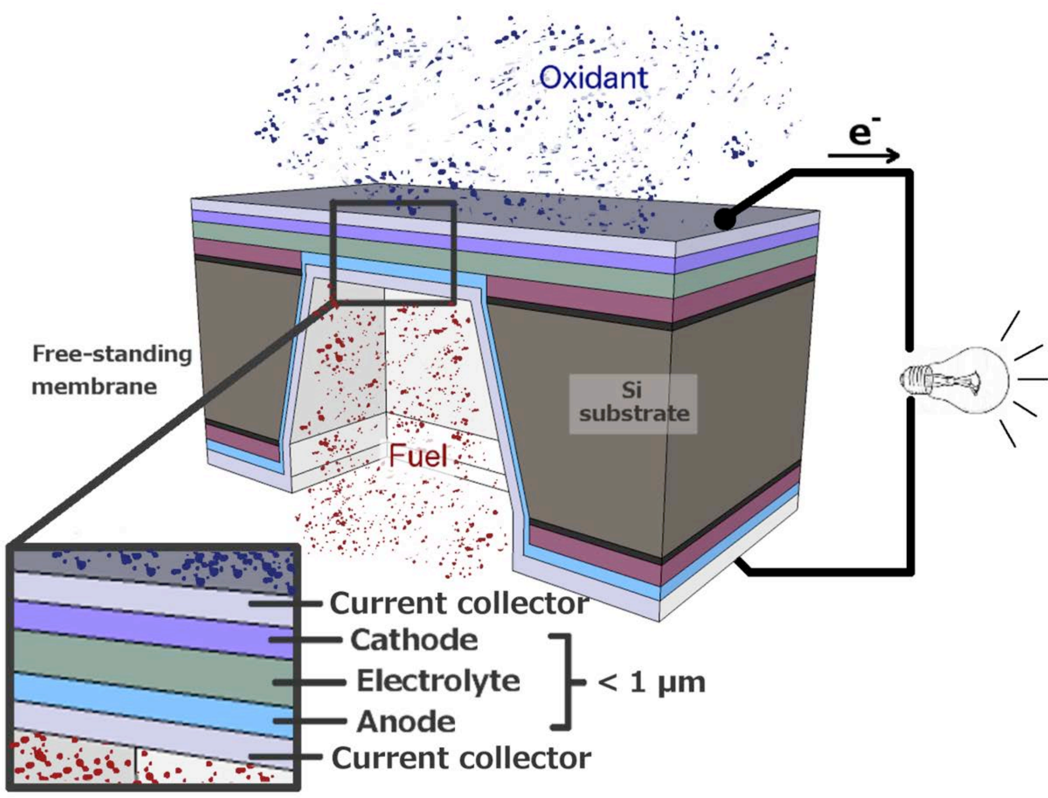

Figure I-6. *Schematic view of a micro SOFC.*

I.3.2. State-of-the-art in micro SOFC

Thin film electrolytes

The main requirements ascribed to an electrolyte in micro SOFC are:

- Sufficiently high **O^{2-} conduction** when heated up to operating temperature[4]. This specific temperature will depend on the electrolyte dimensions, i.e. thickness and active area[5]. Therefore, one of the main goals on the development of micro SOFCs has been the reduction of the electrolyte thickness, in order to operate at lower temperatures than those required for bulk SOFC. Additionally, the reduction of the grain size on the electrolyte film to the nm-level has been proposed for reducing the electrolyte-associated resistance losses [38,65,66].
- **High density and homogeneity**. The obtaining of a high quality film (i.e. without cracks and/or pinholes) is basic for avoiding (i.) electrical contact between the two electrodes, which would short-circuit the cell, and (ii.) gas leakages between both sides that would reduce the fuel cell electrochemical performance (electrolyte must be gas-tight).

The state-of-the-art material used as electrolyte in bulk SOFC and micro SOFC is the yttria-stabilized zirconia (YSZ). Zirconia is doped with different yttria percentages (from 3 to 10%) in order to increase its ionic conductivity, being the most common the fully-stabilized (cubic structure) 8% Y_2O_3 - 92% ZrO_2 (8YSZ). 8YSZ provides the highest ionic conductivity among YSZs, while exhibiting negligible electronic conductivity up to 1500°C [67]. In addition, YSZ offers matching secondary requirements such as chemical stability with other SOFC components or durability and good high-temperature mechanical properties [68]. Some of the most important physical features of 8YSZ are listed in Table I-4 [69-71].

Table I-4. *Physical properties of 8YSZ.*

Property	Value
Melting temperature	2750°C
Conductivity at 1000°C	$0.1\ S/cm$
Conductivity at 600°C	$1 \cdot 10^{-2}\ S/cm$
Dielectric constant	26
Density	$5.9\ g/cm^3$
Young modulus (25°C)	$210\ GPa$
Thermal Expansion Coefficient $(20 - 1500°C)$	$10.23 \cdot 10^{-6}\ cm/cm\,K^{-1}$
Thermal diffusivity	$0.89\ mm^2/s$
Specific heat (25°C)	$0.47\ J/(g \cdot K)$

[4] In pure ionic conductors, conductivity follows an Arrhenius-type dependence with temperature,

$$\sigma = k \cdot e^{-E_a/RT}$$

where σ is the conductivity, k a constant, E_a the activation energy of the process, R the universal gas constant and T the temperature.

[5] The conductivity is defined as follows:

$$\sigma = \frac{1}{R} \cdot \frac{t}{A}\ (S/cm)$$

where R is the resistance associated to the electrolyte and t and A its thickness and area, respectively.

Normalized resistance values associated to the electrolyte (also used for the electrodes) are usually expressed as Area Specific Resistance (ASR), i.e. the resistance normalized to the functional area. Typical target values for either the electrolyte or each one of the electrodes are $ASR = 0.15\ \Omega \cdot cm^2$ [64].

The use of thin film deposition techniques allows fabricating high-quality films i.e. without defects (cracks, holes...) of several hundreds of nm, being ideal for the implementation of thin film YSZ electrolytes onto free-standing membranes-based micro SOFC systems. Many works have been published up to now on the deposition of thin YSZ films, showing the feasibility of fabricating YSZ films by different (physical and chemical) vapour deposition techniques, i.e. pulsed laser deposition, sputtering, chemical vapour deposition or atomic layer deposition [39,72-79].

Electrodes

The electrodes for micro SOFC are also needed in the form of thin film in order to ensure good mechanical stability of the free-standing membranes and maintain the low thermal-mass structure. The main functional requirements for an electrode in micro SOFC are:

- Good **structural and chemical compatibility** with the electrolyte and the rest of components of the micro SOFC (substrate, current collectors).
- Enough **electronic conductivity** for collecting the electrodes released on the redox reactions.
- High enough **Triple Phase Boundary (TPB) length**. On a certain electrode, redox reactions will only take place on the specific zones (TPBs) where all the needed reactants co-exist, i.e. oxide ions (O^{2-}), electrons (e^-) and fuel/oxidant (depending on the anode or the cathode). Figure I-7 shows a cross-sectional scheme of an electrode-electrolyte bi-layer, pointing out the TPB area and co-existence of species.

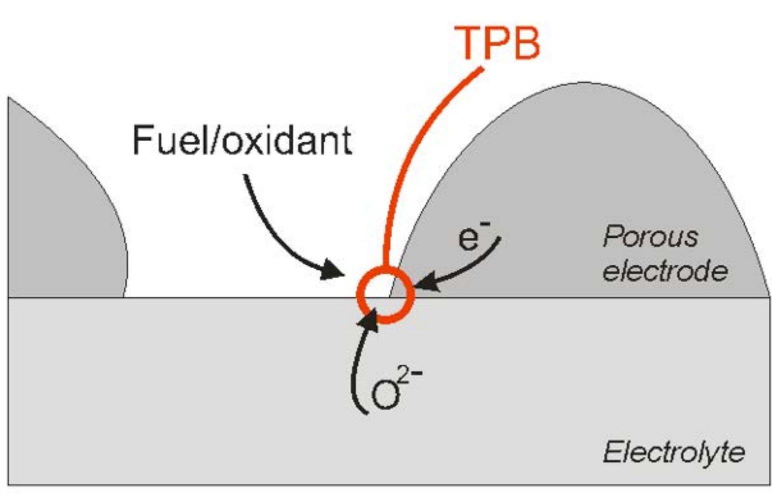

Figure I-7. *Scheme of electrode-electrolyte interfaces and TPB.*

The microstructure of the electrode is therefore of extreme importance for reaching good electrode capabilities. An electrode will be microstructural-optimized as long as its TPB length is enlarged while maintaining good interconnection within the electrolyte and enough electrical conductivity (for current collection). In this sense, the main objectives for the fabrication of effective thin film electrodes are obtaining highly porous but still continuous films, while maintaining good thermal stability (no degradation within operating temperatures).

First published results on micro SOFC incorporated thin metallic films as electrodes (mainly Pt, both as anode and cathode). Thin metallic films suffer dewetting with temperature, thus permitting (if well-controlled) the fabrication of porous networks with very high TPB length. Alternatively, in order to enlarge even more the TPB length, Mixed Ionic Electronic Conductors (MIEC) can be also implemented as electrodes. The combined ionic and electronic conductivity of these materials permits enlarging the TPB

length (not any more restricted to the electrode/electrolyte interface but extended to the whole electrode area). Less investigated than metallic electrodes and barely implemented onto micro SOFC configurations, these materials have been deeply studied in bulk SOFC (metallic electrodes are unstable at such high temperatures). First approximations on the scalability to thin film are being currently addressed presenting them as a very promising alternative for micro SOFC electrodes.

Current collectors

Micro SOFC systems usually require the implementation of current collectors for reducing the overall resistance associated to the electrodes, especially if moving to thin film MIECs. Although high values of conductivity can be reached on these films (hundreds of S/cm), their in-plane associated resistance is usually too high due to nanometric thickness scale, becoming a major source of resistance losses. For example, assuming a conductivity of $200\ S/cm$ for the electrode and a thickness of $250\,nm$, the approximate resistance associated to the in-plane electronic collection would be in the order of hundreds of ohms[6]. With this value of series resistance, the overall performance of the micro SOFC would be extremely lowered. Taking into account the target area specific resistance (ASR) values typically ascribed to micro SOFC ($0.15\ \Omega cm^2$ for each functional layer, $< 0.5\ \Omega \cdot cm^2$ for the whole cell [64]) and the typical functional areas ($< 1mm^2$), the total resistance should be ideally less than 50Ω. Therefore, current collectors must be implemented on the micro SOFC design in order to reduce this in-plane resistance and ensure a good collection of the electrons formed in the reaction.

Current collectors in micro SOFC are usually made of patterned "micro"-porous (several μm in size) metallic films, deposited over the electrodes in both sides of the membranes [58,80]. Compared to thin film metallic-based electrodes, current collectors are based on dense and thicker ($> 100\ nm$) films, for ensuring good thermal stability under micro SOFC operating conditions (avoid thermal dewetting). Being fully dense, the area covered by them is catalytically inactive (no TPB), thus being confined to only the pores present on the collecting grid. The main objective when fabricating current collectors is reaching an effective compromise between losses of active area (the higher the porosity, the larger the active area) and sufficiently low pore size (minimize the in-plane percolation length through the less-conductive electrode).

Micro-fabricated platforms as substrates

The use of silicon as supporting material for micro SOFC has been found to be very convenient as it is widely used in Micro Electro Mechanical Systems (MEMS) technology. The wide and well-known series of techniques already developed for Si micromachining allows the fabrication of complex and optimized micro SOFC designs [24]. In particular, by different consecutive etching and/or film deposition processes, Si micromachining permits creating the functional membranes accessible from both sides of a bulky substrate, which is then much easy to handle. A proper fuel delivery directly to the membrane is therefore ensured and easy encapsulation is permitted.

It is important to notice here that, although Si is the most widely used substrate material among the micro SOFC community, some alternative materials have also been tested. In particular, there exist several reports on the use of glass-based materials (*Foturan*) [32], or the use of metallic-based supports (nickel plates) [81] for micro SOFC.

---

[6] Reference values were taken as measured in this work for porous $La_{0.6}Sr_{0.4}CoO_{3-\delta}$ films deposited by PLD. Details on *Chapter V*.
Simple calculations were carried out by using $\sigma = 1/R \cdot l/A$, where $A = l \cdot t$ and thus $R = 1/(\sigma \cdot t)$ for the in-plane associated resistance calculation.
(σ: in-plane conductivity, R: associated resistance, t: film thickness)

Device performance

A wide variety of micro SOFC performances (power density) have been reported by different research groups, depending on the specific materials chosen as electrodes and measuring conditions. The highest power density have been published by Kerman et al. [53], who recently reported $1037\ mW/cm^2$ on a free-standing Pt/YSZ/Pt membrane supported on silicon. Up to now, the complete series of published results use metallic electrodes as either anode, cathode, or both (symmetrical micro SOFC). However, as recently reported by Ramanathan et al. [53,58,61], the low stability of those electrodes under micro SOFC operating conditions still hinders the way for further optimization of this device.

A complete review of the state-of-the-art on micro SOFC device performance is given on *Chapter VII*, where they are compared to the performance of the micro SOFC developed in the present thesis.

I.3.3. Key aspects for further optimization of micro SOFCs

Three main aspects are currently considered for further optimization of micro SOFC systems:

- **Increasing maximum power achievable per single device**. Several investigations have dealt with the optimization of membrane-based micro SOFC designs. In this sense, main concerns were placed on enlarging the maximum free-standing membrane area (active area of the fuel cell), which can be directly extrapolated to a higher total power per single device. Two main membrane optimization alternatives have been reported up to now, namely the development of (i.) corrugated or (ii.) large-area membranes. First, Su et al. [40] published a very promising work on the fabrication of corrugated membranes, through which the authors were able to increase the surface utilization by 30% to 64% (respect to the projected area) and obtained a maximum power density of $861\ \mathrm{mW/cm^2}$ at $450°\mathrm{C}$, with a total power of $3.10\ \mathrm{mW}$ per single micro SOFC. More recently, Chao et al. [42] also published a similar work reporting corrugated membranes with a maximum power density of $820\ \mathrm{W/cm^2}$ and a total power at $500°\mathrm{C}$ of $134\ \mu\mathrm{W}$.

  The second alternative consists of the fabrication of large-area membranes [43,58,80]. In this sense, a few works have been reported the use of dense grids as support for larger free-standing areas. Using a Nickel grid, Tsuchiya et al. [58] reported area enhancements up to $\sim 200\mathrm{x}$ over previous results and a total power output from a single membrane of $21.1\ \mathrm{mW}$ at $500°\mathrm{C}$ ($7x$ versus best Su's result). Su et al. [43] has also recently reported the fabrication of "nanoscale membrane electrolyte arrays", this time supported on a silicon grid achieved by controlled etching of the silicon substrate. In that work, they reached a peak power of $2.98\ \mathrm{mW}$ at $450°\mathrm{C}$ with a single membrane.

  Within this scenario, a new alternative for fabricating large-area membranes never used before in micro SOFC is presented in this thesis, based on the use of doped silicon slabs as robust support for the large-area membranes.

- **Fabricating stable thin film electrolytes in the whole micro SOFC operating system**. Identified as the main problem on high temperature SOFC, main efforts among the micro SOFC community (also including part of this thesis work) were firstly placed on reducing the electrolyte-associated ohmic resistance and understanding the interplay of nano-grained microstructure and ionic transport. Significant developments have been already made in the optimization of thin film electrolyte membranes, showing the potential of micro SOFC for working at temperatures below 500°C [16,46,58]. Free-standing membranes of YSZ were satisfactorily fabricated on silicon-based bulky substrates [32,44]. In this sense, the present work contributed to the development of YSZ electrolytic membranes thermo-mechanically stable on a wide range of operating temperatures (up to $800°\mathrm{C}$) for being used as micro

SOFC electrolytes, either on basic (smaller) squared membrane designs or on the lastly developed large-area membranes.

• **Developing durable electrodes compatible with the micro SOFC configuration**. As already commented, micro SOFC systems reported up to now are based on the use of thermally instable metals as electrodes (degradation with time reported by [53,58,61,82-84], and also observed in this work - see *Appendix B*). Therefore, further research is needed for fabricating reliable micro SOFC systems (stable with time under operating conditions). This entails the fabrication of more effective electrodes, including development of new materials and understanding of their structure-transport properties, reducing operating temperature while maintaining enough internal hydrocarbon reforming and diffusion kinetics, and reducing electrode-electrolyte interfacial losses.

This thesis contributes to the state-of-the-art on micro SOFC by fabricating ceramic-based thin film electrodes and implementing them on micro SOFC configurations. First results on full ceramic-based micro SOFCs are presented here, opening new insights for more reliable power supply systems based on micro SOFC technology.

I.4. Scope of the thesis

I.4.1. Frame of the thesis

This thesis is encompassed on three different projects, namely µ-Pila ("Development of monolithical micro fuel cells based on silicon technology") and MICAELA ("Microtechnology-based fuel cells for ambient intelligence and low power applications") projects at IMB-CNM, and Power Pack project ("High Energy Density (Bio)Ethanol-Fuelled Power Source for Consumer Electronics Applications and Microsystems") at IREC.

The first two projects were devoted to the integration of micro SOFC (and other types of micro FC) into silicon technology. This included the cell design optimization and integration of the different functional materials onto the micro-fabrication process. On the other hand, the Power Pack project addressed all the challenges related to the integration of a complete power generator in which the micro SOFC developed in this thesis will represent the central part of the system (see Figure I-8). In this sense, the project also dealt with a gas processing unit (that includes a micro-reformer of (bio)ethanol), the thermal management system and the packaging and encapsulation. Current research is being devoted at IREC to the fabrication and testing of these additional components integrated on silicon and compatible with the micro SOFC system presented here.

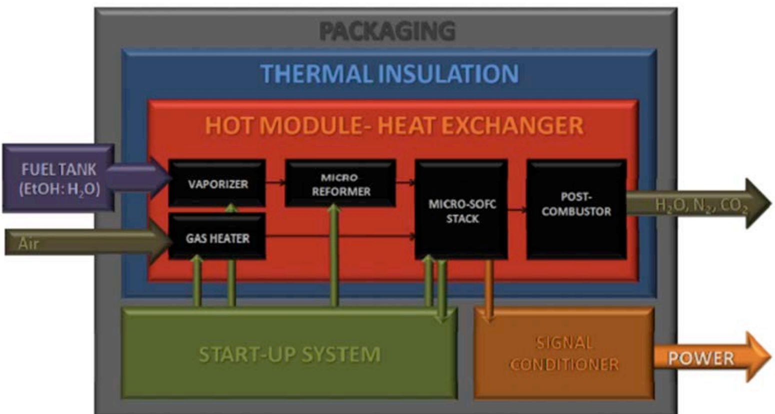

Figure I-8. *Basic scheme of the POWER PACK system.*

I.4.2. Outline of the thesis

The present thesis describes the development of a micro SOFC integrated on silicon, work carried out on the IMB-CNM (CSIC) and IREC. The thesis is fully encompassed in the current state-of-the-art of micro SOFC, and covers the key aspects identified for further optimization of the device (see *Section I.3.3*). Therefore, it increases the background in micro SOFC technology concerning new design concepts, optimized electrolytes and new perspectives on thin film electrodes. The thesis is organized as described in the following. Additionally, Figure I-9 shows a schematic outline of the thesis, reflecting that all aspects relating to the fabrication of micro SOFC systems have been assessed in this work.

- ***Chapter II*** is devoted to describe technological aspects concerning micro SOFC. The different fabrication and characterization techniques utilized during the thesis for the development of this work will be briefly described here.
- ***Chapter III*** describes the design and fabrication of micro SOFC systems. Here, the two designing strategies carried out in this thesis for the fabrication of free-standing membranes can be found (including the innovative large-area membrane design), as well as a detailed description of the microfabrication process yielding to functional membranes. Moreover, the fabrication of effective current collectors implementable on free-standing membranes is also described.
- The three following chapters are devoted to the description of each functional layer of the micro SOFC:
  - ***Chapter IV*** presents an extensive study of the thermo-mechanical stability and electrochemical properties of YSZ membranes to be used as micro SOFC electrolytes.
  - ***Chapter V*** describes the fabrication and characterization of porous $La_{0.6}Sr_{0.4}CoO_{3-\delta}$ (LSC) films as micro SOFC cathodes.
  - ***Chapter VI*** depicts a similar study but focused on porous $Ce_{0.8}Gd_{0.2}O_{1.9-\delta}$ (CGO)-based films as micro SOFC anodes.
- Finally, ***Chapter VII*** presents the micro SOFC performance by using all the functional layers described in previous chapters.
- Two additional appendixes are included in this thesis, in order to describe specific studies carried out to complement the previously presented work:
  - ***Appendix A*** presents a strategy developed for obtaining pinhole-free electrolytic membranes, thus solving one of the major source of failures on functional micro SOFC systems.
  - ***Appendix B*** shows the series of tests performed for the development of thin film metallic electrodes, which in the end were found to be inappropriate for fabricating reliable micro SOFC systems (unstable during operation conditions).

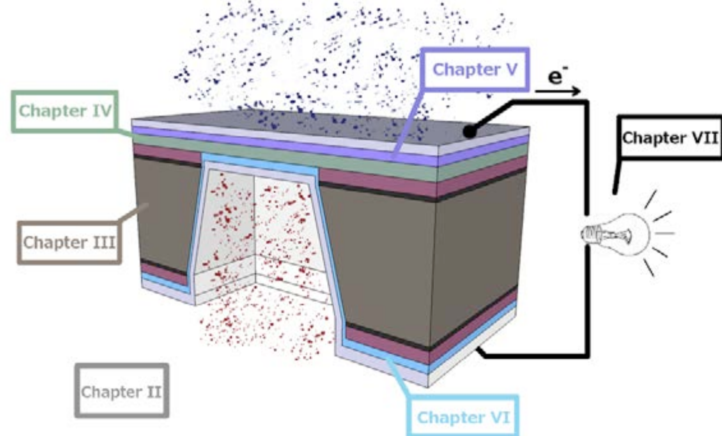

Figure I-9. *Schematic outline of the thesis*

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II.1. Introduction

Fabrication of a micro solid oxide fuel cell (micro SOFC) requires the integration of two different technological approaches into a single process, i.e. **the compatibility of micro fabrication and SOFC technologies**. Firstly, developing a micro fuel cell implies the use of tools from the micro fabrication field. The functional components of the micro SOFC are prepared by thin film deposition techniques, thus reducing as much as needed electrode and electrolyte thicknesses; physical and chemical etchings are used for micromachining the device for obtaining free-standing membranes; even the characterization is completely different from that used in conventional fuel cells due to the reduced size of the system to be analyzed. Meanwhile, on the other side the micro fuel cell is indeed a solid oxide fuel cell, meaning that will be based on the same reaction paths and processes than a conventional SOFC. In order to fulfill the basic requirements of a SOFC, the materials used here are similar than those used on conventional ones, whose mechanical properties and micromachining capabilities are actually far away from the typical materials used in micro fabrication [1, 2]. Therefore, one of the first and most important barriers that had to be overcome in this thesis was to ensure the compatibility between typical SOFC materials and needed micro fabrication steps and processes, since in many senses a micro SOFC is a totally different device than a conventional SOFC.

The aim of this chapter is then to give a general view of the specific series of techniques and processes required for the fabrication of a micro SOFC, paying special attention on the functional layers fabrication in thin film form. It will be then used as basic background for a better understanding of the following chapters, where the different techniques are explicitly applied and the obtained results are shown.

It has been already shown in *Chapter I* the most extended micro SOFC design, based on free-standing functional membranes supported on silicon micro platforms [3-12]. By reducing the electrolyte thickness and its implementation into low thermal mass structures, it is possible to operate at a lower temperatures than standard bulk SOFCs, also reducing the start-up time [13-19]. Compared to a conventional self-supported SOFC a new element appears in this configuration, the supporting silicon micro platform used as substrate; and it has to be considered in terms of fabrication and materials compatibility. In this sense, ***section II.2*** of this chapter is devoted to the description of silicon micro fabrication technology, and the main micro fabrication processes involved in this work for the fabrication of this supporting platform.

The functional part of the device, i.e. the self-supported membrane, includes the electrolyte and the electrodes in thin film form. Many research studies have shown the applicability of complex solid oxides in SOFC technology, either as electrolytes or electrodes. For this work, classical SOFC materials were used, i. e. yttria-stabilized zirconia (YSZ) was the chosen electrolyte while $La_{0.6}Sr_{0.4}CoO_{3-\delta}$ (LSC) and $Ce_{0.8}Gd_{0.2}O_{1.9-\delta}$ (CGO) were considered for ceramic electrodes. The applicability of these materials on a micro SOFC depends on many factors, such as their behavior at the lower working temperatures used, and of course the possibility of depositing them in thin film form. The main requirement for the correct thin film growth of such complex oxides is a good transferability of the stoichiometry from the bulk material (target) to the growing film. In this sense, Pulsed Laser Deposition (PLD) has been proven to be highly effective since allows excellent stoichiometric transferability from a target material to the substrate [20]. The technique has been successfully used for depositing a large amount of complex polycrystalline oxides, including the functional layers used in this work [21-28]. In this chapter, a complete description of the PLD technique and the deposition conditions used for each material can be found on ***Section II.3***.

It is important to notice here that, as pointed out in *Chapter I*, thin film Ot was also tested as electrodes in micro SOFC configurations. In this particular case, a more standard micro fabrication deposition technique such as sputtering was used and is therefore described on *Section II.2.2 – film deposition* as a common technique on silicon micro fabrication technology).

Additionally, a big effort was placed on the scalability of the whole fabrication process to large-area substrates (i.e. 4" wafer level). In particular deposition of functional layers by PLD was especially challenging. Usually limited to substrate areas as big as $2x2\ cm^2$, the possibility of fabricating high quality functional films over larger areas ($10x10\ cm^2$) represents a big improvement for a batch fabrication and cost reduction, allowing the integration of PLD into a wafer level micro fabrication flow. ***Section II.3.3*** of this chapter is dedicated to describe the large-area PLD process used in this work.

Finally, in the last part of the chapter (***Section II.4***) there is a brief description of all the characterization techniques used for the study of the micro SOFC. Chosen Si for its easy micro machining capabilities, and the functional thin films for their good performance as functional materials, their mechanical properties were however quite far away [1], what made the study of mechanical and thermo-mechanical issues such as stress compensation to avoid fractures very important (see ***section II.4.2***). At the same time, the study of electrochemical performance of each component of the micro SOFC, as well as the micro fuel cell performance as a whole was the last and most important step to prove the functionality of the fabricated device (***section II.4.3***).

II.2. Silicon micro fabrication technology

II.2.1. MEMS fabrication

Micro electromechanical systems (MEMS) allude to small integrated devices that combine electrical and mechanical components. Any system capable of sensing, controlling or activating mechanical processes on the micro scale, thought to generate effects on the macro scale can be classified as a MEMS, i.e. a micro SOFC [29, 30].

Two main objectives are pursued on MEMS development, **miniaturization and multiplicity**. From the point of view of the final customer, a new device becomes attractive basically if it enables a new function, and/or provides significant cost reduction. By miniaturizing electromechanical systems, new compact and quick-response devices are manufactured, offering to the customer a lighter, easy-handling and, in general, more accessible product. Micro SOFC devices fabricated in this work are thought for its integration on powering systems of a maximum volume of $1\ cm^3$, thinking on their application onto compact portable devices. Because of that, the standard substrate area used in this work for supporting the whole functional components of the device was always of $1\ cm^2$ or less.

On the other side, multiplicity refers to batch fabrication, the capability of fabricating thousands of components simultaneously. This capability allows then a cheap mass production, considerably reducing the manufacturing price and making the product accessible for the customer. That was the reason why integration of micro SOFC fabrication into a batch production process was one of the main concerns in this work, and thus many efforts were put on the scalability of all the steps of the process to large area substrates, to be able to fabricate tens of devices in parallel. Special interest had the deposition of large

area functional layers by PLD, described on *Section II.3.3*, scaling the technique to 4” wafer level, same substrate as the one used on the whole silicon micro fabrication process.

II.2.2. Main micro fabrication processes

Decades of research and development on micro fabrication technology have lead to a huge, well known and precise set of micro fabrication processes. On a typical micro fabrication flow, several of these processes are combined on different steps, finally leading to the device that had been previously designed.

This section is a resumed compilation of the most important processes used on a standard micro fabrication flow, grouped in four major categories: (i.) *lithography*, where a pattern is transferred from a master to a resin covering the silicon wafer; (ii.) *etching*, where an amount of material from the silicon wafer is removed, usually following a pattern defined by a previous lithography; (iii.) *film deposition or growth*, where a new material is added to the silicon wafer; and (iv.) *doping*, where the silicon structure itself is modified by introducing a doping agent on it. All of them are actively used on the fabrication flow for obtaining the silicon based micro platform used in this work as support for the micro SOFC (*Chapter III*).

Lithography

Lithography is a method for defining patterns on a substrate. It is based on the ability of transferring copies from a master where the pattern has been pre-defined to the substrate (wafer) where the functional device is being fabricated. It is used as the first step for afterwards modifying the substrate only on some desired zones by adding, removing, growing or depositing any material. That is why lithography is commonly considered as the basic process on micro fabrication technology.

Nowadays the most extended lithography technique is the one using UV light as developer, thus called photolithography. Alternative lithographies, such as X-Ray or charged beam lithographies appeared in the last decades, looking for a higher resolution, but were not needed for the current application.

The three basic steps concerned on a photolithographic process are (i.) spin coating of a resist, (ii.) exposure through a mask and (iii.) development. A resist (usually a polymer) is first spinned over the silicon wafer covering the whole area with a thin and homogeneous film. This resist is specially chosen for changing its solubility when being irradiated with a radiation source. Then, the coated wafer is irradiated through a mask where the desired pattern has been pre-defined. Finally, the resist is eliminated only from the desired zones (exposed or non-exposed zones, depending on the resist polarity) by dissolving it on the proper solvent. The patterned resist film can be used then as mask for any other process.

There exist two different types of resists, depending on its polarity; *positive* resists, that drastically change to soluble when being irradiated, and *negative* resists, referring to soluble materials that switches to insoluble when being irradiated. All the photolithographic processes carried out in this work used positive resists (standard photolithographic resin). The photolithographic masks were designed as a function of this type of resist. A typical photolithographic mask is made of a UV transparent substrate (glass) covered by an absorber film patterned with the design to be transferred (chromium). Two different kinds of masks can be also distinguished, i.e. *light field* masks where the features appear dark over a light substrate, and *dark field* masks where the features are transparent on a dark substrate. Both types of

masks were used in this work, in different steps of the micro fabrication flow. As an example, Figure II-1 shows the design of a dark field mask used in the fabrication process of a micro SOFC, in particular for patterning the back side of a silicon wafer where the silicon would be etched in order to release free-standing membranes on the opposite side. Yellow zones correspond to the transparent zone on the mask, while black zone is opaque.

In the micro SOFC fabrication flow, photolithography was used several times, either for defining the zones where the silicon was etched or for defining paths where the substrate was going to be doped or modified.

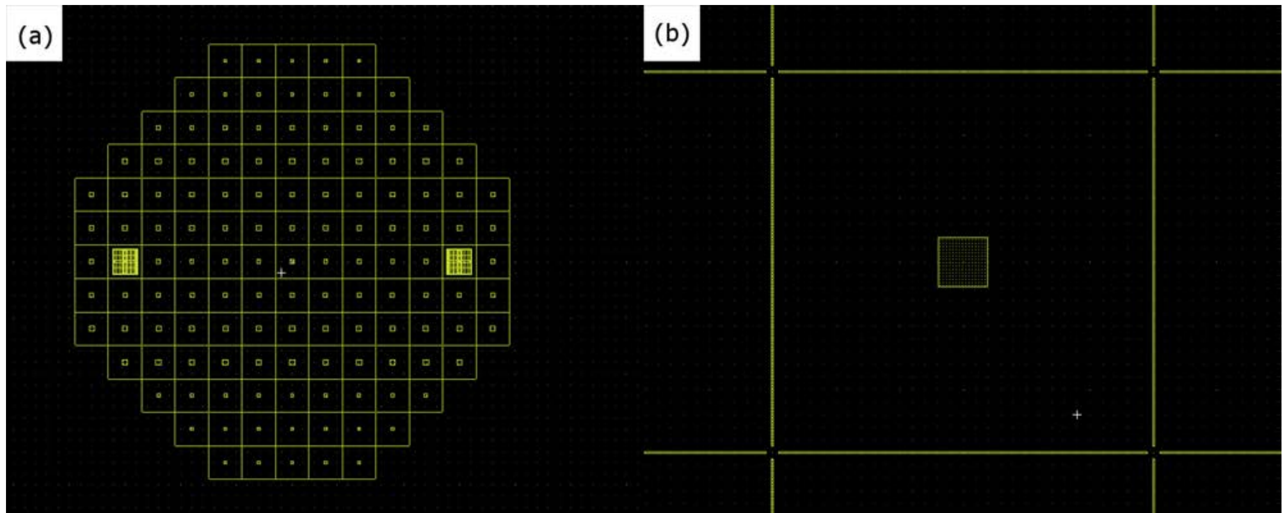

Figure II-1. *Design of a photolithographic mask. (a) General wafer-level view. (b) Detail of one of the designs.*

Etching

After a lithographic step, the pattern copied on the resist can be transferred to the wafer by basically two ways: adding any material on top of it, or removing part of the substrate material from the exposed zones. Etching refers to this second way, the pattern transfer by either chemical or physical removal of solid material from the substrate.

The different ways to etch the substrate wafer are usually grouped into two categories, dry etching and wet etching techniques. Selection of the proper etching technique for a specific process is not arbitrary, as it affects on the shape that is formed (the etching mechanism, which can be either isotropic – similar etch rate in all directions, or anisotropic – different etch rate depending on the direction). At the same time, selectivity of the etching technique must be considered (the difference in etch rate between the mask and the substrate to be etched).

Dry etching techniques

On a dry etching, a solid surface is etched to the gas phase either physically by inert ion bombardment, chemically by a chemical reaction, or both. There are many types of dry etching techniques depending on many factors, but all of them are based on the use of plasma as etchant. During the etching process, areas of high-energy electric and magnetic fields are generated, which rapidly dissociate any gas present on the

chamber forming energetic ions, photons, electrons and highly reactive radicals and molecules. These energetic species are then accelerated to the substrate surface to be etched.

The most common and only *dry etching technique* used in this work was the Reactive Ion Etching (RIE), considered the most complete etching technique as it combines physical and chemical etchings. Two plasma species are therefore used as etchants, i.e. accelerated ions from neutral species (to either modify surface state making it more reactive to the chemically active species or help etched products to desorb) and reactive species (that diffuse to substrate surface to react with the substrate material forming volatile reaction products).

In this work, this technique played a major role on the fabrication flow, as it was used for releasing the electrolyte free-standing membranes by etching the silicon nitride sacrificial layer (see fabrication flow in *Chapter III*). A combination of CHF_3 plus O_2 was used for etching the Si_3N_4 layers, being the products of the reaction SiF_4 plus CO and CO_2. Figure II-2 shows an image of the most frequently used RIE equipment, located at the Clean Room of the Autonomous University of Barcelona. Other RIE machines, placed at IMB-CNM´s Clean Room, were also used in some cases, for some specific purposes.

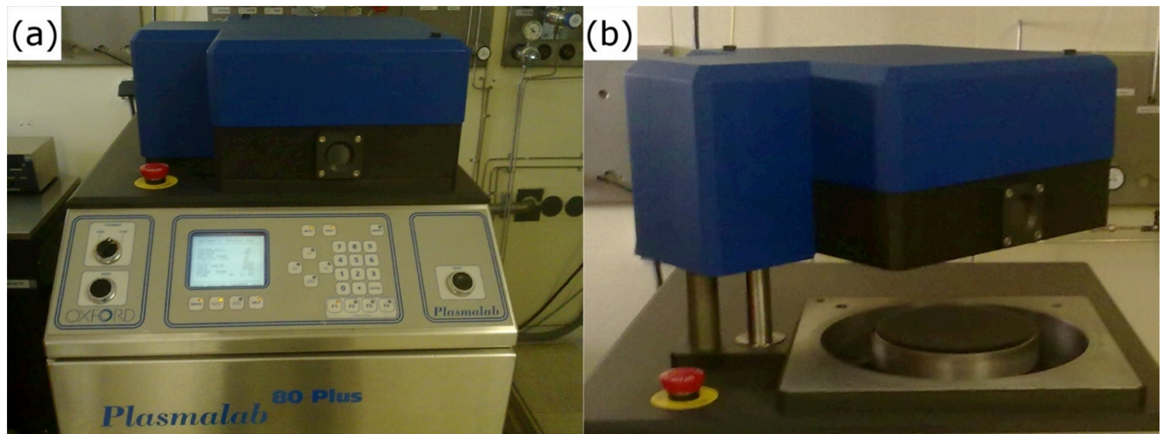

Figure II-2. *(a) Image of the Reactive Ion Etching machine used on the micro SOFC fabrication process. (b) Detail of the etching chamber opened.*

Wet etching techniques

The second alternative for a controlled etching of a substrate consists on the use of chemical solutions for dissolving the material to be etched. No plasma is then needed; the substrate is just immersed on a chemical bath filled with the etching solution. Compared to the dry etching, wet chemical etching provides higher selectivity being often faster. Depending on the etchant and/or substrate material, etching can be orientation-dependent (anisotropic) or orientation-independent (isotropic).

In general, wet anisotropic etching is widely used for machining silicon substrates. Due to its particular and well-known crystal structure, i.e. a diamond type cubic structure, there is a high degree of predictability on the recess features. Silicon orientation plays then here a very important role. When using the typical anisotropic etchant KOH, the (111) planes are not attacked (their etch rate is negligible compared to the other planes). This makes really easy to predict the angle generated on a specific feature being etched. For the most widely used (100)-oriented silicon (the one used for this work), the etching generates sidewalls leaning $54°$ from the vertical. Thus, when etching square features, truncated pyramids are generated, which sidewalls are the (111) planes and the bottom plane is a (100) plane, parallel to the

wafer surface. (110) and (111) oriented silicon wafers are also often used in micro fabrication and they generate different etching structures, but were not used on this work.

The high selectivity provided by wet etching techniques is only ensured if a proper mask is used for a specific etchant. The main requirement to be a good mask for etching is a good resistance and stability during the process, being its etch rate far away from the one of the material to be etched. Typical masks for anisotropic etching of silicon are photo-resists, SiO_2, or the most common one Si_3N_4.

In this work, wet etching of silicon was used for removing the silicon below the self-supported membranes. Square features were defined on the back side of the wafer by etching the silicon nitride layer used as mask, and then the wafer was immersed on KOH solution for $40\ min$. Figure II-3 shows one of the machined substrates from the back side, once etched the silicon substrate. The truncated pyramid can be distinguished, forming the bended planes and the free-standing membranes on the opposite side of the substrate.

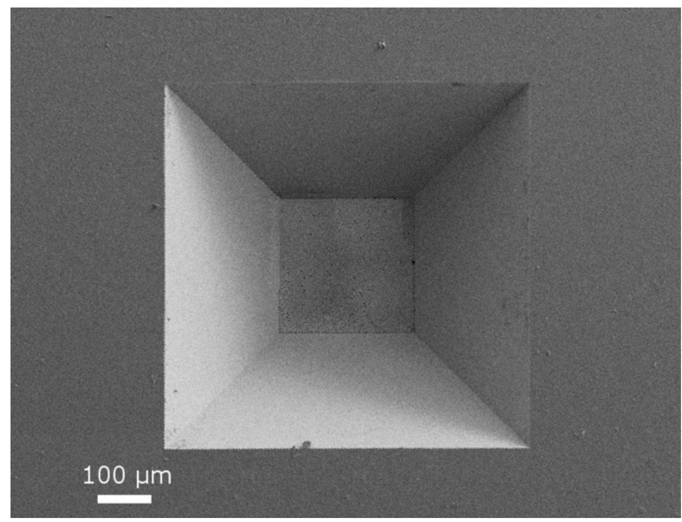

Figure II-3. *SEM top view of a membrane, seen from the back side.*

Film deposition or growth

Thin films can play key roles on the fabrication of any micro device for many different reasons, which can be either chemical or mechanical. For example, depositing an insulating film can be useful for protecting the substrate materials against corrosion. In this sense, film deposition or growth on a silicon wafer encompasses all the techniques where a surface is being modified for a specific purpose, what can be made by basically annealing the substrate material or depositing a new material on its surface. Depending on the application, thicknesses of the grown/deposited films can range between a few tens to hundreds of nanometers.

From a fundamental point of view, there is a basic difference between deposition and growth, although their objectives could be similar. On one side, when growing a film no addition of any material is involved but only a phase change (as for example the oxidation of silicon). On the other side, deposition refers to the act of adding a completely new material over the substrate.

Film growth

On silicon-based microfabrication technology, there is one basic growing process that must be considered: the thermal oxidation of silicon. This process is one of the most required processes on a typical microfabrication flow, as it can be used for insulation, masking, or just as sacrificial layer for any process. The oxidation of silicon takes place when heating the wafer to elevated temperatures. Depending on the chosen temperature (usually ranging between 600 and 1250℃) and the chamber atmosphere (air, or O_2/N_2 mixtures), SiO_2 film properties can be slightly tuned. However, due to the high temperature required and the phase change that takes place on the surface, compressive oxide films are always obtained, generated by the molecular volume mismatch and the different thermal expansion of each material. For this reason, SiO_2 layers are usually combined with tensile Si_3N_4 layers that together form a more relaxed and stable multilayer. The bilayer Si_3N_4/SiO_2 is thermo-mechanically stable and acts as an excellent ionic barrier.

In this work, SiO_2 layers were grown on the two sides of the Si wafers, and worked as insulation layers together with Si_3N_4 layers that were deposited on top of the oxide. 100 nm thick SiO_2 layers were grown on the Si by heating the wafers for 20 min at $950°C$ on a wet oxidant atmosphere.

Film deposition

The process of adding a new material on top of the surface substrate forming a thin film is known as film deposition. Basically any material can be deposited on a thin film form by using one of the multiple deposition techniques available for micro fabrication applications. The deposition technique and conditions of choice will depend on the material itself, the desired film properties and the ability of depositing it with a specific technique.

The film deposition techniques can be grouped into two major categories: physical vapor deposition (PVD) and chemical vapor deposition (CVD) techniques. On one side, in a PVD process no reaction takes place during deposition but only a material is vaporized and directed to the substrate. On the contrary, on a CVD reactor a reaction involving some reactant gases is required to happen just on top of the substrate surface. In any case, either on a PVD or a CVD process, the chosen deposition parameters will be crucial for the final film properties. They will affect on the purity of the films (as a general rule, higher the vacuum, purer the film), crystalline phase (depending on the specific phase diagram of the material being deposited), type of growth (either epitaxial or polycrystalline), strain on the film (that will depend on the deposition temperature, and also on the substrate and thin film material themselves) and any possible shadow effect (depending on the directionality of the deposit).

Among the different PVD techniques, apart from PLD (used for growing most of the functional layers and deeply described on *Section II.3*), sputtering was also actively used in this work. Sputtering is based on the bombardment of a target of the material to be deposited with inert ions (usually Ar^+), from plasma created on the deposition chamber. The target, placed in the cathode plate, is then etched and sputtered away by momentum transfer, and ejected to the substrate which is intentionally placed on the opposite plate of the deposition chamber (anode). This technique is very often used for film deposition in microelectronics, because almost any material can be deposited by it.

In this work, sputtering was the chosen technique for depositing functional metallic films on the fabricated devices. Platinum films of different thicknesses were deposited on a sputtering equipment (Alcatel A610) over PLD deposited electrolytic layers. Dense Pt films were obtained by using a pAr of $0.01\ mbar$, $100\ W$ of power and a RF velocity of $13.6\ MHz$, and the deposition time was varied according to the desired thickness on each case. Their film microstructure and evolution with the temperature are described on *Appendix B* of this thesis.

On the other hand, there also exist different types of CVD techniques depending on the specific conditions used during the process. However, only one, low pressure CVD (LPCVD), was used ***in this work***, for depositing Si_3N_4 layers. In LPCVD, the deposition process is carried out under pressures below $10\ Pa$ allowing a better uniformity on the films and a reduction of particulate contamination.

LPCVD deposited Si_3N_4 films had also a fundamental role on the device, as it was used for isolation the silicon substrate avoiding direct contact with the functional layers. Si_3N_4 was deposited over previously oxidized Si wafers at $800°C$ and a pressure of $0.25\ mbar$, using diclorosilane and ammoniac as chemical precursors. The goodness of the LPCVD deposited Si_3N_4 layers made them great for electrical isolation between the functional layers deposited on top of it and the silicon substrate.

Doping

Doping is commonly used for modulating the silicon substrate, basically changing its electrical properties. During the process, some impurities are intentionally introduced on the silicon crystal structure. The most commonly used elements for doping are boron (one less valence electron than Si) for p-type and phosphorous, arsenic and antimony (one more valence electron than Si) for n-type doped silicon.

Two main techniques have been commonly used for doping processes, diffusion and ion implantation. During a diffusion doping process, dopants are induced to diffuse into the substrate by heating it in a furnace up to $950-1280°C$. On the contrary, on an ion implantation a beam of energetic ions directly introduce (implants) the dopants into the substrate. With this more powerful technique, any ion can be placed at any depth of the sample, independently of the thermodynamics of diffusion.

On the micro SOFC fabrication flow, doping was used for specifically change some properties of the materials involved on the process. In particular, Si_3N_4 layers were doped with boron for reducing their tensile stress by ion implantation, using a dose of $4\cdot10^{15}\ at/cm^2$ and $100keV$. Moreover, on the fabrication of large-area self-supported membranes, doping was also used for modifying the silicon substrate and thus avoiding its etching with KOH on some desired zones (doped-silicon supporting nerves). In this case, a boron doping was made by solid source diffusion at high temperature ($1250°C$).

II.3. Thin film fabrication by Pulsed Laser Deposition

II.3.1. Deposition of functional layers by PLD

The deposition of thin films by PLD is based on the ablation of a target material often in vacuum conditions with a pulsed laser focalized onto it. Each laser pulse ablates then a small amount of the material creating a plasma plume (see Figure II-4). This plume, perpendicular to the target surface, is

directed to the substrate placed just on top of it, allowing the deposition. The nonequilibrium nature of the PLD ablation process, due to absorption of high laser energy densities by a small volume of material on the target, allows growing films with similar stoichiometry than the one of the target material [20]. It is then possible growing crystalline films at temperatures much lower than the typical crystallization temperatures required for most complex oxides (usually higher than 1000℃). Therefore, there is no need of post-thermal treatment for crystallization of the deposited materials, what makes the technique very practical for implementing them on silicon-based micro fabrication flow in which some components could not bear high temperatures.

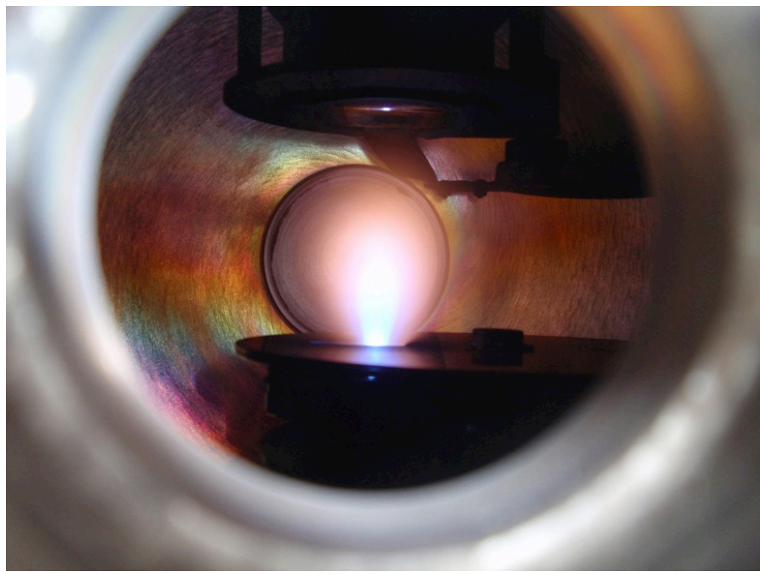

Figure II-4. *Image of a plume generated by the ablation of an YSZ target material.*

An appropriate choice of the ablation laser wavelength is needed for the efficient ablation of the target material. As mentioned before, the nonequilibrium excitation of the material requires the absorption of high energy densities on small volumes, thus the vaporization is not dependent on the vapor pressures of the constituent cations. In this sense, the usual choice for PLD equipments are excimer lasers, which provide reliable average powers ranging from $6\ W$ up to $300\ W$ at $248\ nm$ (KrF) – the laser utilized in this work –, or $308\ nm$ (XeCl).

A general view of a PLD deposition chamber can be seen in Figure II-5, which shows the one used in this work as an example of a conventional PLD chamber. The main components involved on a PLD process are labeled. The substrate holder, kept just in the vertical of the target material to be ablated, usually supports samples as big as $2x2\ cm^2$, and is commonly heated up by means of a resistive heater in contact to it. Laser incident angle is intentionally fixed to be $45°$ to the substrate surface, producing a plume perpendicular to the target surface and directed to the substrate. In this particular case, the chamber had a target carousel allowing the set of four different targets at the same time for multi-layer depositions, being the active target position the one placed just below the substrate holder.

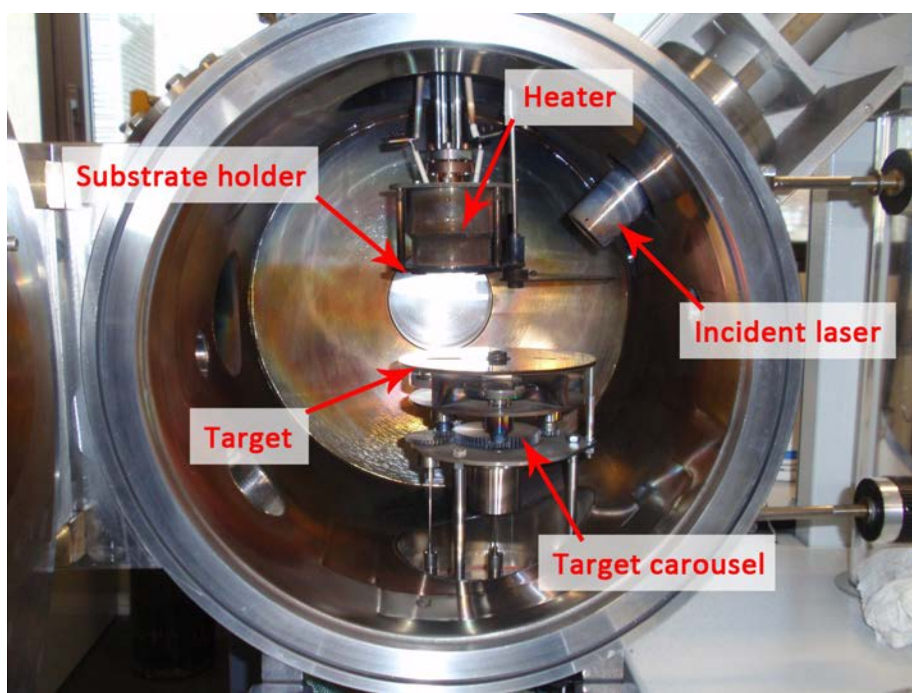

Figure II-5. *Image of the PLD chamber used in this work, pointing out its main components.*

Effect of main deposition conditions on the growing films

Deposition of complex oxides is commonly made on controlled vacuum atmospheres. The **background pressure** used on a specific process is the main parameter affecting to the final thin film microstructure, being able to tune the film porosity by only changing the pressure on the chamber. During the deposition, the background pressure is usually maintained constant by introducing a small flux of a certain gas (typically O_2 if growing oxides) while pumping the chamber. This gas flux is actually required for two different reasons, first to reduce the kinetic energies of the ablated species (which can reach values on the order of several hundreds of eV) and second to favor the desired phase formation, by providing O^{2-} anions to the film growth. As an example, a flux of $1.8\,sccm$ of O_2 was used in this work for obtaining a background pressure of $0.025\,mbar$ on the chamber. As a general rule, higher the pressure greater the porosity obtained on the film (much more interactions of ablated material with background species).

The growing rate is also deeply affected by the deposition conditions. PLD enables a precise control of the deposition process, the typical growing rate ranging from 0.001 to 1Å per pulse (a single shot corresponds to a submonolayer growth), however many parameters must be considered as they condition the final growing rate. These parameters include (i.) target material, (ii.) separation between target and substrate, (iii.) laser fluence or (iv.) spot size. Firstly, harder the **target material** lower the growing rate since less material will be ablated. The **separation between target and substrate** has also a clear effect on the growing rate, although the choice of this distance is not independent of the plume size (the substrate is usually maintained at least as separated as the size of the plume). In any case, as much far the substrate is from the target, lower is the growing rate because less material would arrive with enough energy for film growth. Finally, higher **laser fluence**, defined as the laser energy per unit area, will be able to ablate a larger volume of material increasing then the growing rate. At the same time, for a given fluence a larger **spot size** will also mean a larger zone of the target exposed to the laser, increasing the growing rate as well.

Specific deposition conditions used in this work

PLD films were grown on a PLD equipment provided by Surface and located at CIN2 (CSIC), as it is shown in Figure II-6. The system had three different deposition chambers, being able to direct the laser to any of them by using a set of mirrors. A KrF excimer laser from Lambda Physik was used for material ablation, which had a pulse width of around $20\,ns$. A repetition rate of $10\,Hz$ was generally used, and the laser energy density was fixed to be $1\ J/cm^2$ per pulse.

Figure II-6. *General view of the PLD placed at CIN2 (CSIC).*

PLD films were deposited on one of these chambers (see its inside in Figure II-5) on single device chips (from $6x6\ mm^2$ to $12x12\ mm^2$), for being tested individually. First microstructural tests were made on Si substrates covered with SiO_2 and Si_3N_4 dielectric layers ($100\ nm$ and $300\ nm$, respectively). This substrate configuration was specifically chosen as it was the one needed afterwards for fabricating free-standing membranes, so the deposition conditions could be directly transferred without any change on film properties.

The substrates were pasted to the sample holder placed on top of the plasma plume by using Ag paste, also ensuring a good thermal contact between them for a proper heating. Target-to-substrate distance was fixed at $70\,mm$ for all the deposits made in this work, and a set of different deposition substrate temperatures were tested, ranging from $T_s = 100°C$ to $T_s = 800°C$.

Both 3%-doped (3YSZ) and 8%-doped (8YSZ) yttria-stabilized zirconia films were deposited for being tested as electrolytes (see *Chapter IV* and *Appendix A*). Dense films of different thicknesses, ranging from a few tens of nm to more than half µm were deposited using a low pO_2 pressure of $0.025\ mbar$ in order to achieve the desired density on the films. YSZ deposition conditions were adapted from a previous work by Infortuna et al. [24].

On the other hand, for obtaining porous electrode layers, the pO_2 on the chamber was increased. LSC and CGO porous layers of hundreds of nm (from $100\ nm$ to $1\ \mu m$) were deposited by PLD maintaining a pO_2 of $0.15\ mbar$ on the chamber. In this case, further information about the thin film electrodes can be found on *Chapter V* and *VI*.

II.3.2. PLD target fabrication

The direct transfer of stoichiometry from the target to the grown film makes the preparation of targets a key point on the process of depositing high quality thin films by PLD. Actually, not only target stoichiometry has influence on the final thin film properties. Other target properties, such as its density, particle size or surface roughness can also affect the film, being able to modify the film density, the amount of ejected particulates or even the growing rate. Having a good target, i.e. controlled stoichiometry, high density and flatness, is then important to obtain high quality films. Different types of targets can be used for PLD, i.e. polycrystalline ceramic targets, single crystal targets or multi-targets. The most common alternative is the use of polycrystalline targets and they were the only ones used in this work.

Target properties optimization for particulate-free ablations

Probably the most important PLD phenomena directly related to the target properties is the ejection of particulates, resulting from local heating and melting of the target during the ablation. This is actually the biggest drawback for growing functional thin films by PLD, and it had a special bad influence in the present case for the fabrication of dense self-supported membranes. The presence of particulates on the electrolyte thin films is directly related to the generation of pinholes on the membrane, which causes fatal failure on the system by shortcutting the two electrodes. In fact, even if there is not a clear pinhole formation, a particulate can generate thinner zones on its surroundings due to a shadow effect, so high current densities and the subsequent hot spots can be formed on those zones producing again a dramatic reduction of the device performance. Figure II-7 shows an image of a membrane before and after a PLD deposition of YSZ. The appearance of particulates, in the range of a few µm in size, was then actually observed to happen during the depositions.

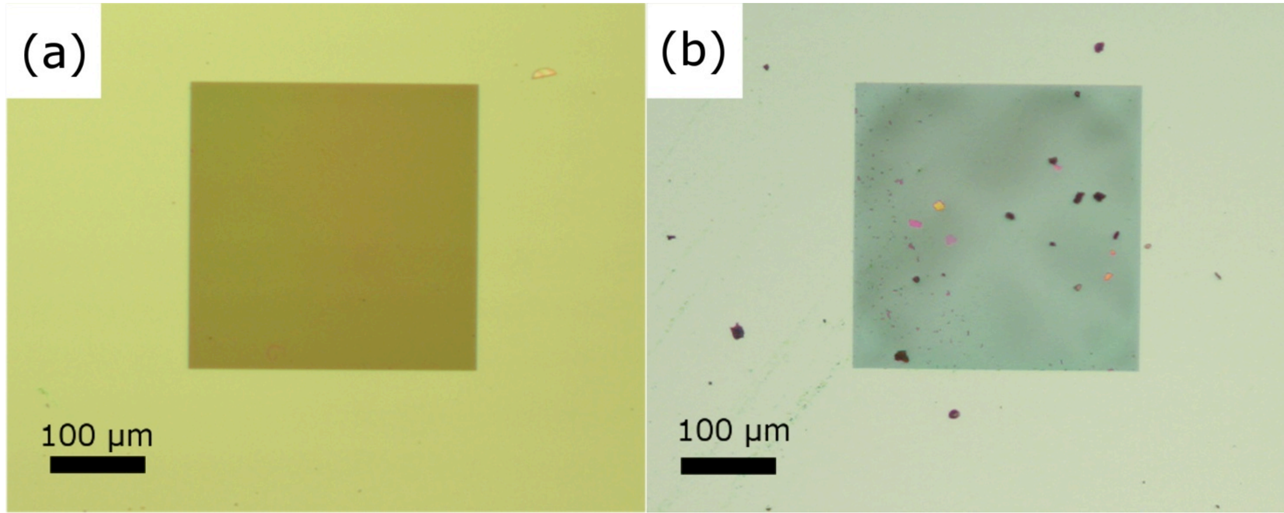

Figure II-7. *Optical images of a substrate used in this work before and after a PLD deposition of YSZ using a conventional target.*

In this work, a great effort was put on reducing the particulate density on the grown films (see *Appendix A*). Among the different strategies carried out, the most significant was the development of ultra high quality targets, looking for the specific properties needed to reduce the ejection of particulates from it [31]. In this sense, it is known that there is a direct correlation between the roughness of the target surface and the particulate density on the deposited film. When the laser hits on a thin edge of a roughness, this small zone of the target material can be easily ablated, pulling up the rest of the roughness not melted, forming the particulate. Thus, fully dense targets were searched, with as smooth surface as possible. The following section shows the strategy carried out in this work for obtaining these properties by modifying the target fabrication method.

Pellet shaping and densification

Conventional sintering (CS) usually provides high quality pellets, good enough for being used as PLD targets. In this simple technique, pellets are just compacted by uniaxial die on a press machine and heated up to the proper sintering temperature. By adjusting applied pressure and sintering temperature, close-to-theoretical density can be obtained on the targets. By this method, effective YSZ, CGO and LSC targets were prepared in this work and then used on PLD processes (see Figure II-8). Initial powders were bought in nano powder form from different companies (Tosoh, NanoE, Fuel Cell Materials and Kceracell) and compacted into cylindrical pellets of 1.5 to $3\ cm$ in diameter. Sintering temperatures for YSZ, CGO or LSC were fixed at $1450°C$ for $7h$.

However, the high temperature and long sintering process caused the final target to have a relatively big grain size (in the order of hundreds of nm) and slightly lower density. These facts and the subsequent faster surface degradation on these targets generated a high particulate ejection relatively soon. The alternative technique of choice was *spark plasma sintering* (SPS), as it allowed us to synthesize targets with a very high density (very close to the theoretical one) and with much lower grain size, ensuring the flatness of their surface. During this rapid sintering technique, a combination of pulsed DC current and high pressure is applied to a graphite die containing the raw powder. Then, high energy and low voltage pulses generate internal heating allowing rapid heating and cooling ramps and high densification of nanosized powders. As the problem of pinhole formation basically affects to the electrolyte layer (the electrolyte is the barrier layer between the two electrodes, thus the layer that prevents short-cuts), the effort was focused on the development of high-quality YSZ targets. Figure II-8 shows some of the fabricated targets, both by CS and SPS techniques.

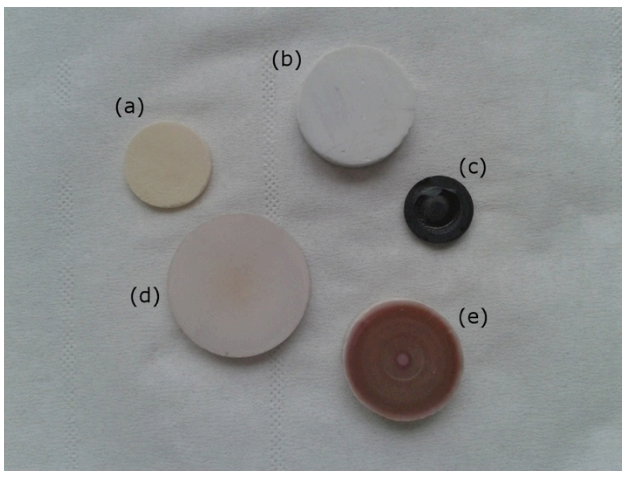

Figure II-8. *Some of the targets used in this work. (a) CS CGO, (b) SPS 8YSZ, (c) CS LSC, (d) CS 8YSZ and (e) SPS 3YSZ*

II.3.3. Wafer level integration: large-area PLD

In a conventional stationary PLD configuration, the deposited area is determined by the plume size, which is intentionally confined to a certain size by the interactions with the background species. The highly forward-directed nature of the ablation plume makes the thickness distribution from a stationary plume quite nonuniform, and determines the typical deposition area to be usually less than $25\ mm$. This can be reasonable for research purposes or single device development, but thinking on batch fabrication clearly supposes an important drawback.

Looking for a batch fabrication where many devices are fabricated in parallel, standard processes and machines in MEMS technology are wafer level integrated, i.e. at least $100\ mm$ (4”) substrates. Thus, for a complete integration of PLD deposited films on a MEMS fabrication flow and achievement of batch fabrication, it was required the scale of the PLD process to large-area depositions.

Fortunately, this problem could be solved by using recently developed large-area PLD equipment [20]. In these configurations the principle of actuation consists of manipulating the relative plume-substrate position. This way, instead of having the plume fixed on a single position, it goes moving all around the bigger substrate covering its whole area. The raster scanning of the ablation beam over the target and subsequently over the large-area substrate has been found as an effective way to obtain large uniform film coverages. The scanning is usually achieved by placing a programmable raster mirror on the optical train being able to move the laser spot all along the target surface.

The large-area PLD equipment utilized in this work was a PLD5000 from PVD, located at IREC facilities, which allowed depositing functional layers over substrates as big as 4” in diameter. Figure II-9 shows an image of the equipment where the experiments were carried out.

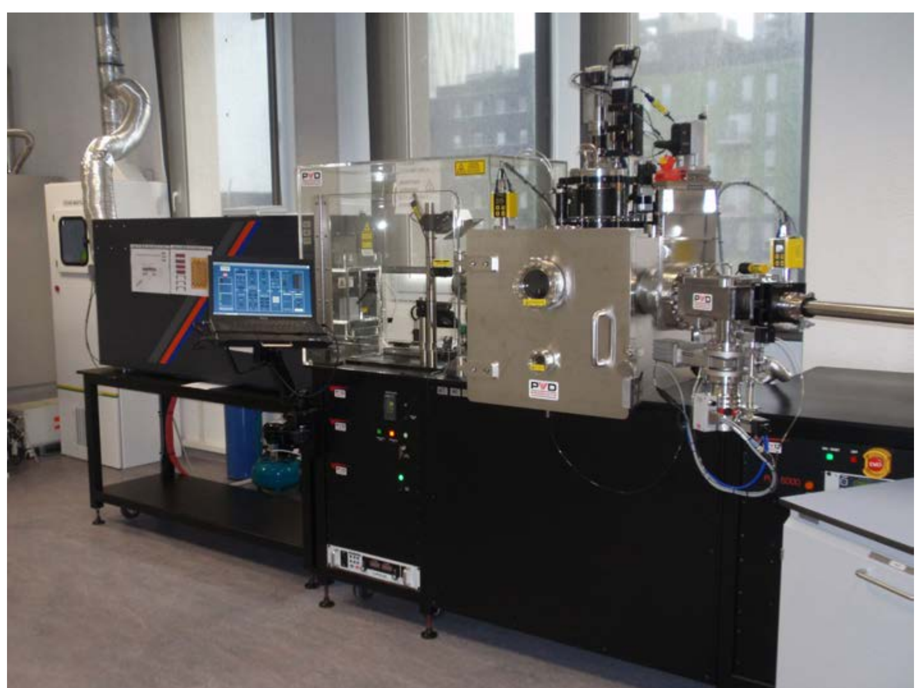

Figure II-9. *General view of the large area PLD located at IREC.*

Special issues related to large-area PLD depositions

The fact of working with larger substrate areas adds some extra issues to the PLD process that had to be taken into account, mainly concerning the targets and their preservation. First of all, it is important to notice that this configuration requires bigger targets to be effective, usually of the same size or a bit smaller than the substrate for covering the whole substrate area. Many times, the sintering of big targets is complicated, requiring a bigger amount of material and improving the probabilities of crack forming. Nevertheless, in this work, big targets of 3” in diameter were fabricated with high reproducibility, by using the same sintering conditions described before for the smaller targets. Moreover, in general the deposition of films over larger substrates requires the use of higher laser powers to achieve an acceptable growing rate. This could also generate problems on ceramic targets because, due to their low thermal conductivity, laser could cause localized heating and then cracking of the target. This effect can be partially solved by moving the spot at higher velocity all over the target, avoiding non-uniform thermal expansion.

The erosion of the target has to be carefully controlled too. Figure II-10 shows a scheme of the two main effects that can appear on large-area targets due to laser ablation, namely trenching effects and cone formation. The first effect is macroscopic, and appears if raster scanning is not properly defined. It can cause important plume tilting affecting film quality and growing rate. The second effect, formed by repeated melting, cooling and recrystallization of material on the surface, is quite common in PLD processes and can cause lowering of the deposition rate and an increment of particle ejection. It can be partially solved by raster scanning the laser through the whole target area, but not completely eliminated until polishing it resurfaces the target.

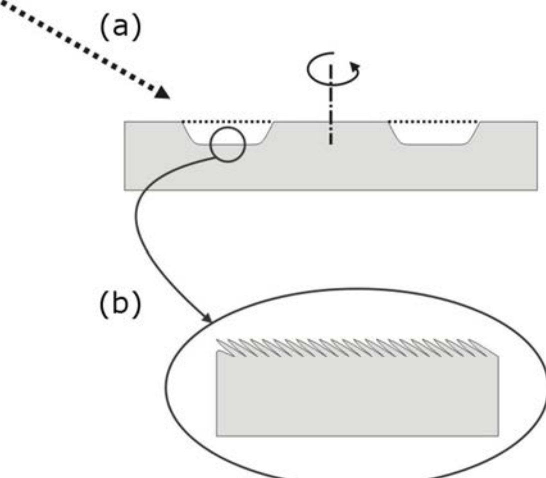

Figure II-10. *(a) Macroscopic trenches formed by the incident laser when using small rastering; (b) Microscopic cones formed by the laser interaction with the substrate surface.*

Specific deposition conditions used in this work

In this work, YSZ, CGO and LSC functional layers were deposited by the use of this PLD. First, film micro structure and growing rate was tested on smaller $10x10\ mm^2$ substrates, by using a special holder provided by PVD Products (see Figure II-11 (b)). Same substrates as the ones utilized on the stationary PLD ($Si_3N_4/SiO_2/Si$) were used for these tests. During the depositions, target was rotated with a velocity of $15\ rpm$, but the plume was fixed to be just below the substrate position, instead of rastering the whole 4”.

Then, to ensure uniform target erosion a computed rastering program had to be added, providing movement to the target thus the laser ablated homogenously the whole target surface.

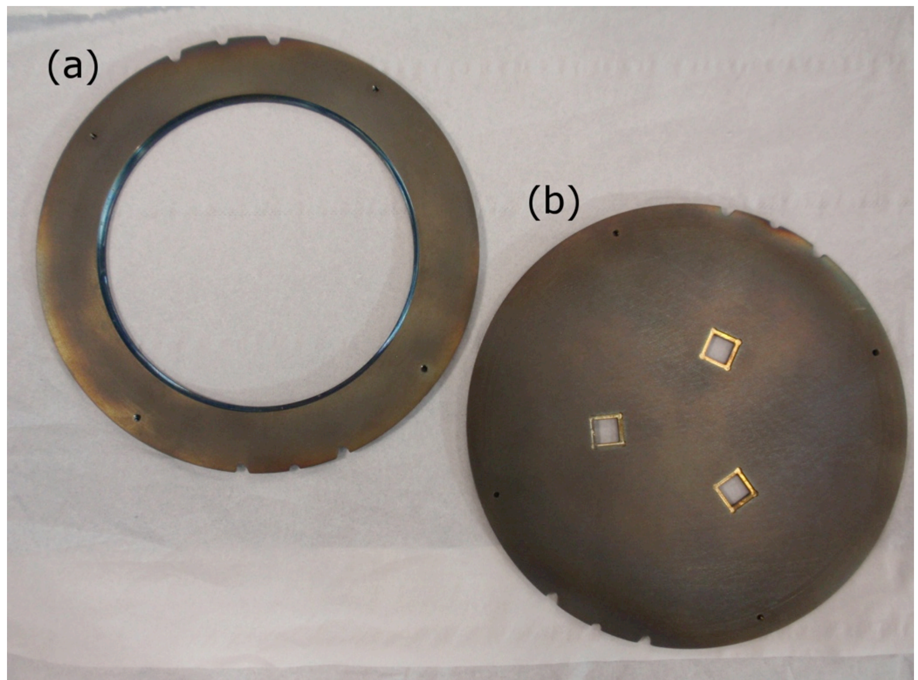

Figure II-11. *Sample holders used for wafer level depositions (a) and small substrate depositions (b) on the large area PLD at IREC*

Dense YSZ thin films were obtained using a background pressure of $0.025\ mbar$ (similar to the one used on the stationary PLD) and a distance between target and substrate of $90\ mm$. The substrate temperature was fixed at $T_s = 600$°C and the laser fluence $0.5\ J/cm^2$. In the case of CGO and LSC, porous films were obtained using a background pressure of $0.13\ mbar$. Temperature was fixed at $T_s = 100$°C and the target-to-substrate distance maintained at $90\ mm$. Target rastering was adjusted for each case, depending on the target dimensions.

Once determined the desired deposition parameters, functional layers were deposited over 4” silicon wafers. The wafers used for this experiment had the same $Si/SiO_2/Si_3N_4$ structure as the $10x10\ mm^2$, and were mounted on a sample holder as the one shown in Figure II-11 (a). In this case, during deposition both the target and the wafer substrate were rotated with a velocity of $15\ rpm$ and $5\ rpm$, respectively. The target rastering was switched over to a computed mirror rastering program for scanning the laser spot over its surface so the plume could cover the whole substrate area.

Figure II-12 shows the film thickness homogeneity over one of the deposited wafers. Due to the plume geometry, to ensure a good homogeneity rastering had to be adjusted to be much faster in the center of the wafer than in the borders. Spot velocities 300 times faster were used for rastering the central part of the wafer than the border. It is important to notice that there is always a significant reduction on film thickness on the very extreme of the wafer. This effect can be ascribed to a shadowing effect due to the PLD sample holder, and it must be considered as it cannot be avoided but changing the sample holder design.

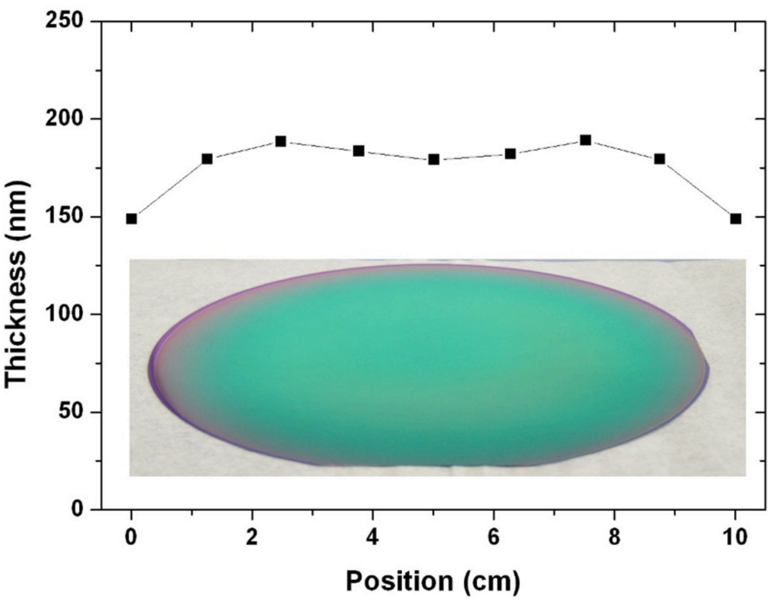

Figure II-12. *YSZ film thickness homogeneity over one of the deposited wafers.*

II.4. Thin film characterization techniques

The characterization of the functional thin films has been categorized in three parts. The first one is the *compositional and structural characterization*, which seeks the control of the physical-chemical properties of the deposited films, i.e. stoichiometry, phase purity, crystallinity, density or particle size and shape. Afterwards, the functionality of the films must be ensured by both characterizing its thermo-mechanical performance and its electrical properties. The second section of characterization techniques, the *thermo-mechanical characterization*, refers to the study of the mechanical stability of the films and membranes at working conditions, which in this particular case means temperatures in the intermediate-temperature (IT) range. Finally, on the third section of characterization, the *electrochemical characterization*, the performance of each component of the fuel cell is studied, measuring its ionic/electronic conductivity, or its contact resistance depending on the film functionality.

II.4.1. Compositional and structural characterization

X-Ray diffraction

X-Ray diffraction (XRD) is commonly used in crystallography for compositional analysis and phase identification of crystalline materials either powders, pellets or even thin films. The exposition of the sample to X-rays is recorded and analyzed. The X-rays wavelength is of the order of magnitude of the interatomic distances in the crystal, so the sample can actually act as diffraction net. Then, the X-rays are diffracted with specific directions and intensities, generating a certain pattern characteristic of each crystalline structure.

This technique was used in this work for basic phase identification of the different films deposited by PLD, as well as the corresponding fabricated targets utilized for the depositions. Thus, direct comparison

between target and thin film patterns could be performed. Different XRD equipments were used, located at IREC and CIN2 (Bruker-D8 Advance and X'Pert Pro MRD-Panalytical, respectively). Most of the XRD experiments were carried out at room temperature in flat plate $\theta/2\theta$ geometry. However, for some specific experiments, a temperature-controlled stage was mounted on the XRD equipment to be able to acquire the XRD pattern at different temperatures, ranging from room temperature up to $800℃$. This allowed the study of the XRD pattern evolution with temperature, being able in such cases to observe phase changes or just crystallization of thin films and then establish the specific temperature needed for a certain process (for example, crystallization temperature).

Raman spectroscopy

Raman spectroscopy is a technique also used for phase identification on crystalline samples and thin films. It is based on the observation of the vibrational, rotational and other low-frequency modes when illuminating a sample with monochromatic light. The light interacts with molecular vibrations, phonons or other excitations in the crystal, and this interaction results on shifts in the energy of the laser phonons that can be related to the vibrational modes of the system and thus the crystalline structure.

The sample is usually illuminated with a laser beam, and the reflected light coming from the sample is collected with a set of lenses and sent through a monochromator. Wavelengths close to the laser line due to elastic Rayleigh scattering are filtered out, while the rest of the light is dispersed onto a detector giving the corresponding signal.

In this work, micro-Raman spectroscopy was used as an alternative way to identify the phase of the deposited YSZ films. The Raman spectra were excited with the $514.5\,nm$ line of an Ar^+ laser. The experiments were performed at room temperature in a backscattering geometry using a confocal microscope with an x50 objective lens. The scattered light was analyzed by means of a Jobin Yvon T64000 equipped with a LN2-cooled CCD detector.

Reflectometry

Reflectometry consists on the measurement of the amount of light reflected from a thin film, measured over a certain range of wavelengths, with the incident light normal to the sample surface. This optical technique, together with ellipsometry, is very common for the characterization of thin film thicknesses and optical constants. This technology is very attractive due to its high accuracy and the fact of being nondestructive (actually, it requires very little or no sample preparation).

The measurement is based on the study of the fraction of light reflected at each interface between two films, which is determined by the discontinuity in their optical constants n and k. When having multiple interfaces, the total amount of reflected light is then the sum of all the individual reflections. Reflections may then add together either constructively or destructively, depending on their phase relationship, which is again determined by the optical constants, but also by the thickness of the film and the incident wavelength. Then, the resultant spectra can be fitted by using some mathematical models to obtain either the thickness of the film, if knowing the optical constants, or vice versa. Reflectometry, although less powerful than ellipsometry, is capable of measuring thickness, roughness and optical constants on a broad range of thin films. Its only limitation is the need of a certain minimum thickness on the measured films for getting the required amount of information to be able to adjust a mathematical model.

This technique was routinely used in this work for measuring the film thickness on PLD deposited YSZ thin films. Thus, without destructing the sample, it allowed us to perfectly know the thickness of each sample to be characterized. The reflected light on a wavelength range from 400 to $800\ nm$ was acquired on a NanoSpec 6100 reflectometer equipment, placed at IMB-CNM (CSIC). Film thickness was then calculated by fitting the collected data using n and k values for YSZ taken from the literature.

Optical microscopy

On optical microscopy (OM), visible light plus a set of lenses is used to magnify images of small samples. The use of visible light source for imaging make the technique very useful and accessible, as the samples can be observed by eye.

Most microscopes have their own adjustable and controllable light source, often a halogen lamp. Two basic acquisitions can be made, depending on the position of the light source with respect to the sample, i.e. transmission and reflection images. Respectively, the corresponding image comes from the transmitted light through the sample or the reflected light when illuminating it.

In this work, OM (Nikon Eclipse ME600) was regularly used to check the sample state after each fabrication step. This technique was particularly useful for studying the reduction of particulate ejection from PLD depositions, as the particulates, in the range of some μm in size, could be already seen by this technique. Moreover, pinholes on the membrane could be easily distinguished by using transmission light once a reflective film (such as thin platinum) was deposited over the membrane, as the light was only transmitted through these spots. Unfortunately, YSZ was not reflective enough to be able to locate the pinholes and these could not be identified until an extra Pt layer was deposited over it.

Scanning electron microscopy

Scanning electron microscopy (SEM) is probably the most common electronic microscopy used for microstructural study of thin films and microstructures. SEM is a technique capable of getting high resolution images of either sample surfaces or thin film cross sections.

In a SEM, images are generated by scanning a sample with a focused beam of electrons. The interaction of these electrons with the sample produces a series of signals that are detected on their corresponding detectors, generating the images. The focused beam is formed by accelerating electrons emitted from a tungsten cathode towards an anode, and is directed to the sample by using condenser lenses capable to focus the beam into a spot of $1-5\ nm$ sized. Better resolutions than $1\ nm$ can be achieved by SEM.

Depending on the signal collected (and thus the detector used), there exist different types of imaging, being the most common the use of low energy secondary electrons. These electrons are emitted from the sample when the electron beam enters into it. Depending on the surface morphology, the beam enters with different angles of incidence, changing then the number of secondary electrons emitted. Edges and steep surfaces are thus usually brighter than flat surfaces, due to the larger emission of secondary electrons from these zones, producing well-defined images. For some specific purposes, the use of backscattered electrons is preferred. In particular, backscattered electrons are useful for identification of areas with different chemical compositions as they are generated by elastic scattering interactions with specimen

atoms. Finally, X-rays produced by the interaction of the electrons with the sample can also be detected and analyzed. This specific detection is called energy-dispersive X-ray spectroscopy (EDX), and allows identifying the elements present on a certain zone of the sample.

SEM was routinely used in this work to analyze the morphology of all the deposited films and fabricated targets. It allowed us to study the porosity of the films when required, or study the grain size both on the targets and films. Moreover, the technique was used in combination with reflectometry as a method to check the thickness of the PLD deposited thin films and thus determine the growing rate. However, unlike reflectometry, SEM forced us to break the samples each time to study the cross section, so it was kept only for comparison purposes. Several SEM equipments were used during this work, either at IMB-CNM (LEO 1530) or IREC (Zeiss Auriga).

Transmission electron microscopy

Transmission electron microscopy (TEM) is a microscopy technique that uses the electrons transmitted through an ultra thin specimen when illuminating it with a focused electron beam to create an image of the sample. This image is formed from the interaction of the electrons with the sample. The observation is then made by magnifying and focusing the signal either onto a screen (fluorescent or photographic film), or onto a detector to be detected by a sensor.

A similar source of electrons than that for SEM is also used on TEM. The intensity of the transmitted beam is dependent on the volume and density of the film, which must be very thin not to absorb the entire beam. The transmitted electrons can also suffer diffraction, due to the interaction with the crystalline material being observed. Two different types of imaging are then possible, depending on which electrons are collected. On one side, bright field images are obtained when looking only at unscattered electrons. The diffracted electrons are blocked by deflecting them away from the optical axis of the microscope, obtaining high contrast images. This is made by placing an aperture that only allows unscattered electrons to go through it. On the other side, the observation of those diffracted electrons results on a different image, known as dark field image. This second type of imaging is acquired by either moving the aperture or tilting the electron beam, in such way that the diffracted electrons can pass through it while the unscattered ones are blocked. The two types of imaging are complementary, and are used depending on the information required. Much higher resolutions than in SEM can be obtained by TEM, reaching values as high as $0.8\ \text{Å}$ when using high resolution TEM microscopes.

TEM was used in this work also for studying the influence of the fabrication parameters on the microstructure of YSZ films, i.e. grain size and crystallinity. A JEOL JEM-2100 microscope was used operating at $200\ kV$, located at the Scientific Technical Services of the University of Barcelona. $60\ nm$ thick membranes fabricated at different deposition temperatures (from $200°C$ to $700°C$), were used for TEM analysis, allowing then the transmission of electrons through them.

II.4.2. Thermo-mechanical characterization

A detailed study of the residual stress generated during the fabrication process of YSZ free-standing membranes was performed, in order to yield to a set of experimental conditions that would allow tuning their stress state and thus their thermo-mechanical stability.

The residual stress state of released YSZ membranes was characterized by different methods. First, for the obtained compressive membranes, analysis of deformation patterns of released buckled square membranes could be used to determine the in-plane pre-stress. Moreover, complementary X-Ray diffraction studies based on the analysis of the variation of the angular position, 2θ, of the (111) reflection as a function of the tilt angle, ψ, were carried out according to the d_{hkl} versus $sin^2\psi$ method for both compressive and tensile membranes. Results and discussion about the thermo-mechanical stability and stress evolution are detailed in *Chapter IV*.

Buckling Profile Analysis of Compressive Membranes

Compressive membranes over a certain critical stress can release their in-plane stresses into out-of-plane deflection. The onset of the buckling occurs at a well defined negative critical strain ($\varepsilon_{cr1} < 0$). The associated buckling profile is controlled by the mechanical properties and geometrical configuration of the membrane, so it is possible to determine the in-plane strain (ε_0) and stress (σ_0) present before buckling by analyzing the generated deformation pattern. Ziebart et al. [32] derived a method for direct extraction of pre-stress values from mildly buckled square membranes, i.e. below a certain value of critical stress ε_{cr2} ($\varepsilon_{cr1} < \varepsilon_0 < \varepsilon_{cr2}$), by center deflection measurements (w_0).

Considering a square membrane with side length a and thickness h presenting a compressive pre-strain (ε_0), it is possible to establish a relationship between two dimensionless reduced magnitudes, the reduced center deflection ($\overline{w_0} = w_0/h$) and the reduced pre-strain ($\overline{\varepsilon_0} = \varepsilon_0 a^2/h^2$). This relationship is expressed in equations 17 to 19 from reference [32]. Then, by assuming values of Young's modulus (E) and Poisson's ratio (ν), this reduced pre-strain can be used to obtain the pre-stress value of the membrane:

$$(\sigma_0 = \varepsilon_0 E/(1-\nu)) \qquad \textit{(II.1)}$$

In this work, values of Young's modulus of $E = 308\ GPa$ and Poisson's ratio of $\nu = 0.25$ were assumed for YSZ. Moreover, in order to keep the strain values of the membranes in the region of validity of the model ($\varepsilon_{cr1} < \varepsilon_0 < \varepsilon_{cr2}$), only small membranes of 50 to 150 μm long and 120 nm thick could be used for this test.

Micro X-Ray diffraction: d_{hkl} versus $sin^2\psi$ method

The classical stress determination method through the study of the hkl planar spacing (d_{hkl}) variation versus $sin^2\psi$ was also used for stress calculations [33]. When polycrystalline films are submitted to an in-plane biaxial stress, which is generally the case of films obtained by vapor phase deposition techniques on flat substrates, the individual grains are strained in a different amount depending on their particular crystal orientation. In the simplest case of a randomly-oriented polycrystalline film, the response to the stress

could be considered isotropic and the residual strain ε_{ψ}, calculated from the planar spacing d_{ψ} (weighted average from different reflections) measured at different ψ angles, follows the expression:

$$\varepsilon_{\psi} = \frac{d_{\psi}-d_0}{d_0} = \frac{1+\nu}{E}\sigma_{||}sin^2\psi - \frac{2\nu}{E}\sigma_{||} \qquad (II.2)$$

where d_0 is the non-stressed planar spacing, $\sigma_{||}$ is the in-plane stress, E and ν are respectively the Young's modulus and Poisson's ratio of the isotropic material. This expression shows a linear dependence of d versus $sin^2\psi$ and the stress $\sigma_{||}$ is simply extracted from the slope of the curve if one knows the E and ν constants of the material. Both E and ν constants are positive numbers therefore when d increases with ψ the slope of the curve is positive and $\sigma_{||} > 0$, which corresponds to a tensile stress, and the opposite for a compressive stress. A similar expression applies when analyzing d values measured by X-ray diffraction from a selected hkl reflection. Since E and ν values depend on the hkl choice, the expression takes a more general form:

$$\varepsilon_{\psi} = \frac{d_{hkl}-d_0}{d_0} = \left[\frac{1}{2}s_2(hkl)\right]\sigma_{||}sin^2\psi + 2[s_1(hkl)]\sigma_{||} \qquad (II.3)$$

where s_1 and $1/2\,s_2$ are the so-called diffraction elastic constants (DECs) related to the elastic compliances s_{ijkl} from the 4-rank elastic tensor. For a cubic material like YSZ the elastic tensor simplifies to only three independent elastic compliances s_{1111}, s_{2222} and s_{1212} (equivalent to s_{11}, s_{12} and $1/4\,s_{44}$, respectively). Following Reuss approximation for a material evenly stressed the DECs can be calculated as:

$$s_1 = s_{12} + \Gamma s_0 \quad \text{and} \quad \frac{1}{2}s_2 = s_{11} - s_{12} - 3\Gamma s_0 \qquad (II.4)$$

where $\Gamma = \frac{h^2k^2+k^2l^2+h^2l^2}{(h^2+k^2+l^2)^2}$ and $s_0 = s_{11} - s_{12} - \frac{s_{44}}{2}$. Here, we used values of s_{ij} derived from a previous report from Fujikane et al. on YSZ single crystals [34].

The total stress in the films was characterized by means of X-ray diffraction in a Bruker-D8 Advance diffractometer with a four circle goniometer and GADDS-HiStar detector. The diffractometer equipment used for this work presents a parabolic mirror and a double pinhole collimator ($0.3\ mm$ diameter) in the primary beam in order to reduce the beam divergence in both the diffraction and axial planes. This makes possible the accurate determination of the planar spacing without substantial defocalization problems in a wide range of different ψ angles from zero to almost 75 degrees. Besides, the small size of the X-ray spot area on to the sample ($0.3\ mm$) allows for local residual stress analysis in the area of the self-supported YSZ membranes. The analyzed areas were selected by means of an XYZ stage and a laser positioning system.

In this work, a complete set of films deposited at different temperatures by PLD was analyzed with this technique. For each temperature, three separated free-standing YSZ membranes with different size were used plus one zone with YSZ film far from the membranes for comparison. The small thickness of the films of about $120\ nm$ limited the X-ray diffraction study to low index hkl reflections with intensity enough to reduce statistic errors. For the XRD acquisition the 2θ detector goniometer angle was fixed to 35° and omega incidence angle to 17°. Under these conditions (at a fixed sample-to-detector distance of $150\ mm$) the 2D detector was capable of measuring simultaneously in a single frame a 2θ range from 19° to 52°, along the detector axis, and an equivalent $\Delta\psi$ range of $\pm 30°$, in the crossed direction, thus containing 111, 200 and 220 reflections. The determination of 2θ peak position from one single frame for the ψ range far

from the detector axis was not as accurate as it was requested for the residual stress determination, because of insufficient correction of the flat detector optical aberration. Thus, the data integration was limited to an area on the detector axis of $\Delta\psi$ of $\pm 5°$ (that means using the detector almost as if it was 1D), and performed separated acquisitions at different sample stage tilt angle ψ from $0°$ to $80°$ with $\Delta\psi = 5°$ intervals. Since the inclusion of 200 and 220 reflections in the analysis did not seem to provide additional information we decided to restrict this study to the variations of the 111 peak position, for clarity reasons.

II.4.3. Electrical characterization

Electrical characterization set ups for micro SOFCs

The special characteristics of the micro SOFC, i.e. small dimensions and high temperatures required, made the development of a well-defined and controlled measuring set up more complicated than expected, as the separation of two atmospheres at each side of the membrane had to be ensured for the study of the power supplied.

Firstly, the optimization of electrolytic self-supported membranes and electrodes could be made on a Linkam HFS91 PB4 temperature controlled stage, as each study was made on a single atmosphere. Figure II-13 shows an image of the stage utilized for these first measurements. The stage has four metallic tips, which were used to mechanically contact either the top-side and back-side electrodes for cross-plane studies or the different contact pads for in-plane measurements. The sample to be characterized is placed over a heating plate, and the system allows introducing gases in order to control the atmosphere inside the chamber. A refrigeration circuit is also included to avoid stage damage when heating over $300°C$.

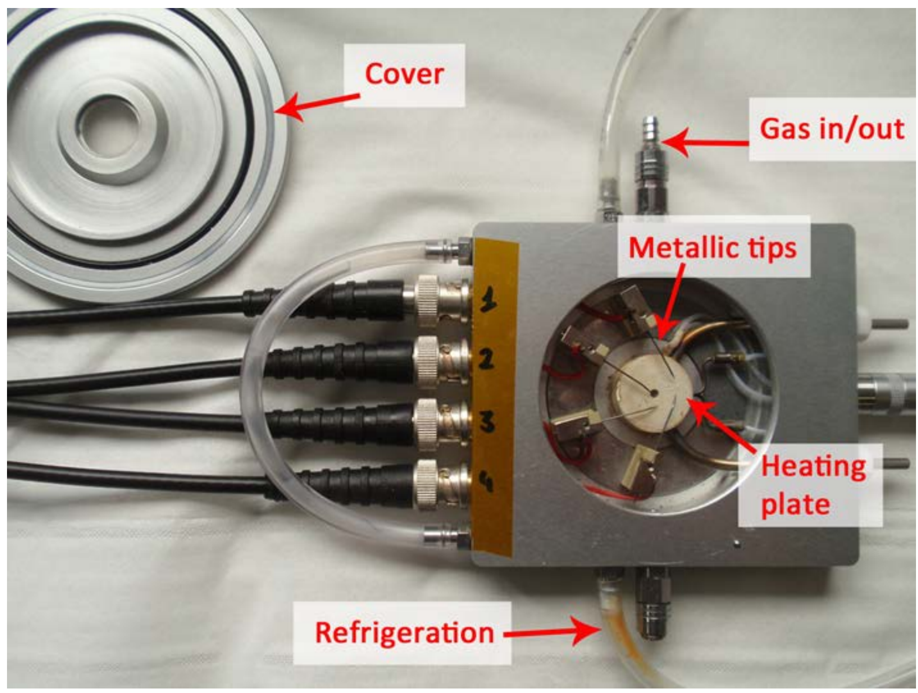

Figure II-13. *Linkam stage for basic measuring of single devices*

The electrical properties of the fabricated YSZ, LSC and CGO thin films and free-standing membranes were studied by both DC and AC techniques in this stage, in the range of temperatures between 250℃ and 650℃.

For the characterization of the power supplied by the cell, the stage had to be completely changed as the reduced dimensions of the Linkam did not allow us to introduce on it a system capable of separating two atmospheres, one at each side of the membrane. Thus, in this case, Probostat measuring stages had to be used, and the characterization was made on tubular furnaces that allowed the temperature control. Figure II-14 shows an image of one of the Probostat stages. The sample was placed on top of an alumina tube, and sealed by the use of silver rings (c). Three springs provided the needed pressure for a proper sealing (b). The collection of current was made by placing Pt meshes on top and back sides of the sample, always avoiding direct contact with the membrane for not breaking them by scratching. The special design of the Probostat stage allowed the introduction of different atmospheres inside and outside the alumina tube. In some cases, Probostat was also used for basic DC or AC measurements of ceramic thin films and membranes by using the same configuration, but without the need of sealing the sample to the tube.

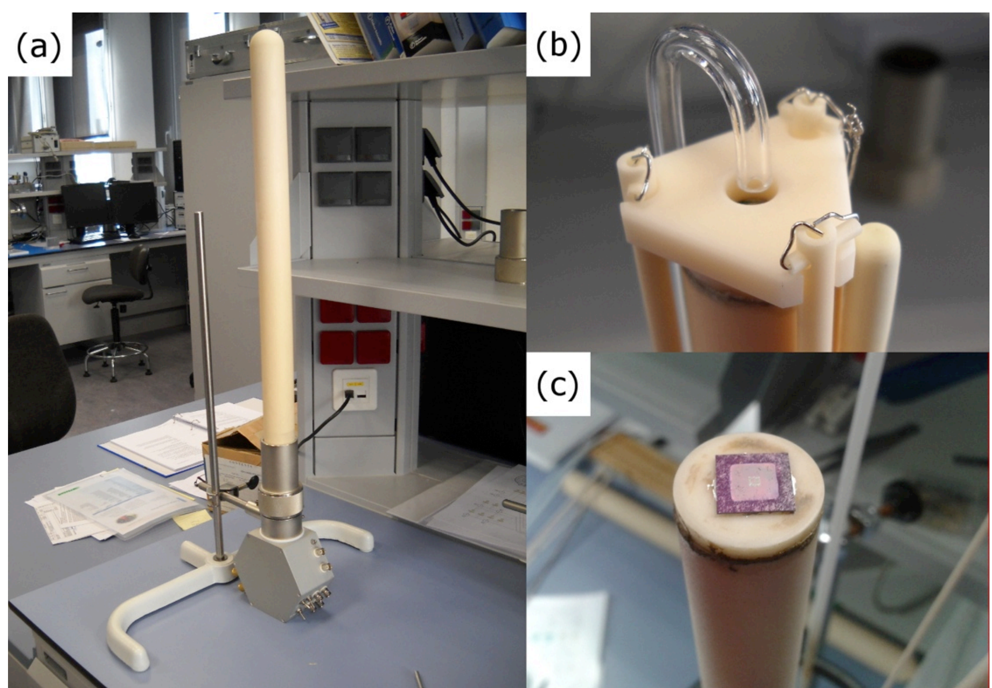

Figure II-14. *Probostat stage for two atmospheres measuring. (a) General view of the stage. (b) Detail of the top side of the alumina tube. (c) Image of one of the sample sealed on top of the alumina tube.*

Electrochemical impedance spectroscopy

Electrochemical impedance spectroscopy (EIS) is the most common method for studying the electrical properties of materials in solid state ionic systems [35], and was indeed the main technique used in this work for characterization of the different components of the micro SOFC. The ability of separating the contribution of each component to the total resistance on a complex measurement is extremely useful for the study of either the electrolyte or the electrode performance, separating its contribution from the rest of contributions on the cell.

EIS is based on the application of an AC voltage through the system, in a certain frequency range. The sweep in frequencies allows separating the different impedance contributions depending on the characteristic time constant of each process occurring on the system. The voltage applied can be expressed by $E(t) = E_0 \cdot e^{i\omega t}$, where E_0 is the amplitude and ω the variable angular frequency. Similarly, the generated current can be expressed in the same way, as $I(t) = I_0 \cdot e^{i(\omega t+\theta)}$, being θ a phase shift of $I(t)$ generated with respect to $E(t)$. Impedance can then be define as the quotient between these two values,

$$Z(\omega) = \frac{E(t)}{I(t)} = |Z|e^{(-i\theta)} \qquad \textit{(II.5)}$$

This complex impedance number can also be expressed in terms of a real and an imaginary component as,

$$Z(\omega) = |Z|\cos\theta - i|Z|\sin\theta = Z'(\omega) - iZ''(\omega) \qquad \textit{(II.6)}$$

The applicability of this expression requires a linear dependence of the current with respect to the voltage. Unfortunately, most of the electrochemical systems present nonlinear behaviors, as for example the charge transfer resistance which strongly depends on the potential. Thus, small AC voltages have to be applied in order to keep into a pseudo-linear regime.

The representation of the imaginary part $Z''(\omega)$ versus the real part $Z'(\omega)$ is the most common way to study the experimental data, on the so-called Nyquist plots. On the simplest plot, found for a system with an only conduction mechanism, a semicircle of diameter R (the material´s resistance) appears with the center on the Z' axis at the position $(R/2\,,0)$. When looking at more complex system such as an electrode/electrolyte/electrode multilayer, several different mechanisms take place, i.e. ionic conductivity through the electrolyte, charge transfer or mass transport on the electrode/electrolyte interface. Each of these mechanisms contributes to the total resistance on the system, and is reflected as different semicircles on the Nyquist plot, appearing separated from the others as their time constants (τ) differ.

The specific time constant of a process is defined as $\tau = 1/RC$, so it is not only dependent on the resistance, but also on the capacitance associated to the process. Depending on the characteristic R and C values of each process, their τ can differ some orders of magnitude, and the semicircles appear separated and well-defined on the Nyquist plot. However, most of the times different semicircles appear overlapped, happening when the values of time constant are less than two orders of magnitude apart. It is important to notice that values of τ are strongly dependent on the temperature, due to the variation of the resistance, so the range of ω in which a certain mechanism is seen changes when varying temperature.

The most common way to study the Nyquist plots is by fitting the spectrum by using *equivalent circuits*. Each semicircle appeared on the Nyquist plot can be associated to a (RC) sub-circuit, and the whole process can then be related to an equivalent electrical circuit. Figure II-15 shows a Nyquist plot that would correspond to a simple fuel cell system, with the associated equivalent circuit also depicted. The different mechanisms involved are reflected as multiple semicircles in the graph, each one corresponding to a RC on the equivalent circuit. In case a significant overlapping is observed, a more accurate analysis is necessary for a correct understanding of the impedance spectrum.

In this work, EIS across thin YSZ self-supported membranes was carried out on the Linkam stage with a potenciostat/galvanostat working as an impedance analyzer (Gamry reference 3000), using small AC voltage signals of $50\ mV$ in order to keep the linear regime. On this first experiment, the corresponding electrodes were provided by metalizing the samples by sputtering $240\ nm$ of Pt in both sides, thus forming a Pt/YSZ/Pt self-supported membrane. The selective sputtering only over the membranes was achieved using a Teflon mask, avoiding short-cuts along the edges of the sample.

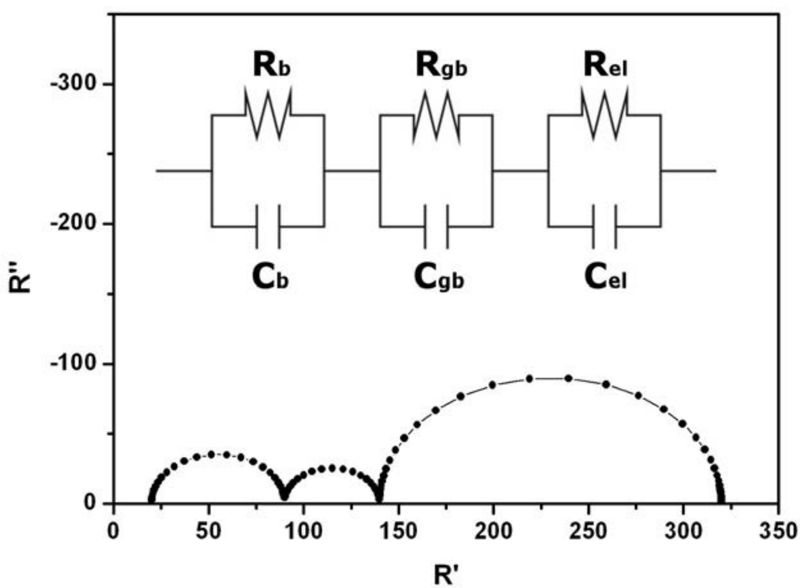

Figure II-15. *Nyquist plot of an EIS for a simple electrolyte cell. The electric circuit represents the simplest equivalent circuit associated to the plot.*

The electrode performance, i.e. the resistance associated to the electrode, was also studied by this technique on the final micro SOFC configuration. EIS across LSC/YSZ/LSC and CGO/YSZ/CGO self-supported membranes was carried out this time on Probostat cells using either a Novocontrol (Alpha-A High performance frequency analyzer) or a Parstat (2273 Advanced Electrochemical System) equipment. Single oxidizing or reducing atmospheres were forced onto the cell respectively, to characterize each material working either as cathode or anode. For these experiments, porous Pt films were deposited by sputtering on both sides of the membrane to provide the samples with the corresponding current collectors and contacting was made by placing Pt meshes on both sides.

In all the cases, EIS data was analyzed by using the *Z-view* analysis software.

In-plane electrical characterization techniques

Complementary DC in-plane experiments were also performed to study thin film intrinsic conductivity of both YSZ and electrode films. In this case, only the total conductivity was measured, as the result comes from a DC signal. The measured values were used for comparison with the results of the EIS experiments.

Regarding the electrolyte, YSZ in-plane electrical resistivity was measured using a Keithley 2400 sourcemeter by painting two Ag-paste electrodes separated $1\ mm$ on top of a YSZ thin film deposited over

$Si_3N_4/SiO_2/Si$ substrates. The sample was mounted on the Linkam stage so contacting was ensured by the use of two of the Linkam metallic tips.

On the other hand, both LSC and CGO in-plane conductivities were characterized by the Van der Pauw method [36]. This 4-prove method is commonly used for characterization of the DC resistivity on thin films, when the materials to be measured have such high conductivity that the EIS characterization is useless. It is a powerful method as it allows to accurately measure samples of any arbitrary shape. Just some basic conditions must be fulfilled to be able to apply the technique on a certain sample, i.e. (i.) the sample must be flat and homogeneus in thickness, (ii.) the contacts must be sufficiently small (at least one order of magnitude smaller than the area of the entire sample) and placed on the very edges of the sample, (iii.) the sample must not have isolated holes and (iv.) the sample thickness must be much less than its length and width. The measurement is then carried out by placing four contacts on the edges of the sample, numbered from 1 to 4 in a counter clockwise order. If a current I_{12} is then applied between the two corresponding contacts 1 and 2 and the voltage difference V_{34} is recorded between the other two (3 and 4), a resistance $R_{12,34}$ is defined following the basic expression $R_{12,34} = V_{34}/I_{12}$. Analogously a resistance $R_{23,41}$ can be measured applying the current between 2 and 3 (I_{23}) and measuring the voltage between 4 and 1 (V_{34}). According to this method, the sheet resistance (R_s) of any sample with any shape can then be determined from these two resistances, following the expression:

$$e^{-\pi R_{12,34}/R_s} + e^{-\pi R_{23,41}/R_s} = 1 \qquad \textit{(II.7)}$$

In this work, LSC and CGO thin films (always of less than 1 μm) were measured deposited over $1x1mm^2$ and $300\mu m$ thick square Si substrates, previously covered with Si_3N_4 and SiO_2 dielectric layers to avoid unwanted electrical effects from the substrate. Measurements were made on Probostat cells, allowing temperature controlling and easy contacting. Figure II-16 shows an image of one of the samples mounted on the Probostat cell. Very small contacts were painted with Au paste on the very corners of the deposited zone, and thin Au wires were pasted to them for current collection.

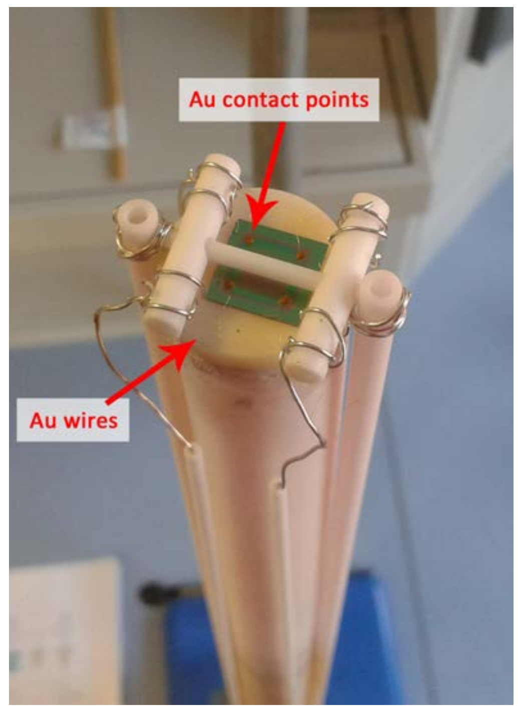

Figure II-16. *Image of the one of the samples characterized by the Van der Pauw method.*

Potentiostatic and Galvanostatic Measurements

As already mentioned in *Chapter I*, characterization of the overall performance on a fuel cell is made by the measurement of IV curves, i.e. measuring the current flow (I) between the two cell electrodes at different voltages (V) applied between them. A direct correlation can be then made for calculating the power generated, by following the expression $P = I \cdot V$.

Two types of measurement can be carried out for characterizing it, namely potenciostatic and galvanostatic measurements. The most common potenciostatic measurement uses a potentiostat for controlling the voltage difference between the two electrodes, while measuring the resultant current flow between them. The controlled variable in a potentiostatic measurement is then the cell potential and the measured variable the cell current. When measuring in a galvanostatic mode, the feedback is switched from the cell voltage signal to the cell current signal. The galvanostat instrument controls the cell current flowing between the two electrodes and measures the resultant voltage.

Open circuit voltage (OCV) of the cell is usually measured on galvanostatic mode, by applying a negligible current flow between the electrodes and measuring the voltage generated between them. Getting a close to theoretical value of OCV on the cell is not only important to ensure each component of the micro SOFC is working properly, but also allows us to control the goodness of the sealing between the two sides of the membrane. As the OCV value is mainly dependent on the difference on pO_2 between both sides, any leak on the sealing would be reflected as a decrease on the OCV value with respect to the theoretical one.

In this work, potenciostatic and galvanostatic measurements were carried out free-standing micro SOFC membranes. The measurements were always carried out on a Probostat measuring stage, sealing the samples to the alumina tube by using Ag rings.

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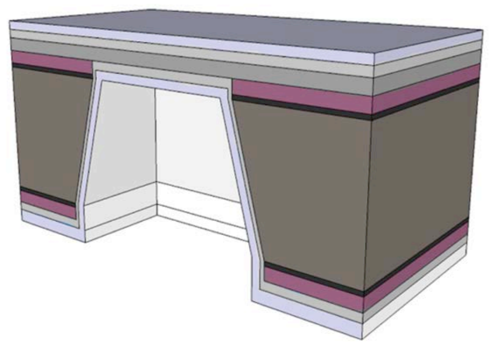
III. SOLID OXIDE FUEL CELLS INTEGRATION IN SILICON: DESIGN AND MICROFABRICATION



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III.1. Introduction

The main goal for a proper design of miniaturized SOFCs is the reduction of the high operating temperatures typically ascribed to bulk SOFC to lower values, i.e. the Intermediate temperature (IT) range $400-800°C$). Two designing strategies are followed to achieve this goal, namely the development of ultra-thin electrolytes and the integration of them into low thermal mass structures [1-3]. First, the reduction of the electrolyte thickness down to the range of $50-500\,nm$ by using thin film deposition techniques considerably reduces the resistance associated to it, enabling lowering the operating temperature of the fuel cell to values between $400°C$ and $600°C$. Second, the integration of SOFCs into silicon-based micro electromechanical systems (MEMS) allows the fabrication of the desired low thermal mass structures, reducing the thermal response, i.e. warm-up and cycling periods, and lowering the energy consumption.

As already mentioned in *Chapter I*, mainly one basic design has been proposed up to now following these two strategies, i.e. the fabrication of ultra-thin self-supported membranes of the fuel cell functional components supported on thicker robust substrates [1-15]. A silicon substrate is commonly used to support the functional membrane of tens to hundreds of nanometres thick, including the electrolyte, the two electrodes (one at each side of the electrolytic film) and the current collectors. This way, the fabrication of thermo-mechanically stable and functional membranes supported on manageable and robust substrates is the cornerstone for the fabrication of reliable micro SOFC devices.

Utilizing silicon for fabricating robust supporting micro platforms is extremely useful. The wide series of techniques already developed for its micromachining (see *Chapter II*) allows the fabrication of accessible membranes with very high reproducibility. At the same time, it permits optimizing the device design due to the high resolution associated to MEMS fabrication processes.

In this chapter, the design and fabrication process for obtaining the free-standing functional micro SOFC membranes is described. ***Section III.2*** is devoted to describe the design and fabrication of a basic micro SOFC system, based on simple squared free-standing membranes. This design has been used in this thesis as the basic configuration for studying the compatibility between the different techniques and materials used (i.e. silicon-based materials and state-of-the-art SOFC ceramics). Also, it was used for the characterization of thin film electrolyte (YSZ) membranes on real operating conditions (described on *Chapter IV*).

Additionally, this section includes the description of an original strategy developed in this work for fabricating metallic current collectors compatible with the free-standing membrane design (***Section III.2.3***). This strategy is based on the use of *nanosphere lithography* to generate *micro*-porous metallic layers on both sides of the membranes.

Section III.3 describes a fabrication strategy that allows the obtaining of large-area membranes (up to $8\,mm^2$). As detailed later, this design means a completely new approach for the fabrication of large-area membranes, never reported before for the fabrication of micro SOFC systems. This design was used in this work for the specific characterization of the thin film electrodes developed (*Chapter V* to VII) and, finally, for the fabrication of the final micro SOFC systems including all the developed functional layers (*Chapter VII*).

III.2. The basic micro SOFC configuration

III.2.1. Micro SOFC design

Fulfilling the basic design requirements described in the introduction, a silicon-based micro platform was developed to support an ultra thin electrolyte membrane. This structure allows simple mechanical and electrical access to the functional layers involved on the fuel cell operation (the membrane). Figure III-1 shows a cross-sectional scheme of the system, where the composition of the free-standing membrane (electrode/electrolyte/electrode trilayer and current collectors) has been depicted.

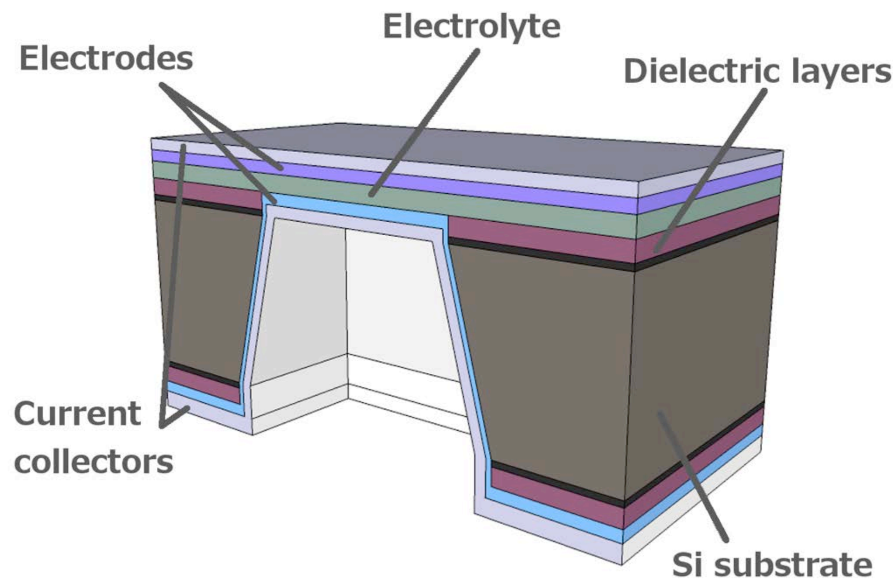


Figure III-1. *Cross-sectional scheme of the proposed device.*

The micro platform was fabricated on a $300\ \mu m$-thick Si substrate, whose centre was etched from the back side. The Si is passivated with a SiO_2/Si_3N_4 dielectric bilayer that prevents direct contact of the electrolyte with the Si substrate (which would generate electrical effects or shortcuts between the two electrodes on the future micro SOFC). Moreover, the high mechanical stability of the Si_3N_4 layer (deposited by LPCVD, see *Chapter II section II.2.2*) allowed the fabrication of silicon nitride membranes with high reproducibility and zero defects, which therefore served as excellent substrate for the deposition of functional layers by PLD.

An YSZ film was deposited on the silicon nitride for its use as electrolyte, followed by the deposition of a porous thin film cathode on top. The anode was deposited on the back side, completing the PEN (positive electrode/electrolyte/negative electrode) element of the fuel cell. The obtaining of thin and stable membranes of these functional layers is crucial for the achievement of reliable devices. It become then essential to ensure membrane thermo-mechanical stability not only after fabrication but also during operating conditions. In this sense, compatibility of the electrolyte and electrode thin films with the silicon micro platform has to be ensured, which implies the minimization of thermal mismatches that could generate cracks or delamination problems. Any defect or crack on the PEN membrane could generate fuel leaks or electrical shortcuts between the two electrodes, reducing the fuel cell performance. The specific characterization of the thermo-mechanical stability of the free-standing membranes concerning each functional layer (electrolyte, cathode, anode) is described in detail in the following chapters (*Chapters IV* to *VI)*.

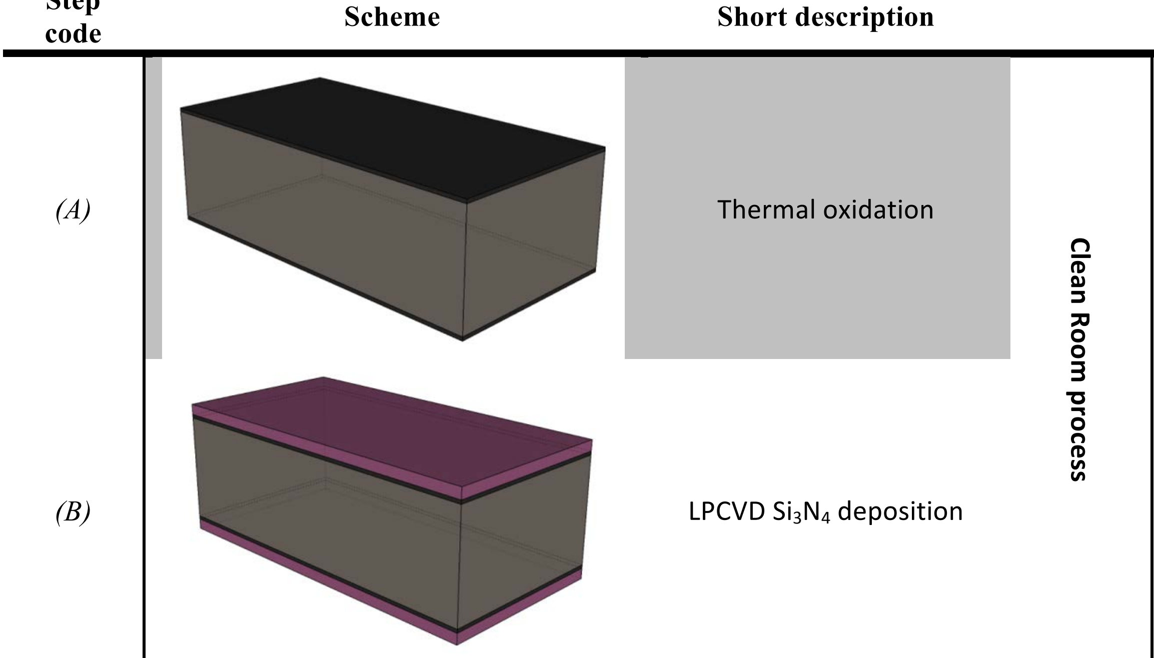
Once the PEN membrane was fabricated, current collectors were added on both sides of the membrane to reduce the in-plane resistance typically associated to thin film ceramic electrodes (see *Chapter I*, *Section I.3.2*). Nanosphere lithography was used to obtain thick patterned Pt layers, as described on ***section III.2.3*** of this chapter.

III.2.2. Micro fabrication flow

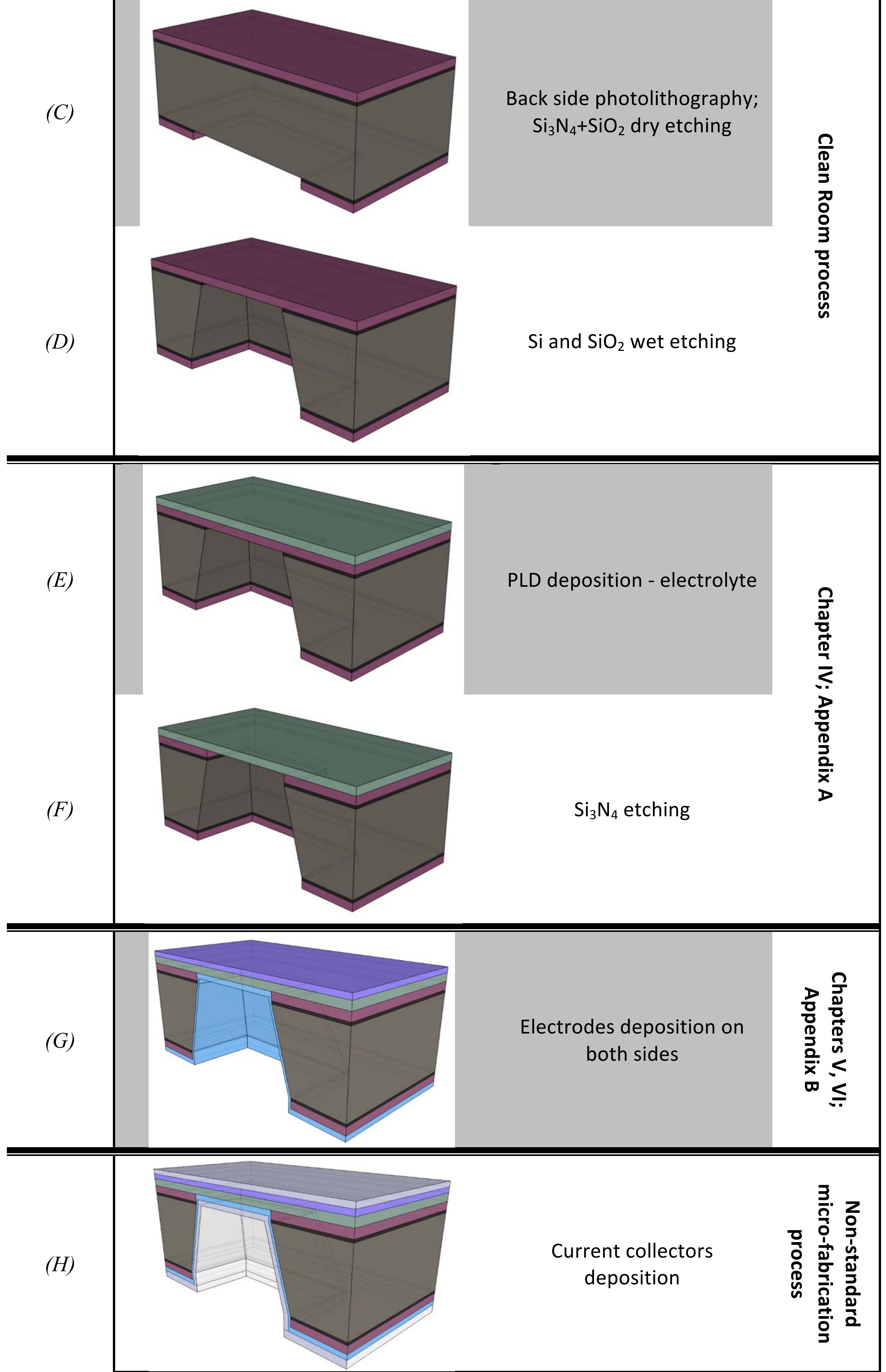
The technological processes involved in the fabrication of a basic micro SOFC are described in this section. This process combines standard silicon microfabrication technology [16], with thin film deposition techniques such as PLD [17]. The process was carried out in the Clean Room facilities at IMB-CNM until reaching the functional layers deposition step, which was performed at CIN2 and IREC facilities.

Table III-1 depicts the consecutive steps of the fabrication flow for obtaining the free-standing membranes. Starting from single crystal (100)-oriented p-type silicon wafers of $100\,mm$ diameter and $300\,\mu m$ thick, the substrates were first thermally oxidized obtaining a $100\,nm$ thick layer of SiO_2 (*A*). Afterwards, low-pressure chemical vapour deposition (LPCVD) was used to grow $300\,nm$ thick layers of Si_3N_4 on both sides of the wafer (*B*). The previously deposited SiO_2 layer ensures a good adherence of silicon nitride to the substrate. This double deposition provided thin dielectric bi-layers for a proper isolation between the functional layers and the silicon substrate, and was also used as basic structure for the deposition of layers by PLD.

Table III-1. *Scheme of the fabrication flow of a standard micro SOFC*



Step code	Scheme	Short description	
(A)		Thermal oxidation	Clean Room process
(B)		LPCVD Si_3N_4 deposition	


(C)
Back side photolithography; Si_3N_4+SiO_2 dry etching
(D)
Si and SiO_2 wet etching
Clean Room process
(E)
PLD deposition - electrolyte
(F)
Si_3N_4 etching
Chapter IV; Appendix A
(G)
Electrodes deposition on both sides
Chapters V, VI; Appendix B
(H)
Current collectors deposition
Non-standard micro-fabrication process

Then, a photolithographic step on the back side of the wafer was carried out to define the membrane opening windows (from $260x260\ \mu m^2$ to $930x930\ \mu m^2$) on the silicon nitride. Back side Si_3N_4 layer was used as mask during the silicon micromachining process. An image of the mask design utilized in this process was already shown in Figure II-1 (*Chapter II*, Section II.2.2). Si_3N_4 and SiO_2 layers were etched by Reactive Ion Etching (RIE) until arriving to the silicon substrate (*C*).

Back side silicon anisotropic etching was then performed in a KOH solution. The process stops naturally when the SiO_2 dielectric layer is reached, therefore releasing SiO_2/Si_3N_4 membranes. The anisotropy of the Si etching (forming truncated pyramids with an angle of 54°) yielded to $210\ \mu m$ smaller membranes in length than the initial back side opening, i.e. from $50x50\ \mu m^2$ to $820x820\ \mu m^2$. Then, a wet etching in HF solution was carried out to remove the SiO_2 layer yielding free-standing membranes of Si_3N_4 (*D*). The resulting Si_3N_4 membranes (top side) were the basic structure used as substrate for the deposition of YSZ by PLD.

It is important to notice here that the low resistance of YSZ to the etchants used in the micromachining process compelled the deposition of YSZ to be made directly onto the Si_3N_4 membranes instead of over the bulk $Si/SiO_2/Si_3N_4$ system. In particular, HF needed to etch SiO_2 layers quickly degraded YSZ films and long exposures to KOH – needed to remove the silicon bulk also had a visible effect on the YSZ film surface.

Fabricated wafers were diced into chips of either $6x6\ mm^2$, $10x10\ mm^2$ (one single Si_3N_4 membrane per chip) or $12x12\ mm^2$ (four membranes per chip). Figure III-2 show images of one of the microfabricated wafers before dicing (a), as well as single $6x6$, $10x10$ and $12x12\ mm^2$ chips as used on PLD depositions (b). When moving to large-area PLD, dicing was no further required as the equipment supported $4''$-wafer level substrates.

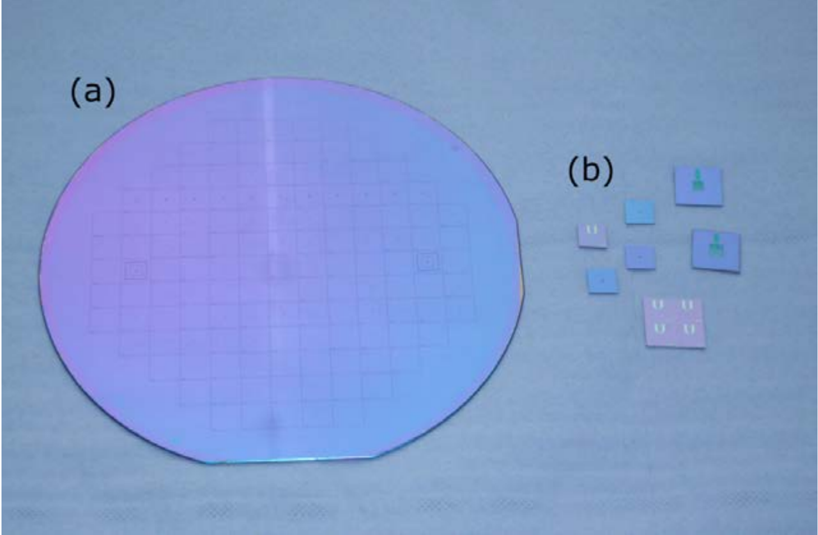


***Figure III-2**. Image of a patterned wafer (a) and different size chips already diced (b), all of them used as substrates for PLD depositions.*

Dense YSZ layers of different thicknesses were deposited on the chips/wafers over the Si_3N_4 yielding Si_3N_4/YSZ membranes (*E*). Deposition conditions are described in detail on *Chapter II*, *Section II.3.1*. A RIE step was used to remove the $300\ nm$-thick Si_3N_4 from the Si_3N_4/YSZ bi-layers, therefore releasing YSZ free-standing electrolytic membranes (F). Complete elimination of the silicon nitride layer was ensured by monitoring its thickness using reflectometry. Etching time had to be calibrated as the fact of etching the Si_3N_4 from the back side through a *cavity* (resultant from the Si wet etching, see scheme on Table III-1 (F)) caused a diminution of 20% on the etching rate. Figure III-3 shows optical images of some of the YSZ membranes after step (F).

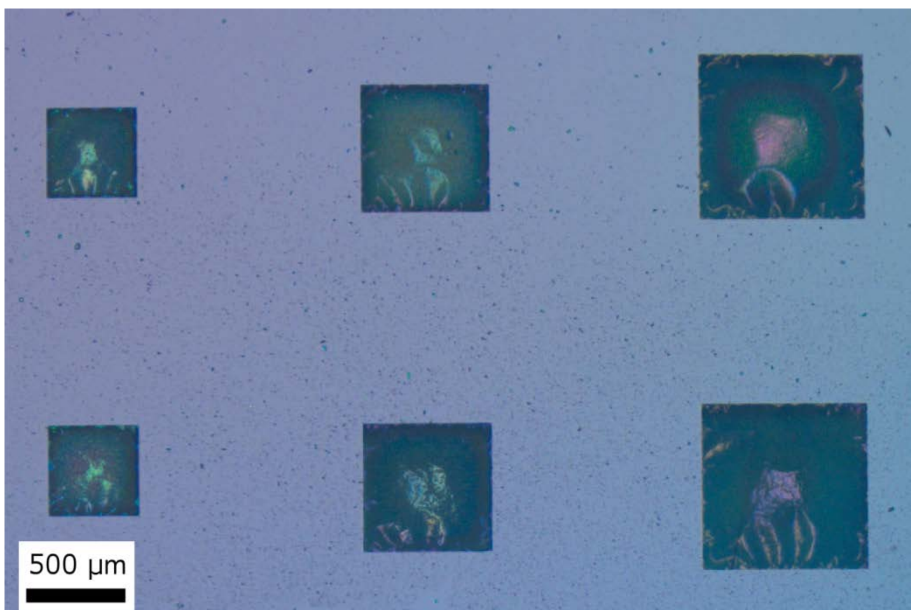


Figure III-3. *Optical images of a series of YSZ free-standing membranes with different sizes.*

The microstructural, thermo-mechanical and electrochemical properties of the YSZ films, both in thin film form (onto Si substrates) or as free-standing membranes, were studied in detail and are presented in *Chapter IV*. From the characterization, it was seen that factors like deposition conditions, target composition and microstructure and presence of particulates appeared during deposition could originate fatal defects on the membranes, such as pinholes or cracks. In this sense, different strategies had to be developed to improve film quality, as described in *Appendix A*.

The micro fuel cell core was completed by depositing the electrodes at both sides of the electrolytic membrane (*G*). Different materials were tested in this work, either based on porous metallic thin films or complex oxides (ceramics). Sputtering (Pt-based electrodes) or again PLD (ceramic-based electrodes) were used for the deposition of these functional layers. Unfortunately, the use of metals as electrodes on the final micro SOFC device was finally discarded due to their thermal instability under operating conditions. The specific experiments and encountered problems related to the use of thin film metals on membrane-based micro SOFC are described in *Appendix B*. On the contrary, ceramic-based electrodes were satisfactorily implemented on functional membranes. The particular studies of porous LSC for working as thin film cathodes and CGO for thin film anodes are presented on *Chapters V* and *VI*.

Finally, last step of the process (*H*) was the implementation of metallic current collectors. This way made by nanosphere lithography, as detailed on next section.

III.2.3. Metallic current collectors for free-standing membrane based micro SOFC

Taking into account that thickness of thin film electrodes in the suspended PEN structure is set below $1\ \mu m$, the in-plane resistivity associated to them is usually high, particularly on ceramic-based films. As described in *Chapter I* (*section I.3.2*), the typical resistance values associated to the in-plane electronic percolation on thin ceramic-based electrode films (such as the used in this thesis) can be hundreds of ohms, which would significantly lower the fuel cell performance (too high associated-resistance). To improve this, metallic current collectors are usually implemented over the electrodes. Typical resistance values associated to several hundreds of nm thick metallic films (as the ones used here for current collection) are below $1\ \Omega$, therefore contributing very little to the whole fuel cell resistance losses.

Opposite to porous thin metallic electrodes, in which maximizing the porosity is very important (reactions are confined to the pores, i.e. TPBs), the only function of current collectors is gathering the electrons from the fuel cell reactions and driving them towards an external load. This way, as there is no need of TPB length maximization, they can be fabricated dense and thicker, which makes them more thermally stable. However, as pointed out in *Chapter I*, the fact of being dense makes the area covered catalytically inactive (as there is no gas diffusion through the metallic layer), and the reactions are confined only to the uncovered area. It becomes then necessary to create a porous network, i.e. dense layer but with patterned micro pores. In this work, dense Pt grids were fabricated by using a non-conventional lithographic step and implemented on both sides of the self-supported membranes.

It is important to notice here that, if a grid is intended to be well-defined on both sides of the membrane, it becomes necessary to use a technique capable of covering substrate steps like the one generated on the back side of the substrate. Conventional optical lithography has been proved unsuccessful on covering 3D morphologies, drastically loosing spatial resolution when defining patterns through deep cavities. Therefore, the fabrication of regularly patterned current collectors (with patterns below $1\ \mu m$) was achieved by implementing a non-standard technique, i.e. nanosphere lithography [18].

Fabrication of current collectors by nanosphere lythography

Figure III-4 shows an scheme of the fabrication process of metallic current collectors by using nanosphere lithography. Top view SEM images corresponding to each fabrication step are also included in the figure for better understanding. First, a monolayer of $\sim 800\ nm$ diameter polystyrene (PS) balls was deposited at both sides of the membrane (a,b). To do so, a monolayer of balls was formed on top of a water-based solution and compacted by adding a surfactant. Afterwards, the monolayer was transferred from the solution to the top of the sample by immersing it below the PS spheres and taking it out. Once dried, a perfectly ordered monolayer of balls was obtained on top of the electrode films.

Then, the ball size was reduced by etching the PS using O_2 plasma RIE ($0.01\ mbar$,$150\ W$) (c,d) [19]. The final ball diameter was fixed to be $600\ nm$, thus defining a separation between balls of $200\ nm$. A $150\ nm$-thick Pt film was then deposited on top of the PS spheres by sputtering (e,f). A dense Pt grid was therefore defined, where the pores correspond to the etched PS balls. Maximum thickness able to deposit was defined by the ball half height (radius), in order to avoid a complete coverage of the balls and ensure the pore formation once the balls were eliminated. This condition set a maximum film thickness of $300\ nm$.

On a final step, the balls were burned in air ($2\ h$ at $T = 500$°C) (g,h). It is important to notice here that, after PS burning and sphere removal, Pt caps coming from the Pt deposited over the PS balls still remained on the surface. A FIB analysis was carried out in order to ensure the complete removal of PS and the caps cross-section. As shown in the inlet of Figure III-4 (h), Pt caps appeared empty and semi-dettached from the Pt film of the base. Therefore, in the end, a dense and well-ordered Pt grid was always obtained.

Figure III-5 shows an optical image of a self-supported membrane covered by PS balls on its back-side. This particular image confirms that this lithography technique allows the fabrication of Pt current collectors on both sides of the membrane, as good resolutions are obtained either on the front and planar side of the membrane or through the back side cavity.

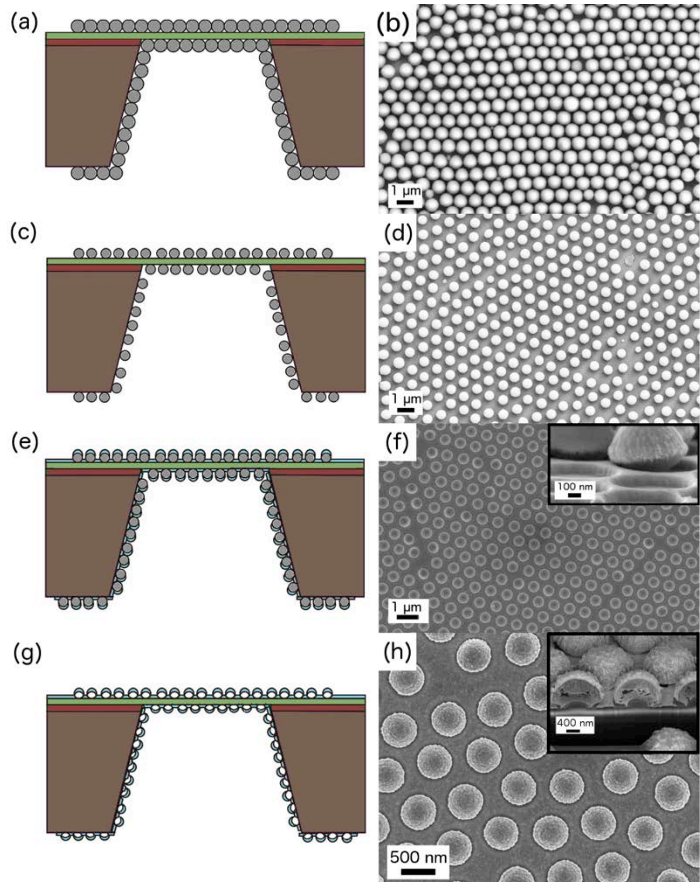


Figure III-4. *Cross-sectional scheme and top view SEM images of the consecutive steps for the fabrication of metallic current collectors by nanosphere lithography. The inlets in (f) and (h) show additional cross-sectional views for better understanding.*

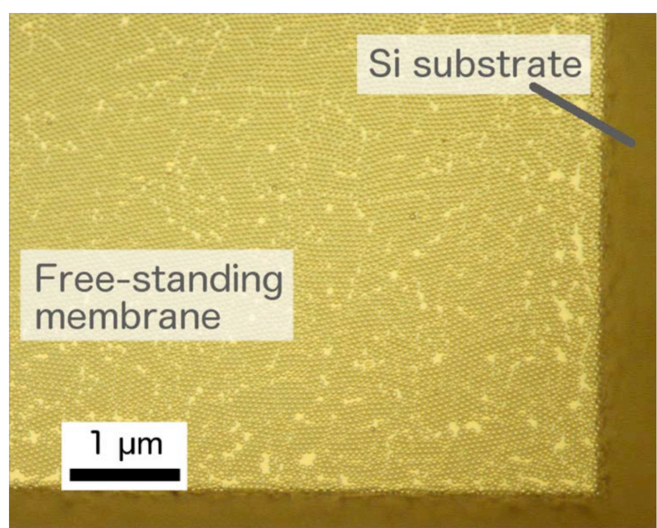


Figure III-5. *Optical image of a membrane covered of balls from the back side (the image shows a corner of the membrane, and the dark yellow/light yellow on the membrane corresponds with the covered/uncovered zones by balls)*

Stability during working conditions

The fabricated Pt grids showed good current collection having low resistance and low degradation with temperature. Top view SEM images on Figure III-6 show the microstructure evolution of the Pt mesh after long-term ($> 10\ h$) operation at $T = 700$°C. The images reveal a microstructural change, but porosity and connectivity on film are maintained. Moreover, it was seen that the caps disappeared after thermal cycling

of the samples, presumably due to the extreme working conditions and the gas flow applied to each side of the membrane (oxidizing and reducing gases).

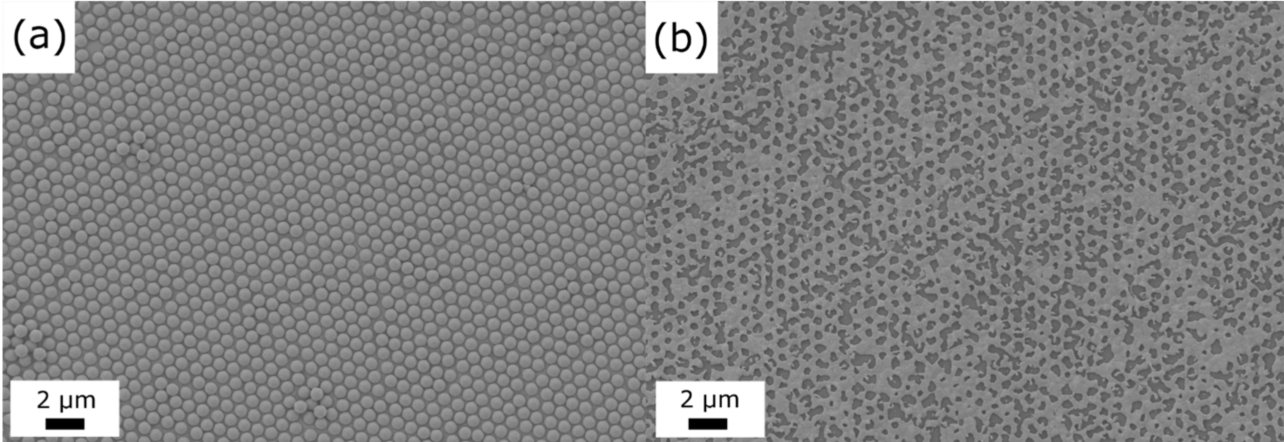


Figure III-6. *SEM top view images of a Pt current collector fabricated by nanosphere lithography, as-deposited (a) and post-measurement (b).*

III.3. Large-area micro SOFC: Second generation of micro SOFC

III.3.1. Large-area micro SOFC design

The reduction of the thickness of the membrane (required to minimize the resistance associated to the electrolyte) usually generates a limitation on the maximum area obtainable on a single self-supported membrane. The aspect ratio obtained on square membranes using the basic micro SOFC design is already huge ($1:10^7$), but still the maximum membrane size is commonly limited to less than $500x500\ \mu m^2$. Free-standing membranes with higher areas suffer cracks, which provoke leakages between both sides of the electrolyte and shortcuts the anode and the cathode of the cell. This limitation on the maximum area achievable imposes a limitation on the maximum power that can be obtained with a single device. In the last few years, only a few groups have presented strategies for enlarging the membrane area [9,20,21]. Among them, Ramanathan and co-workers proved the fabrication of large-area membranes with sizes of $5x5\ mm^2$ (a maximum free-standing area of $4x4\ cm^2$ was achieved but not tested), based on the use of dense metallic grids as support. Those metallic grids were deposited at one side of the membranes (top side) by standard photolithography after the fabrication of the anode/electrolyte/cathode tri-layer and served also as current collectors.

In this work, we propose a new approach for enlarging the size of the membranes. Membrane dimensions are enlarged by using a mesh of silicon slabs as supporting structure. Figure III-7 shows a schematic view of the proposed large-area micro SOFC, where the different components of the device are pointed out. Compared to previously published strategies, this approach involves fabrication processes fully compatible with silicon micro fabrication technology. Through this strategy, free-standing membranes up to $8\ mm^2$ were fabricated, which means an increment of $\sim 30x$ versus the basic squared membrane designs previously presented.

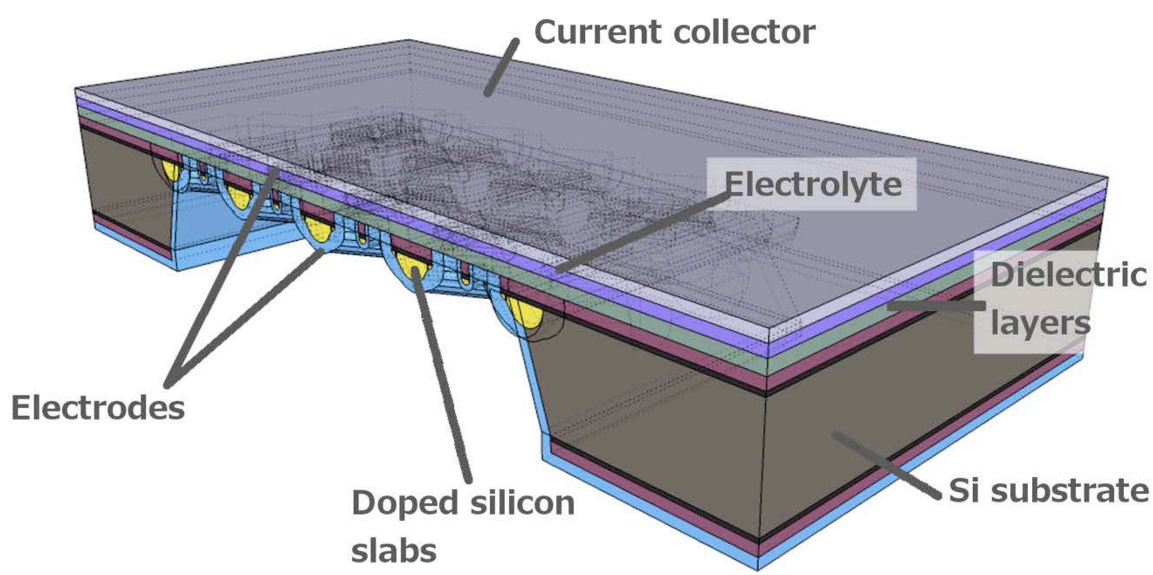


Figure III-7. *Cross-sectional scheme of the proposed large-area micro SOFC.*

Main designing considerations

A top-view optical image of the large-area membrane is depicted in Figure III-8. The image shows the hexagonal packing that was chosen as optimal grid design. After testing different alternatives, i.e. squared and circular designs, the hexagonal geometry was chosen as it guaranteed the best packaging and membrane stability. Silicon slab thickness was fixed to be 5 μm and a series of narrower *secondary* slabs were added dividing single hexagonal cells in the central part of the membrane into six triangles[1]. Simulations on heat distribution along the membrane (not presented here) showed these secondary slabs to be beneficial for temperature homogenization, either during start-up operation (heat distribution from external source) or during steady state (extra heat releasing). Membrane sizes and *primary* slabs density (width and separation between them) were systematically varied in order to test the maximum total membrane area and single hexagonal membrane area achievable. Table III-2 summarizes the main features varied in the designs and the obtained areas in each case.

[1] ***Note:*** Membrane designs and, in particular, grid designs also included several considerations for heat distribution and future micro heater integration, supported on the silicon slabs grid. While micro heater operation, external single hexagonal cells are considered inactive (heat isolation function), and for this reason secondary slabs are only implemented on the central part of the large-area membrane.
At the same time, slab sizes slightly varied too as a function of their position on the large-area membrane, according to the micro heater design (see Table III-2).
This is explained with greater detail in *Section III.3.3* of this chapter.

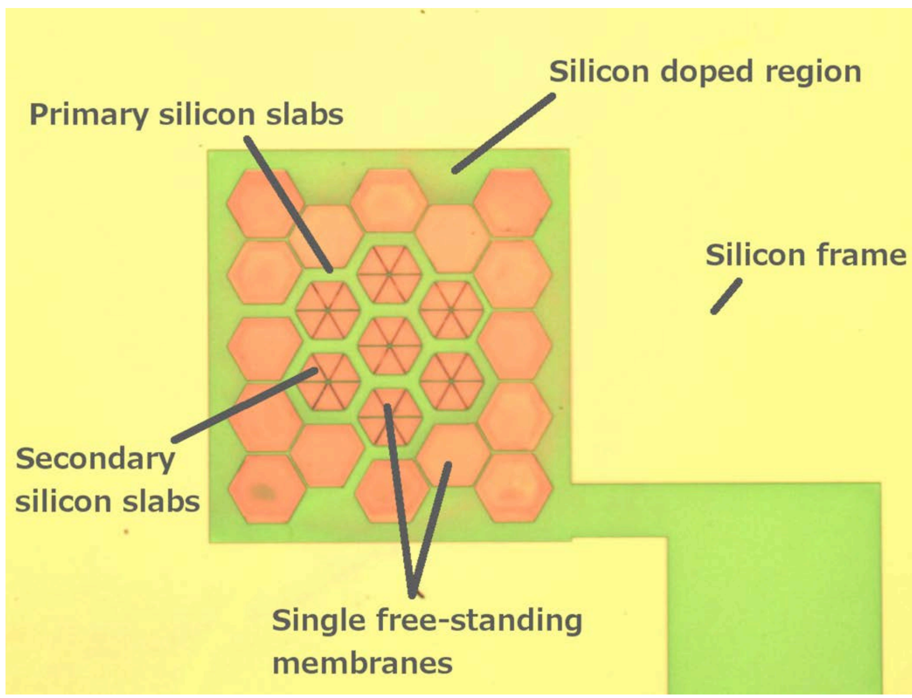


Figure III-8. *Top-view optical image of a large-area free-standing membrane.*

Table III-2. *Single membrane and total large-area membrane sizes of the different designs fabricated in this work.*

Membrane code	Silicon primary slabs width (μm)	Single hexagonal membrane size (μm^2)	Total membrane size (including slabs) (mm^2)	Total membrane size (only active area) (mm^2)
31D	$15-50$	$5.85 \cdot 10^4 - 8.05 \cdot 10^4$	2.20	**1.70**
31A	$25-75$	$5.85 \cdot 10^4 - 8.80 \cdot 10^4$	2.50	**1.80**
31C	$15-75$	$5.85 \cdot 10^4 - 9.40 \cdot 10^4$	2.50	**1.90**
31B	$25-75$	$1.60 \cdot 10^5 - 2.10 \cdot 10^5$	5.85	**4.50**
51D	$15-50$	$5.85 \cdot 10^4 - 8.05 \cdot 10^4$	4.25	**3.20**
51A	$25-75$	$5.85 \cdot 10^4 - 8.80 \cdot 10^4$	4.90	**3.30**
51C	$15-75$	$5.85 \cdot 10^4 - 9.40 \cdot 10^4$	4.90	**3.40**
52A	$25-75$	$5.85 \cdot 10^4 - 8.80 \cdot 10^4$	8.00	**6.10**
51B	$25-75$	$1.60 \cdot 10^5 - 2.10 \cdot 10^5$	11.30	**8.35**

III.3.2. Micro fabrication flow

Similar to the basic micro SOFC fabrication flow, the fabrication of large area membranes is based standard microfabrication processes. Table III-3 summarizes the fabrication steps required for finally obtaining the large area micro SOFC. The main modification here is the introduction of a new photolithographic step at the beginning (A), which was used to expose a silicon area to boron doping. Doped silicon regions yielded the membrane supporting grids at the end of the microfabrication process. Figure III-9 shows the mask design used for this photolithographic step, in which the different membrane designs are distributed along the wafer area in $1x1\ cm^2$ chips.

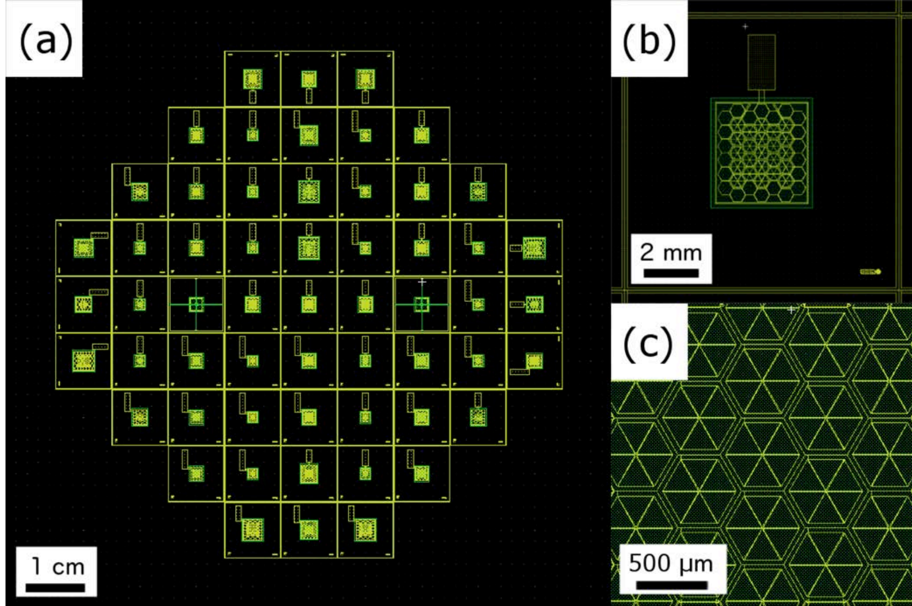
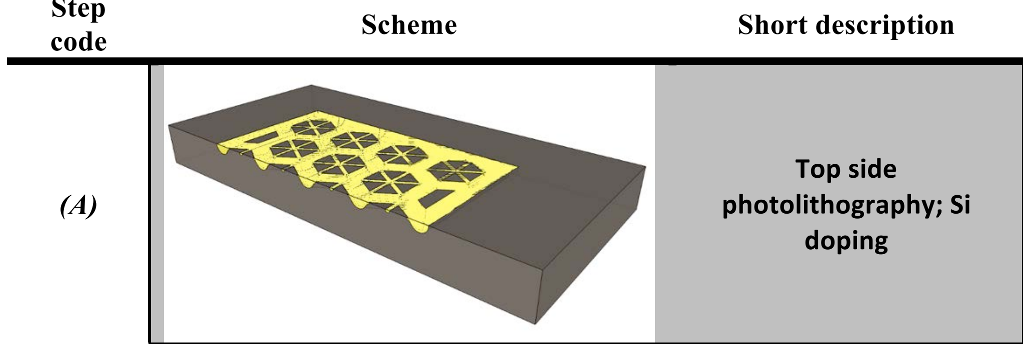


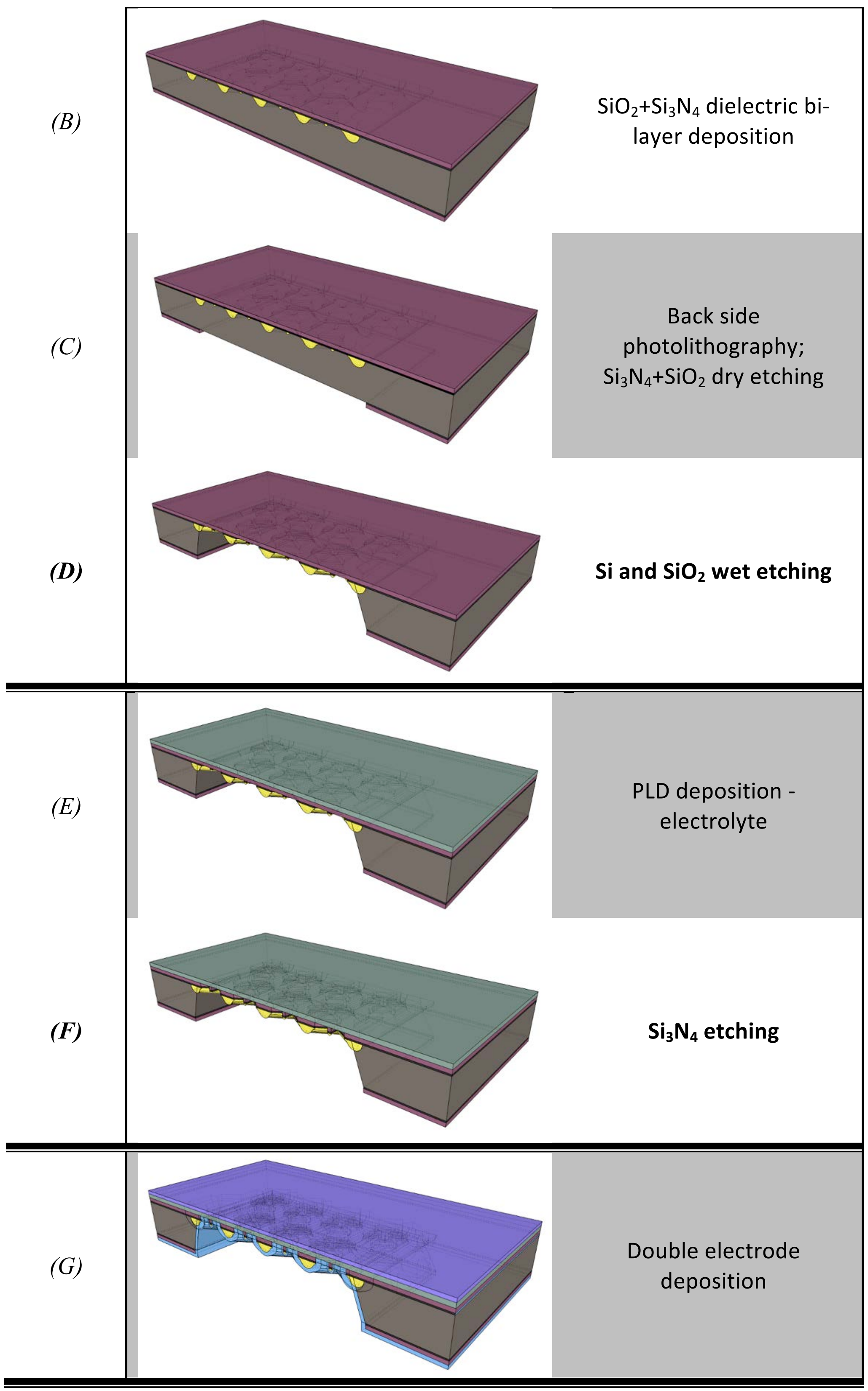
Figure III-9. *Layout of the set of masks used for the fabrication of large-area membranes; general view (a) and different magnifications of a single device (b,c). Two different photolithographic levels are represented, i.e. top side photolithography for step (A) in the process – yellow, and back side photolithography for step (C) in the process – green.*

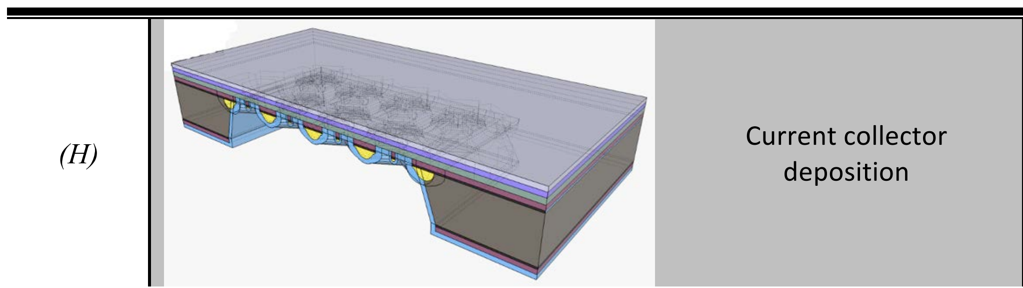
Si anisotropic etchants like KOH do not affect heavily doped p regions since the etch reaction needs free electrons to proceed and the presence of electrons is scarce in the material. In the case of those p^{++} regions, the etch rate is not zero but drastically decreases when boron concentration is above $1019\ cm^{-3}$ [22]. The high boron concentration required the use of solid sources and high processing temperatures (1240℃). The doped silicon slabs have a semi-circular section due to the isotropic diffusion profile obtained during the doping process.

In a second step (*B*), the SiO_2/Si_3N_4 isolation bi-layer was grown over the silicon substrate, which was also used as passivation of the highly doped silicon slabs. Then, a photolithographic step defined rectangular pads where the dielectric layers were removed by RIE (*C*), much bigger in this case than in the process described in *section III.2.2* fro basic squared membranes. Windows from $2x2\ mm^2$ to $3.7x3.7\ mm^2$ were defined, coinciding with the doped silicon zone in each of the membrane designs.

Table III-3. *Scheme of the fabrication flow of large-area micro SOFC. The steps significantly different from process described in Table III-1 are marked bolded.*

Step code	Scheme	Short description
(A)		**Top side photolithography; Si doping**


(B)
SiO_2+Si_3N_4 dielectric bi-layer deposition
(C)
Back side photolithography; Si_3N_4+SiO_2 dry etching
(D)
Si and SiO_2 wet etching
(E)
PLD deposition - electrolyte
(F)
Si_3N_4 etching
(G)
Double electrode deposition



The silicon substrate was then etched (*D*) from the back side by wet etching. As previously mentioned, doped silicon zones were not etched due to their high selectivity to KOH etching, thus the silicon slabs grids were obtained after this step. The obtained membranes ranged from $1.8x1.8\ mm^2$ up to $3.5x3.5\ mm^2$ and were then used as substrate for the electrolyte deposition on next step.

The electrolyte layer was deposited over the silicon nitride by PLD (*E*). Once obtained the YSZ/Si_3N_4 bi-layer membrane, the silicon nitride was etched by RIE from the back side to release the YSZ membranes (*F*). RIE etching selectively removed the Si_3N_4 layer, leaving unaltered the silicon slabs. Finally, the electrodes and current collectors were deposited on both sides (*G*). As described in the following section, doped silicon high electronic conductivity could be used for current collection. Therefore, as the back side electrode is in direct contact with them, depositing additional current collectors on that side can be avoided.

Figure III-10 shows optical images of two YSZ large area membranes of two different sizes already released, compared to similar Si_3N_4 membranes before PLD deposition. A buckled pattern was always obtained when releasing YSZ, due to a combination of different stresses generated during the fabrication process (see *Chapter IV*).

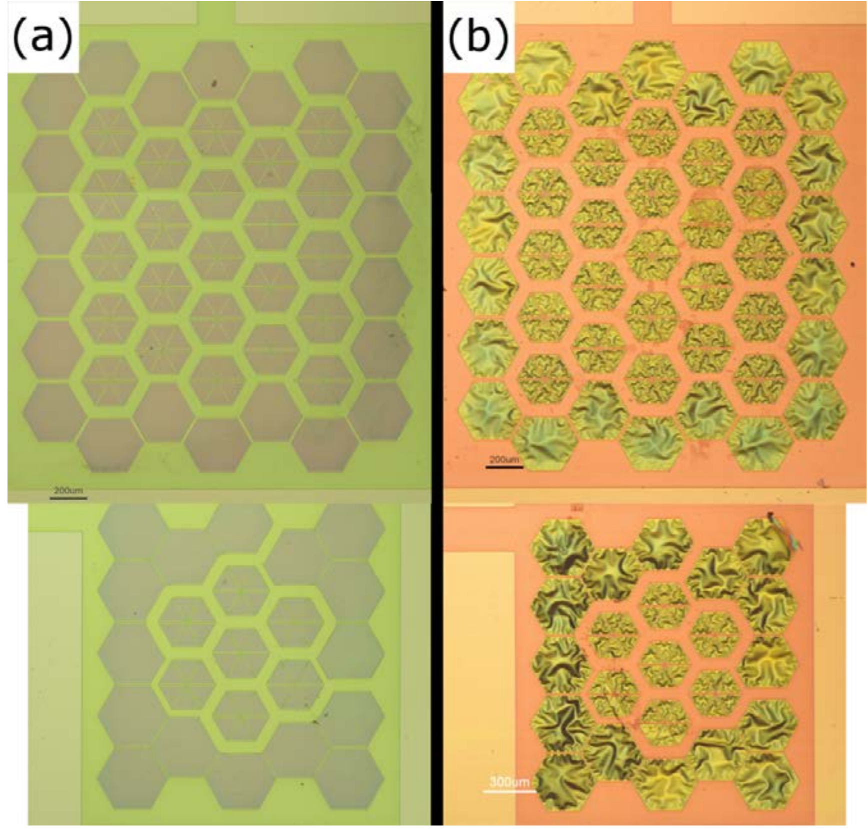


Figure III-10. *Optical images of Si_3N_4 (a) and YSZ (b) free-standing membranes of different sizes.*

III.3.3. Main advantages of the large-area configuration

Silicon slabs, besides serving as robust support for the free-standing membrane, can be used for further functions, namely current collection, temperature distribution and/or micro heater integration. First, it has been already pointed out that doped silicon slabs can be used for collecting current from one of the electrodes of the cell. Deposition of back side electrode is directly made over the doped silicon slabs at the same time as the free-standing electrolytic membrane, thus establishing direct contact with them and allowing the current collection (see Figure III-7, back side electrode). Electrical connections for both the anode and the cathode can then be placed on the same side of the device, thus simplifying the device encapsulation and contacting. In this sense, buried doped silicon paths can connect the grid with an opening contact pad. Figure III-11 shows an optical image of one of this doped silicon buried paths coming from the slabs grid to an opening pad on top side of the substrate.

At the same time, the highly conductive silicon slabs are useful for heat distribution along the membrane. Both during start-up (when out-coming heat is needed for operation) and on steady state (when extra heat from the exothermal reactions must be taken out), the silicon slabs act as temperature homogenizer. The exothermic nature of micro SOFC fuel cell reaction [23] generates an amount of heat that must be released from the membrane in order to maintain reliable working temperatures. Taking into account the low thermal conductivity of the functional layers [24,25], added to the large size and small thickness of the membrane, the presence of the silicon slabs could be useful for releasing the extra heat.

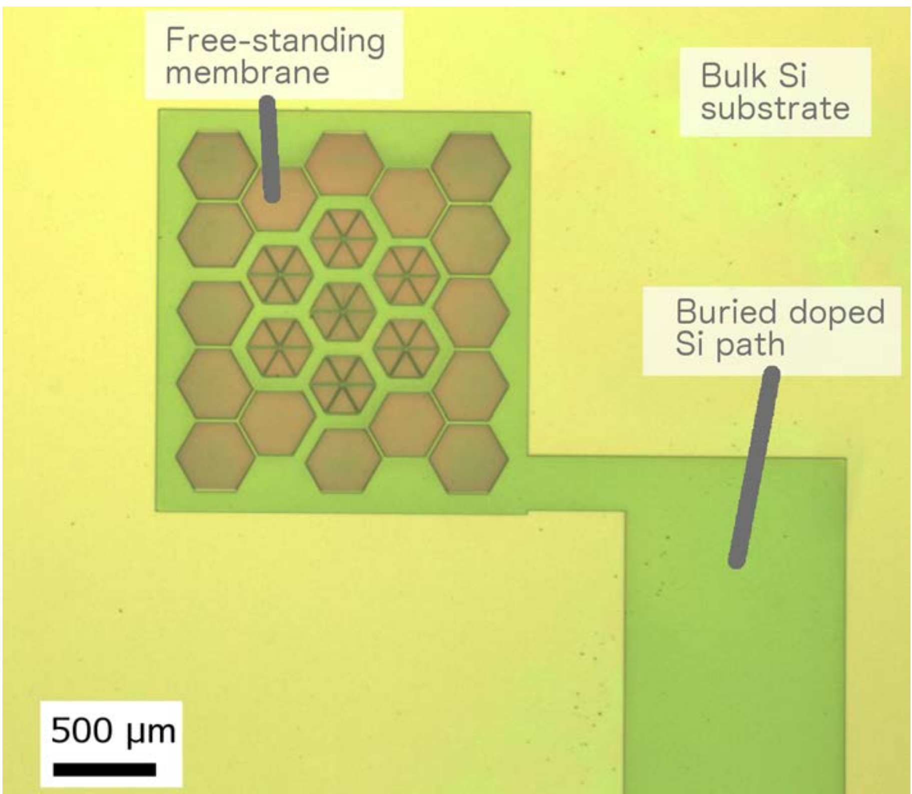


Figure III-11. *Optical image of a membrane showing the buried doped silicon path.*

Moreover, although only slightly addressed in this work, integration of micro heaters onto the free-standing membrane is a very interesting approach for a fast and energy efficient start-up of micro SOFC systems (important to remember here is the high temperature needed for operation). By implementing a micro heater for directly heating the low thermal mass free-standing membrane, the energy consumption on the start-up process is minimized. Silicon slabs grid designs developed in this work already include the possibility of direct implementation of micro heating coils. In particular, the silicon slabs have a double

purpose for the heater integration. On one hand, they act as robust support for the micro heater paths, being thermomechanically (when heating up) and electrochemically (dielectric layers for isolation) stable. On the other hand, the few μm-thick silicon under the heater in the membrane is very useful as a heat spreader, uniformizing the temperature in the device active area, that otherwise would exhibit a spatial distribution replicating the meander shape of the heater [26]. In this sense, the developed design additionally includes a series of narrower *secondary* slabs for heat spreading to the free-standing zones far from the micro heater coil.

Special wider paths were fabricated for supporting metallic coils serving as heaters (this particular work was based on previous simulations, not included in this thesis work but detailed in [27]). Testing devices were fabricated as proof-of-concept, although characterization and device optimization is yet to be performed. $250\ nm$-thick tungsten films were deposited over the silicon wafers after depositing the dielectric layers (between step (*B*) and step (*C*) on Table III-3) and the metallic coils were defined afterwards by photolithography and subsequent metal etching (lift-off process). An additional dielectric bi-layer ($200\ nm$ SiO_2 + $300\ nm$ Si_3N_4) was then added as passivation layer prior to free-standing membrane releasing and functional layers deposition on top of it (steps (*C*) and following on Table III-3). Figure III-12 shows a Si_3N_4 free-standing membrane already with a micro heater integrated. In this configuration, the series of single hexagonal membranes close to the bulky substrate are considered inactive during start-up process.

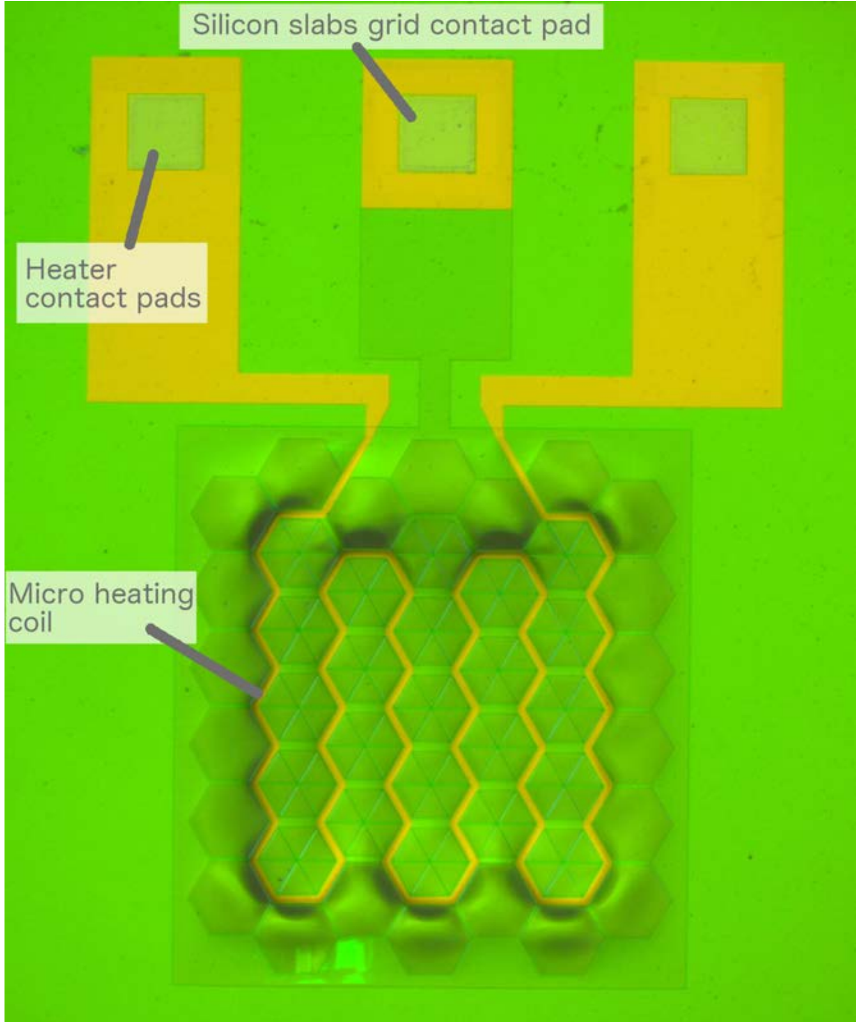


Figure III-12. *Si_3N_4 free-standing membrane with an integrated micro heating coil supported on the silicon slabs grid. Heater and slabs grid (for current collection) contact pads can be also seen.*

III.4. Conclusions

The fabrication processes required for obtaining two different membrane configurations have been presented in this chapter. First, a basic micro SOFC configuration based on squared free-standing membranes was fabricated. Several groups have already reported this basic structure as the standard configuration for micro SOFC systems. In this work, the fabrication process was adapted to IMB-CNM's Clean Room facilities, and a high reproducibility on fabricating it was obtained in this work. Functional cathode/electrolyte/anode square free-standing membranes were satisfactorily fabricated using YSZ as electrolyte material and either metals or complex oxides (LSC cathode, CGO anode) as electrodes.

Then, a new large-area membrane design was developed in this work for the first time, based on the use of a silicon slabs grid as robust support for the larger membranes. Being able to completely integrate the silicon grid fabrication on the microfabrication flow of the micro SOFC, this strategy represents a completely new approach for the fabrication of reliable large-area functional membranes, and permits enlarging the maximum achievable power per single micro SOFC device. Free-standing membranes of the functional materials were fabricated reaching to an increment on the total free-standing area of $\sim 30x$ compared to the basic membrane design. Additionally, the use of the silicon slabs for further functions i.e. current collection and micro heater integration was presented here.

Finally, the fabrication of metal-based current collectors implementable on both sides of the micro SOFC membranes was also shown. Based on the use of nanosphere lithography, dense Pt grids thermo-mechanically stable were fabricated and their stability was proved during real micro SOFC operating conditions.

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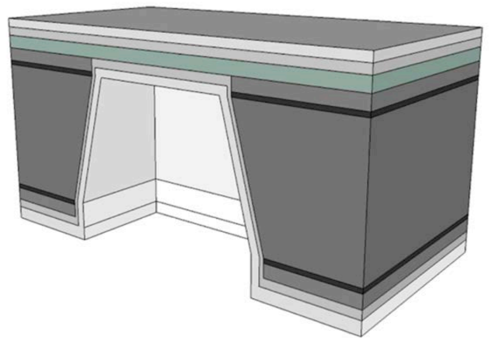
IV. MICRO SOFC ELECTROLYTE: SELF-SUPPORTED YSZ-BASED ELECTROLYTE MEMBRANES



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IV.1. Introduction

One of the major drawbacks usually ascribed to SOFC technology is its high operating temperature ($T > 800$℃), mainly due to the low values of conductivity reported for the state-of-the-art electrolytes such as yttria-stabilized zirconia (YSZ) [1]. However, as it has been mentioned in previous chapters, problems associated to high operating temperatures and long start-up times partially disappear when SOFCs are integrated in micro electromechanical systems (MEMS) [2]. In combination with a reduction of the electrolyte thickness below the micron range by using thin film deposition techniques, e.g. Pulsed Laser Deposition (PLD), it is possible to lower the operating temperature to the range between 300℃ and 700℃ suitable for micro SOFCs [3,4].

When reducing the electrolyte thickness to the sub-millimeter range, its contribution to the overall fuel cell resistance is decreased. In this sense, not only the reduction of the electrolyte thickness to values comparable to the grain size but also the reduction of this grain size to the nanoscale have been proposed as strategies for reducing the resistance associated to the electrolyte ionic conduction [5,6] and surface exchange [7]. In the last years, big efforts have been devoted to understand these and other effects of nanoscale on ionic transport. The fact that thin films cannot be prepared without a substrate intrinsically affects thin film properties, e.g. stress induced by the substrate, thus complicating any type of characterization.

The overall performance and reliability of thin film-based devices primarily depend on their thermomechanical stability, which is directly related to the residual stress generated during the fabrication process. In thin films, the presence of important residual stresses might reduce the adhesion or produce delamination of the deposited layer and, in the worst case, lead to failure of the micro fabricated PEN structure when it is released from the substrate. Recently formulated design maps for micro SOFCs pointed out the importance of understanding the origin of thermal and intrinsic residual stresses in order to maximize device resistance to fracture and buckling [8,9].

In addition, comprehensive understanding of the ionic conduction across the thin electrolyte as well as the evolution with the temperature of its microstructure and mechanical stress is of the utmost importance if the final performance of the device is to be optimized. In all of the reported micro SOFCs [10], the active area is restricted to the free-standing part of the thin film; therefore, special emphasis should be put in its specific characterization. Strong differences are expected between attached and suspended thin films, e.g. in the stress state [11-13] and the electrical behaviour [14,15].

The present chapter, based on the published works [11,16] addresses the characterization of YSZ free-standing membranes fabricated by PLD. A detailed study of the residual stress generated on the membranes is presented on ***section IV.2***, yielding a set of experimental conditions that allow tuning their state of stress. The study puts particular emphasis on the stress evolution of the membrane with the temperature, i.e. the thermomechanical stability, and the correlation of this mechanical evolution with microstructural changes on the films. ***Section IV.3*** deals with the electrochemical characterization of the electrolytic membranes. Both in-plane and cross-plane conductivity of YSZ thin films are presented and discussed here.

IV.2. Thermo-mechanical behavior of YSZ membranes

As described on *Chapter III*, two different membrane designs were fabricated in this work, referred as *basic* and *large-area* self-supported membranes. However, the characterization of YSZ membranes was only made on basic squared membranes. Their simpler design allowed an easier study of some of the properties (i.e. stress buckling profile). YSZ square membranes of thicknesses $t = 60 - 500\ nm$ and edge lengths ranging from $a\ =\ 50\ \mu m$ to $820\ \mu m$ were fabricated.

IV.2.1. Microstructural optimization on YSZ membranes

YSZ thin film deposition

Dense YSZ films were obtained by using the set of conditions detailed on *Chapter II* (*Section II.3.1*), in a range of temperatures from $T_S = 200°C$ to $T_S = 800°C$. A simple $8\ mol\%$ YSZ (8YSZ) target prepared by conventional sintering (see *Chapter II*, *Section II.3.2*) was used for the whole series of PLD depositions performed in this study.

Films from $60\ nm$ (4,000 pulses) to almost $500\ nm$ thick (30,000 pulses) were fabricated, thus deposition rate was estimated at $0.15\ Å/pulse$ for 8YSZ films. Reflectometry was routinely used for measuring YSZ film thicknesses and growth rate calibration, in combination with cross-sectional SEM imaging. Figure IV-1 shows an example of a reflectometry interferogram obtained in this work, fitted for an YSZ/Si_3N_4/SiO_2 multilayer over bulky Si. By fixing the known SiO_2 and Si_3N_4 thicknesses (tested before YSZ deposition, being $100\ nm$ and $300\ nm$ respectively), it was then possible to get the YSZ film thickness from the fitting. Similar thicknesses than those obtained from reflectometry were always obtained by SEM, validating the use of the technique for the rest of the study.

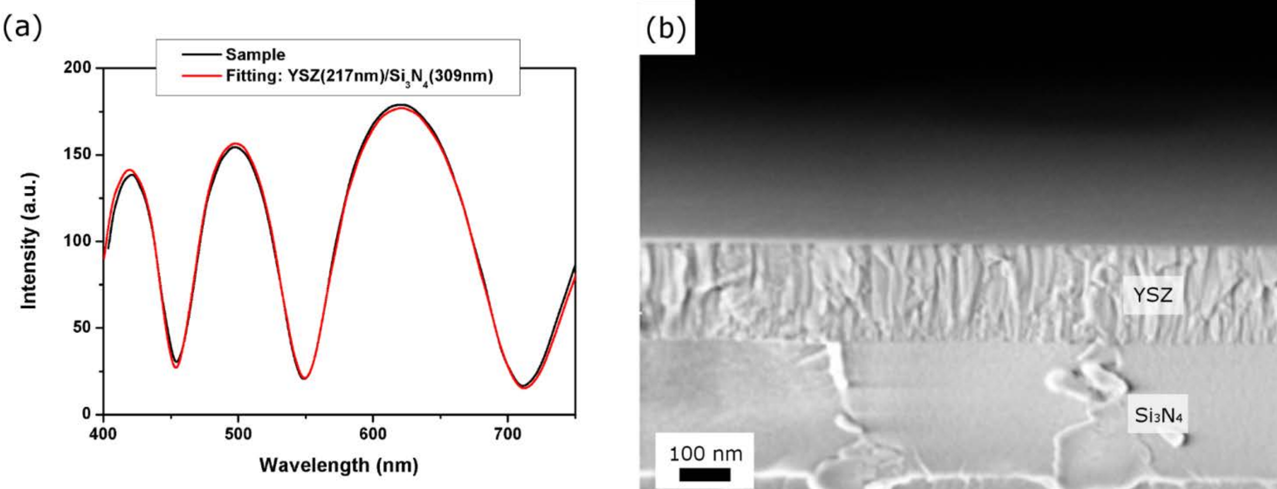

Figure IV-1. *(a) Reflectometry interferogram of an YSZ/Si_3N_4/SiO_2 multilayer on a Si substrate. Red line corresponds to the fitting of the first two samples thicknesses ($217\ nm$ of YSZ, $309\ nm$ of Si_3N_4), by fixing the value of SiO_2 layer at $100\ nm$. (b) SEM cross-sectional image of an YSZ thin film deposited on a Si_3N_4/SiO_2/Si substrate.*

Figure IV-2 shows the typical XRD pattern obtained for an 8YSZ films deposited by PLD in this work. In all the cases, the expected crystalline phase was obtained on the grown films. Highly crystalline YSZ layers

were clearly observed by the presence of diffraction peaks corresponding to a pure cubic *Fm-3m* structure (JCPDS-ICDD #30-1468). Among the different substrate temperatures (T_S) tested, even the lowest deposition temperature ($T_S = 200$°C) resulted in mainly crystalline films, as evidenced from the lack of amorphous background in the XRD patterns. Angle-dependent TEM imaging study (presented below as studied on free-standing membranes) confirmed those high rate of crystallinity over the whole range of T_S.

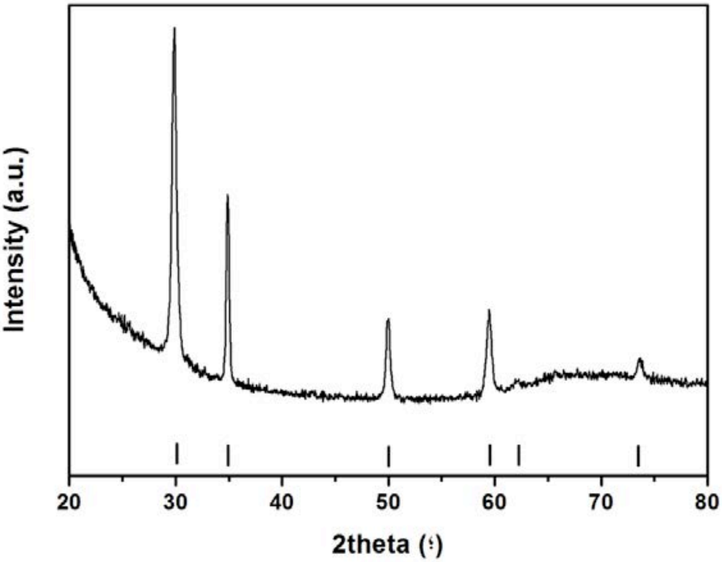

Figure IV-2. *X-Ray diffraction pattern for an 8YSZ thin film deposited by PLD. Solid lines mark peak positions for the cubic Fm-3m structure.*

Figure IV-3 shows the typical microstructure of as-deposited YSZ thin film, observed by top-view and cross-section SEM. Films presented absence of surface defects and high homogeneity yielding a high film density. High thickness uniformity was also observed on the YSZ films, either by SEM and reflectometry. When using the stationary PLD configuration (see *Chapter II*, *Section II.3*), film thickness uniformity measured for tens of samples by reflectometry yielded values below $\pm 0.5\%$ over areas of $5x5\ mm^2$, thus covering the maximum size of the basic squared membranes. Meanwhile, when moving to the large-area PLD configuration the thickness uniformity was ensured over the whole wafer area ($10\ cm$ in diameter), as shown in Figure II-12 (*Chapter II, section II.3.3*).

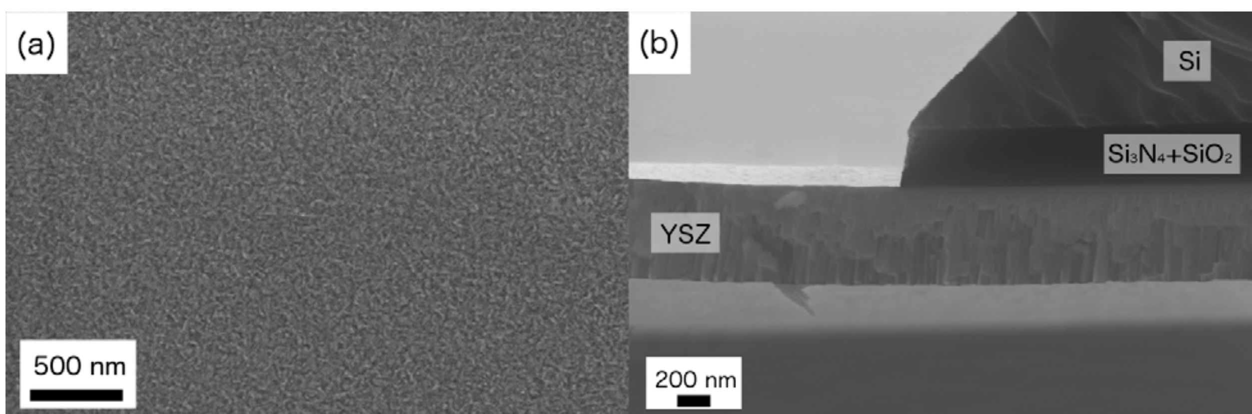

Figure IV-3. *SEM top-view and cross-section images of an YSZ thin film deposited by PLD at $T_S = 600$°C. Cross-sectional view shows a membrane border, i.e. free-standing film on the left side of the image and film over bulky substrate on the right side of the image.*

Cross-sectional images confirmed the expected dense and well-ordered columnar-like grain growth for the YSZ in the whole range of T_S at such low background pressure ($0.03\ mbar$) [17]. This type of growth was thought to be beneficial for the electrochemical performance of the film, as the number of grain boundaries across the membranes were drastically reduced (see *section IV.3*).

Evaluation of crystallinity on YSZ membranes

A microstructural study was performed on ultra-thin YSZ free-standing membranes ($60\ nm$ in thickness) by TEM in order to check their microstructure, crystallinity and film density. Specific chips of $2x2\ mm^2$ were fabricated so they could be fitted into the TEM sample holder. Very thin membranes were used allowing the study of the transmission signal through the self-supported membranes without any further sample preparation. PLD deposition temperatures were varied from $T_S = 200$°C to $T_S = 800$°C in order to see the microstructural evolution with the deposition temperature.

TEM images on Figure IV-4 illustrate how dense the YSZ membranes are, confirming the observed by SEM on YSZ thin films. This high density was observed independently on the substrate temperature deposition. This feature was essential for the membranes to be suitable for micro SOFC applications, as the presence of porosity would then reduce dramatically the power generation efficiency and inhomogeneous thickness could generate hot spots due to local high current densities.

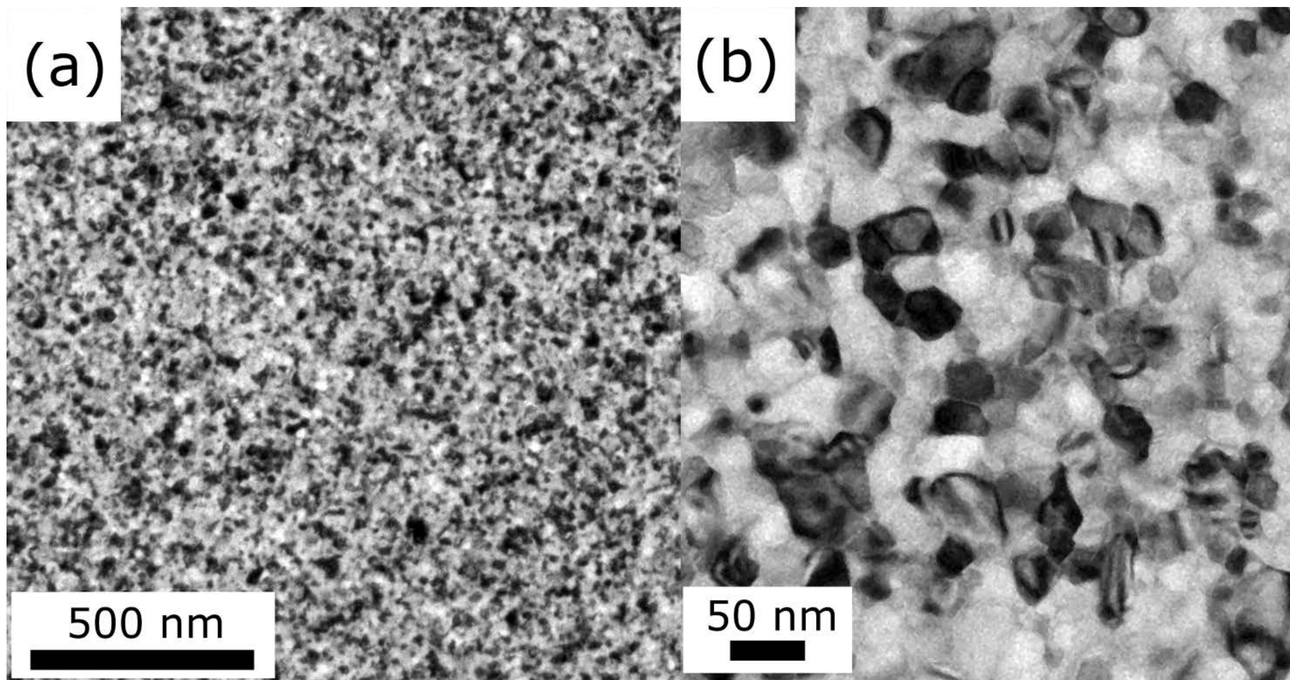

Figure IV-4. *TEM top-view images of a free-standing YSZ membrane of* $60\ nm$ *thick deposited by PLD at* $T_S = 600$°C*, with different magnifications.*

The fabricated YSZ films showed grain sizes on the order of $10\ nm$ for the whole set of deposition conditions (see histograms in Figure IV-5 for the particular cases of $T_S = 200$°C, 400°C and 700°C). However, for the YSZ films under study, a microstructural enhancement based on the improvement of the grain interconnectivity and higher level of crystallinity was promoted by the deposition temperature. Figure IV-5 (d) shows a close comparison of the microstructure when increasing the deposition temperature. The

enhancement of the grain interconnectivity with temperature could be observed as well-faceted grains and better-defined grain boundaries.

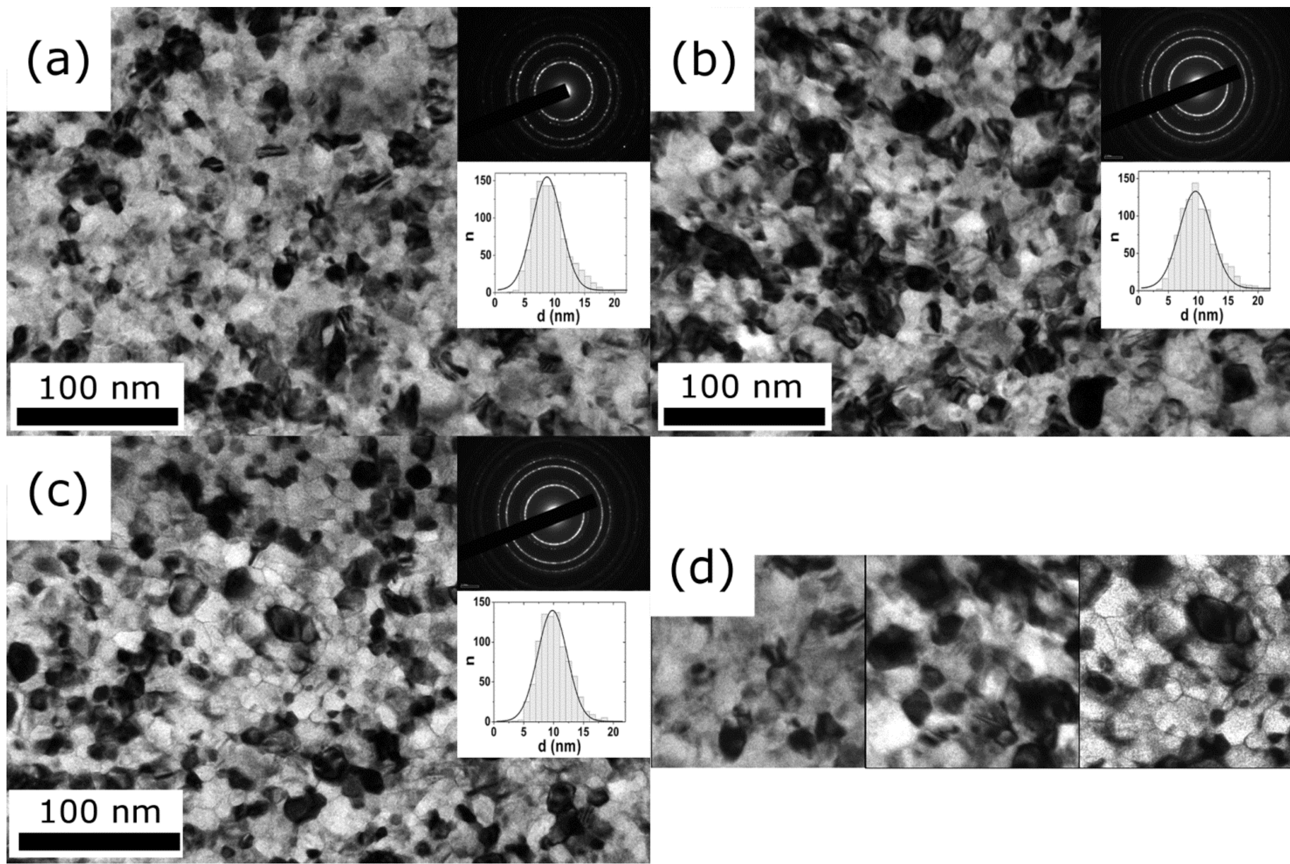

Figure IV-5. *TEM images of the microstructure of* $60\ nm$*-thick YSZ membranes deposited by PLD at different substrate temperatures: (a)* $200℃$*, (b)* $400℃$ *and (c)* $700℃$*. Insets show both SAED diffraction and grain size distribution histogram for the corresponding images. (d) contains a zoom of the microstructure of samples deposited at* $T_s = 200$*,* $400℃$ *and* $700℃$ *(from left to right) for direct comparison.*

The amorphous-to-crystalline phase ratio was evaluated by using TEM angle-dependent bright field diffraction contrast imaging [18], as shown in Figure IV-6. For this study, TEM images of the same area of the membrane were obtained at different tilt angles (from $0°$ to $11°$). Regions showing change in contrast during tilting were associated to well-crystallized grains presenting crystal planes in diffraction conditions. Covering a wide range of tilt angles, bright regions could be ascribed to amorphous areas. An image composition overlapping the dark areas reached along the tilting allowed roughly evaluating the amorphous-to-crystalline phase ratio.

Threshold images were then used for quantitatively assess the crystalline ratios of each film. Increasing the operating temperature from $T_s = 200℃$ to $T_s = 700℃$ reduced the percentage of amorphous phase from 16% to $4\%vol$. Therefore, better cristallinity and grain connectivity was observed increasing the deposition temperature until best values were obtained at $T_s = 700℃$.

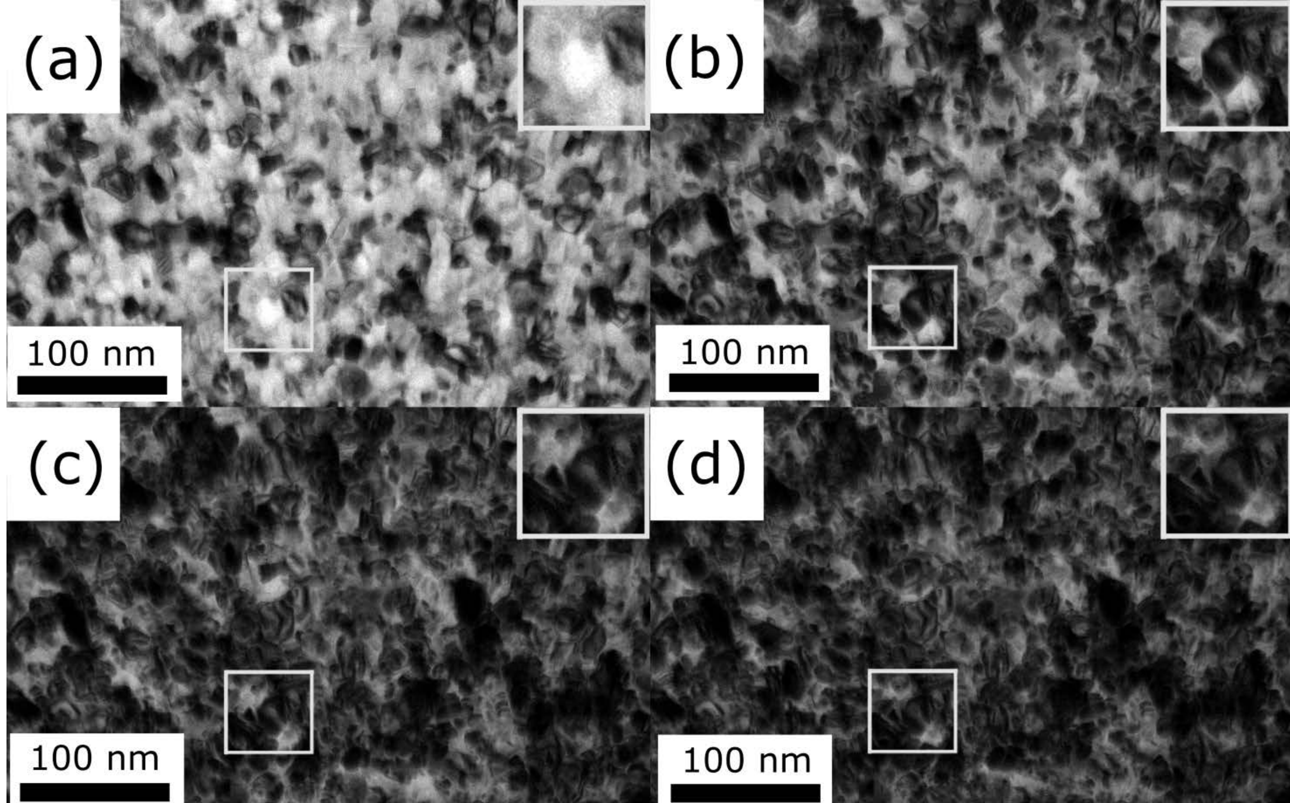

Figure IV-6. *Cumulative TEM bright field images of the microstructure of YSZ free-standing membranes (deposited at* $700°C$*) after tilting from* $0°$ *to* $11°$ *with steps of* $1°$*. Intermediate stages are presented: (a)* $0°$ *(b)* $0°$ *to* $4°$*, (c)* $0°$ *to* $8°$ *and (d)* $0°$ *to 11°. Evolution of the same small area is squared with solid line and detailed on the corner; grain contrast by tilting is clearly observed in (a) and (b) zoom images.*

IV.2.2. Mechanical properties of as-deposited YSZ membranes

The mechanical properties of YSZ free-standing membranes and their evolution with temperature (up to operating conditions) was studied in order to establish the optimal fabrication conditions for getting reproducible and mechanically stable YSZ membranes. The parameters under study were the PLD deposition conditions (T_S, the substrate temperature during deposition) and the membrane dimensions (free-standing area and thickness), as they are the most relevant concerning final stress state of the membrane.

First of all, it is important to remark that the fabrication process of the YSZ self-supported membranes was highly reliable, despite changing the fabrication conditions (see an image of a series of released membranes fabricated at different T_S in Figure IV-7). In order to determine the reliability of the process, the survival rate (SR, ratio between the total number of fabricated membranes and the membranes broken after the deposition) was computed over more than one hundred membranes. Membranes deposited at $T_S = 200 - 700°C$ yielded a high survival rate ($SR > 90\%$) while those deposited at $T_S = 800°C$ presented very low survival rate ($SR < 20\%$). Because of this, membranes deposited at 800 °C were not further considered in the rest of the study and the range of deposition T_S was fixed to be $200 < T_S < 700°C$.

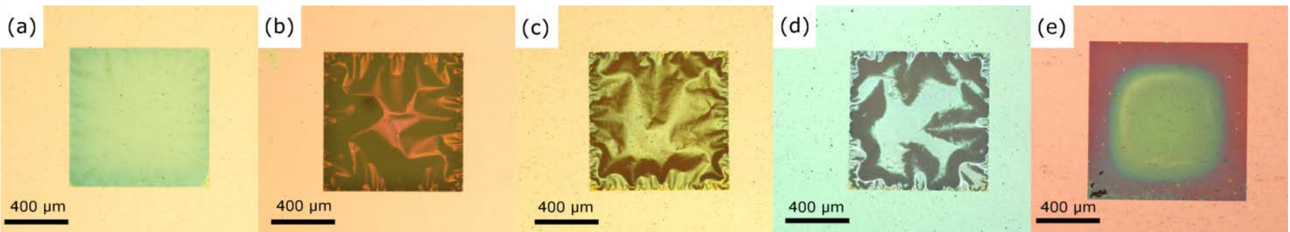

Figure IV-7. *YSZ free-standing membranes fabricated at different T_S; (a) 200°C, (b) 400°C, (c) 600°C, (d) 700°C and (e) 800°C.*

Secondly, it was observed that the buckling profile obtained after the membrane release significantly varied when changing T_S, ranging from almost flat to strongly buckled membranes. Figure IV-8 depicts the maximum deflection at the center of a series of released membranes as a function of the deposition temperature. The difference between YSZ membranes deposited at the different T_S is evident. An exhaustive study of the stress evolution with the deposition conditions was then performed in order to find the most favorable conditions for long-term stability. Two different techniques were used for studying the variability in the stress state of the membranes, i.e. buckling and XRD.

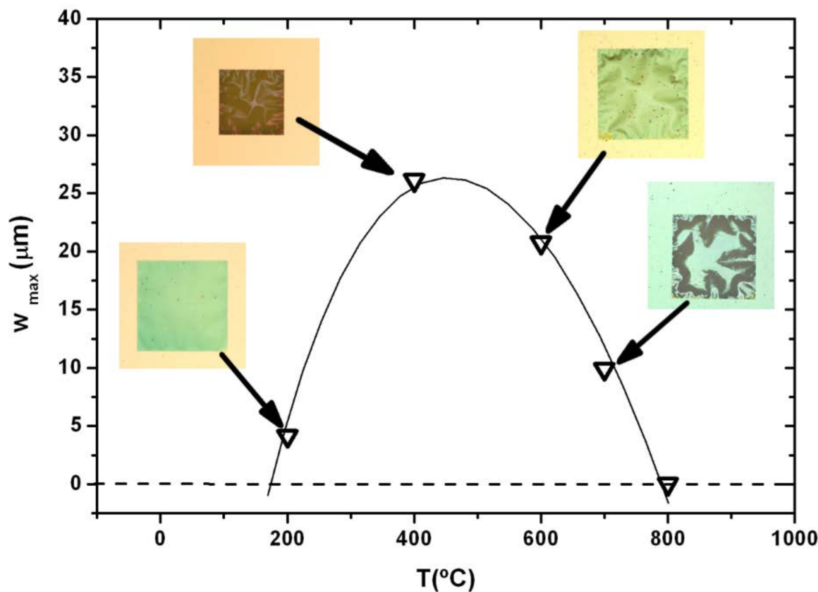

Figure IV-8. *Maximum central deflection of YSZ membranes of thickness $t = 120\ nm$ and side length $a = 620\ \mu m$ as a function of the substrate temperature during deposition.*

Strain analysis by buckling

Residual stress values of compressive membranes deposited by PLD were extracted from buckling profiles of a series of membranes with side lengths ranging from 50 to 150 μm. The residual thin-film strain was extracted by interferometry from the center deflection of the membranes. As an example, Figure IV-9 shows four interferometry maps of a series of buckled YSZ membranes, with identical thickness ($t = 120\ nm$) and side length ($a = 100\ \mu m$), deposited by PLD at different temperatures ($T_S = 200$, 400, 600 and $700°C$). Values of pre-stress obtained from the buckling profile for each membrane are also included on the figure, as calculated from equation (*II.1*) (see *Chapter II*, *Section II.4.2*). This series of membranes

clearly shows the influence of the deposition temperature on the state of stress of YSZ membranes deposited by PLD.

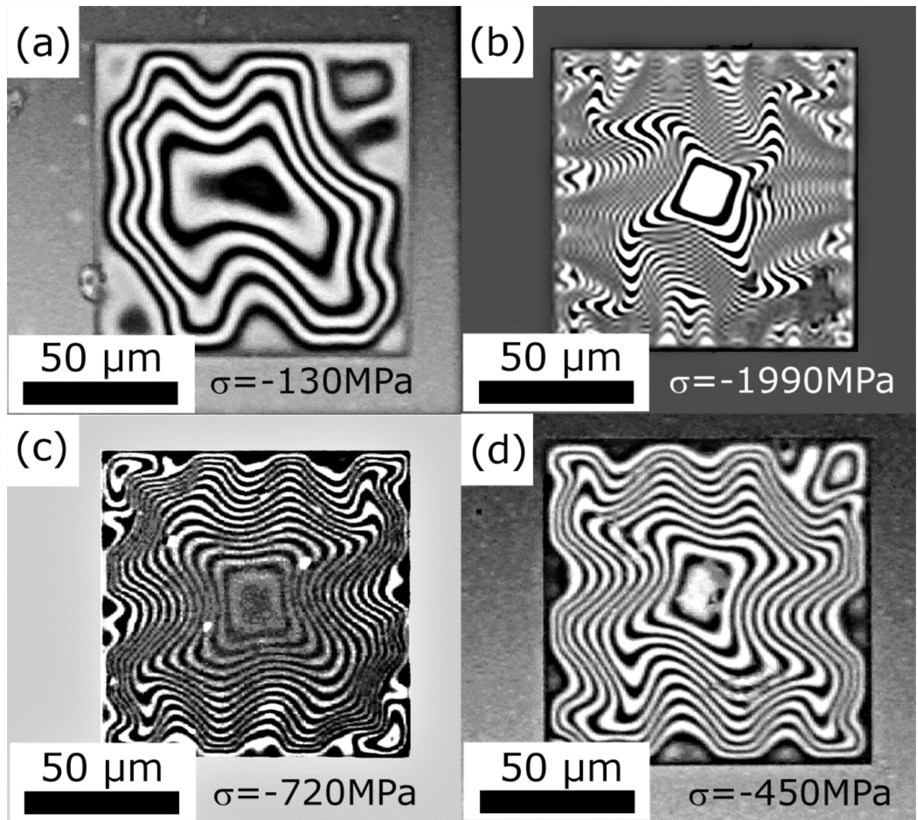

Figure IV-9. *Interferometry maps of YSZ membranes of thickness* $t = 120\ nm$ *deposited by PLD at (a)* $T_s = 200°C$*, (b)* $T_s = 400°C$*, (c)* $T_s = 600°C$ *and (d)* $T_s = 700°C$*. Values of pre-stress yielding from the buckling profiles are included.*

Strain analysis by X-ray diffraction

The classical stress determination method through the study of the hkl planar spacing (d_{hkl}) variation versus $sin^2\psi$, i.e. the observation of the variation of the angular position of the (111) reflection as a function of the tilt angle, was also used to calculate membrane stresses (see *Chapter II* and reference [19] for further explanation about the technique). Figure IV-10 (a) shows an example of the (111) reflection variation at different ψ angles for one large YSZ membrane ($820x820\ \mu m^2$) fabricated from a $120\ nm$ film deposited at $400°C$. It is clear from the graph that the peak is shifted towards higher 2θ values when increasing ψ tilt angle. This would correspond to a d_{111} inter-planar spacing reduction consistent with a compressive in-plane stress. In Figure IV-10 (b) are depicted the calculated d_{111} values against $sin^2\psi$, along with the peak intensity calculated from the area under the fit curve, for the same membrane. The dependence of the planar spacing is almost linear, although a slight undulation is observed. The peak intensity is not constant over the measured ψ range as shown in Figure IV-10 (c). There is a progressive decrease with ψ that reaches a minimum value at about $\psi = 40°$ ($sin^2\psi = 0.41$) and starts to increase again. This indicates for this film a slight orientation of the crystallites with the (111) direction perpendicular to the film surface. The complementary observation of (200) and (220) reflections supported this assumption. This is a general observation for the rest of the films deposited by PLD. The presence of a partial preferential orientation in the films might be the reason for the deviation from the

linear dependence of d versus $sin^2\psi$ and makes difficult to extract an accurate $\sigma_{||}$ stress value. However, for a comparative study between the films deposited under different conditions a linear dependence was assumed, resulting from a biaxial in-plane stress, and stress value proportional to the measured slope was calculated.

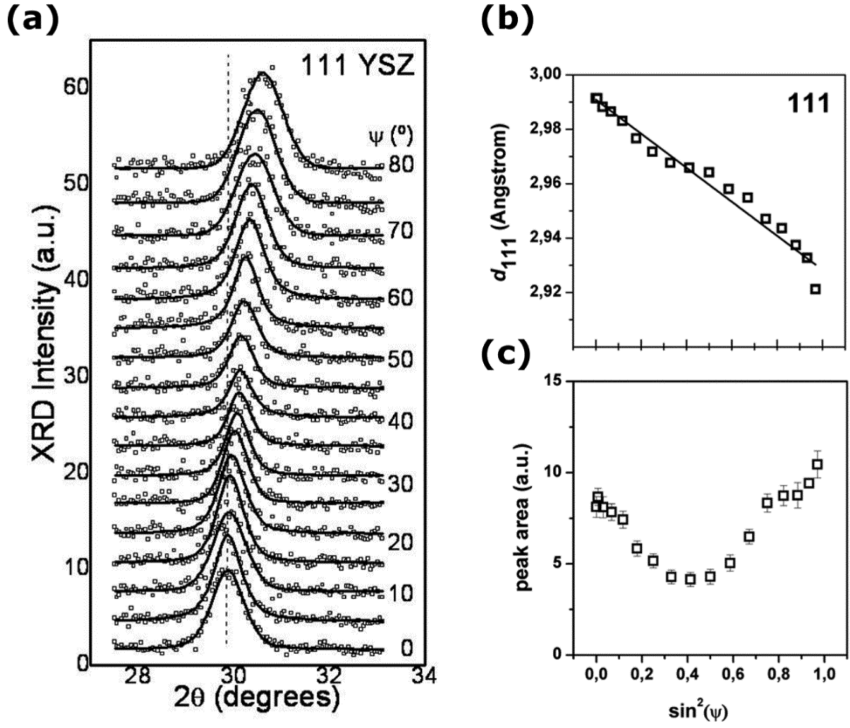

Figure IV-10. *(a) XRD micro diffraction patterns of the* 111 *reflection at different sample stage tilt angles for one large YSZ free-standing membrane (*$820x820\ \mu m^2$*) fabricated from a* $120\ nm$ *film deposited by PLD at* $T_s = 400°C$*. Dependence of (b) interplanar spacing and (c) peak area with* $sin^2\psi$ *for the same* 111 *reflection.*

The same analysis was performed for membranes fabricated from YSZ films deposited at other T_S. Figure IV-11 shows the comparison of $d - sin^2\psi$ dependence for YSZ films of $120\ nm$ thickness deposited by PLD at different temperatures $T_s = 200°C$, $400°C$ and $600°C$. Depending on deposition temperature there is a clear variation of the average slopes of the curves, thus indicating a variation of the residual stress in the films. At low temperatures of $200°C$ the slope is slightly positive, indicating a tensile stress, while at higher temperatures of 400 and $600°C$ the slope is negative corresponding to a compressive stress. It is remarkable that all the curves coincide in a common d_{111} value of 2.963 Å at about $\psi = 50°$, that would correspond to the non-stressed part of the material (d_0) with a cubic cell parameter $a = 5.132$ Å, as expected for an in-plane biaxial stress. This value is consistent with reported cell parameter values of $a = 5.137$ Å for cubic 8YSZ nanocrystalline powders [20]. By using this experimental d_0 value, along with reported values for the Young's modulus $E = 308\ GPa$ and Poisson's ratio $\nu = 0.25$ for the isotropic material, it is possible to calculate the values of the elastic compliances: $s_{11} = 2.59 \cdot 10^{-3} GPa^{-1}$, $s_{12} = -0.33 \cdot 10^{-3} GPa^{-1}$, $s_{44} = 9.48 \cdot 10^{-3} GPa^{-1}$ (equation (*II.3), Chapter II, Section II.4.2*), and therefore, the in-plane stress $\sigma_{||}$ values. As an example, the data in Figure IV-10 could be analyzed by following both approximations in equations (*II.2*) and (*II.3*). For 111 reflection the Γ parameter is $1/3$ and DECs values of $s_1 = -0.934 \cdot 10^{-3} GPa^{-1}$, $1/2\, s_2 = 4.74 \cdot 10^{-3} GPa^{-1}$ are obtained. From the slope and intercept values of the linear approximation in-plane stress values of $\sigma_{||}^{slope} = 3.94 GPa$ and $\sigma_{||}^{intercept} = 3.94 GPa$ were

calculated from eq. (*II.2*), and of $\sigma_{||}^{slope} = 3.38GPa$ and $\sigma_{||}^{intercept} = 4.33GPa$ from eq. (*II.3*). There is an important dispersion of $\sigma_{||}$ from 3 to 5 GPa to take into consideration the absolute values of the stress. However, from a comparative point of view, the $\sigma_{||}$ values derived from the slope of the $d - sin^2\psi$ were taken into account, assuming the validity of Reuss approximation (that is, using the first term of eq. (*II.3*)).

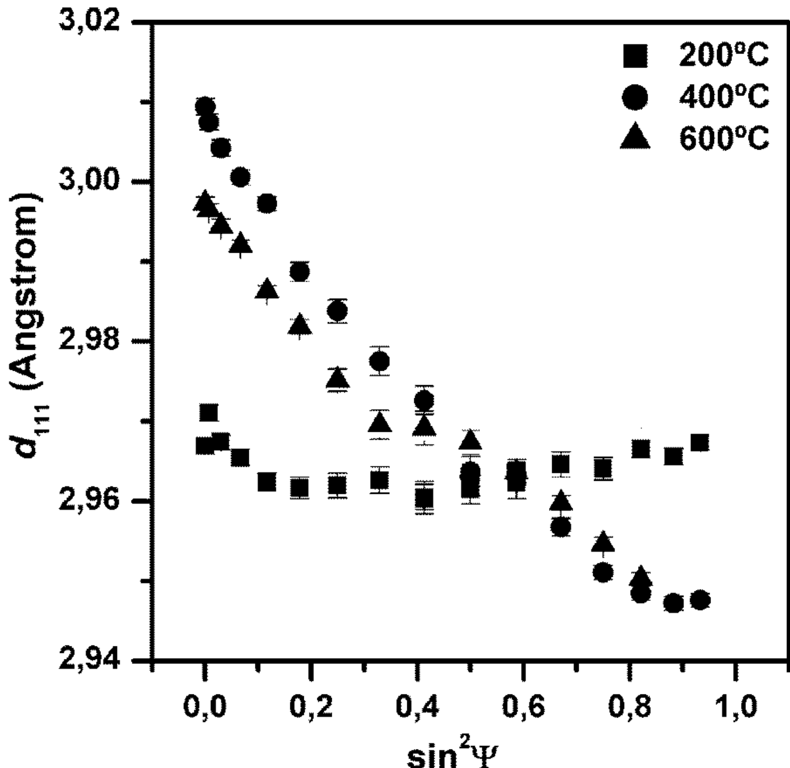

Figure IV-11. *Plot of $d - sin^2\psi$ for a set of YSZ deposited at different temperatures by PLD. The measurement has been taken in a zone of the film where the membranes were still supported on the substrate.*

Key fabrication parameters controlling the strain

Residual stress values obtained from the two analysis methods for the complete series of membranes deposited at different temperatures are gathered in Figure IV-12. An almost free-stress state was observed for the lowest temperature, $T_S = 200°C$, whereas at $T_S = 400°C$ a maximum in compressive stress was reached. From this temperature the stress is progressively reduced until the maximum substrate temperature studied, $T_S = 700°C$.

Although this trend is shared by results obtained from buckling and X-ray diffraction, XRD measurements yielded higher absolute values of stress than those obtained by buckling profile analysis. This is due to the different nature of both evaluation methods. While buckling gives the in-plane biaxial stress that originates a certain out-of-plane deformation, XRD method evaluates the remaining stress after deformation. The discrepancy observed between both techniques indicates that stress generated by PLD cannot be fully released by a mere macroscopic deflection of the membrane. In addition, PLD induces the formation of other components (out-of plane, shear stresses) that cannot be released by a vertical deflection.

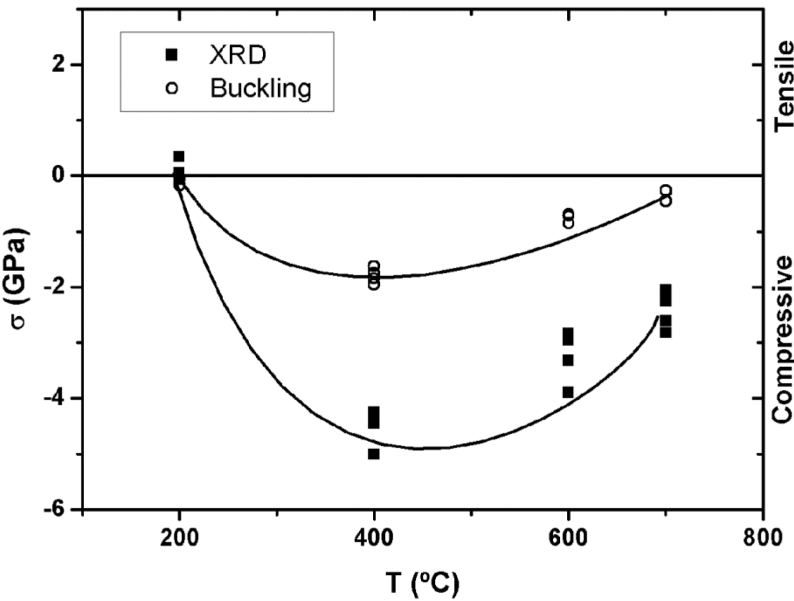

Figure IV-12. *Stress evolution with substrate temperature for YSZ free-standing membranes as measured by buckling analysis and XRD diffraction.*

Related to the high values of stress obtained, it is important to notice that all the techniques employed here required a particular value of the Young's modulus to be assumed, restricting the validity of the absolute values of stress obtained in this work due to the large dispersion of Young's modulus reported for YSZ in the literature ($E_{YSZ} = 100\text{–}400\ GPa$). However, these stress magnitudes were in line with the observations of Carneiro et al. [21] and Knoll et al. [22], who obtained compressive stress values of some GPa in sputtered YSZ films for high energetic deposition conditions (high power densities and substrate bias). Still, it is difficult to compare them with previously reported results, because a wide variety of stress levels can be found in the literature depending on the deposition conditions, e.g. significantly lower values on the order of few hundreds of compressive MPa were reported by Quinn et al. [23] or Gao et al. [24].

The trend of the stress as a function of the deposition temperature obtained in Figure IV-12 is similar to the originally reported by Thornton and Hoffman [25] for metal thin films. According to Thornton and Hoffman, for the range of temperatures covered in this work the combined effects of two main opposite contributions yield a maximum in compressive stress: (i) a linearly increasing tensile stress occurring after deposition during the cooling step due to the lower thermal expansion coefficient (TEC) of the silicon frame ($2.5 \cdot 10^{-6}\ K^{-1}$) compared to the YSZ layer ($10.5 \cdot 10^{-6} K^{-1}$); (ii) a compressive stress induced by atomic impingement (also called "atomic peening") typically present in plasma assisted deposition techniques like PLD [26,27].

On one side, the thermal stress is given by (neglecting the Poisson effect),

$$S_{th} = E_{YSZ}(\alpha_{YSZ} - \alpha_{Si})(T_s - T_f) \qquad \textit{(IV-1)}$$

where E_{YSZ} is Young's modulus, α_{YSZ} and α_{Si} are the average coefficients of thermal expansion, T_s the substrate temperature during deposition and T_f the temperature during measuring. Provided that there

were only extrinsic thermal stresses, a tensile component (proportional to the difference between deposition and room temperatures) is expected for all the deposited YSZ films. However, Figure IV-12 shows both compressive states and non-linear dependences with temperature making clear that thermal stress is not enough to describe the observed behavior.

The high compressive values of stress observed in the films are likely originated by lattice displacements associated to highly energetic impinging particles typically present in plasma assisted deposition techniques (PLD). This mechanism, the atomic peening, has already been observed by other authors for YSZ sputtered films [13,23]. It is actually well known that the dependence of atomic peening on both the deposition parameters (working gas pressure, deposition rate, energy density…) and the microstructure of the film, since the impingement becomes more significant when films present a high crystalline and well-interconnected microstructure. As all the deposition parameters except substrate temperature T_S were fixed for this experiment, the microstructure changed as a function of T_S, according to the micro structural description previously presented – see *Section IV.1.2*. The slightly compressive stress observed at $T_S = 200℃$ was explained due to the lower crystallinity and interconnectivity of the film [25,28]. Then, the compressive contribution due to the deposition method increases continuously until a constant value for a deposition temperature high enough to generate YSZ films with high crystallinity and grain interconnectivity ($T_S = 400℃$).

Additionally, the increasing compressive stress is also reduced due to a third effect: the activation of the well-known recovery process that tends to relax the films (by vacancy, interstitial and dislocation movement) [25]. This recovery process generally occurs in the range of $T/T_m = 0.1 - 0.3$, where T_m is the melting temperature. Thus, for the particular case of YSZ ($T_m \sim 2700℃$) the recovery process takes place in the range of $T = 300℃ - 800℃$. Higher values of temperature would be required to start the process or recrystallization and therefore it does not apply for the present work.

Finally, another effect typically put forward for explaining stress variation with temperature is the existence of a crystallographic change. In this sense, crystalline YSZ sputtered thin films presenting monoclinic [29], tetragonal [24], cubic [30] and mixed phases [31] have been presented in the literature in their as-deposited form with different values of stress. In order to evaluate any possible phase change, micro Raman spectroscopy was carried out on the membranes at different temperatures. Figure IV-13 shows this micro-Raman study for four samples obtained at different deposition temperatures ($T_S = 200 - 700$ ℃). The only presence of a clear peak at $622\ cm^{-1}$ corresponding to the cubic phase is observed with no trace of the presence of either tetragonal or monoclinic YSZ phases [32,33]. Therefore, despite the wide range of stress states and the high sensitivity of YSZ to stress-induced phase transformations [34], the whole set of membranes presented a single cubic phase so no relation of the stress evolution with any phase change could be ascribed.

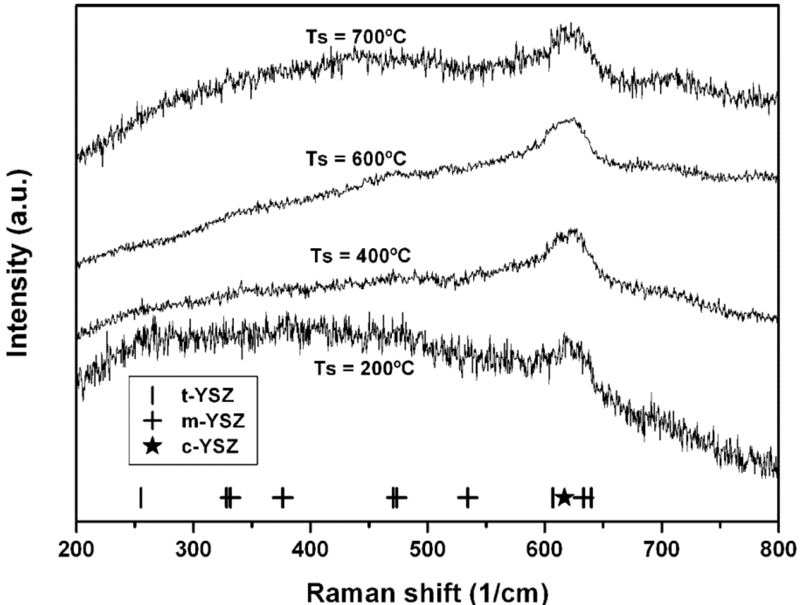

Figure IV-13. *Micro Raman spectra of* $240\ nm$ *YSZ/*$300\ nm$ *Si_3N_4 membranes deposited at different temperatures (*$T_s = 200 - 700℃$*). Raman bands indicative of monoclinic (m), tetragonal (t) and cubic phases (c), extracted from [32,33], are marked and labeled.*

To summarize, different and complex stress and relaxation mechanisms take place during PLD depositions depending on the substrate temperature. All the contributions are highly overlapped; however it is possible to determine the dominant contribution by differentiating two temperature regimes:

- Low temperature ($T_s \leq 200℃$), almost free-of-stress state due to low impact of atomic peening and tensile thermal stress compensation.
- Intermediate temperature ($200℃ < T_s < 700℃$), highly compressive stress controlled by intrinsic stress induced by atomic impingement.

Stress values obtained by XRD were also dependent on the film thickness and membrane area. Figure IV-14 shows the measured values for a film deposited at $T_s = 600℃$. The different curves correspond to different membrane thickness ($60\ nm$, $120\ nm$ and $240\ nm$). The zero coordinate corresponds to YSZ films still supported on the substrate. The general trend indicates that the absolute value of stress is progressively reduced when increasing the membrane size. Besides, the thicker the membrane the larger the stress released. Increasing the thickness of the membranes may induce the formation of defects which help releasing the stress. However, from Figure IV-14 is clear that size and thickness are second order effects when compared to changes in residual stress due to substrate temperature during the deposition (Figure IV-12).

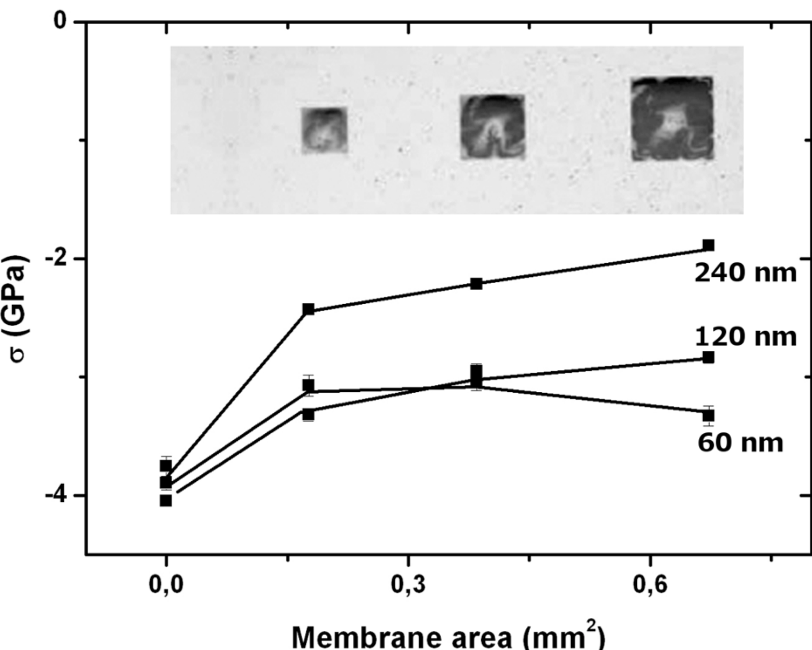

Figure IV-14. *Stress obtained by XRD analysis for YSZ membranes of different thicknesses and membrane sizes deposited at $T_s = 600°C$. Membrane area equal to zero indicates that the measurements were carried out in the frame of the membrane.*

IV.2.3. Thermo-mechanical stability of YSZ membranes

In order to study the performance of fabricated YSZ membranes close to the operating conditions, thermal treatments up to three different temperatures ($T_a = 500°C$, $600°C$ and $700°C$) were performed. These process had a double purpose: i) ensure mechanical stability at working temperatures and ii) ensure oxygen stoichiometry since high temperatures and low oxygen partial pressures during deposition cause non-stoichiometric oxygen content in YSZ affecting its mechanical and electrical properties [17,35-37].

High survival rates were observed for samples deposited at $T_s > 200°C$ after consecutive annealing at the three different temperatures (see Table IV-1). However, survival rates for membranes deposited at $T_s = 200°C$ were very low. This is in accordance with Baertsch et al. that reported very low fracture temperatures ($< 200°C$) for YSZ membranes deposited at room temperature [13]. Therefore, not only post-annealing but high deposition temperatures were required for fabricating thermo-mechanically stable YSZ free-standing membranes.

Table IV-1. *Survival rate of YSZ free-standing membranes fabricated at different deposition temperatures (Ts) as a function of the annealing temperature*

T_a(°C)	$T_s = 200°C$ (%)	$T_s = 400°C$ (%)	$T_s = 600°C$ (%)	$T_s = 700°C$ (%)
500	71	100	92	93
600	42	70	83	93
700	0	70	75	93

Figure IV-15 (open symbols) shows the stress variation of YSZ membranes, deposited at different substrate temperatures ($T_s = 200 - 700°\text{C}$), after annealing at the three temperatures. As a general trend, the residual stress of the YSZ membranes shifts towards a more tensile state after thermal treatment with significant higher variation for lower deposition temperatures. After re-oxidation of the film and homogeneous recovery process taking place during the annealing, the dominant factor at high temperatures ($T > 500°\text{C}$) is the linear thermal stress described in eq. *(IV-1)* (see the dashed line representing the thermal stress slope in Figure IV-15). Assuming this, the whole curve can be fitted by this linear response overlapped to an exponential decay asymptotically going to a constant value of intrinsic compressive stress ($\mathrm{S_{HT}}$) at high deposition temperatures (solid lines in Figure IV-15). These constant values (listed in Table IV-2) indicate a good thermal stability at temperatures up to $\mathrm{T_s} = 700°\text{C}$ for membranes deposited at $\mathrm{T_s} > 500°\text{C}$ and annealed at $500°\text{C} < \mathrm{T_a} < 700°\text{C}$. In addition, these membranes present compressive value that, as pointed out by Baertsch et al. [13], is preferred for micro SOFC applications to compensate tensile stresses during heating.

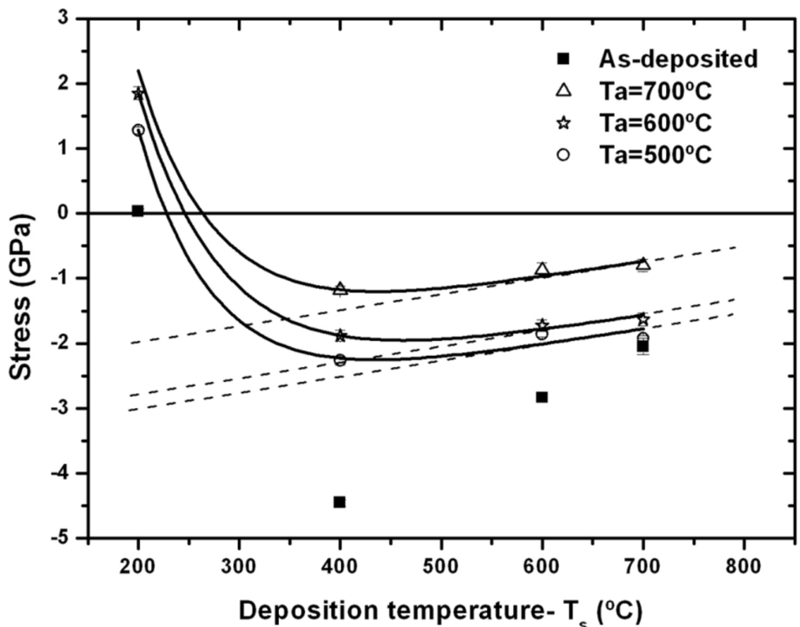

Figure IV-15. *Stress evolution with the deposition temperature ($T_s = 200 - 700°\text{C}$) of as-deposited and post-deposition annealed ($T_a = 500 - 700°\text{C}$) YSZ membranes of $120\ nm$ thick and $820x820\ \mu m^2$ size, determined by X-ray micro diffraction. The dashed lines represent the slope of the thermal stress contribution of eq. (IV.1). The solid lines represent a fit considering both a tensile contribution due to thermal stress a compressive one induced by the PLD.*

Table IV-2. *Asymptotic values of intrinsic compressive stress of high deposition temperature YSZ free-standing membranes as a function of the annealing temperature (T_a).*

T_a (°C)	S_{HT} (GPa)
500	$-3.5(1)$
600	$-3.23(7)$
700	$-2.40(8)$

Figure IV-16 presents the typical grain mean size evolution after membrane heat treatment at $T_a = 600℃$ (calculated by TEM image analysis). For $T_s = 200℃$, comparison of the images of the same membrane as-deposited at such low temperature and after annealing at $T_a = 600℃$ revealed an enhancement of the grain interconnectivity (sharper definition of the grain boundaries) and marked grain growth, as illustrated in Figure IV-17 (a,b) and zoomed in (c,d) for better comparison. This evolution explains the extra tensile stress observed and the subsequent low survival rate. Similar mechanisms of tensile stress development due to grain growth and microstructural enhancement during annealing have been proposed by other authors [38,39].

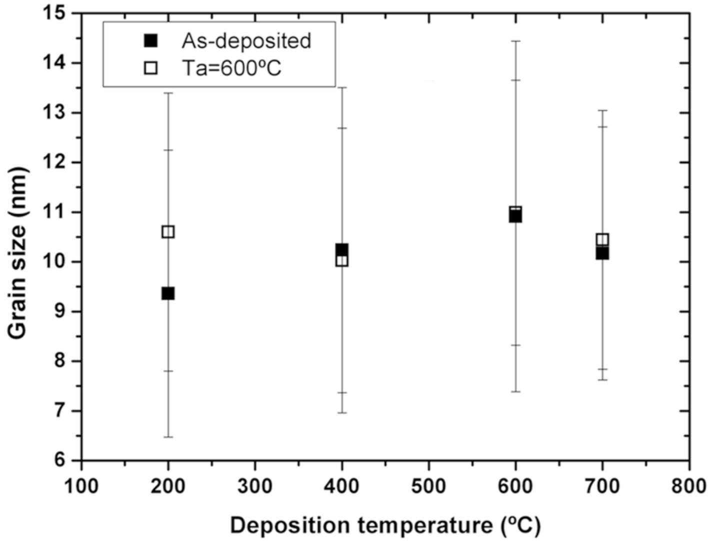

Figure IV-16. *Mean grain size evolution with deposition and annealing temperatures of* $60\ nm$ *thick YSZ membranes (bars represent the standard deviation of the grain size distribution histograms obtained by TEM analysis).*

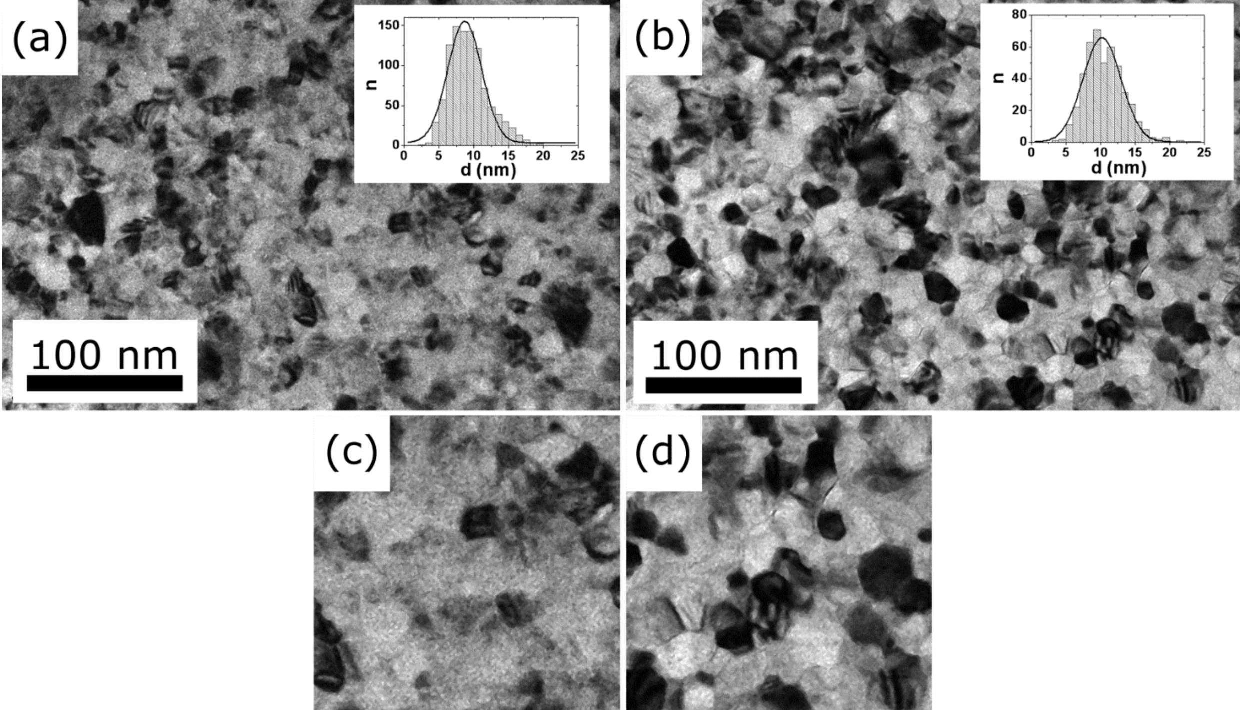

Figure IV-17. *TEM images of the microstructure of 60 nm-thick YSZ membranes fabricated at* $T_s = 200℃$ *are presented in (a) as-deposited and (b) after a thermal treatment at* $600℃$ *during* $2.5\ h$*. (c) and (d) contain a zoom of (a) and (b) images for better comparison.*

Conversely, for $T_S \geq 400$°C, grain size growth stabilized ca. 10 nm and well-connected grains were also present before the annealing, therefore the previous analysis cannot explain the tensile contribution. In addition, no significant difference in the amorphous-to-crystalline ratio between as-deposited and post-deposition annealed membranes (studied by angle-dependent TEM analysis as in the previous section and depicted in Figure IV-18 for as-deposited versus post-annealed comparison) was observed indicating that no recrystallization process took place during the thermal treatment. Accordingly, the crystallinity of the film was established during the deposition process and higher annealing temperatures would be required to improve it. The only factor contributing to the compressive stress relaxation was then the activation of the always present recovery processes [25,28].

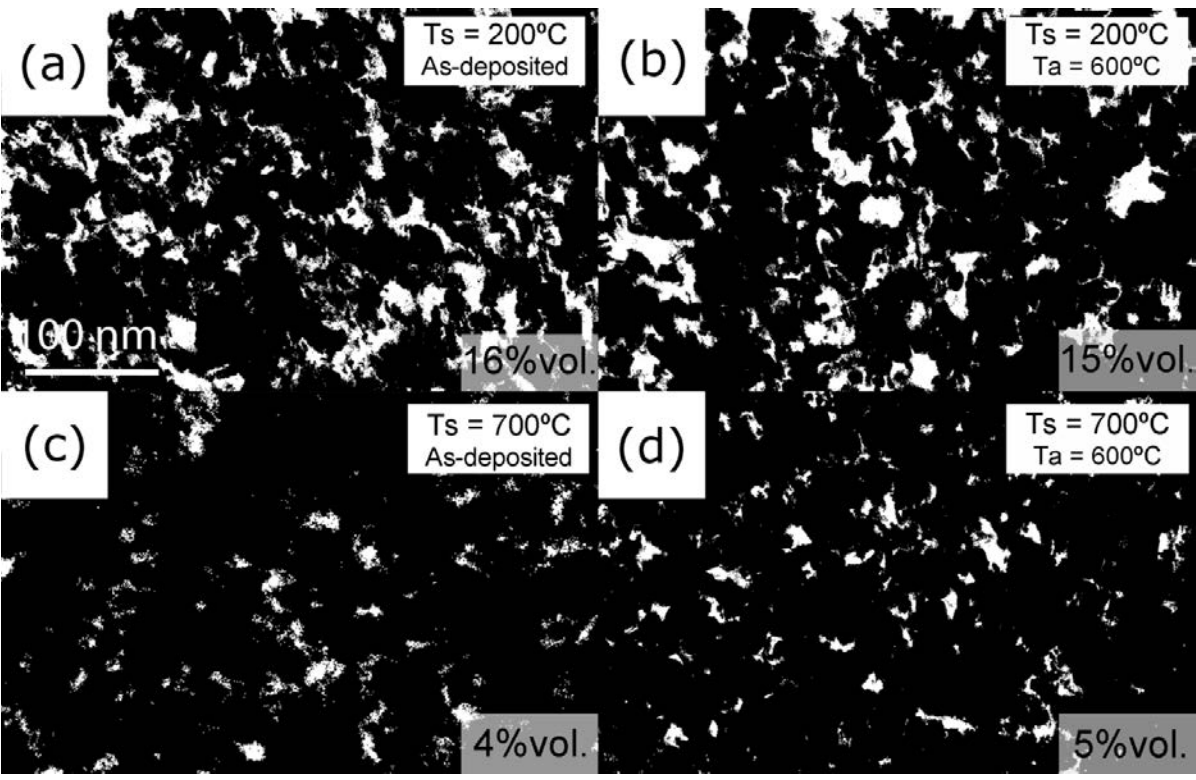

Figure IV-18. *Threshold images derived from an angle-dependent TEM study to determine the amorphous-to-crystalline phase ratio of YSZ free-standing membranes. Black areas correspond to crystalline zones while white ones to the presence of amorphous phase. Membranes fabricated at* $T_S = 200$°C *and* 700°C *are presented as-deposited in (a) and (b) and post-deposition annealed at* $T_a = 600$°C *in (c) and (d), respectively. The percentage of non-crystalline zones on each film is indicated for each case.*

To summarize, the origin of this post-deposition annealing mechanical behavior, presented in Figure IV-15, was found different depending on the deposition temperature:

- For low deposition temperatures below the annealing temperature ($T_S \ll T_a$), an extra tensile contribution was generated because of grain growth and enhancement of grain interconnectivity (i.e. grain boundary surface energy reduction), yielding to low values of SR.
- For elevated deposition temperatures close to the annealing temperature ($T_S \sim T_a$), a structural relaxation took place due to a recovery process (i.e. defect associated energy minimization). High SR was observed in this case.

Therefore, an optimal technological window of fabrication of functional electrolyte membranes for micro SOFC was defined in this work. Thermo-mechanically stable YSZ membranes were fabricated by PLD deposited in a range of temperatures between $T_S = 400$℃ and $T_S = 700$℃, and their mechanical behavior during working conditions (500℃ to 700℃) was satisfactorily tested, observing a reduction on the membrane stress after annealing.

IV.3. Electrochemical properties of YSZ membranes

IV.3.1. YSZ in-plane conductivity: thin films

First of all, standard DC measurements of YSZ in-plane conductivity were performed, to serve as a reference for the electrical characterization of the membranes. Figure IV-19 shows Arrhenius curves of in-plane DC conductivity of YSZ thin films deposited at different T_S. Both activation energy and absolute values of conductivity were similar for all the deposition temperatures, while one order of magnitude lower conductivity was obtained compared to other reported bulk YSZ (also included in the figure for comparison [1,40]). As shown in Table IV-3, the here obtained values of conductivity were in line with other in-plane measurements for YSZ thin films with grain sizes in the order of 10 nm [17,41,42]. Only reported results with the same grain size are used here for comparison as variation in grain size is suggested as one of the main factors affecting the conductivity [15] together with the strain [14,15] and crystallographic phase [42,43]. In this study, no significant differences were observed between the samples deposited at different conditions.

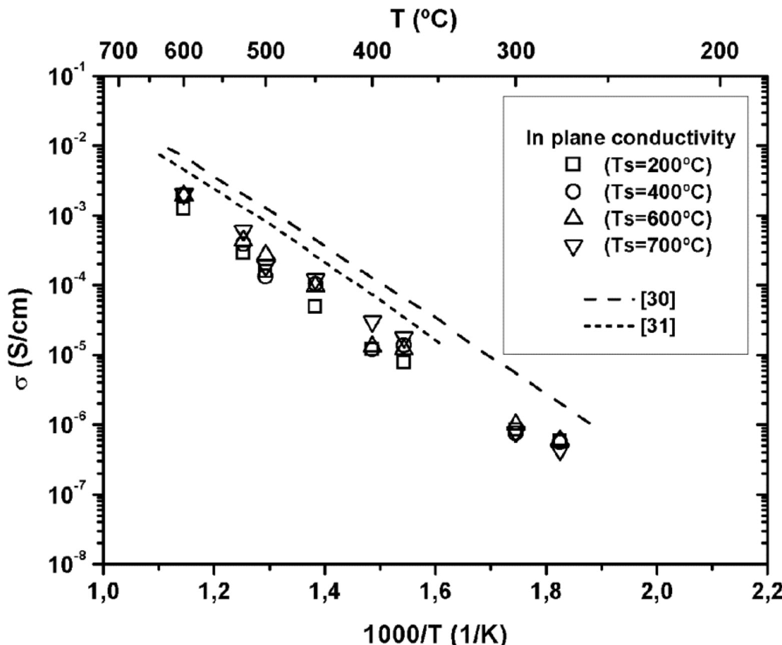

Figure IV-19. *Arrhenius plot of in-plane electrical conductivity of $240\ nm$ thick YSZ thin films deposited at different temperatures. Bulk YSZ conductivity extracted from references [40] and [1] were also included for comparison.*

Table IV-3. *Activation energy and conductivity at* 500℃ *for the in-plane measurements carried out in this work compared to other studies in the literature for 8YSZ bulk and thin films.*

T_s(℃)	Conductivity at $T = 500$℃ (mS/cm)	$E_a(eV)$	Notes and references
200	**0.16**	**0.99(4)**	**This work**
400	**0.13**	**1.03(6)**	**This work**
600	**0.27**	**1.05(4)**	**This work**
700	**0.19**	**1.08(4)**	**This work**
-	1.39	1.03	Bulk, [40]
-	0.95	1.05	Bulk, [1]
RT	0.15	$0.9 - 1.1$	Thin film, [41]
400	1.30	1.1	Thin film, [17]
600	0.45	1.08	Thin film, [42]

It is worth to mention here that DC measurements add electrode-electrolyte contributions to the electrolyte resistance (which could be particularly significant at low temperatures). This factor could partially explain the lower conductivity measured on the films when compared to the bulk. However, although all these contributions (bulk vs. grain boundary and contact resistances) could be discriminated by AC impedance spectroscopy, in the present case it was not possible to obtain reliable AC measurements due to parasitic contributions of the insulation layer in the substrate, as highlighted by Johnson et al. [41]. Thus, only DC measurements could be performed in this in-plane configuration.

IV.3.2. YSZ cross-plane conductivity: membranes

The cross-plane measurement configuration utilized in this work is depicted on Figure IV-20, compared to the more common in-plane configuration used in the previous section. While on the in-plane measurement two electrodes are deposited on top of an YSZ film, on the cross-plane the electrodes are placed one at each side of the electrolytic membrane. Thus, different data is acquired, i.e. the conductivity *along* the thin film and the conductivity *across* the thin film, respectively. This difference is especially significant in the present case. The columnar microstructure obtained for the YSZ films (see SEM images on *Section IV.1.2*) reduce the number of grain boundaries to minimum when measuring across the film, so one single contribution to the total electrolyte resistance (YSZ bulk contribution) is expected on this configuration. Meanwhile, both grain boundary and bulk contributions are measured on an in-plane configuration as the number of grain boundaries crossed along the film is much higher. Moreover, it is worth to mention that the cross-plane measuring configuration is exactly the same as the final device configuration, so measured resistance values are directly transferrable to fuel cell performance calculations.

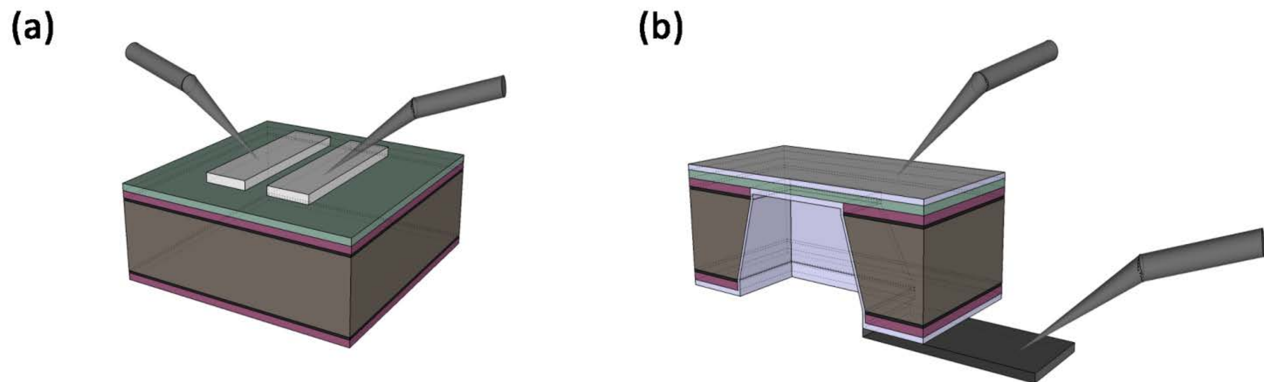

Figure IV-20. *Schemes of both in-plane (a) and cross-plane (b) electrochemical measurement configurations. Metallic tips are used in both cases for contacting.*

Cross-plane YSZ conductivity was analyzed by impedance spectroscopy on free-standing membranes. Taking into account the thermo-mechanical study of the YSZ membranes and the obtained in-plane conductivities for YSZ films fabricated at different temperatures (similar values in all the cases), a set of fabrication conditions was fixed as standard for the electrochemical study of the membranes. Thus, substrate temperature was set at $T_s = 600$°C, while the post-thermal treatment was made at $T_a = 600$°C.

Figure IV-21 (a) shows the equivalent circuit used for the whole system under evaluation. Two parallel paths are present due to the platform itself and the membrane. As shown in the figure, there is a parasitic contribution due to the Pt/Si_3N_4/SiO_2/Si system. In this sense, Figure IV-21 (b) depicts the impedance spectra of this parasitic contribution alone at high temperatures, showing a capacitor-like response. This measurement proved the insulator behavior of the substrate, thus being the membrane the only active part of the device when present. Since the employed insulators show a very high resistance (R_{in}), this path never overlaps the contribution of the membrane when this is present, allowing its study by EIS. Figure IV-21 (c) shows the typical impedance arcs observed for one of the 8YSZ membranes fabricated; these arcs can be fitted with excellent goodness using the right branch of the equivalent circuit in Figure IV-21 (a). The model includes a resistance associated to wiring and current collection (R_s), in series with both the contribution of the YSZ (R_{YSZ} in parallel with a constant phase element, Q_{YSZ})[1] and the contribution of the electrodes (R_{el} in parallel with a constant phase element, Q_{el}). The impedance spectrum shows that no grain boundary contribution was present, as expected for nanometric scale thicknesses due to the typical PLD columnar-like grain growth [17].

[1] C*onstant phase elements*, CPE, were used here instead of just capacitances. CPE is a non-intuitive circuit element commonly used for better fitting the response of real-world systems. It is utilized when depressed semicircles are observed on the EIS spectra, which most probably are due to a dispersion of the value of some physical property of the system (either capacitance or time response). CPE is given by,

$$\frac{1}{Z} = Y = Q(j\omega)^n$$

where Q has the numerical value of the admittance ($1/|Z|$) at $\omega = 1\ rad/s$. The phase angle of the CPE impedance is independent of the frequency and has a value of $-(90 \cdot n)$ degrees. When $n = 1$, Q is equal to C; else, in some cases the true capacitance can be calculated by,

$$C = Q(\omega_{max})^{n-1} = \frac{(Q \cdot R)^{1/n}}{R}$$

(ω_{max}: frequency at which the imaginary component reaches a maximum)

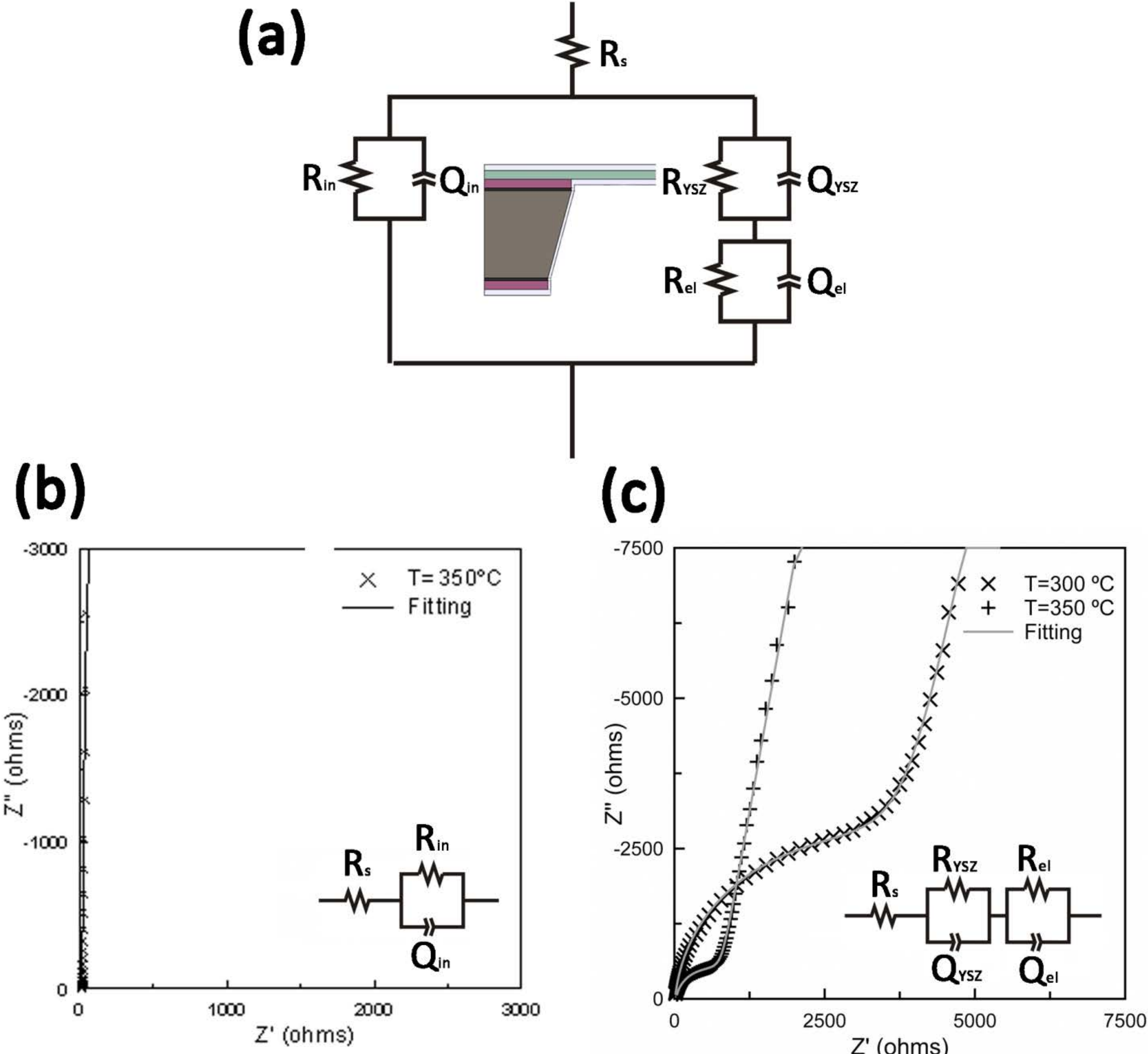

Figure IV-21. *(a) Equivalent circuit for the cross-plane measurements. Two parallel paths are present, one through the insulator and the other across the membrane. (b) Impedance spectra of Pt/Si_3N_4/SiO_2/Si systems. (c) Impedance spectra of symmetrical cells based on $240\ nm$ thick and $500\ \mu m$ side YSZ membranes deposited at $T_s = 600$℃ and annealed at the same $T_a = 600$℃ for $2.5\ h$. Results of the measurements at $T = 300$℃ and 350℃ are presented. The insets show the equivalent circuits employed to fit the arcs. The corresponding fittings are represented by solid lines.*

From the resistance values associated to YSZ (R_{YSZ}) and taking into account the thickness and the area of the membrane, the conductivity of the free-standing YSZ membranes was calculated for each temperature. Conductivity values were plotted on Figure IV-22 compared to previously measured in-plane conductivity and to 8YSZ bulk conductivity (values measured on the same PLD targets and some taken from the literature).

Slightly higher total conductivity is systematically observed for the membranes when compared to the target and reported values. This effect can be related to the columnar grain growth and small thickness of the YSZ films that virtually eliminates the grain boundary contribution. Therefore, the contribution to the total conductivity is mainly dominated by the bulk. At the same time, comparing 8YSZ membranes

conductivity to in-plane measurements of the same 8YSZ depositions, one order of magnitude increase in conductivity was observed. This difference should be again mainly related to the grain boundary contribution, which is obviously expected to be more significant for in-plane measurements due to the high electrode separation and columnar-shape of the grains on the film. Moreover, as detailed in previous section, electrode-electrolyte contributions must be taken into account on DC measurements, adding an extra resistance especially significant when measuring at low temperatures.

From the device point of view, the most important parameter related to the electrolyte is the Area Specific Resistance value ($ASR = thickness/conductivity$), that should take values below $ASR < 0.15\,\Omega cm^2$ [44]. As shown in Figure IV-22, for the membranes fabricated in this work, this value was achieved at temperatures as low as $400°C$ for $250\,nm$ thick free-standing membranes fabricated at $T_s = 600°C$ and after $T_a = 600°C$, showing the fabricated YSZ membranes as an excellent electrolyte for covering the intermediate-to-low range of operating temperatures in micro SOFC.

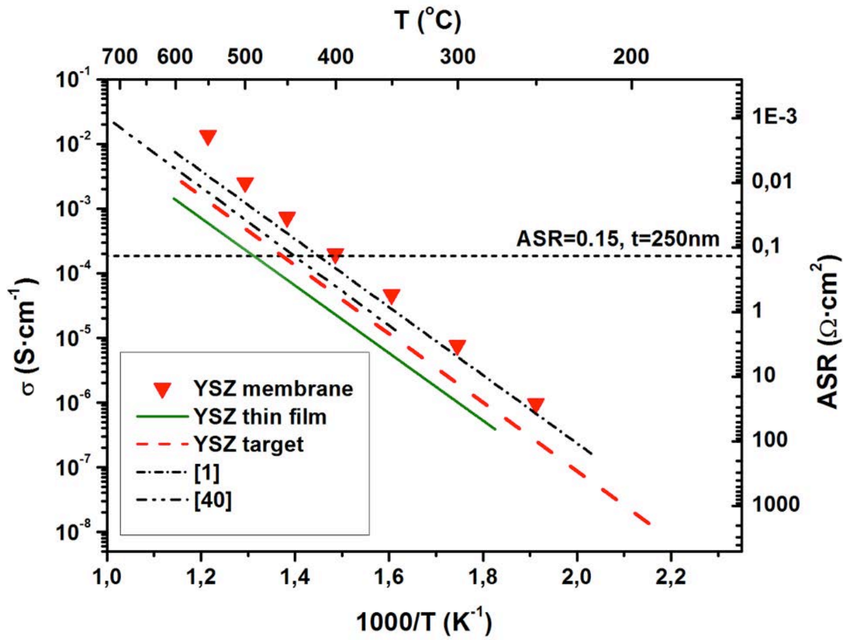

Figure IV-22. *Arrhenius plot of cross-plane conductivity of a $250\ nm$ thick YSZ membrane fabricated by PLD. Thin film YSZ in-plane conductivity and bulk YSZ conductivity (measured on the PLD target used for deposition and other taken from Ref. [1,40]) are also included for comparison. Right Y axis represents the ASR values calculated for a $250\ nm$ thick YSZ film.*

IV.4. Conclusions

The evaluation of as-fabricated residual stresses in YSZ membranes was carried out. Different stress regimes were found when varying the deposition temperatures (from $T_s = 200°C$ to $T_s = 800°C$), depending on the dominant residual stress mechanism. In comparison to the deposition temperature, membrane size and YSZ thickness was found to represent second order effects in the present range of study. The presently developed ability of tuning stresses in YSZ thin membranes is essential for their applicability in micro SOFCs where strong thermo-mechanical stability and good control over the ionic conduction (variable with the state of stress) is of fundamental importance.

High density, homogeneity and excellent thermo-mechanical stability at post-deposited annealing temperatures as high as $700℃$ were observed for a range of deposition temperatures of $T_S = 400–700℃$. This high deposition temperature was identified as the critical point for thermo-mechanically stabilizing the membranes. Correlation between the microstructural changes and the membrane state of stress evolution with deposition and annealing temperatures was confirmed by TEM analysis.

Finally, in-plane conductivity of a wide range of stressed YSZ films was evaluated without observing significant differences. In addition, cross-plane conductivity measurements on free-standing membranes was performed for the first time obtaining values of conductivity one order of magnitude higher than the in-plane measurements and slightly higher than bulk YSZ. Target values of ASR required for electrolytes in SOFC applications ($ASR = 0.15\,\Omega cm^2$) were achieved in the low temperature regime ($T = 400℃$ for $250\,nm$ thick membranes) opening new perspectives for micro SOFCs based on silicon platforms.

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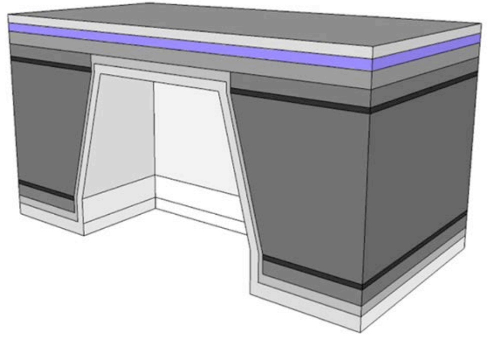
V. THIN FILM ELECTRODES FOR MICRO SOFC: THE CATHODE



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V.1. Thin film cathodes for micro SOFC

As shown in the previous chapter and related references [1], great performances have been reached on the functionality of thin film free-standing YSZ electrolytic membranes. YSZ membranes present thermo-mechanical stability through the whole intermediate temperature range (up to $700°C$), and reach the target value usually established for the Area Specific Resistance ($ASR = 0.15\ \Omega \cdot \mathrm{cm}^2$, [2]) at temperatures as low as $400°C$ [3,4]. However, despite the good performance achieved by the thin electrolytes themselves, the quick degradation shown by the typically implemented metallic electrodes at operating temperatures [5-9] still hinders the way to the commercialization of micro SOFC devices. Two opposite issues are confronted for the development of reliable metallic-based thin film electrodes. On one side, there is a need of certain thinness to promote dewetting of the metal with temperature, in order to form a porous film and enlarge the triple phase boundary (TPB) length while not loosing the connectivity. On the other side, the same dewetting process make these ultra-thin films unstable at operating temperatures. Agglomeration of the metal takes place during operation and time promotes the formation of isolated metallic islands, with the loss of in-plane percolation and/or dramatic reduction of active area. Fast degradation of metallic thin films implemented on micro SOFC configurations have been already reported by Ramanathan et al. [9,10], and some specific problems observed in this work related to the use of metallic electrodes are also described in *Appendix B*.

As a consequence of this, the development of more reliable and thermo-mechanically stable thin film ceramic-based electrodes seems to be the next natural goal for the micro SOFC community. In principle, the already shown good performances of state-of-the-art ceramic-based materials being used as electrodes in bulk SOFC make them ideal for their scalability to thin films and implementation as new micro SOFC electrode generation. Some attempts have been reported on the development of pure oxide-based electrodes for fabricating fully-ceramic micro SOFC, either working as cathodes [11-19] or as anodes [20]. However, up to the author best knowledge no deep investigation based on integration of these films in a free-standing micro SOFC has been undertaken. Only few results devoted to implement them in real micro SOFC configurations have been reported prior to this work [21-24].

In this chapter and the following, the fabrication of non-metallic based electrodes as well as their characterization in real micro SOFC configurations is described. Two different materials were chosen, one for acting as a cathode (this chapter) and the other for the anode side (*Chapter VI*). In particular, for the cathode side, this work focuses on the use of a lanthanum strontium cobaltite ($La_{0.6}Sr_{0.4}CoO_{3-\delta}$, LSC) for the fabrication of porous thin film cathodes for micro SOFC.

LSC is one of the most extended and studied cathode materials for SOFCs (together with other similar perovskites such as lanthanum ferrites or manganites), especially when working in the intermediate range of temperatures. However, reactivity issues between LSC and yttria-stabilized zirconia (tendency to form insulating $La_2Zr_2O_7$ or $SrZrO_3$ phases in the cathode/YSZ interface [25-27]) added to a large mismatch in the thermal expansion coefficient of LSC vs. YSZ ($TEC_{LSC} = 23\ ppm/K; TEC_{YSZ} = 11\ ppm/K$ [28-30]) limit its applicability at high operating temperatures or in devices involving high T fabrication steps ($T > 800°C$). Alternative electrolytes or barrier diffusion layers are sometimes introduced between the electrolyte and the cathode for reducing these effects but still degradation by detachment is present [31-33]. The implementation of the LSC layer in porous thin film form has been recently proposed as a good solution for this particular problem showing very promising results in the intermediate range of temperatures ($T <$

$700°C$) [13-15,34]. It is important to notice here that either increasing the density of LSC thin films (internal lattice strain fields involved, [35,36]) or lowering the pO_2 [37] can induce Sr segregation and mid-term quick degradation.

In this chapter, ***section V.2*** is first devoted to the microstructure optimization and electrochemical characterization of porous LSC thin films. Here, LSC was deposited on top of dense YSZ electrolyte films on bulky silicon-based substrates, fabricating LSC (electrode)/YSZ (electrolyte) bi-layers completely by PLD. After a complete microstructural and thermo-mechanical characterization, in plane conductivity measurements on the whole operating temperature range (up to $700°C$) were performed in order to evaluate the current collection capability of the electrode.

Then, the optimized thin film cathodes were implemented on real micro SOFC configurations, i.e. free-standing membranes. In ***section V.3*** the specific characterization of the thin film cathode on LSC/YSZ/LSC symmetrical membranes is detailed. In this thesis, the electrode testing on real micro SOFC configurations (either thin film cathodes or anodes, this chapter and the following) was performed using the lastly-developed large-area YSZ free-standing membranes as electrolyte. The design and fabrication of these membranes have been already described on *Chapter III* (*Section III.3*).

V.2. Porous LSC thin films: fabrication and characterization

Deposition conditions for obtaining LSC and YSZ layers with porous or dense microstructures respectively are detailed on *Chapter II* (*Section II.3.3*). Figure V-1 shows top view and cross section SEM images of as-deposited (a-b) and post-annealed at $700°C$ (c-d) LSC porous layers on top of dense YSZ films. The typical columnar growth of PLD-deposited complex oxides [38] was observed for both the YSZ and LSC layers. However, while YSZ presented strongly ordered and well defined compact grains, LSC appeared as disordered columnar clusters with open porosity all along the whole thickness of the films. The origin of these differentiated microstructures corresponds to the set of PLD deposition conditions selected for each material, mainly temperature and pressure. According to Infortuna et al. [38], a high background pressure promotes the mobility of species allowing the formation of single clusters on the film, while the substrate temperature is the responsible of re-crystallization and grain growth during the deposition. Thus, low-temperature and high-pressure depositions, like the ones employed for LSC, usually provide disordered films formed by separated clusters with a high percentage of amorphous phase and porosity. Meanwhile, high-temperature and low-pressure conditions, as employed for YSZ, yield to ordered dense layers.

The comparison of the Figure V-1 (a,b) and (c,d) shows the evolution of the microstructure with a thermal treatment up to maximum expected working temperatures ($T = 700°C$). While the YSZ layer remains essentially the same, showing a great stability against temperature, the microstructure of the LSC layers shows a greatly beneficial more open porosity. This microstructural evolution is likely associated to the combined effect of the crystallization of the film from its initial amorphous nature and the partial sintering and densification of the original clusters in bundles. By simple image processing of the SEM images, the in-plane porosity was found to be of *ca.* 30% ensuring good percolation, large TPB lengths and reasonable diffusion of gas species. The porosity also balances the big difference in thermal expansion coefficient (TEC) reported for both materials and avoids Sr segregation [29,30,36]. An excellent adhesion between YSZ and LSC was clearly observed in the SEM analysis.

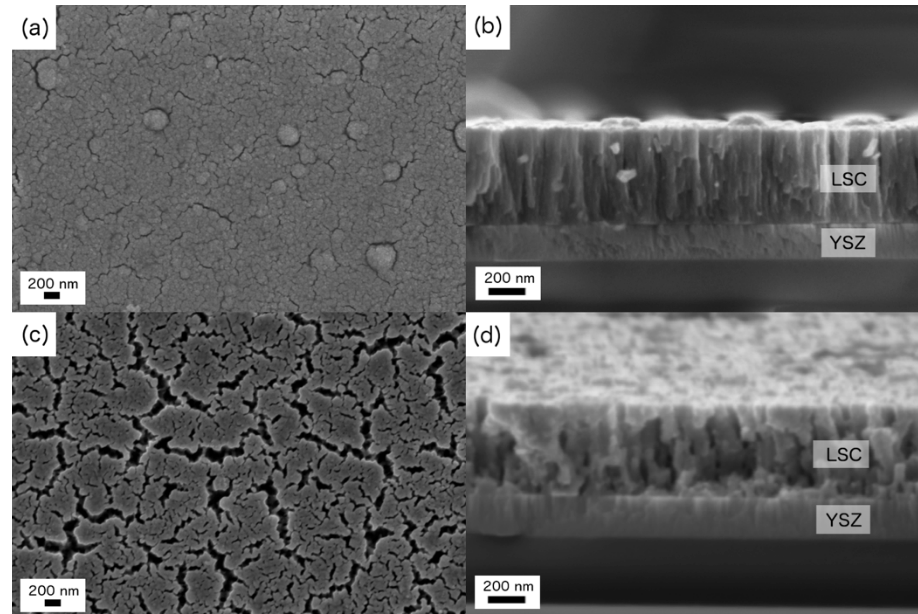


Figure V-1. *Top view and cross section SEM images of as-deposited (a, b) and post-annealing (c,d) porous LSC layers over previously deposited dense YSZ.*

Figure V-2 shows the evolution with temperature of the XRD patterns of the LSC/YSZ bi-layer deposited on $Si_3N_4/SiO_2/Si$ substrates from room temperature to 700℃. The pattern acquired at room temperature corresponds to the as-deposited sample. Since deposited at high temperatures, a crystalline YSZ layer is clearly shown by the presence of diffraction peaks corresponding to a pure cubic *Fm-3m* structure (JCPDS-ICDD #30-1468). No diffraction peaks were observed for as-deposited LSC indicating an amorphous nature of the layer prior to annealing. As previously mentioned, this is mainly due to the low substrate temperature employed during the PLD process. The evolution of the XRD patterns with temperature shows a crystallization of the LSC layer between 500 and 550℃ by the appearance of new diffraction peaks corresponding to the cubic *Pm-3m* structure (JCPDS-ICDD #48-0121). The LSC crystallization at such low temperatures is very convenient for reaching the main goal of avoiding high temperature steps in the fabrication process. It is also important to notice that no reactivity between LSC and YSZ was observed up to 700℃, showing the applicability of LSC on a great range of temperatures covering the typical intermediate temperature range ascribed to the micro SOFC.

Figure V-3 shows the evolution of the in-plane conductivity with the temperature on a $250\ nm$ thick LSC film, measured by using the Van der Pauw method. Starting from as-deposited samples, an improvement of more than one order of magnitude was observed at $T = 500 - 525$℃. No hysteresis was observed for the subsequent cooling and heating curves, suggesting the irreversibility of the phenomenon. Therefore, and in concordance with the XRD study (Figure V-2), the abrupt change could be associated to the crystallization of the LSC layer and the corresponding increase of electronic conductivity [34]. A maximum value of $200\ S/cm$ on in-plane conductivity was observed after crystallization. This is well over the target values typically required for SOFC electrodes ($20\ S/cm$), even more assuming the sub-μm size of the fabricated cathode. No degradation or drastic losses in conductivity were observed neither with temperature nor time up to 700℃ and for more than $60\ h$.

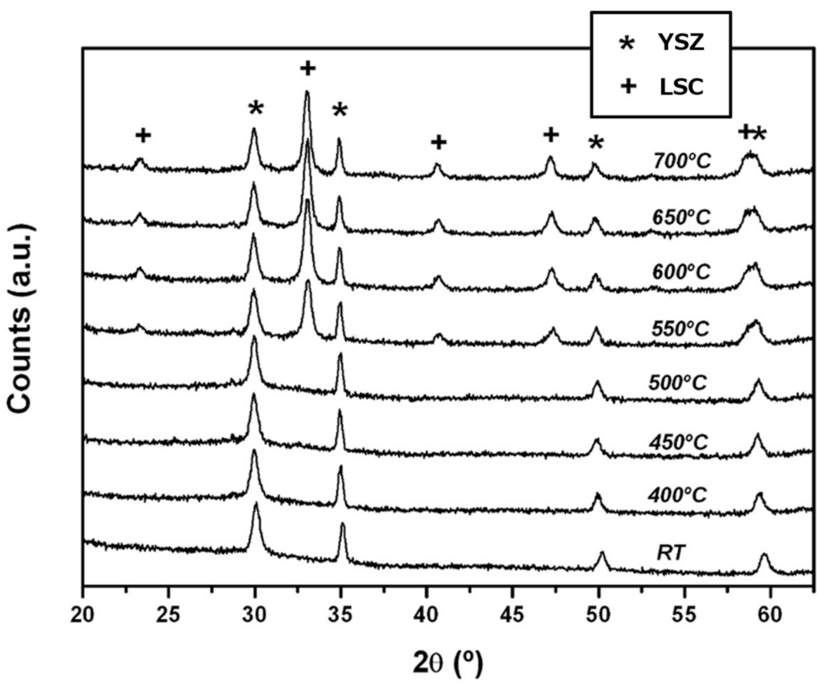


Figure V-2. *X-Ray diffraction patterns of a porous LSC film deposited over dense YSZ on a $Si_3N_4/SiO_2/Si$ substrate, measured at different temperatures. The stars correspond to YSZ diffraction peaks, while the crosses point out the main peaks of a crystalline LSC pattern, appeared between* $T = 500℃$ *and* $T = 550℃$

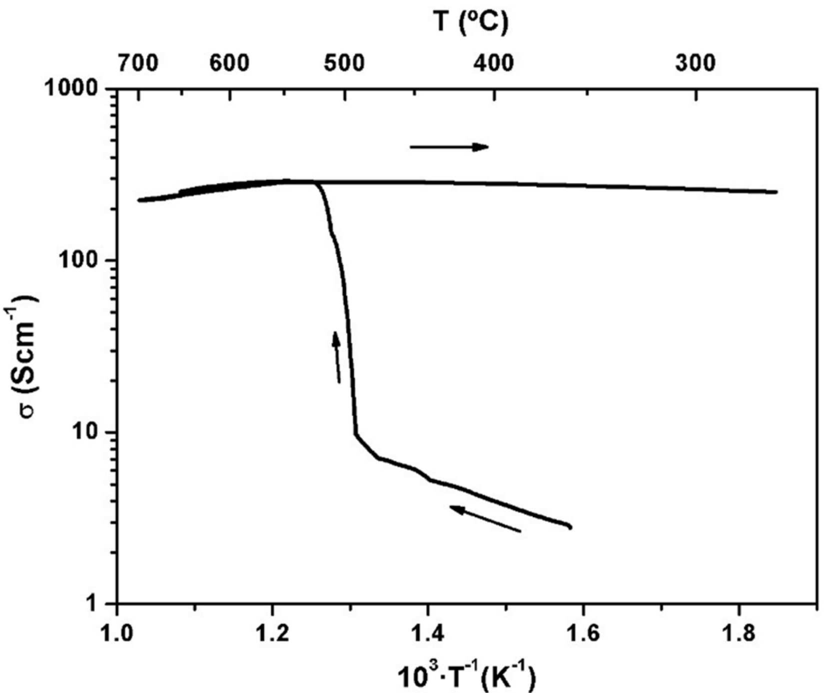


Figure V-3. *Evolution of the in-plane conductivity of a porous LSC cathode deposited over dense YSZ on a $Si_3N_4/SiO_2/Si$ substrate, measured by the van der Pauw method.*

V.3. Implementation and electrochemical characterization of LSC films as cathodes for large-area micro SOFC

Figure V-4 shows top view and cross section images (optical and SEM, respectively) of the self-supported large area membranes fabricated in this work (see *Chapter III, Section III.3*), after deposition of YSZ and LSC. LSC/YSZ/LSC membranes as high as $8\ mm^2$ were fabricated, although the standard size for testing was fixed to be $2.5\ mm^2$ (total active area -without silicon slabs- of $1.9\ mm^2$). As mentioned on *Chapter III*, an increasing on total active area of $\sim 30x$ is reached by using this membrane design, compared to the basic squared design previously reported (by the authors, and other groups [1,3,10]). The typical buckling profiles obtained on free-standing YSZ membranes (see *Chapter IV*) were also observed when fabricating large-area LSC/YSZ/LSC membranes, although adjusted to the hexagonal geometry of the single membranes (free-standing area limited by the silicon grid). No change was observed on the buckling pattern before and after the LSC double deposition, thus the contribution of the porous LSC to the total membrane stress was considered negligible compared to the high stress already present on YSZ free-standing films (as expected being LSC a porous and therefore adaptable film). The functional tri-layer (LSC/YSZ/LSC) presented a total thickness of less than $1\ \mu m$ with $500\ nm$ of dense YSZ electrolyte and $250\ nm$ of porous LSC at both sides, as can be seen on Figure V-4 (b). The porous and columnar structure of the LSC film observed on deposits over bulky substrates (see Figure V-1) was maintained when fabricating membranes. Meanwhile, YSZ layer remained highly dense, as can be observed in the image. Therefore, the obtained microstructure on both free-standing layers was considered ideal for functioning as cathode/electrolyte bi-layer on a micro SOFC.

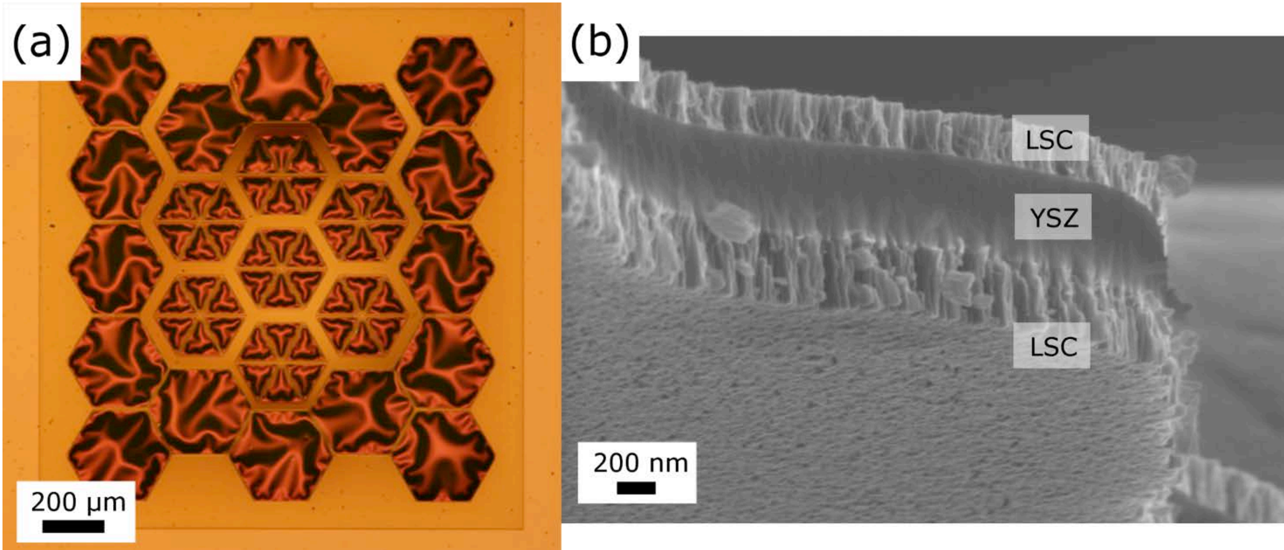


Figure V-4. *(a) Top view optical image of a large area LSC/YSZ/LSC free-standing membrane supported on a doped silicon nerves grid. (b) SEM cross sectional view of a flying free-standing LSC/YSZ/LSC tri-layer.*

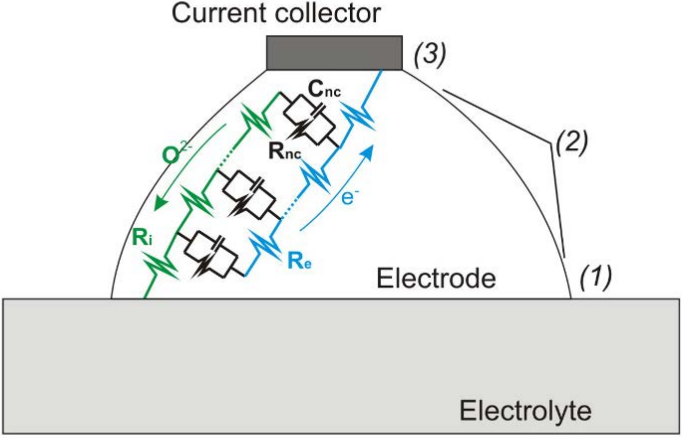
The LSC/YSZ/LSC membranes were characterized by EIS in order to evaluate their electrochemical performance in the final micro SOFC configuration. As described on *Chapter I* (*Section I.3.2*), to ensure a good electrode performance on porous thin films with limited in-plane electronic conductivity (as it is the case of LSC), high electronic conducting layers have to be implemented as current collectors on top of the electrode films. This way, although loosing active area (zones covered by the dense current collectors become inactive), the percolating distance is significantly reduced and the associated resistance is greatly lowered. Here, patterned $150\ nm$ thick Pt films were implemented on both sides of the membrane. This

pattern was defined by nanosphere lithography as described in *Chapter III* (*Section III.2.3*), maintaining a substantial porosity after high temperature characterization.

Figure V-5 depicts two Nyquist plots corresponding to impedance spectra obtained at different temperatures. Below $350°C$, two arcs were clearly observed. A small arc appeared at high frequencies due to the resistance associated to the ionic conduction through the bulk electrolyte ($T = 300°C$ spectrum on Figure V-5) while a big arc present at lower frequencies is presumably associated to poor performance of the electrodes. Due to the columnar-like growth observed for the PLD deposited YSZ, no grain boundary contribution to the resistance was expected (neither observed) for the electrolyte (see *Chapter IV*, *Section IV.3.2*). At higher temperatures, the arc corresponding to the electrolyte became a pure serial resistance while the low-frequency arc associated to the symmetrical electrodes showed a great reduction in resistance ($T = 600°C$ spectrum on Figure V-5). This arc could be fitted by the Adler Lane Steele (ALS) continuum model[1], typically employed for the characterization of porous mixed ionic-electronic conductor (MIEC) materials. The excellent agreement between model and experimental data (see the continuous line representing the fitting) suggests that the non-charge transfer phenomena (solid-state oxygen diffusion and O_2 surface exchange) and the gas-phase diffusion dominate the electrochemical behaviour of the system. No arcs associated to charge transfer phenomena were observed.

[1] The ALS model is commonly used for describing mixed ionic-electronic conductors (MIEC) in base of a transmission line model. The figure below shows a scheme of an electrode/electrolyte system, with the associated equivalent circuit. The electrode behaviour is described as two coupled transmission lines, i.e. an ionic pathway (R_i) and an electronic pathway (R_e). A series of coupling elements connect the two channels, representing the non-charge transfer phenomena occurred on the electrode ($R_{nc}C_{nc}$). In principle, if sufficient electronic and ionic conductivity, the non-charge transfer phenomena could take place along an extended part of the surface of the electrode, thus the use of a transmission line to define the ionic pathway is required (the voltage is different depending on the distance to the electrolyte).

Then, three opposed scenarios can be then found depending on the electrode properties. First, if the electrode presents high resistances associated to the ionic conduction (high R_i), the reactions (non-charge transfer phenomena, $R_{nc}C_{nc}$) would be limited to the zone *(1)*, close to the electrolyte. Second, if the electrode presents very low electronic conductivity but good ionic conduction (high R_e), the active area would be limited to the zone *(3)* (problems with gas diffusion could be an extra cause of this second behaviour). Finally, the ideal situation would be having both good electronic and ionic conductivity on the electrode with perfect gas diffusion and thus the whole electrode area (zones *(1)*, *(2)* and *(3)*) would be catalytically active. This last scenario corresponds to a MIEC behaviour and can be explained by the ALS model (semi-infinite electrode length assumed, where the whole electrode area is active). On the contrary, the two first scenarios mean that only a part of the electrode is actively used, while the rest of it remains catalytically inactive.



Further information and a complete description of the model can be found at [39].

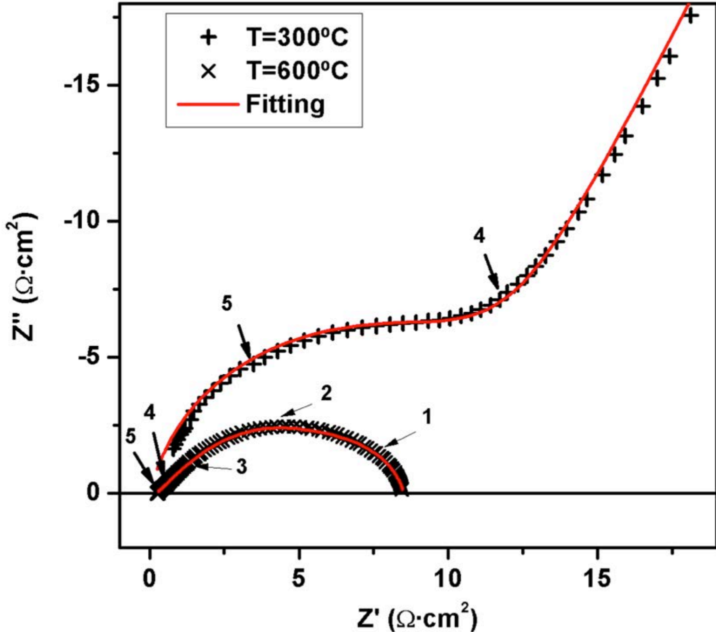


Figure V-5. *Impedance spectra of a symmetrical LSC/YSZ/LSC free-standing membrane, measured at* $T = 600°\text{C}$ *and* $T = 300°\text{C}$. *Solid red lines represent the fitting for the two different spectra. The numbers refer to the frequency decades covered by the EIS analysis.*

Figure V-6 shows Arrhenius plots of the ASR of the electrolyte (ASR_{YSZ}) and the electrolyte-cathode interface (ASR_{LSC}) as a function of the temperature. These values were obtained from the equivalent circuit fitting of the set of impedance spectra. Only the active area of the membrane was used for the calculations. The ASR dependence on temperature follows an Arrhenius-type law for both the YSZ and the LSC, with activation energies of $E_a = 0.9\ eV$ and $E_a = 1.6\ eV$, respectively. The obtained E_a are found to be similar to other reported values for each material ([23,38,40-42] for YSZ, [13,14,16,34] for LSC).

The YSZ electrolyte presented similar ASR_{YSZ} values to those previously measured on standard YSZ free-standing membranes (see *Chapter IV*, *Section IV.3.2*). Although thicker films were used, the target value of $0.15\ \Omega cm^2$ [2] was already attained in the present case at $450°\text{C}$. Therefore, the low ASR values measured for the electrolyte clearly pointed at the ceramic cathode as the resistance-limiting element on the all-ceramic fuel cell configuration. This observation represents a new insight for the development of micro SOFC, as until now main effort had been devoted to the optimization of the electrolyte (firstly identified as the limiting element).

LSC resistivity values were in the same range as previously published works on thin film form, some of them also plotted on the figure for direct comparison [13,34]. Since the target value of cathode/electrolyte bi-layer ASR is $0.3\ \Omega cm^2$ [2], results shown here suggest the need of temperatures as high as $700°\text{C}$ for reaching this ASR target for the LSC/YSZ bi-layer (dot line in Figure V-6). Although this forces to work at higher temperatures than some previously published micro SOFC devices based on a Pt/YSZ/Pt configuration, the proven stability of the LSC films at such temperatures makes the system more reliable considering the fast degradation observed for pure metallic based electrodes under working conditions (see *Appendix B*). In addition, working at such high temperatures allows substantially increasing the electrolyte thickness to several hundreds of nm. Thicker electrolytes make the membrane more robust

reducing the probability of pinhole formation, i.e. minimizing one of the most frequent reasons of dramatic failure for free-standing electrolyte membranes [4].

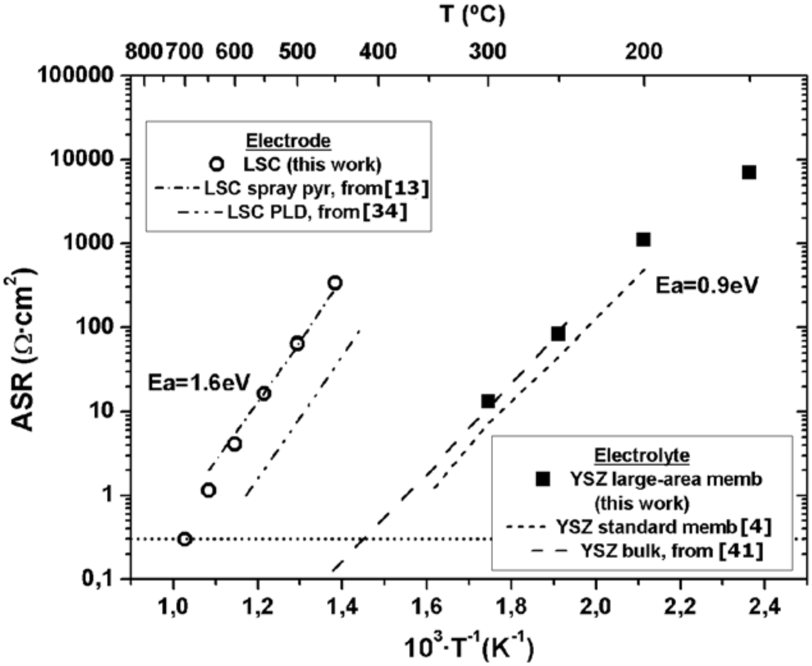


Figure V-6. *Evolution of the ASR of both LSC electrode and YSZ electrolyte with temperature, measured on symmetrical LSC/YSZ/LSC free-standing membranes. Reference values from previously published works [4,13,34,41] are also plotted for comparison. Dot line marks the* $0.3\ \Omega cm^2$ *target value for the cathode/electrolyte bi-layer.*

V.4. Conclusions

Highly porous LSC thin films (up to 33% in-plane porosity) were deposited by PLD over dense YSZ electrolytic layers. The obtained microstructure on both films was found to be appropriate for the fabrication of cathode/electrolyte bi-layers for micro SOFC applications. An in-plane conductivity of $200\ S/cm$ was measured on the porous LSC films at the typical range of temperatures of micro SOFC ($450 - 700$℃), well over the values typically required for SOFC cathodes. No degradation was observed neither with temperature nor time up to 700℃ and for more than $60\ h$.

The implementation of LSC porous layers is presented in large-area symmetrical LSC/YSZ/LSC free-standing membranes (using dense Pt grids as current collectors). The thermo-mechanical stability of the membranes was ensured up to 700℃ (no cracks appeared after thermal cycling). Target values of Area Specific Resistance required for SOFC cathode/electrolyte bi-layers ($ASR = 0.30\ \Omega cm^2$) were achieved in the intermediate range of temperatures ($T = 700$℃). These results showed the feasibility of using the fabricated LSC/YSZ bi-layers as cathode/electrolyte on micro SOFC at 700℃ anticipating more reliable all-ceramic-based micro solid oxide fuel cells.

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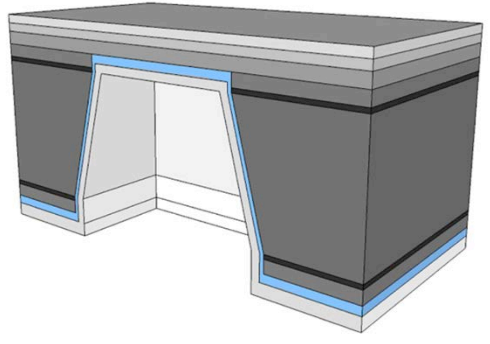
VI. THIN FILM ELECTRODES FOR MICRO SOFC: THE ANODE



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VI.1. Thin film anodes for micro SOFC

Apart from the general requirements assessed to FC electrodes (high electronic conduction, optimized microstructure to enhance TPB length), anodes in particular must be stable under reducing atmospheres. Most of the ceramics typically employed on the cathode side are however unstable and/or degrade under low pO_2 atmospheres on the anode. Only a few materials have been proposed for fabricating symmetrical SOFC as functional materials for anode and cathode [1]. The state-of-the-art anodes on standard bulk SOFC systems are usually based on cermet materials, i.e. composites of an oxide ionic conductor (ceramic) and an electronic conductor (metal), which present very good performances [2]. The typical materials utilized for the ceramic component are state-of-the-art electrolytes such as YSZ or CGO, while the most widely used material for the metallic part is Ni, due to its reduced price and good electrochemical and mechanical compatibility with both YSZ and CGO [3,4].

However, cermet transferability to thin films has been shown to be a difficult task. Only a few works dealing with thin film anodes (below 1 µm) have been published up to now [5-9], opposite to the relatively high number of publications appeared recently on the development of thin film cathodes (see previous *Chapter V*), and just one report on the implementation of a thin film cermet on real micro SOFC configurations has been published [9], showing quite fast degradation with time (62% of the initial power density within $3\ h$). In this sense, the difficult transferability to thin films of state-of-the-art anode materials for bulk SOFCs still means a great challenge for the micro SOFC community. By reducing the thickness of the porous ceramic network when scaling it down, there is usually a limited metal permeation onto it, favouring the typical metal coarsening happening at relatively low temperatures, especially for Ni. As a consequence, there is a fast loss of electronic conductivity (in-plane percolation) on the cermet already at operating temperatures, i.e. IT range [10-13].

According to this, two main strategies appear to be the most suitable for fabricating more reliable thin film anodes for micro SOFC, namely the use of more stable fully ceramic anode materials or the implementation of cermets based on more stable metals. On one side, the proven stability of state-of-the-art ceramics with temperature (tested to be stable under bulk SOFC conditions, $> 800℃$) ensures no degradation of the electrode with time if moving to *thin film fully ceramic anodes*. Moreover, using outstanding thin film deposition techniques such as PLD would permit a microstructural tuning looking for the best electrode performance [14]. In this sense, although in general complex ceramic oxides present lower anode performance than cermet materials (when being tested in bulk SOFC), there exist some promising options apparently suitable for their transferability to thin film. I.e. the use of porous doped ceria films (already tested in thick (several μm) films [7]) or other single oxides such as $La_xSr_{1-x}CrO_{3-\delta}$ or their derived B-site doped materials ($La_xSr_{1-x}Cr_yM_{1-y}O_{3-\delta}$ (M = Mn, Fe, Co, Ni)) [3]. On the other side, if thin film cermet is still the choice, it seems that moving to *thermo-mechanically more stable metals* such as Pt is the natural next step [8].

Ceria-based oxides (either gadolinia-doped, CGO, or samaria-doped, SDC) have been commonly used on SOFC technology due to its relatively high oxide ionic conductivity [15-17]. In this sense, reports on the transferability of functional doped-ceria films to thin films for micro SOFC applications have been published [18-27]. In particular, PLD has been proven to be highly effective for depositing thin films with tuned microstructures [21,23]. It is important to notice here that ceria-based oxides typically suffer reduction under reducing atmospheres [16,28,29] loosing the electronic isolation. Although this has commonly limited their applicability as electrolyte (unless extra barrier layers are added), this electronic conductivity has however found to be attractive for the anode. Becoming a mixed ionic-electronic conductor, doped-ceria films could act as pure ceramic anodes or as optimum ceramic component on cermets [28].

In this sense, a recent publication by Jung et al. [7] have already shown the capabilities of porous SDC films as an excellent fully ceramic anode in the intermediate temperature regime, with no need of extra

metallic component into it due to the already high electronic conductivity of the SDC itself. According to Jung et al., a certain thickness (several μm) is required on the SDC films for enlarging enough the electrode length and thus reaching reliable values of resistance per unit area.

In this work, porous $Ce_{0.8}Gd_{0.2}O_{1.9-\delta}$ (CGO) thin films have been fabricated and tested to be used as anodes in micro SOFC. First, the characterization of thin CGO films deposited over dense YSZ films (electrolyte layer) is presented in ***section VI.2***. Different thicknesses were tested on the PLD-deposited films, in order to test the maximum thickness achievable while still remaining thermo-mechanically stable. Then, the electrochemical performance of the stable films was studied. As shown below, although very promising microstructures were obtained, these films presented (i.) a limitation on the maximum thickness on less than $1\ \mu m$ and (ii.) a low electronic conductivity on the IT range of temperatures. These facts limited the applicability of the porous CGO films as fully ceramic anodes on micro SOFC.

Therefore, thin film CGO-Pt cermets were alternatively fabricated (***section VI.2.2***). Pt films were deposited over the porous CGO layers by sputtering and a good interconnection between both materials was ensured by thermal treatment and the subsequent metal dewetting [30-34]. Pt-CGO/YSZ/CGO-Pt free-standing membranes were fabricated using the large-area membrane configuration previously presented (see *Chapter III*) for testing the anode on real micro SOFC configurations (see ***section VI.3***). Its electrochemical performance was characterized by impedance spectroscopy, showing the applicability of the fabricated CGO-Pt films working as anode on a micro SOFC at temperatures above $700℃$. An electrical model for explaining the electrochemical behaviour is given here, suggesting ways for further improvement of the fabricated films (i.e. reduce the operating temperature and improve the anode performance).

VI.2. Ceria-based thin films: fabrication and characterization

VI.2.1. Porous CGO: microstructure and electrical properties

CGO/YSZ electrode/electrolyte bi-layers were deposited by PLD on $Si_3N_4/SiO_2/Si$ substrates for their microstructural and electrochemical characterization. The deposition conditions described on *Chapter II* were used during the PLD process. Porous-to-dense microstructure variation was accomplished by changing background pressures on the deposition chamber from $0.13\ mbar$ for CGO to lower pressures i.e. $0.025\ mbar$ for YSZ

Figure VI-1 shows the evolution with temperature of the XRD pattern of one of those bi-layers, where spectrum marked as RT (room temperature) corresponds to the as-deposited sample and consecutive annealing temperatures are shown, from $400℃$ to $700℃$. Diffraction peaks from both crystalline YSZ and CGO diffraction patterns (cubic *Fm-3m* structure from JCPDS-ICDD #30-1468 and #75-0161, respectively) were already observed on as-deposited samples, despite having been prepared with very different conditions, i.e. $100℃$ for the CGO, $600℃$ for the YSZ. As expected since deposited at high temperatures, YSZ layer was fully crystalline as-deposited and no peak evolution was observed when heating up to $700℃$. However, sharpener and more intense peaks were observed for the CGO when increasing the temperature (see the increment on T_a on Figure VI-1). This observation corresponds to the crystallization of a certain amount of amorphous CGO thought to be present on the as-deposited films due to the low deposition temperature utilized. In terms of fabrication, this improve on crystallinity at such intermediate temperatures is considered very convenient. More crystalline films are expected to present better electrochemical performance, due to the improvement on mass transport properties of the crystallites compared to the amorphous form.

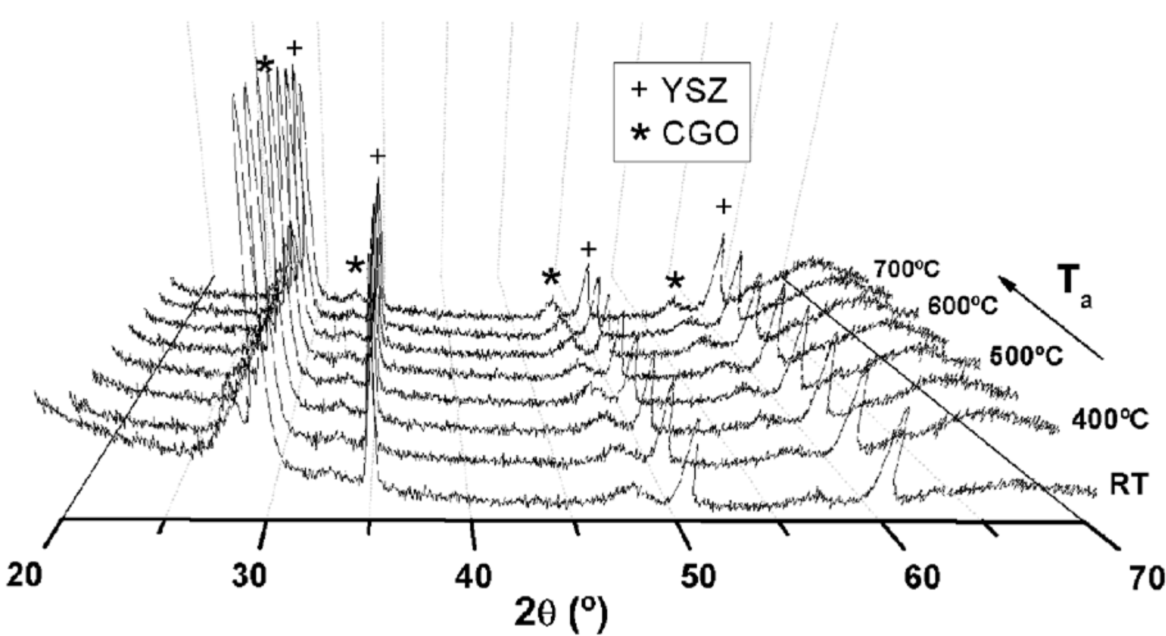

Figure VI-1. *X-Ray diffraction patterns of a porous CGO film deposited over dense YSZ on a Si_3N_4/SiO_2/Si substrate, measured at different temperatures (T_a)*

Figure VI-2 shows top view and cross-section SEM images of as-deposited (a,b) and post-annealed at 700℃ (c,d) CGO porous layers deposited over dense YSZ films, as complementary microstructural study to the XRD experiment. A columnar and well-ordered grain growth was observed for both CGO and YSZ as-deposited layers. However, lower density was obtained on the CGO when compared to the compact and fully-dense YSZ film. The higher background pressure during PLD deposition of CGO favoured the formation of this type of microstructure, due to a higher mobility of species on the ablation plume and subsequent formation of separated clusters when arriving to the substrate, forming the porous network [23]. After thermal treatment, no significant differences were observed on the YSZ film, showing a great stability against the temperature (consistent with previous XRD observations). Meanwhile, more faceted grains were observed on the CGO film and a much more open porosity was attained (Figure VI-2 (c)). The crystallization of the partially amorphous CGO is probably the reason for the microstructural change promoted by the temperature, and it is thought to be beneficial for the electrode performance as it facilitates the diffusion of gas species through it.

Porous CGO films of both $250\ nm$ and $1\ \mu m$ thick were fabricated, for testing the maximum thickness achievable while remaining thermo-mechanically stable. According to Jung et al. [7], thick porous films ($> 1\mu m$) are needed to reach good electrochemical performances on pure ceramic doped-ceria anodes. However, in the present case problems of detachment and cracking unfortunately appeared under operating conditions ($T = 700℃$) on the thicker films, while the thinner ones remained stable. Figure VI-3 shows top view and cross-sectional images of a $1\ \mu m$-thick CGO/ YSZ bi-layer delaminated from the Si-based substrates, opposite to the $250\ nm$-thick films shown in Figure VI-2. Therefore, maximum CGO thickness for fabricating reliable CGO/YSZ bi-layers was limited to less than $1\ \mu m$, which reduced the CGO capabilities for working as anode (high anode resistance), most probably becoming necessary the addition of an electronic conductor element to the system.

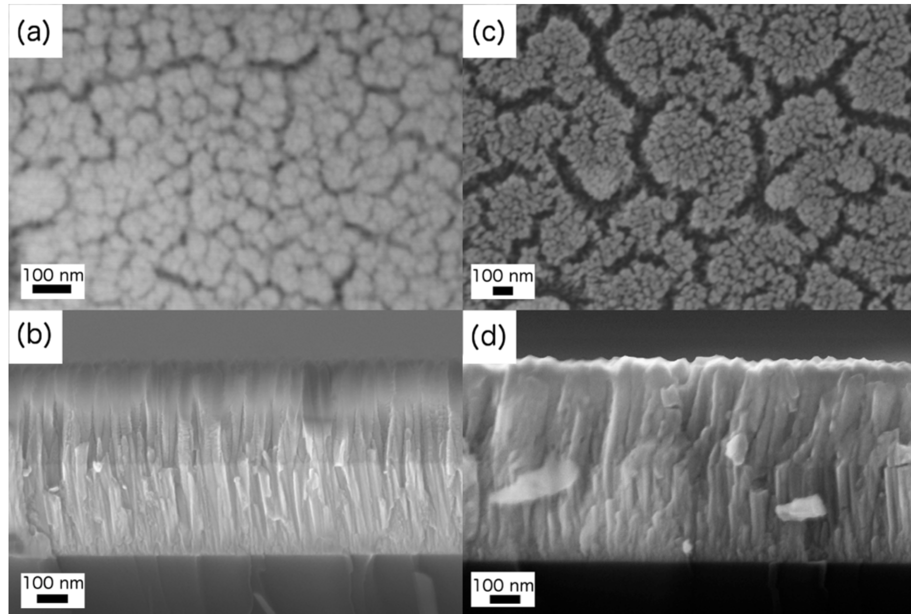

Figure VI-2. *Top view and cross-section SEM images of as-deposited (a,b) and post-annealing (c,d)* $250\ nm$*-thick porous CGO layers over previously deposited dense YSZ.*

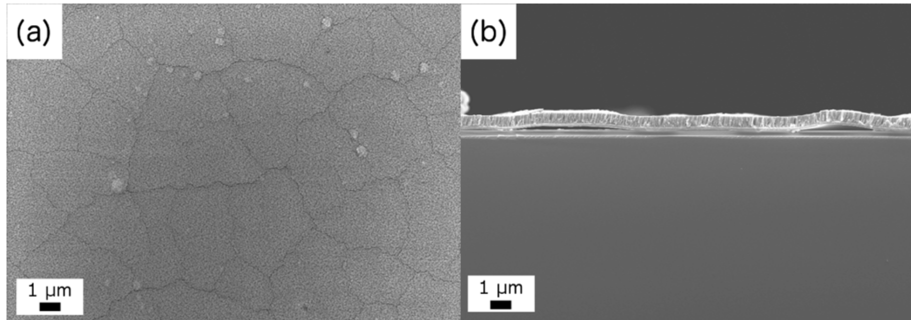

Figure VI-3. *Top view and cross-section SEM images showing the delamination occurred when increasing CGO thickness up to* $1\ \mu m$.

In order to evaluate the electronic conductivity of the thin CGO, in-plane conductivity measurements were carried out by four-probe Van der Pauw technique on the stable $250\ nm$-thick porous CGO films under reducing atmospheres ($5\%H_2$ - $95\%Ar$). Figure VI-4 shows an Arrhenius plot of the CGO conductivity as a function of temperature. As expected, low conductivity values (less than $0.1\ S/cm$) were measured on the porous films in the whole range of operating temperatures, i.e. up to $700°C$. Although still showing the anode functionalities of the fabricated CGO films, that low conductivity is clearly insufficient for current percolation. Therefore, for the fabrication of effective thin film anodes, adding an electronic conductor element was definitely needed in order to provide sufficient electronic conductivity to the electrode.

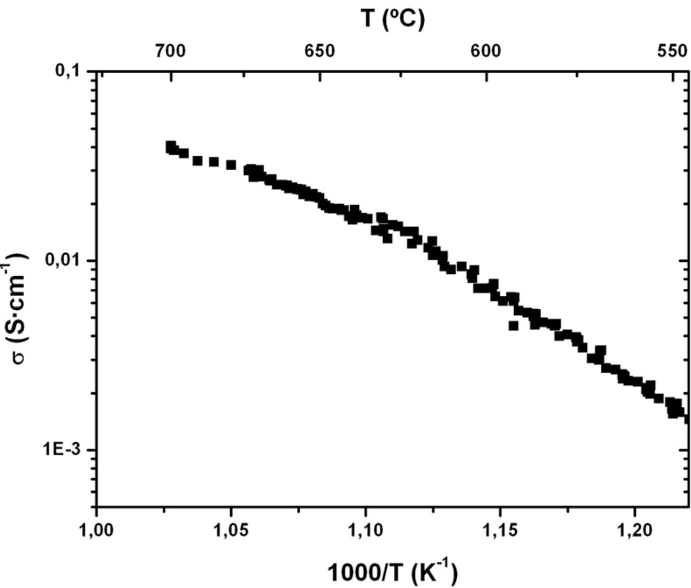

Figure VI-4. *Evolution of the in-plane conductivity of a* $250\ nm$*-thick porous CGO anode deposited over dense YSZ on a* $Si_3N_4/SiO_2/Si$ *substrate, measured by the van der Pauw method.*

VI.2.2. Pt-CGO cermets: thin film microstructure

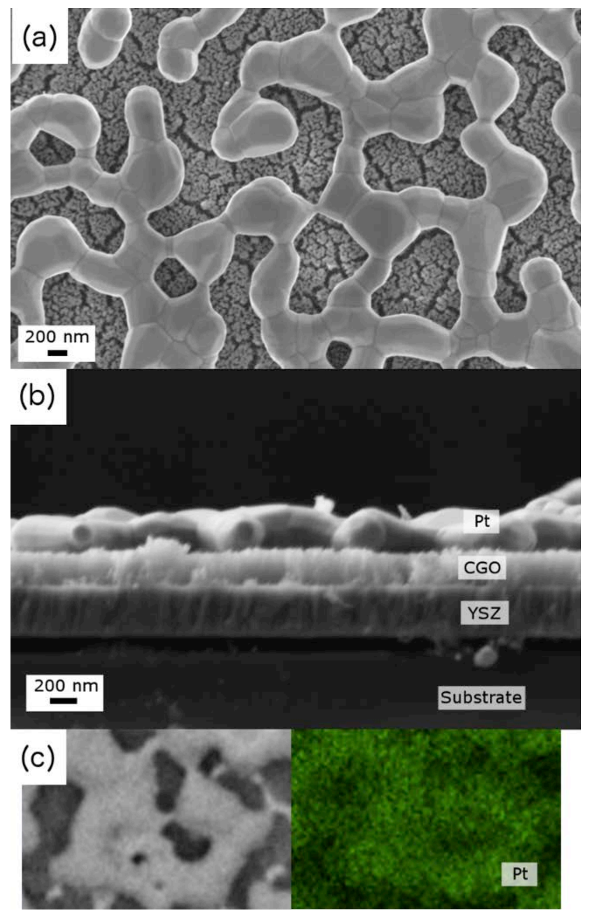

Figure VI-5. *Top view (a) and cross-section (b) SEM images of Pt-CGO films annealed at 700ºC. (c) shows the EDX Pt signal (green) in comparison with the electron image from the same region.*

$150\ nm$-thick Pt films were deposited by sputtering over the porous CGO films in order to provide the thin film anodes with sufficient electronic conductivity. Figure VI-5 (a,b) shows top view and cross-sectional SEM images of a Pt-CGO bi-layer deposited on top of dense YSZ, already after a thermal treatment up to $700°C$. As shown in the figure, although deposited dense, the typical dewetting of metal thin films [30] was observed to happen during annealing, thus forming agglomerates and a porous but continuous Pt network. Nevertheless, additional EDX analysis on top view images (Figure VI-5 (c)) confirmed the presence of Pt not only on the formed dense grid but also over the porous CGO (Pt present on the *uncovered* zones). Therefore, despite the formation of agglomerates on top of the CGO film, it is assumed that part of the Pt also percolates into the CGO porous network, favouring CGO-Pt interconnection and the formation of the cermet.

VI.3. Implementation and electrochemical characterization of Pt-CGO anodes for large-area micro SOFC

Pt-CGO/YSZ/CGO-Pt symmetrical free-standing membranes as the one shown in Figure VI-6 were fabricated, in order to evaluate the cermet electrochemical performance in the exact final micro SOFC configuration. As already mentioned, large-area YSZ free-standing membranes supported on silicon nerves were used here for testing (membrane active area $1.9\ mm^2$ on a total membrane are of $2.5\ mm^2$). The fabricated membranes showed the typical buckling pattern already observed on the YSZ membranes and LSC/YSZ/LSC membranes, and similarly to the cathode, no visible change on the patterns were observed when adding the Pt-CGO films on both sides (negligible stress contribution of the porous anode film compared to the dense YSZ membrane).

Great film homogeneity was observed along the whole free-standing membrane. As shown in Figure VI-6 (b), YSZ film was slightly thicker than CGOs ($300\ nm$ for the YSZ versus $200\ nm$ in the case of CGO). When adding the $150\ nm$-thick Pt films on both sides of the membrane, total thicknesses still remained below $1\ \mu m$. Same microstructures than those obtained on previous study over bulky substrates (i.e. porous and columnar CGO films, highly dense and columnar YSZ film) were achieved when fabricating membranes.

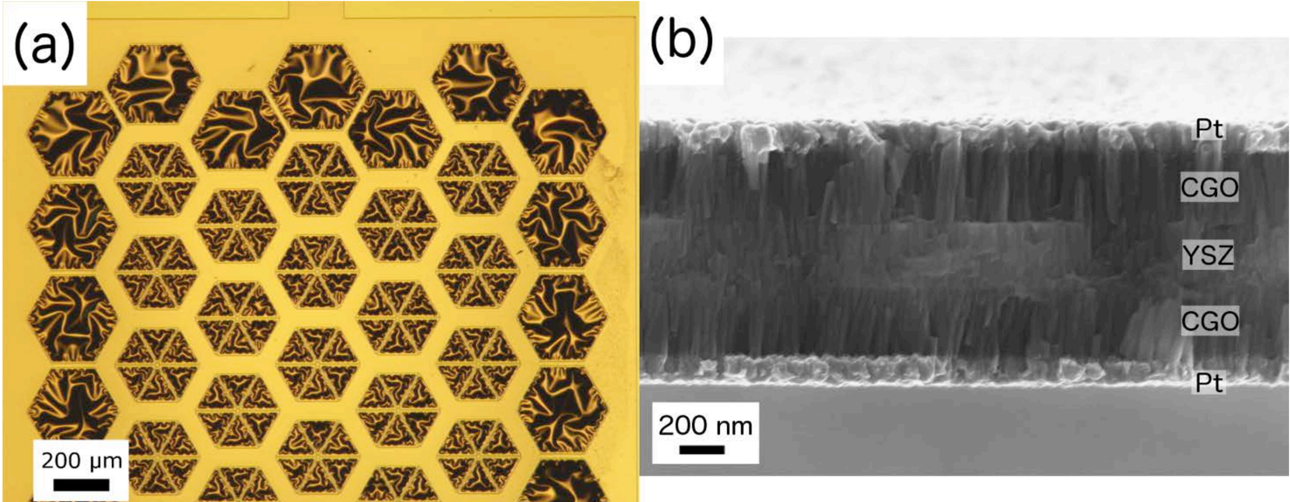

Figure VI-6. *Top view optical image (a) and cross-section SEM image (b) of one of the free-standing membranes tested.*

The anode electrochemical performance was characterized by impedance spectroscopy (EIS). Figure VI-7 depicts a Nyquist plot corresponding to impedance spectra obtained for the symmetrical membrane at 650°C, under a single 5%H_2-95%Ar reducing atmosphere. Two separated arcs were clearly observed with resistance values in the same order of magnitude, but clearly separated due to the difference on their associated capacitance. Therefore, the data was fitted according to the equivalent circuit depicted on Figure VI-7 (b)[1] (R_S correspond to a series resistance that includes contact resistances and cables).

It is important to notice here that the contribution from the dense YSZ electrolyte is expected to be negligible at such temperatures, as shown on previous studies on the same type of substrates (see *Chapter IV*). Thus, both arcs observed on the spectra were associated to the Pt-CGO electrode. Compared to thicker ceria-based porous films reported in [7], the here-obtained Nyquist plot for thinner porous CGO suggests a different behaviour. As already mentioned, thicker films were unfortunately not supported by the micro

[1] Similarly to which is done in *Chapter IV*, constant phase elements were used here instead of just capacitances (see *section IV.3.2*).

SOFC configuration due to delamination of the anode/electrolyte bi-layer from the silicon-based substrate (see previous section). Therefore, it was not possible to directly extrapolate Jung's film characteristics to our system for obtaining MIEC behaviour on the porous CGO and thus improving anode performance. Instead, contrary to the typical MIEC behaviour (controlled by non-charge transfer processes according to the ALS model), we report here a double arc response. The first arc, appeared at high frequencies, presents a capacitance of $C_{HF} = 10^{-9}\ F/cm^2$, while the second arc observed at lower frequencies has a capacitance two orders of magnitude lower ($C_{LF} = 10^{-7}\ F/cm^2$). These capacitances are kept almost constant with temperature.

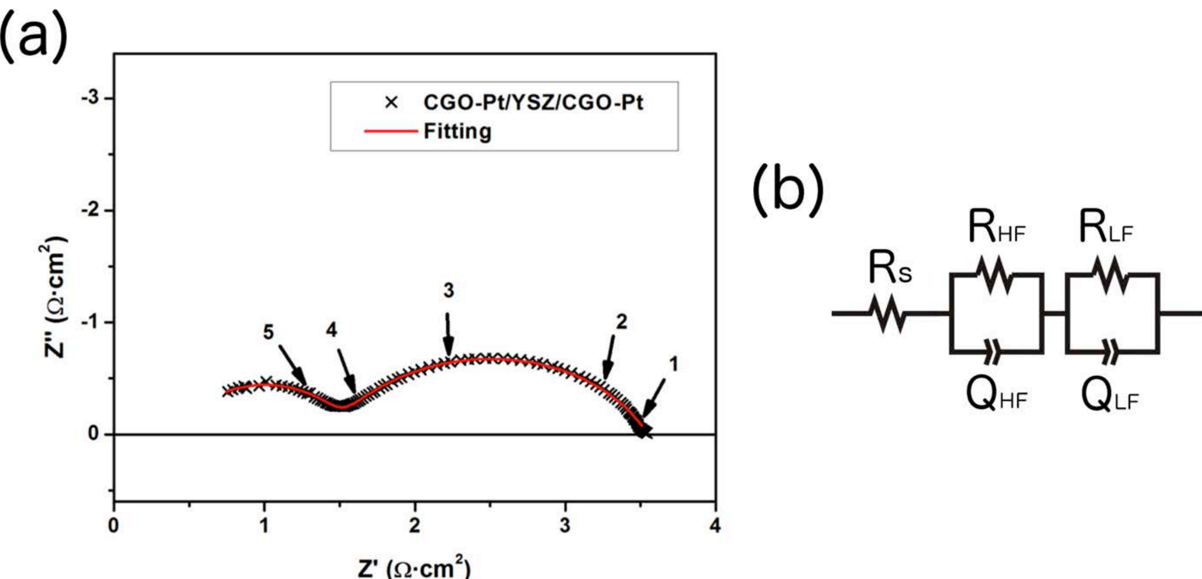

Figure VI-7. *(a) Impedance spectra of a symmetrical CGO-Pt/YSZ/CGO-Pt membrane, measured at T=650°C. Solid red line represents the fitting using the equivalent circuit* $-R_s - (R_{HF}Q_{LF}) - (R_{LF}Q_{LF}) -$ *depicted in (b). The numbers refer to the frequency decades covered by the EIS analysis.*

For a better understanding of impedance observations, detailed cross-sectional SEM was performed in order to check the specific microstructure all along the electrode depth. Figure VI-8 shows higher magnification cross-sectional SEM images of one of the measured CGO-Pt electrodes. As shown in the figure, the relatively closed porosity observed on the CGO film limited the penetration of the metal into the porous network, thus restricting the cermet formation only to the upper part of the electrode (close to the fuel, far from the YSZ electrolyte, marked as *(a)* in the figure). Meanwhile, the majority of the CGO film remains unfilled (zone *(b)* in the figure).

These observations were in perfect agreement with the observed electrochemical behaviour. On one side, the thin porosity and subsequent gas diffusion problems makes improbable the CGO reduction when deepening, what would explain the low CGO electronic conductivity measured and the no-MIEC behaviour. On the other side, once the MIEC behaviour is not achieved, the catalytically active area of the electrode would be restricted to the small part where the CGO-Pt cermet is formed (the upper part, close to the fuel and far from the YSZ electrolyte), while the rest of the CGO film would act as mere extra electrolyte. This way, the non-charge transfer phenomena (reactions) would be restricted to the upper part where the Pt-CGO cermet is formed, corresponding to the low frequency arc. On the contrary, the high frequency arc would correspond to the extra ionic resistivity associated to the rest of CGO film unfilled and/or charge transfer processes at the interface.

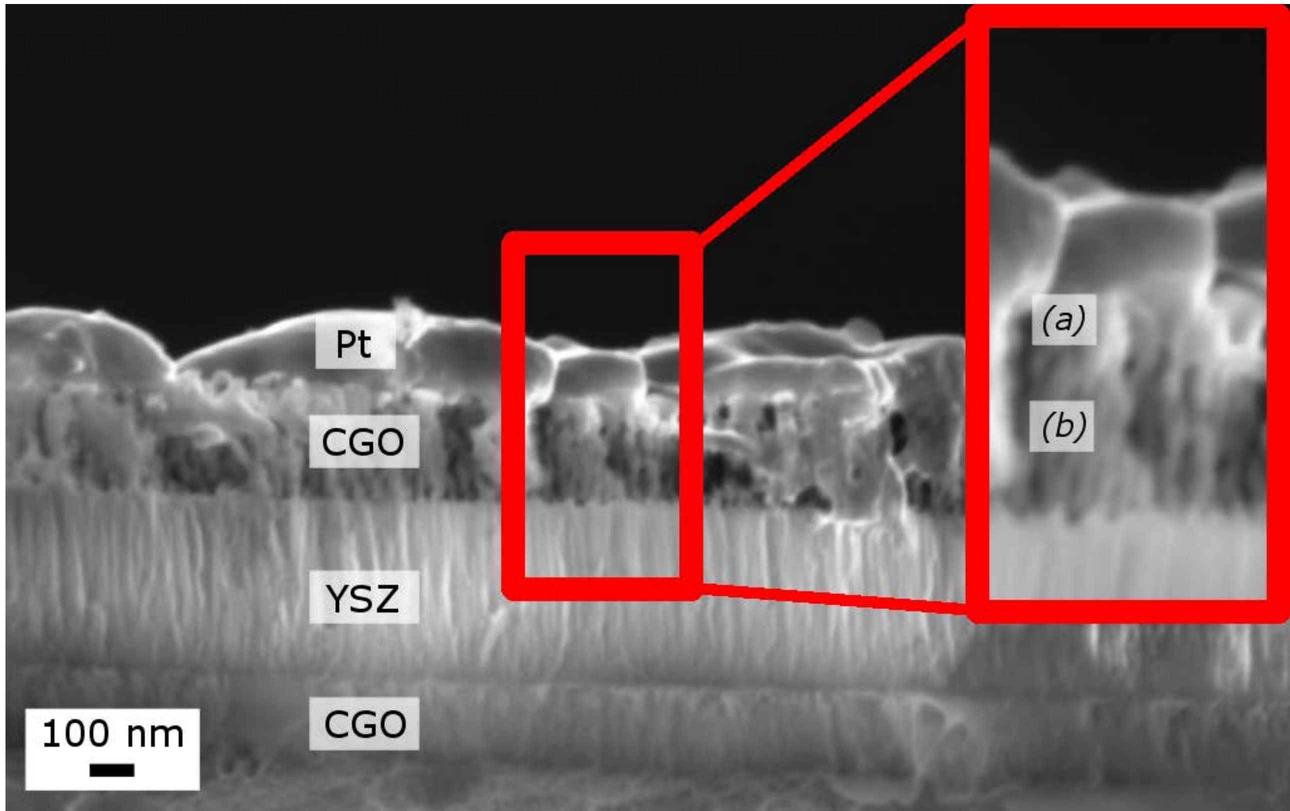

Figure VI-8. *Cross-section SEM image of a Pt-CGO/YSZ/CGO-Pt self-supported membrane. The inlet shows a magnification of the highlighted zone, for better identification of the different microstructures.*

Figure VI-9 shows Arrhenius plots of the Area Specific Resistance associated to high frequency (ASR_{HF}) and low frequency (ASR_{LF}) arcs as a function of the temperature. In both cases, the ASR dependence on temperature follows an Arrhenius-type law, with activation energies of $E_a = 0.9\ eV$ and $E_a = 1.5\ eV$, respectively. These values are again in concordance with the previously proposed explanation. Activation energies around $0.8 - 1.0\ eV$ were previously reported for oxide-ion conduction on CGO films [16] (high frequency arc in this work), while other reported thin film cermets was found to have an activation energy of $1.4 - 1.5\ eV$ [5,8] (as the one observed for the low frequency arc here).

Target value for anode/electrolyte bi-layer ASR is usually ascribed to $0.30\ \Omega cm^2$ [35]. According to this, results showed here present the fabricated CGO-Pt thin film as a suitable anode for micro SOFC application above $700°C$. Although some previous works already reported micro SOFC devices based on a Pt/YSZ/Pt configuration working at much lower temperatures ($T = 400 - 600°C$), the fast degradation observed on those pure metallic based electrodes still limits their applicability onto real devices. In this sense, the here-presented anode opens new possibilities for the fabrication of more reliable ceramic-based anodes for micro SOFC, by using thin film cermets.

However, further work is still needed for improving CGO-Pt anode and reducing the operating temperature. From the here-shown results, it is obvious that the contribution of CGO ionic conduction and charge transfer processes at the CGO/YSZ or CGO/Pt interfaces, i.e. high frequency arc on Nyquist plots, generates an extra resistance that drastically lowers the electrode performance. Therefore, further work should be devoted to reduce or even eliminate this contribution. Two main strategies appear to be suitable for optimization of the porous CGO-based anode, i.e. (i.) fabricating thinner CGO-Pt cermet films, thus eliminating the ionic resistance associated to the CGO or (ii.) further opening the porosity on the CGO film in order to promote gas diffusion and CGO reduction, thus activating it for working as a MIEC and even eliminating the need of an extra electron-conducting element.

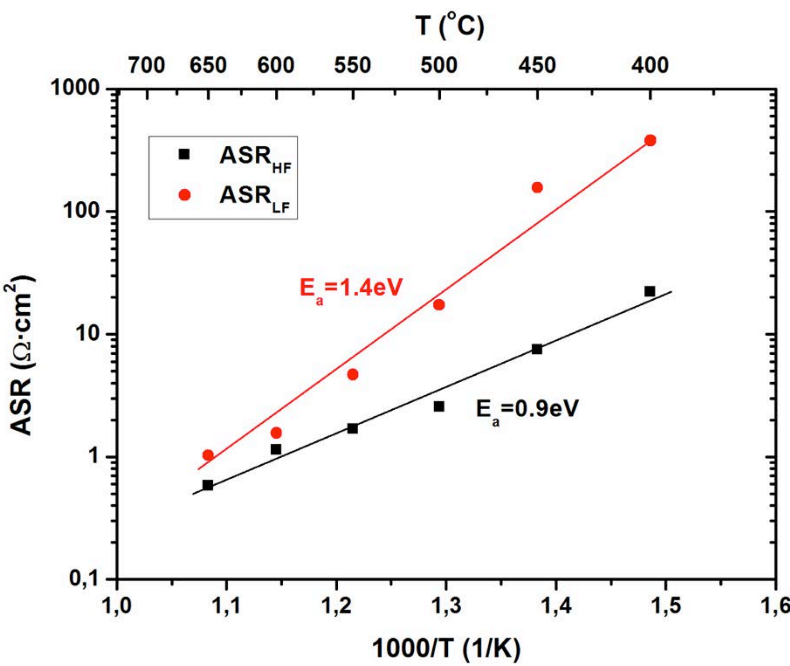

Figure VI-9. *Evolution of the ASR of both phenomena appeared on the EIS analysis of symmetrical CGO-Pt/YSZ/CGO-Pt free-standing membranes, i.e. high frequency arc (HF) and low frequency arc (LF).*

VI.4. Conclusions

Porous CGO thin films were deposited by PLD over dense YSZ thin film electrolytes for testing them as anode/electrolyte bi-layers for micro SOFC applications. Although good thermo-mechanical stability and no degradation were observed on the CGO films, very low in-plane conductivity was measured in the whole range of micro SOFC operating temperatures i.e. $400 - 700°C$ ($< 0.1\ S/cm$) under anode reducing atmospheres. An extra electronic conductor layer (porous Pt deposited by sputtering) was therefore added on top of the CGO films in order to provide the anode with sufficient in-plane conductivity. Good interconnectivity between CGO and Pt was observed by SEM, and in-plane percolation through the Pt network was ensured. However, low Pt wettability into porous CGO was observed, thus limiting the cermet formation to a few tens of nm.

Pt-CGO thin film cermets were implemented onto large-area symmetrical Pt-CGO/YSZ/CGO-Pt free-standing membranes for testing their electrochemical performance on real micro SOFC configurations. The Area Specific Resistance of the electrode was studied by cross-plane EIS characterization. Target values for SOFC anode/electrolyte bi-layers ($ASR = 0.30\ \Omega cm^2$) were reached at temperatures above $700°C$, showing the applicability of the proposed thin film cermet for anode in micro SOFC working at such temperatures. An unwanted extra resistance was found to be associated to the porous CGO not filled with the Pt, lowering the performance of the anode and restricting their applicability to high operating temperatures. Therefore, further work is proposed in order to reduce or even eliminate this associated resistance being then able to operate at lower temperatures.

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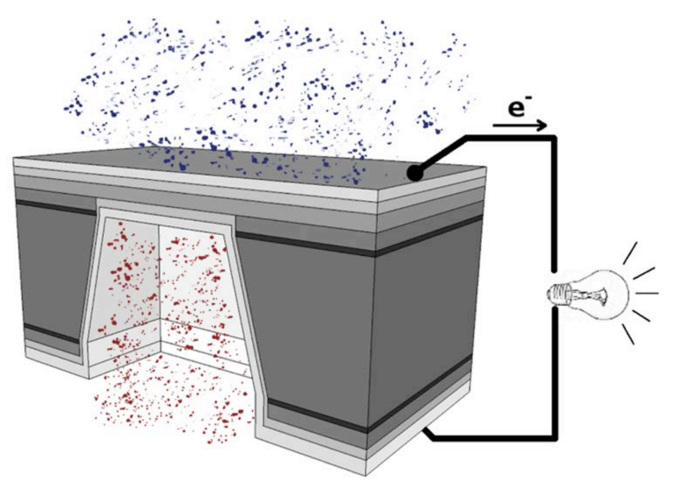
VII. FULLY CERAMIC MICRO SOFC: DEVICE PERFORMANCE



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VII.1. Current status of micro SOFC device performance

Major constrains on the commercialization of any power supply system are related to economic considerations. In this sense, the capital cost ($€/kW$) will determine whether a specific powering system will succeed or not on the real market [1,2]. Target values of $130\,€/kW$ have been recently proposed by the DOE's-SECA program for bulk SOFC stacks for stationary electricity production [3]. However, in the particular case of micro SOFC, being a portable application is commonly considered as an additional high-added value that usually moderates these cost restrictions. Additionally, the wafer-level integration presented in this work (see *Chapter II*, *Section II.3.3*) allows a batch mode fabrication (tens to hundreds of devices fabricated in parallel), strongly minimizing the fabrication costs. Therefore, the optimization of micro SOFC can be mainly focused on technical considerations. In this sense, dodging the overall fuel cell efficiency, which would also depend on the heat management, packaging and other stack designing considerations (balance of plant), the most important parameter to be enlarged on the micro SOFC development is the output power density (mW/cm^2).

In general, although high power densities ($\sim 1\,W/cm^2$) have been reported on proof-of-concept bulk SOFC devices, considerations on thermal management and fuel utilization usually restrict the maximum power density in final SOFC-based systems to several hundreds of mW/cm^2 [1]. Particularly, in micro SOFC a wide range of output power densities have been published up to now, relative to the operating temperature, materials and techniques used or membrane size. Evans et al. [4] presented in 2009 a compilation of main achievements in this sense by the different groups dealing with micro SOFC, i.e. ETH Zurich [5,6], Stanford University [7-9], EPF Laussane [10] and KIST [11]. The range of power outputs presented in that review ranged from $< 1\,mW/cm^2$ [10] to a maximum value of $861\,mW/cm^2$ (at 450°C, using corrugated membranes) [9]. Since then, main achievements prior to this work were carried out mainly by Prof. Ramanathan and co-workers at Harvard University [12-23], who published several works showing power densities up to $1037\,W/cm^2$ (at 500°C) [14]. Table VII-1 summarizes the complete series of power outputs published by the different groups, updating Evans' review from 2009 [24-30].

Although the varying set of conditions (both on fabrication and measuring) makes difficult to directly compare the different power densities published, several general conclusions can be obtained from the results compiled in the table. First, there is a clear variability on the maximum power reported, even within the same group. It is significant that promising results were firstly published followed by works showing lower performances apparently using similar fabrication conditions. For example, Prinz et al. reported power values of $270\ mW/cm^2$ in 2007, $120\ mW/cm^2$ in 2009, $520\ mW/cm^2$ in 2011 and finally $198\ mW/cm^2$ in 2012, always using the same Pt/YSZ/Pt structure. Ramanathan et al. also published power densities ranging from $\sim 30\ mW/cm^2$ (2011, 2012) to $> 1000\ mW/cm^2$ (2012), although in this case the functional materials were slightly varied for each case. Moreover, reported values from Gauckler et al. also ranged from $10\ mW/cm^2$ in 2008 to $> 150\ mW/cm^2$ (2008, 2012). This wide range of published power densities shows the difficulties faced by the different research groups to obtain reproducible values. According to the literature, the principal cause appears to be related with the low stability and fast degradation of the widespread thin film metallic electrodes at micro SOFC working temperatures (reported by [31-34] and also observed in this work, see *Appendix B*). However, although fast degradation has been reported on metallic thin film over bulky substrates already at micro SOFC working temperatures, no deep investigation on its effect on micro SOFC device performance along time has been

Group	Pub. year	Anode (dep. tech.)	Electrolyte (dep. tech.)	Cathode (dep. tech.)	PEN total thickness (nm)	Max active area (mm^2)	OCV (V)	Power output ($mW cm^{-2}$)	T (°C)	Power stability	Ref.
Stanford Univ. (Prinz et al.)	2007	Pt (sp) Pt (sp)	YSZ (sp) YSZ/GDC (sp)	Pt (sp) Pt (sp)	80 + 50 + 80 80 + 100 + 80	0.01 0.01	1.05 1.10	130 200	350°C 350°C	-	[7]
	2007	Pt (sp)	YSZ (ALD)	Pt (sp)	80 + 60 + 80	0.01	1.10	270	350°C	-	[8]
	2008	Pt (sp)	YSZ (ALD)	Pt (sp)	120 + 70 + 120	0.01 *	1.09	861 *	450°C	-	[9]
	2009	Pt (sp) Pt (sp)	BYZ (ALD) BYZ (PLD)	Pt (sp) Pt (sp)	80 + 110 + 80 80 + 130 + 80	0.01 0.01	1.09 1.12	136 120	400°C 450°C	-	[24]
	2011	Pt (sp)	YSZ (ALD)	Pt (sp)	60 + 80 + 60	0.01 *	1.11	560 820 *	450°C	-	[26]
	2012	Pt (sp)	YSZ (ALD)	Pt (sp)	120 + 70 + 120	4 (58.9%)	1.12	198	450°C	-	[28]
ETH Zurich (Gauckler et al.)	2008	Pt (sp) Pt (sp) Pt (sp)	YSZ (PLD) YSZ (PLD) YSZ (PLD)/YSZ (s.pyr.)	Pt (sp) LSCF (s.pyr) Pt (paste)	50 + 550 + 50 50 + 550 + 200 50 + 750 + 10^4	0.03	0.77 0.55 1.06	26 10 150	500°C 500°C 550°C	-	[5]
	2012	Pt (sp)	YSZ (PLD)/YSZ (s.pyr.)	Pt (sp)	80 + 500 + 80	0.03	0.57	209	550°C	-	[29]
	2013	Pt (sp)	3YSZ (PLD)	LSC (s.pyr)	80 + 300 + 250	0.15	1.02	12	500°C	-	[30]
EPF Lausanne (Muralt et al.)	2008	Pt (sp)	YSZ (sp)	Pt (sp)	25 + 750 + 25	20 (with Ni grid)	0.28	-	400°C	-	[10]
	2010	Pt (sp)	YSZ (sp)	Pt (sp)	100 + 400 + 100	0.8 (with Ni grid)	0.85	0.02	500°C	-	[25]
Harvard Univ. (Ramanathan et al.)	2010	Pt (sp)	YSZ (sp)	LSCF (sp)	120 + 60 + 67	0.06	0.60	120	560°C	-	[13]
	2011	Pt (sp)	YSZ (sp)	Pt (sp)	80 + 100 + 80	0.03	0.97	1037	500°C	75% P_{max} after 1 h 50% P_{max} after 10 h	[14]
	2011	Pt (sp)	YSZ (sp)	BSCF (sp)	80 + 100 + 100	0.03	1.08	35	520°C	-	[15]
	2011	LSCF (sp)	YSZ (sp)	LSCF (sp)	65 + 60 + 65	0.03	0.18	0.21	500°C	-	[16]
	2011	Pt (sp)	YSZ (sp)	LSCF (sp)	30 + 54 + 47	25 (with Ni grid)	0.75	155	510°C	86% P_{max} after 1 h 50% P_{max} after 10 h	[17]
	2011	Pd (sp) Pd (sp)	YSZ (sp) YSZ (sp)	Pt (sp) Pt (sp)	50 + 100 + 70 50 + 100 + 70	0.03 0.03	1.03 0.77	145 385 (with CH_4)	400°C 550°C	-	[18]
	2011	Ru (sp)	YSZ (sp)	Pt (sp)	30 + 80 + 70	0.03	0.71	450 (with CH_4)	500°C	-	[19]
	2012	Pt (sp) Pt (sp)	YSZ-CGO (sp) YSZ/YSZ-CGO (sp)	Pt (sp) Pt (sp)	80 + 100 + 80 80 + 120 + 80	0.03 0.03	0.41 0.73	1025 930	510°C 510°C	-	[20]
	2012	Pt (sp)	ZrO_2 (sp)	Pt (sp)	55 + 50 + 55	0.03	0.91	33	450°C	-	[21]
	2012	Ru-CGO (sp)	YSZ (sp)	Pt (sp)	30 + 100 + 40	0.04	0.99	275 (with CH_4)	485°C	62% P_{max} after 3 h	[22]
	2013	Ru (sp) Ru (sp)	YSZ (sp) YSZ (sp)	Pt (sp) Pt (sp)	50 + 110 + 70 50 + 110 + 70	0.04 0.04	0.92 0.96	440 (with CH_4) 410 (with nat.gas)	500°C 500°C	-	[23]
KIST (Kwon et al.)	2011	Pt (sp) Pt on AAO (sp)	YSZ (PLD) YSZ (PLD)	Pt (sp) Pt (sp)	80 + 200 + 80 80 + 900 + 80	0.01 0.01	1.06 1.02	- 350	400°C 500°C	-	[27]

Table VII-1. *Comparison of micro SOFC systems previously reported. * Corrugated membrane; power density calculated with respect to the projected area.*

reported. Up to our knowledge, the only results on fuel cell durability for micro SOFC systems were published by Ramanathan et al. [14,17,22]. These results showed a rapid drop on the maximum power density within a few hours of operation at $T \sim 500°C$ (see Table VII-1 power stability). It is significant that no further durability tests have been performed up to now, despite the complete series of published results always use porous Pt electrodes as anode, cathode or both.

A second observation that can be extracted from the table is the wide range of reported OCVs, some of them far away from the theoretical value ($\sim 1.1\ V$) [5,10,13,16,17,20,29]. This seems to be related to sealing problems (set-up chamber) and/or leakages between anode and cathode through the electrolyte (i.e. pinholes on the membrane). Either increasing the electrolyte thickness or depositing multi-layer thin film electrolytes can minimize this problem, by reducing the probability of pinhole formation and therefore eliminating leakages [5,7].

Therefore, it looks clear that (i.) moving to more thermo-mechanically stable functional materials (at micro SOFC operating temperatures) and (ii.) ensuring better encapsulation and leakage control should be the main objectives in order to develop more reliable powering devices. In previous chapters, it has been already presented the fabrication of thermo-mechanically stable YSZ electrolyte membranes, as well as alternative ceramic-based electrodes for metal substitution. At the same time, an exhaustive study on the reduction of pinholes on the membranes was also performed (see *Appendix A*).

Now, in this last chapter of the thesis, the first results on device performance of a fully-ceramic based micro SOFC are presented. ***Section VII.2*** shows the fabrication of free-standing membranes where the three functional layers of the micro fuel cell (electrolyte, anode and cathode) are ceramic-based thin films, i.e. porous LSC as cathodes (*Chapter V*), dense YSZ as electrolyte (*Chapter IV*) and porous CGO-Pt cermet as anodes (*Chapter VI*). Thermomechanical stability of the membranes was ensured below $800°C$, thus covering the range of temperatures needed for reaching good electrode/electrolyte performance on the ceramic-based films. After adding the needed current collectors (patterned dense Pt films) on both sides of the membranes, the obtained power density was measured as a function of the temperature (see ***Section VII.3***). Power output values in the same range of previously reported results on both micro SOFC and bulk SOFC (hundreds of mW/cm^2) were obtained at temperatures close to $750°C$.

VII.2. Fully-ceramic free-standing membranes: fabrication and microstructural characterization

Full ceramic-based free-standing membranes were fabricated by using the materials previously developed and studied as either the electrolyte, anode or cathode thin films. Dense YSZ was used as an electrolyte, porous LSC as a cathode and porous CGO-Pt as an anode. As discussed on *Chapter V*, Pt-based current collectors were also needed on top of the LSC cathode, thus the final micro SOFC structure was Pt/LSC/YSZ/CGO-Pt/Pt. Table VII-2 summarizes the main fabrication parameters used for each functional layer. The specific deposition conditions for each layer, as well as their thermomechanical and electrochemical properties i.e. ASR as a function of temperature, mechanical stability of the membranes/films were already described on their corresponding chapters.

Table VII-2. Materials and main fabrication parameters used for the fabrication of full ceramic-based micro SOFC. (*RT = room temperature)

	Material	Deposition technique	Deposition temperature	Microstructure	Film thickness
Curr. collector	Pt	Sputtering	RT *	Dense patterned	$150\ nm$
Cathode	$La_{0.6}Sr_{0.4}CoO_{3-\delta}$	PLD	100℃	Porous	$200\ nm$
Electrolyte	$(Y_2O_3)_{0.08}(ZrO_2)_{0.92}$	PLD	600℃	Dense	$300\ nm$
Anode	$Ce_{0.8}Gd_{0.2}O_{1.9-\delta}$ - Pt	PLD - sputtering	100℃ - RT	Porous	$250\ nm$

Figure VII-1 shows top view and bottom view images of one of the fabricated micro SOFC (top view by optical microscopy and bottom view by SEM). Free-standing membranes were fabricated supported on silicon substrates using the developed large-area membrane design (see *Chapter III* for further information). The tilted profile generated from the anisotropic silicon etching for releasing the functional membranes can be distinguished in the SEM view (brighter zone surrounding the membrane) on Figure VII-1 (b). The design chosen for those measurements had a membrane area of $2.50\ mm^2$ for a total active area (free-standing area, without considering the silicon slabs) of $1.90\ mm^2$. This means a 75% of (active) area utilization versus the whole membrane, and a 40% if taking into account the silicon frame needed due to the anisotropy of Si etching. Compared to previously reported micro SOFC based on basic square membrane configurations, this large-area micro SOFC means a significant increasing on area utilization, i.e. from $3-13\%$ (depending on the membrane size) up to the here-obtained 40%.

The typical buckling pattern characteristic of strong compressive stress can be observed on the top view optical image of the membrane (Figure VII-1 (a)). This pattern, beneficial for thermo-mechanical cycling, was already observed in ceramic free-standing membranes (see *Chapter IV* for the study of YSZ membranes). No change on the buckling pattern was observed before and after the ceramic-based electrodes deposition, thus the stress contribution of the porous electrodes was considered negligible compared to the stress already present on the free-standing YSZ membranes. Membranes were found to be stable under operating conditions, as no cracks appeared after thermal cycling up to 750℃.

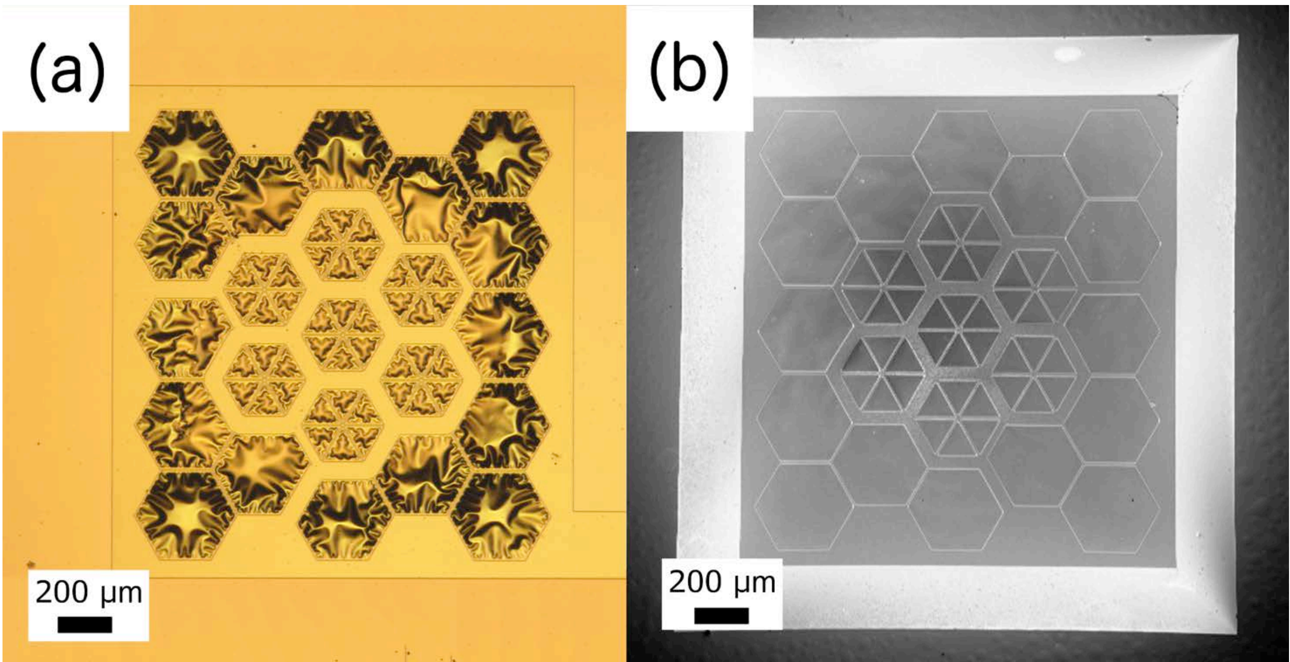

Figure VII-1. *Top view (optical image) and bottom view (SEM image) of one of the fabricated micro SOFC.*

Figure VII-2 presents a SEM cross sectional view of a fabricated free-standing fully-ceramic membrane. Pt current collectors are seen at both sides of the ceramic trilayer, either for current collection on the cathode side or also playing a catalytic role on the anode side (cermet formation). The different microstructure of each layer can be distinguished in the images. High porosity is observed on both LSC (top) and Pt-CGO (bottom) electrodes. Meanwhile, the image shows the high density and packed columnar grains of the YSZ electrolyte film between LSC and CGO films.

The resulting cathode/electrolyte/anode ceramic tri-layer had a total thickness of $\sim 750\ nm$. By adding the Pt current collectors on both sides, the thickness became $\sim 1.05\ \mu m$. Despite thinner electrolyte layers were presented in *Chapter IV*, in this final study we decided to increase the thickness of the YSZ layer to $300\ nm$. As detailed in *Chapter V*, increasing YSZ thickness to several hundreds of nm presents some advantages greatly beneficial for the reliability of the device. On $300 - 500\ nm$-thick electrolytes, a reduction of failure by pinhole formation (thicker the film, lower the probability of pinhole appearance) and an increase of thermo-mechanical stability are expected. Meanwhile, the target ASR value for the electrolyte ($ASR = 0.15\ \Omega cm^2$ [1]) is still reached at temperatures as low as $450℃$ (see *Chapter V*, *Section V.3*). Therefore, as the proven operating temperature of both anode and cathode is $\sim 700℃$ (as shown in *Chapters V* and *VI*), increasing the total thickness of the membrane does not mean a limitation (at least until reliable electrodes working at lower temperatures are developed).

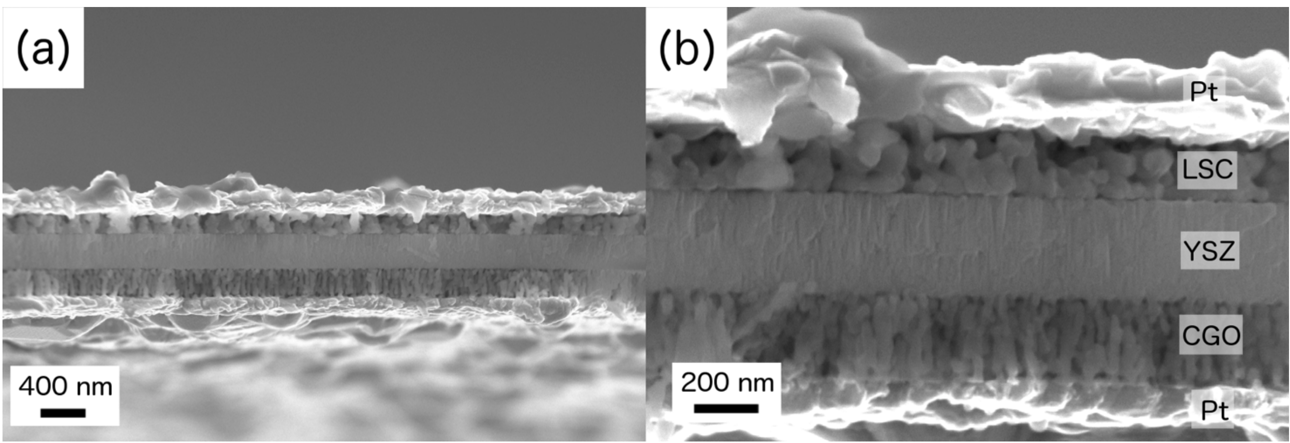

Figure VII-2. Cross-section SEM images of a Pt/LSC/YSZ/CGO-Pt/Pt free-standing membrane with different magnifications, after measuring.

VII.3. Micro SOFC device performance

In order to measure the fuel cell performance, samples were sealed to an alumina tube by using Ag O-ring heated up to $750℃$. Specific characteristics of the measuring setup were given on *Chapter II*, and images of some of the fabricated samples can be seen on Figure VII-3. The size of the silicon chips was $10x10\ mm^2$. The electrodes and current collectors were deposited only on the central part of the sample (see the grey zone -Pt- on the chip, on Figure VII-3), thus covering the membrane plus an extra zone for contacting.

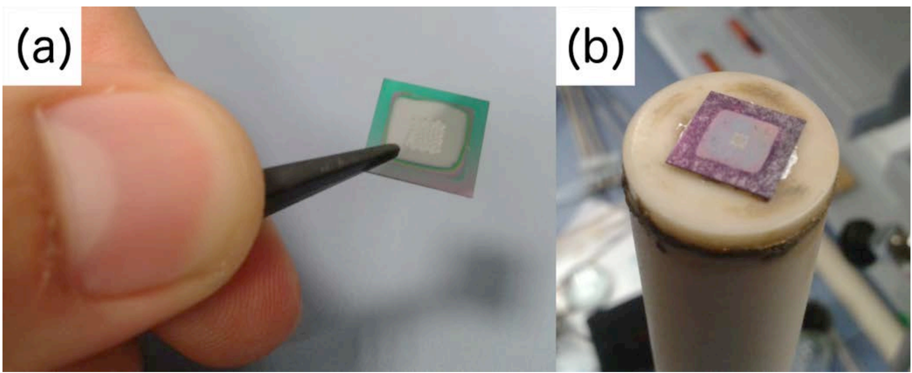

Figure VII-3. Images of micro SOFC chips, as-fabricated (a) and once sealed for electrochemical testing (b).

An OCV close to the theoretical one was obtained once sealed ($OCV = 1.05 - 1.10\ V$), using synthetic air as oxidizing atmosphere (cathode side) and pure H_2 as reducing atmosphere (anode side). These values of OCV ensured that no pinholes or cracks appeared on the membranes during heating up and sealing processes (reduced OCV values would be measured). Figure VII-4 shows IV curves obtained for one of the measured Pt/LSC/YSZ/CGO-Pt/Pt free-standing membranes at different temperatures, up to 800°C. Measurements below 700°C showed insufficient performance (no electrode activation), and tests at higher temperatures ($T \geq 800$°C) yielded to membrane failure (thermo-mechanical limits were presented in *Chapter IV*). The power output was calculated as a function of current density, showing a maximum value of $100\ mW/cm^2$ at 750°C and 65 mW/cm^2 at 700°C.

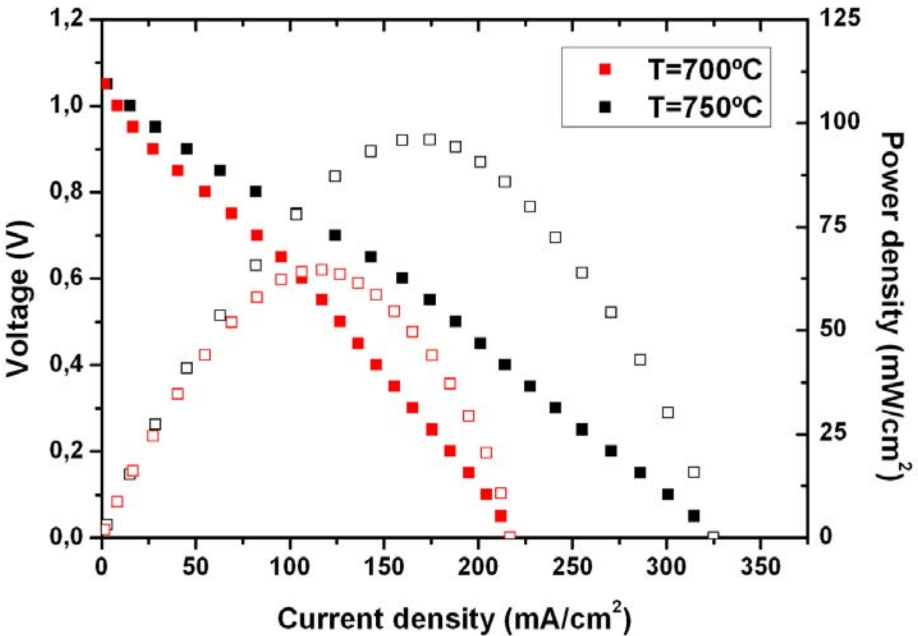

Figure VII-4. IV curve and power density output obtained from a Pt/LSC/YSZ/CGO-Pt/Pt free-standing membranes at 700°C and 750°C.

This power output values are in the typical range for bulk SOFC and metallic-based micro SOFCs, i.e. hundreds of mW/cm^2. In addition, the total power output from a single cell was $\sim 2\ mW$ at 750°C, which is in the same range as that reported by Su et al. for Pt/YSZ/Pt corrugated membranes. Our capability of fabricating thermally stable micro SOFC at intermediate-to-high operation temperatures (up to 800°C) allowed us integrating ceramic electrodes on both sides of the electrolyte membrane for the first time.

Therefore, these are the first reported results on full ceramic-based micro SOFC. The implementation of these ceramic electrodes opens a new insight for the development of more reliable micro SOFC devices, due to the well-known stability of ceramic nanostructures at high operating temperature[1]. As an example, Figure VII-5 shows top view SEM images of the here-fabricated electrodes after operation, compared to one of the traditional metallic electrodes tested on Pt/YSZ/Pt micro SOFC configurations. As can be observed, the ceramic nanostructure remains stable (porous but continuous layer) with temperature while the Pt drastically agglomerates from starting dense layers (room temperature) into isolated particles after annealing, thus loosing the electrode performance (breakdown of in-plane percolation).

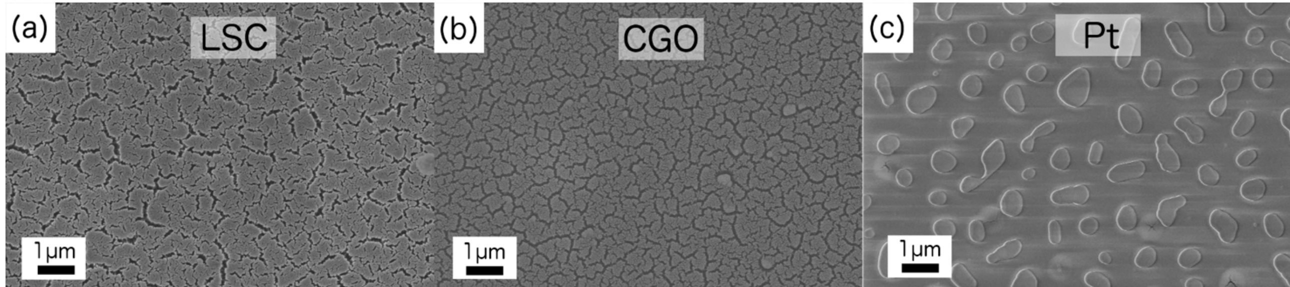

Figure VII-5. Top view SEM images of the different electrodes fabricated in this work after thermal treatment.

EIS experiments were complementary carried out on the measured membranes in order to evaluate the associated resistance to each component of the micro SOFC. Figure VII-6 shows a Nyquist plot corresponding to a Pt/LSC/YSZ/CGO-Pt/Pt free-standing membrane at 750°C under high power output (voltage offset $0.7\ V$). Two separated arcs can be clearly identified in the plot. Given a semi-circular shape of both arcs, we associated this response to that expected from a parallel resistor-capacitor (RQ) circuit. In this work, a more general constant phase element Q was used instead of just a capacitor C (see *Chapter IV*, *Section IV.3.2* for further information). Therefore, the Nyquist plot was fitted by using the following equivalent circuit:

$$LR_s(R_{HF}Q_{HF})(R_{LF}Q_{LF}) \qquad \textit{(VII.1)}$$

where L is an inductance typically ascribed to the measuring equipment, R_s a resistance in series already shown at the highest frequencies and $(R_{HF}Q_{HF})$ and $(R_{LF}Q_{LF})$ the in-parallel resistor-capacitor elements associated to the two arcs (high frequency and low frequency arcs, respectively).

A resistance in series $R_s < 10\ \Omega$ was measured (see a zoom of the highest frequencies on the Nyquist pots on the inlet of Figure VII-6). This R_s encompasses the resistances associated to (i.) the YSZ electrolyte (R_{YSZ}), (ii.) the Pt current collectors (R_{cc}) and (iii.) the cables and contacting, inherent on any measuring set up (R_{cables}). However, according to previous studies (*Chapter IV*), a $300\ nm$-thick YSZ film at $T > 700$°C presents a R_{YSZ} of $\sim 10^{-6}\ \Omega\text{cm}^2$. Therefore, contribution of YSZ is expected to be negligible and R_s would only correspond to the sum of R_{cc} and R_{cables}.

The two arcs observed in the plot were associated to the two electrodes of the micro SOFC. Both high frequency and low frequency phenomena present resistance values in the same order of magnitude

[1] It is important to notice here that although current collectors are also based on metals, the specific characteristics of those films compared to electrodes (dense and thicker films for current collectors, versus thin and porous films for electrodes) make them thermally stable under operating conditions (see *Chapter III, section III.2.3*).

($\sim 2\ \Omega cm^2$), while their associated capacitances clearly differs, i.e. $C_{HF} = 10^{-6}\ F/cm^2$, $C_{LF} = 10^{-3}\ F/cm^2$ (true capacitance were calculated from Q as explained on *Chapter IV, section IV.3.2* and according to [35]). First, the capacitance associated to the high frequency arc (C_{HF}) is in concordance with previously measured capacitance on symmetrical cells for the anode (see *Chapter VI*), therefore this first arc was associated to the non-charge transfer phenomena on the Pt-CGO cermet. It is important to notice here that, opposite to shown in *Chapter VI*, working at such high operating temperatures ($T = 750°C$) we do not expect (neither observed) an extra arc associated to CGO ionic resistivity.

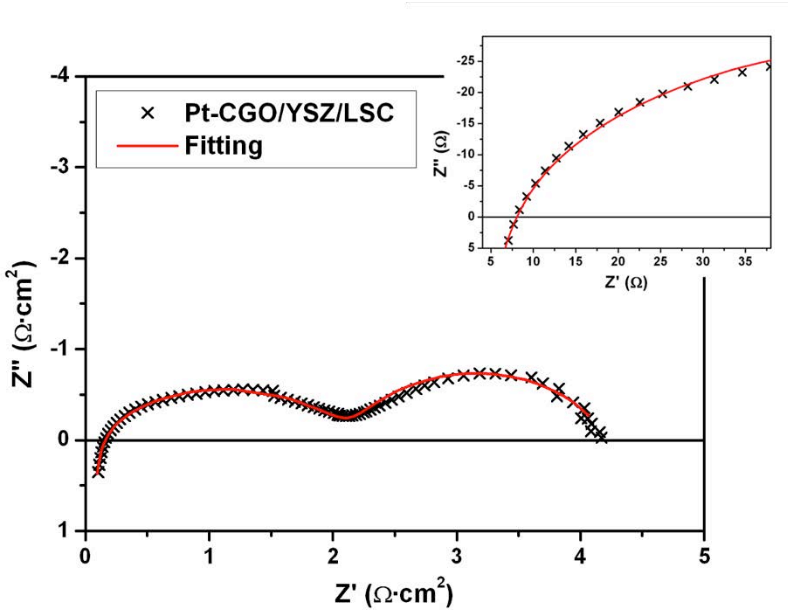

Figure VII-6. Nyquist plots of a Pt/LSC/YSZ/CGO-Pt/Pt free-standing membrane at different temperatures and two different voltage offsets, OCV and $V = 0.7\ V$. The inlet shows a zoom of the high frequency part of the plots.

On the other side, the exceptionally high capacitance observed on the low frequency arc (C_{LF}) is consistent with the concept of a chemical capacitance reported for MIEC electrodes [36-38]. Therefore, this arc corresponds to the LSC cathode that, as shown in *Chapter V* (*Section V.3*), presented such behavior on symmetrical cells. Although here effectively fitted by a resistance-capacitance circuit, in order to confirm the agreement with previous studies of LSC thin film cathodes on symmetrical cells, an additional fitting using the ALS model (similar to *Chapter V*) was performed for the low frequency arc. Figure VII-7 shows a zoom of the low frequency part of previous Nyquist plot with the new ALS fitting, where the match between experimental and fitted values can be observed. Moreover, similar values of resistance and capacitance were calculated from both fittings. A good fitting of experimental data from both approaches suggests that only the first layers of the MIEC are electrochemically active [39].

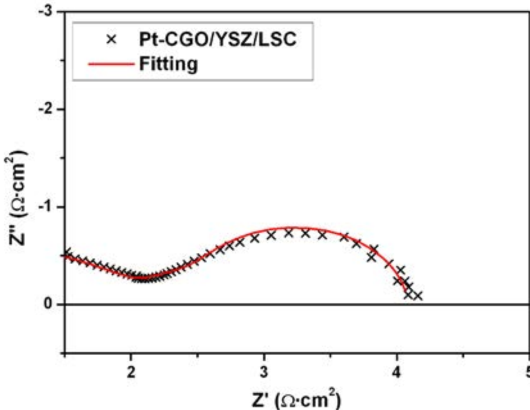

Figure VII-7. Zoom of *Figure VII-6 showing* the low frequency part of the spectra. The fitting was performed by using the ALS model.

Finally, on Table VII-3 it has been summarized the ASR values calculated for each functional layer of the micro SOFC. As already pointed out, electrolyte and current collectors appeared summed on R_s (together with wiring and contacting resistances) and are negligible in comparison with the total resistance of the micro SOFC. Main source of resistance losses are therefore associated to the thin film ceramic electrodes. First, it is important to underline that both anode and cathode present similar values of R. None of them appears as a limiting element at such temperatures, but both contributes similarly to the total resistance. However, the higher activation energy measured on the cathode ($E_a(LSC) = 1.6\ eV$ versus $E_a(Pt - CGO) = 1.4\ eV$, see *Chapters V* and *VI*) indicates that a higher contribution from the cathode is expected if lowering the temperature. Second, it is clear from the obtained values that both electrodes present higher resistances than those expected for efficient fuel cell performance (target values of ASR are usually ascribed to be $0.15\Omega cm^2$ for each functional layer [1]).

Table VII-3. ASR values calculated for each artifact appeared on the Nyquist plot. *c.c.: current collectors

	BIAS: $0.7V$	
	ASR ($\Omega \cdot cm^2$)	C (F/cm^2)
Anode	1.5	$1 \cdot 10^{-6}$
Cathode	2.0	$3 \cdot 10^{-3}$
Electrolyte + c.c.*	< 0.02	-

In this sense, this new generation of ceramic-based micro SOFC opens new challenges in electrode and device optimization. Nevertheless, further work should be focused on reducing the overall electrode ASR (for both anode and cathode) while still keeping the device operating in the IT range of temperatures (≤ 750°C), or even lowering it. As it has been shown, the electrolyte can work at much lower temperatures ($400 - 450$°C), thus there is a wide range of temperatures in which the electrodes can be optimized. This way, the optimization of the device should go mainly through improvement of cathode performance and anode microstructure, in order to (i.) increase the total power density and/or (ii.) reduce the operating temperature.

VII.4. Conclusions

A full ceramic-based micro SOFC is presented here for the first time. Large-area free-standing membranes were fabricated using porous LSC thin films as cathode, dense YSZ as electrolyte and Pt-CGO cermet as anode. Dense Pt networks were implemented on both sides of the membrane for current collection. The thermo-mechanical stability of the membrane was proved up to 750℃ extending the up-to-now reported operating temperatures of micro SOFC (< 550℃).

Measurements of fuel cell performance were carried out at $700℃ - 750℃$. A maximum power density of $100\ mW/cm^2$ was measured at 750℃ under pure H_2 as fuel and synthetic air as oxidant. The obtained values were in the range of other previously reported power densities for metallic-based micro SOFC and bulk SOFC systems working in the IT range. Similar resistance contributions from the anode and cathode films were measured by EIS, with still higher ASR values than those targeted for SOFC functional electrodes. Further optimization of the ceramic electrodes is still needed, particularly the cathode if reducing operating temperature. Nevertheless, the proven stability of ceramics under such range of temperatures compared to the low reproducibility and fast degradation of metal-based systems make the here-presented system the first report of a second generation more reliable full ceramic-based micro SOFC.

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CONCLUSIONS

"I do not think there is any thrill that can go through the human heart like that felt by the scientist as he sees some creation of the brain unfolding to success"

(Nikola Tesla)

The present work was devoted to the development of micro solid oxide fuel cells (micro SOFC) integrated on silicon. Three key aspects were addressed for the optimization of micro SOFC complementarily to the current state-of-the-art; (i.) new designing strategies for large-area free-standing membrane-based micro SOFCs, (ii.) fabrication of thermo-mechanically stable functional electrolytes and (iii.) implementation of more effective and durable thin film electrode materials. In the end, a full ceramic-based micro SOFC was presented for the first time as a second generation of more reliable micro SOFC systems. Edited highlights of all these aspects are listed and detailed below:

- **Micro SOFC design optimization**: Two different membrane configurations were fabricated for their use on micro SOFC systems supported on silicon substrates.

  - A basic micro SOFC configuration was first developed, based on ***squared free-standing membranes***. Window areas from $50x50$ to $820x820\ \mu m^2$ were fabricated using this basic design. Thanks to the use of silicon microfabrication technology, a high reproducibility on the fabrication of functional membranes was attained.
    Compatibility between fabrication of these silicon-based micro-platforms and deposition of nanostructured thin films of the state-of-the-art material in micro SOFC was ensured. **Functional cathode/electrolyte/anode membranes** were satisfactorily fabricated using YSZ as electrolyte material and either metals or complex oxides as electrodes.

  - A new ***large-area membrane*** design was developed here for the first time. The main objective was fabricating membrane-based micro SOFC with increased active area, thus being able to reach higher total power per single device. Free-standing membranes of the functional materials were fabricated with an increment on the total free-standing area of $\sim 30x$ compared to the basic membrane design (up to **$8\ mm^2$ of total free-standing active area**).
    The design was based on the use of a silicon slabs grid as support for the larger membranes. Being able to completely integrate the silicon grid fabrication on the microfabrication flow of the micro SOFC, this strategy represented a completely new approach for the fabrication of optimized functional membranes with larger active area. Additionally, the use of the slabs for further functions i.e. current collection and micro heater integration was addressed.

- **Thermo-mechanically stable functional membranes**: The electrolyte is considered the most critical element for obtaining functional devices, as it has to fulfil several requirements such as being gas tight, having no defect or presenting enough ionic conductivity. Therefore, an extensive study of the thermo-mechanical stability of YSZ electrolyte membranes was performed in this work.

  - An evaluation of residual stresses in as-fabricated and post-annealed (up to micro SOFC working temperatures) YSZ membranes was carried out. Different stress regimes were found when varying the film deposition temperatures, depending on the dominant residual stress mechanism. After annealing, a stress evolution towards more tensile stresses was found.
    A technological window for fabricating **YSZ free-standing electrolyte membranes thermo-mechanically stable** was opened by using PLD as deposition technique, deposition temperatures ranging from $T_s = 400°C$ to $T_s = 700°C$ and post-deposited annealing temperatures as high as $700°C$. The high deposition temperature on PLD was identified as the critical point for thermo-mechanically stabilizing the membranes.

  - YSZ membranes electrochemical functionality for micro SOFC electrolytes was proved by in-plane and cross-plane conductivity measurements. Important to notice here is that cross-plane measurements on free-standing membranes were performed here for the first time, obtaining values of conductivity one order of magnitude higher than the in-plane measurements and slightly higher than bulk YSZ. **Target values of ASR required for electrolytes** in SOFC applications ($ASR =$

$0.15\,\Omega cm^2$) were achieved in the **low temperature regime** ($T = 400$℃ for $250\,nm$ thick membranes) opening new perspectives for micro SOFCs based on silicon platforms.

- **New thin film electrode materials implemented in micro SOFC**: Opposed to the state-of-the-art electrodes widely used in micro SOFC, i.e. thermally instable porous metal thin films, this work presents the fabrication of ceramic-based cathode and anode thin films and their implementation onto membrane-based micro SOFC systems.

    - Highly **porous LSC thin films** (up to 33% in-plane porosity) were deposited by PLD over dense YSZ electrolytic layers for their use as cathodes on micro SOFC. Sufficient in-plane conductivity ($200\ S/cm$, well over the typical values ascribed to SOFC cathodes) was measured on the porous LSC films at the range of temperatures of micro SOFC, and no degradation was observed up to 700℃ and for more than $60\ h$.
    The LSC porous layers were satisfactorily implemented in large-area symmetrical free-standing membranes. The thermo-mechanical stability of LSC/YSZ/LSC membranes was ensured up to 700℃. Target values of ASR required for SOFC cathode/electrolyte bi-layers ($ASR = 0.30\,\Omega cm^2$) were achieved in the intermediate range of temperatures ($T = 700$℃).

    - **Porous Pt-CGO thin film cermets** were deposited over dense YSZ thin film electrolytes for testing them as anodes for micro SOFC applications. Pt layers were added on top of PLD-deposited CGO films in order to provide the anode with sufficient in-plane conductivity. Good interconnectivity between CGO and Pt was observed by SEM, and in-plane percolation through the anode was ensured.
    Large-area symmetrical Pt-CGO/YSZ/CGO-Pt free-standing membranes for testing the anode electrochemical performance on real micro SOFC configurations were fabricated. Target values for SOFC anode/electrolyte bi-layers ($ASR = 0.30\,\Omega cm^2$) were reached at temperatures of *ca.* 700℃, showing the applicability of the proposed thin film cermet for anode in micro SOFC working at such temperatures.

    - Additionally, the fabrication of **metal-based current collectors** implementable on both sides of the micro SOFC membranes was also shown. Based on the use of a non-conventional lithography technique, i.e. nanosphere lithography, dense Pt grids thermo-mechanically stable were fabricated and tested their stability during real micro SOFC operating conditions.

As a combination of the previous partial contributions, a **full ceramic-based micro SOFC** is presented here for the first time, using porous LSC thin films as a cathode, dense YSZ as an electrolyte and Pt-CGO cermet as an anode. Dense Pt networks were implemented on both sides of the membrane for current collection. The thermo-mechanical stability of the membrane was proved till 750℃ extending the up-to-now reported operating temperatures of micro SOFC (< 550℃) and therefore **allowing the use of ceramic electrodes**. Measurements of fuel cell performance were carried out at 700℃ $- 750$℃, obtaining a maximum **power density of $\mathbf{100}\ \boldsymbol{mW/cm^2}$ at $\mathbf{750}$℃ under pure H_2** as fuel and synthetic air as oxidant. The proven stability of ceramics under such range of temperatures compared to the low reproducibility and fast degradation of metal-based systems make the here-presented system the first report of a second generation of more reliable full ceramic-based micro SOFC.

APPENDIXES

A. PINHOLE-FREE RELIABLE MEMBRANES

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A.1. Strategies for obtaining pinhole-free YSZ membranes

The appearance of pinholes on the membranes was the major problem identified in this work for the fabrication of reliable YSZ self-supported membranes. A single pinhole (less than $1\ \mu m^2$) on a membrane generates, on one side, shortcut on the system when placing the electrodes at both sides of the electrolytic membrane, and on the other side gas leakages that reduces electrochemical performance. Great efforts were placed in this work on the development of a consistent strategy for fabricating pinhole-free self-supported membranes.

A single pinhole formation mechanism was identified, i.e. a µm-sized particle acting as shadow mask during YSZ deposition by PLD. The absence of material below the particle (film growth hindered by the masking particle) generates a hole through the YSZ film when the membrane is released and the particle goes away (happening when the Si_3N_4 supporting layer is removed – see fabrication process on *Chapter III Section III.2.2*).

In this sense, two main masking particle sources were identified, namely (i.) the presence of dust over the silicon substrates prior to deposition and (ii.) the ejection of particulates from the target during the PLD process. Unfortunately, both sources are very difficult to eliminate, as first simple sample manipulation can add any dust just before the deposition, and second the ejection of particulates is an intrinsic characteristic of any PLD process. However, some strategies can be carried out in order to minimize their number.

First, for the reduction of possible dust over the substrates, an exhaustive cleaning process right before PLD deposition[1] was applied, minimizing the probability of dust particle appearance over the membranes. This cleaning process was very important because, although silicon-based substrates were fabricated on the Clean Room facilities at IMB-CNM reducing to minimum the presence of particles over them, the fact of dicing the 4" wafers coming from the Clean Room into single chips of maximum $12x12\ cm^2$ compatible with the stationary PLD sample holder introduced an important source of dust that had to be controlled. Additionally, PLD equipment was indeed out of the Clean Room, so sample manipulation since the substrates got out from Clean Room until they were placed onto the PLD chamber meant another important source of contamination.

Second, a complementary strategy was carried out in order to reduce the two particulate ejection during PLD, i.e. the use of YSZ targets with enhanced microstructural properties for the reduction of particulate ejection during the ablation. This appendix addresses the fabrication and characterization of high quality YSZ targets for PLD applications (***section A.2.1***), as well as the effect of the target used on the deposited films and membranes (***A.2.2***).

[1] Cleaning process: Diced substrates were first cleaned with piranha solution (H_2SO_4:H_2O_2 (30%vol.), 3:1) for $5\ min$, eliminating all the organic components present on the surface. Moreover, this cleaning step also helped to reduce the presence of inorganic particles due to the generated bubbling. Then, samples were cleaned consecutively on acetone, ethanol and water for $30\ s$ each just before introducing them on the deposition chamber.

A.2. Enhancing PLD target properties

A.2.1. High quality YSZ targets for PLD

It was of particular interest for this work the effect of target degradation on the increment of particulate ejection during the PLD process. This problem, very common on PLD deposited films [1], is generally associated to the ablation of rough and non-uniform target surfaces and is a typical drawback when fabricating thin films if defect-free films are needed (even more if free-standing membranes are pretended to be released afterwards).

PLD targets with enhanced micro structural properties were achieved by using two different approaches: firstly, by maximizing the tetragonal phase content on the YSZ target (as proposed by Heiroth et al., [2,3]) and secondly by reducing the grain size. The tetragonal phase was reached by three different ways, i.e. keeping the yttria content between 2.5 and $7\ mol\%$, increasing the relative density (the strain induces the tetragonal phase) and lowering the grain size below a critical value of $1\ \mu m$ [4]. On the other hand, the grain size reduction was obtained by using a rapid sintering technique, Spark Plasma Sintering (SPS), instead of Conventional Sintering (CS) – see *Chapter II*, *Section II.3.2* for further information about both techniques. In particular, partially stabilized $3\ mol\%$ YSZ (3YSZ) and fully cubic $8\ mol\%$ YSZ (8YSZ) targets were prepared by CS and SPS.

Microstructural properties of YSZ targets

Dense and homogeneous targets of 3YSZ and 8YSZ were prepared by both techniques, although SPS-fabricated targets showed slightly higher density ($98–100\%$) than the CS targets ($93\%–98\%$). X-Ray diffraction patterns depicted in Figure A-1 showed that the expected crystalline phase was obtained in all cases, i.e. tetragonal-cubic phase for 3YSZ targets (a) while pure cubic for 8YSZ targets (b), independent of the sintering method. Therefore, the sintering method did not affect the crystallographic phase formation at all.

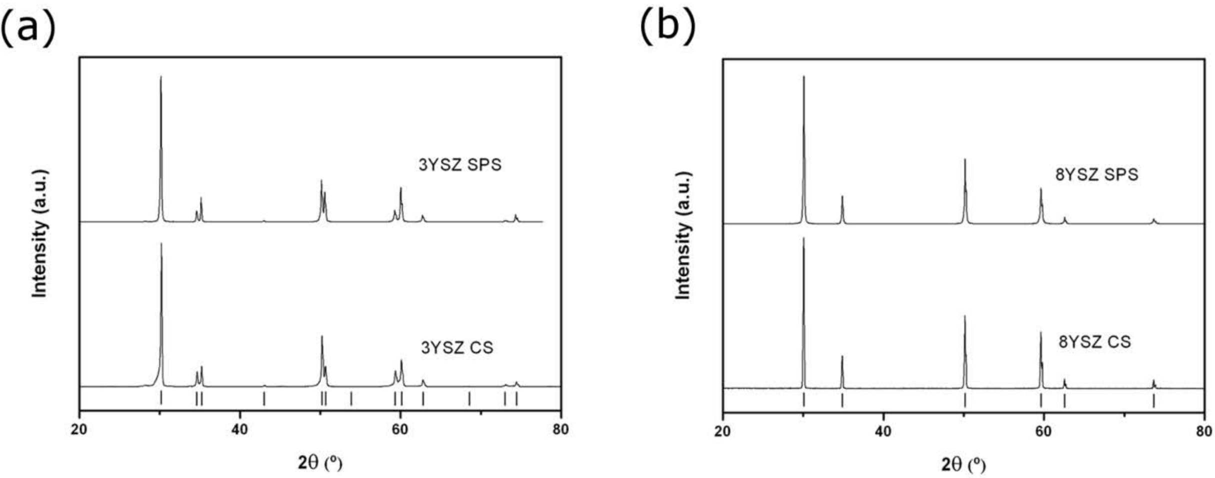

Figure A-1. *X-Ray diffraction patterns for 3YSZ (a) and 8YSZ (b) targets fabricated by CS and SPS.*

On the contrary, significant differences on the grain size and microstructure were observed between CS and SPS targets. From SEM images of Figure A-2, it could be determined that the SPS sintering method reduced the grain size for both 3YSZ and 8YSZ. The average grain sizes obtained for the four targets under study, obtained from size measurements over 1000 grains in each case, are summarized on Table A-1. As expected, using a rapid sintering technique like SPS smaller grain sizes were obtained due to a lower grain boundary diffusion and shorter grain growth time (small grain sizes were observed for both 3YSZ SPS and 8YSZ SPS). This reduction in grain size strongly improved the mechanical properties of the ceramic material since crack propagation was slowed down at the grain boundaries [5].

Unfortunately, the different nature of the raw powders employed for 3YSZ and 8YSZ, acquired from different companies (see Table A-1), did not allow absolute comparison between average grain sizes on SPS sintered targets. However, it can be seen when comparing CS targets (where re-crystallization was allowed by the long-term sintering) that the final grain size on these targets was strongly dependent on the composition: 300 nm for 3YSZ and 1050 nm for 8YSZ. This was due to the well-known slower grain growth kinetics of the tetragonal phase (mainly present in 3YSZ) compared to the monoclinic and cubic phases (up to 10 times slower) [5,6].

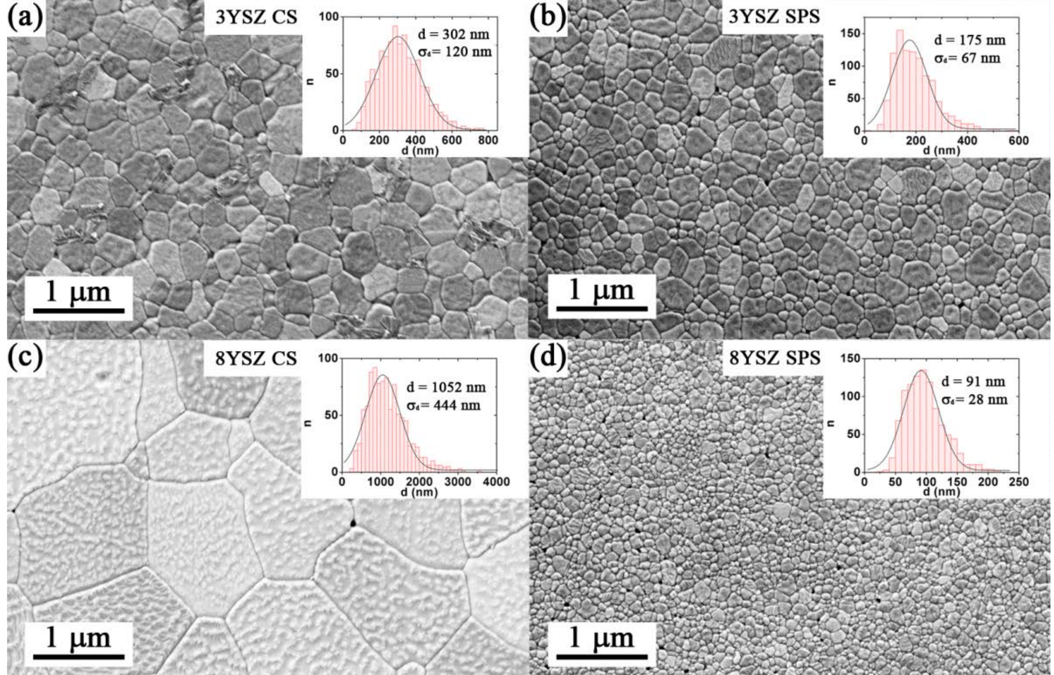

Figure A-2. Top view SEM images of different PLD targets: (a) 3YSZ CS, (b) 3 YSZ SPS, (c) 8YSZ CS and (d) 8YSZ SPS.

Table A-1. *Grain size average values for the different fabricated targets.*

	3YSZ	8YSZ
CS	**302 *nm***	**1052 *nm***
SPS	**175 *nm***	**91 *nm***
Raw powder	*NanoE (3Y-TZP)*	*Mel-Chemicals (Melox-nanosized-8Y)*

Electrochemical properties of YSZ targets

The improved mechanical properties and higher densities obtained on SPS pellets made them preferred for PLD applications. However, an electrochemical characterization was also necessary in order to evaluate their electrochemical performance too. In particular, lower performance was expected for 3YSZ compared to 8YSZ, according to literature [7].

The pellets were characterized by impedance spectroscopy using silver electrodes (painted on both sides of each pellet) in a temperature range from 150°C to 650°C. Arrhenius plots of the total conductivity for the different pellets under study are shown in Figure A-3. As expected, 8YSZ conductivity was slightly higher than that of the 3YSZ in the intermediate range of temperature, although at temperatures below 400°C both 3YSZ and 8YSZ targets presented very similar conductivity values. On the other hand, the conductivity did not change significantly when changing the sintering method, despite the different grain sizes obtained (much more significant between 8YSZs CS and SPS). Activation energies E_a calculated from the slope of each curve presented similar values than those reported for YSZ [6,7], around $1\ eV$ for the four different targets studied (see values on the inset of Figure A-3). As expected, 3YSZ activation energies were slightly lower than those of 8YSZ, as E_a increases with dopant concentration for Y_2O_3-ZrO_2 systems below 800°C [6].

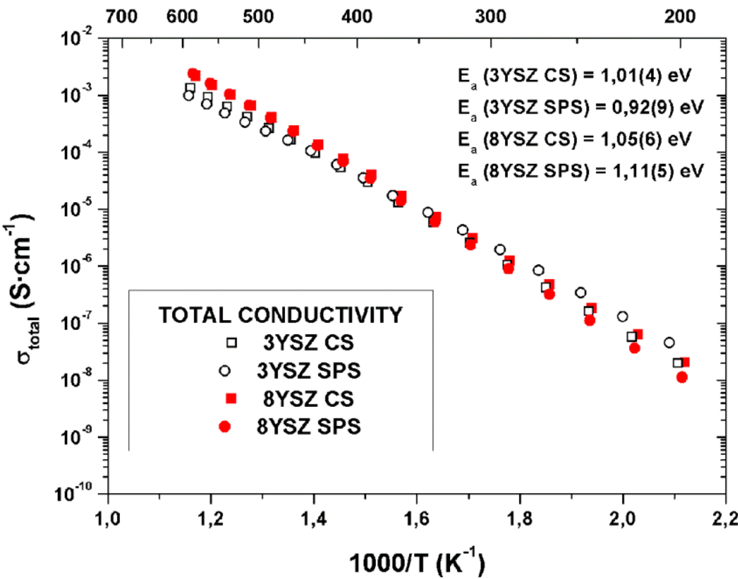

Figure A-3. Arrhenius plot of the ionic conductivity for different targets, 8YSZ and 3YSZ fabricated by CS and SPS methods.

For a better understanding of the results, the contribution of bulk and grain boundary to the total conductivity is depicted in Figure A-4 (a,b). From this figure, it is clear that the grain boundary contribution dominates the total conductivity for 3YSZ CS and SPS and 8YSZ SPS, while in the case of 8YSZ CS the bulk is the dominant. For explaining this behavior, the Brick Layer Model[2] was applied for calculating the intrinsic conductivity of the grain boundaries. Similar values were obtained in all cases, as shown in Figure A-4 (c)),

[2] Since the arcs were slightly depressed, constant phase elements instead of capacitors were used for the fitting. The true capacicances were calculated as described in *Chapter IV, section IV.3.2* and according to [8].

thus the difference observed on the contribution distributions for 8YSZ CS was presumably explained by the lower amount of grain boundary in 8YSZ CS due to the notably larger grain size (see Figure A-2).

As a conclusion, no big differences on the electrochemical performance were found between the four different targets studied. Thus, SPS targets were definitively preferred for PLD applications, according to their improved microstructural properties. Moreover, the lower bulk contribution measured is thought to be beneficial for the thin film electrochemical performance, as the number of grain boundaries across a thin film is drastically reduced due to its low thickness. Thus, close-to bulk contribution values are expected on YSZ cross-plane conductivity.

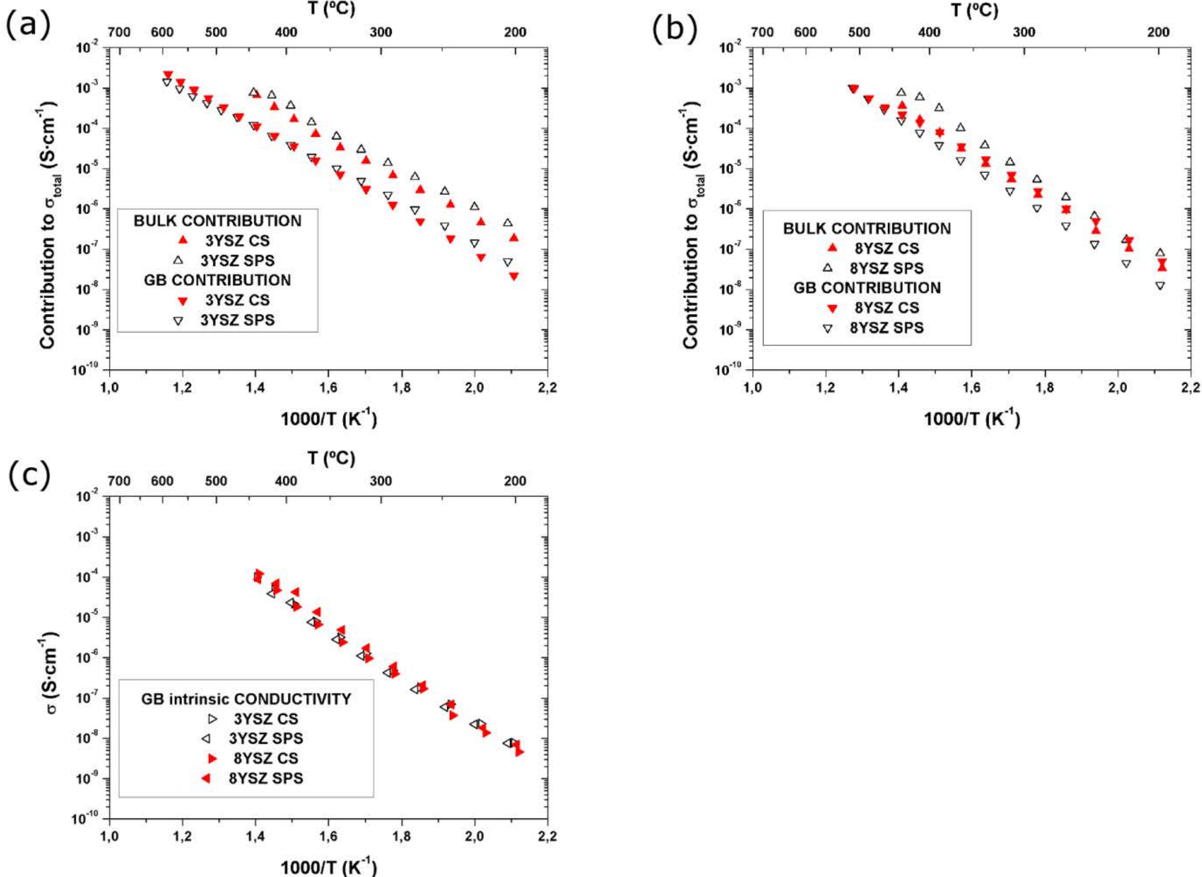

Figure A-4. Arrhenius plot of grain boundary and bulk contributions to the total conductivity for (a) 3YSZ and (b) 8YSZ targets. (c) depicts the intrinsic ionic conductivity of the grain boundaries for the four different targets.

A.2.2. The effect of PLD targets on YSZ membranes

YSZ thin film deposition with different PLD targets

Figure A-5 shows the typical XRD patterns obtained for both 8YSZ and 3YSZ films deposited by PLD using SPS targets. In both cases, the expected crystalline phases were obtained. First, a pure cubic structure was observed on the films deposited with 8YSZ SPS targets, similar to that shown in Figure IV-2 (*Chapter IV*, *Section IV.2.1*) for an 8YSZ film deposited using a CS target. On the other hand, peaks from a tetragonal *P42/nmc* (JCPDS-ICDD #78-1808) structure were obtained when moving to 3YSZ SPS. The difference

between the two structures becomes clear on XRD by the appearance of an extra peak at $43°$ on the 3YSZ films, characteristic of the tetragonal phase. No significant preferential orientation was observed.

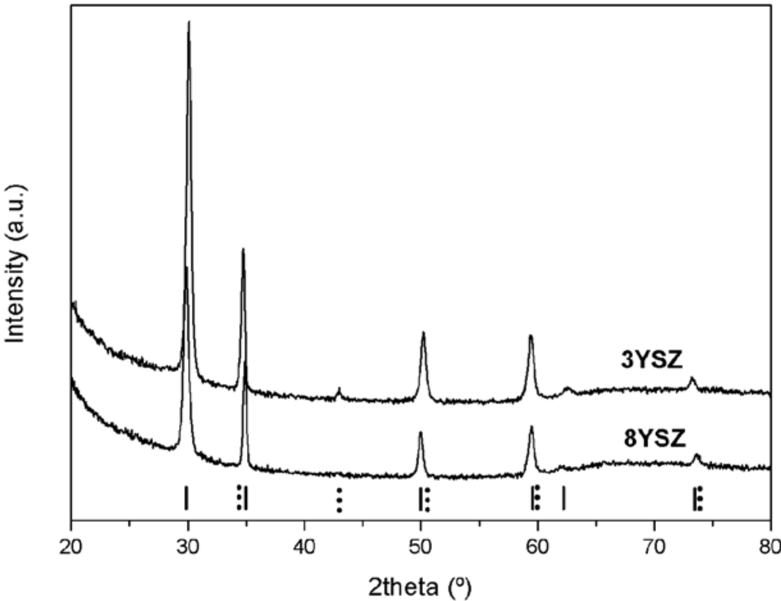

Figure A-5. X-Ray diffraction pattern for 8YSZ and 3YSZ thin films deposited by PLD using SPS targets. Solid lines mark peak positions for the cubic *Fm-3m* structure and dot lines points at extra peaks appeared on the tetragonal *P42/nmc* structure.

Moreover, reflectometry measurements prove the 8YSZ growing rate to be the same by using either CS or SPS targets ($0.15\,Å/pulse$). In the case of 3YSZ targets deposition rate was slightly lowered, estimated at $0.12\,Å/pulse$. At the same time, cross-sectional images on both 3YSZ and 8YSZ films showed similar columnar-like grain growth than that depicted on *Chapter IV* for 8YSZ CS targets grown films. Thus, no effect of the target sintering method on the film microstructure was observed.

Reduction of particulate ejection

Figure A-6 shows typical optical images of three YSZ membranes prepared by using the three different targets. Targets with similar life ablation time were used, thus surface degradation time was equivalent for all of them and the ejection of particulates could be directly compared. The number of ejected particulates per unit area and time is also listed in Table A-2, for a series of samples deposited by the different targets.

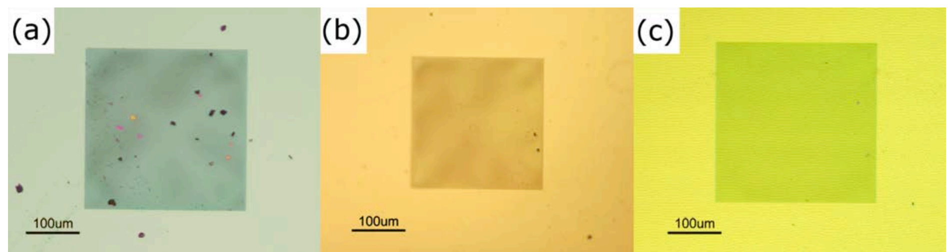

Figure A-6. Optical microscope top view images of typical free-standing membranes prepared with different PLD targets: (a) 8YSZ CS, (b) 8YSZ SPS and (c) 3YSZ SPS.

Table A-2. *Number of particulates ejected from the target to the sample during PLD deposition per unit area and standard membrane ($500x500\ \mu m^2$), for a deposition of $13000\ pulses$ ($200\ nm$ thick YSZ films). Statistics were done over 16 different PLD batches and a total area of $23\ mm^2$.*

Target material	Particulates/mm^2	$Particulates$/membrane
8YSZ CS	$41\ (\pm 19)$	$9-13$
8YSZ SPS	$7\ (\pm 5)$	$1-3$
3YSZ SPS	$3\ (\pm 2)$	$0-1$

From Figure A-6 and Table A-2, it can be concluded that the ejection of particulates from the target to the sample during the PLD deposition was drastically reduced when using SPS targets instead of CS. Moreover, the quality is even better when changing from 8YSZ to 3YSZ (this particular effect of the composition was previously reported by Heiroth et al. [2] and confirmed here). It is remarkable that almost particle-free membranes of $500\times500\ \mu m^2$ could be achieved when using 3YSZ SPS targets.

Electrochemical properties of YSZ membranes

YSZ free-standing membranes fabricated from 3YSZ and 8YSZ SPS PLD targets were tested by EIS as described on *Chapter IV* (*Section IV.3.2*). Cross-plane conductivity values for each material were calculated from the Nyquist plots and plotted in Figure A-7. The obtained values are compared to previously tested 8YSZ membranes fabricated with CS targets, and also to each target's total conductivity and references.

First of all, it is important to notice that no significant differences were observed on conductivity measurements between 3YSZ and 8YSZ membranes, although a slightly higher conductivity was observed for 8YSZ CS membranes compared to the SPS's (not significant for the final performance of the micro fuel cell, as pointed out afterwards). In addition, 3YSZ SPS membranes presented higher conductivity at lower temperatures ($< 300\ °C$) than 8YSZ, what could be important for applications as the operating temperature is reduced.

Area Specific Resistant target values ($ASR = 0.15\ \Omega cm^2$, [9]) were achieved for the membranes fabricated by SPS targets, both 3YSZ and 8YSZ, at similar temperatures than those measured on CS target-fabricated 8YSZ membranes. ASR values at 450°C are summarized on Table A-3 for < 250 nm thick free-standing membranes fabricated at $T_s = 600$°C and after $T_a = 600$°C with the different targets, in all the cases showing $< 0.15\ \Omega cm^2$ values.

Table A-3. *ASR values as a function of target material.*

	$ASR_{450°C}(\Omega \cdot cm^2)$
8YSZ CS	0.03
8YSZ SPS	0.08
3YSZ SPS	0.10

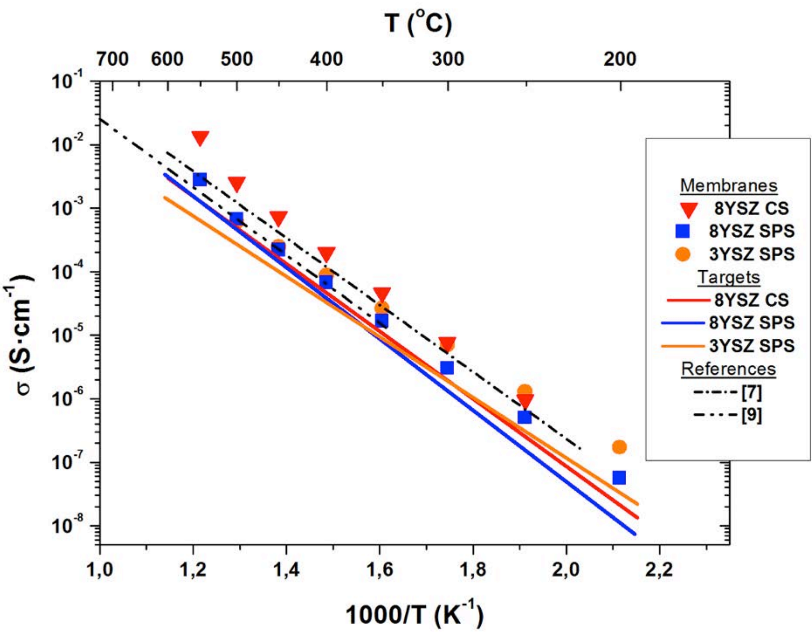

Figure A-7. Arrhenius plot of cross-plane conductivity of 200 nm thick 3YSZ and 8YSZ membranes fabricated by PLD with SPS and CS targets. Target conductivities and bulk YSZ conductivity (from Ref. [7,10]) are also included for comparison.

A.3. Conclusions

The influence of target properties on the reliability and performance of PLD-fabricated self-supported YSZ membranes for micro SOFC was studied in this work. It has been shown that improving the microstructural properties of the targets clearly reduces the number of particulates ejected from the target to the sample minimizing the probability of pinhole formation and short-circuiting of the device. The expected improvement of the mechanical properties of the PLD targets was reached by maximizing the tetragonal phase content, using partially stabilized zirconia (3YSZ) instead of fully stabilized (8YSZ), and by reducing the grain size in fully-dense targets, changing the sintering method from conventional sintering to spark plasma sintering. 3YSZ targets prepared by SPS have been proven to provide almost pinhole-free membranes.

The self-supported membranes fabricated by using 3YSZ SPS PLD targets achieve the called for value of Area Specific Resistance for a SOFC electrolyte, $ASR = 0.15\ \Omega cm^2$, at temperatures as low as 450℃. As a general result, the use of spark plasma sintering for the preparation of targets for PLD is presented as a novel approach to be considered for minimizing the dramatic problem of particulate ejection in the fabrication of other particle-sensitive microdevices.

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B. POROUS METALLIC ELECTRODES FOR MICRO SOFC: PROBLEMS AND LIMITATIONS

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B.1. The use of metal films as electrodes for micro SOFC

As shown in *Chapter VII*, most of the published works on micro SOFC performance use metallic films as electrodes (mainly thin film Pt prepared by sputtering) for either fabricating symmetrical cells (Pt as both anode and cathode [1-5]) or just for one of the electrodes (most common being the anode [6,7]). Although higher catalytic activity has been found for other metals, i.e. Ni for being used as anode in SOFC [8,9], Pt higher stability in both reducing and oxidizing atmospheres and under working conditions make it preferable for its implementation on micro SOFC. Since Pt is a pure electronic conductor, the electrochemical activity (reactions) is confined to the triple phase boundary (TPB) zone, i.e. where all the reactants (fuel/oxidant coming from gas, ions from the electrolyte, electrons from the electrode) are present [10]. Therefore, optimization of Pt-based electrodes goes through the maximization of TPB length, i.e. fabricating highly porous films, while maintaining good in-plane percolation for current collection.

By thermal dewetting, Pt films (usually deposited dense) can be microstructurally tuned in order to enlarge their TPB length while maintaining good interconnectivity and conductivity. Different degrees of porosity can be obtained as a function of deposition parameters [11], film properties (thickness) or post-treatment (annealing temperature and annealing time) [12]. However, this dewetting process implies that Pt electrodes also suffer degradation (agglomeration) over time [13]. Although more thermally stable than other metals typically considered for micro SOFC applications (Pt melting point is $T_{MP}(Pt) = 1768$℃, while for silver $T_{MP}(Ag) = 961$℃ or nickel $T_{MP}(Ni) = 1455$℃), Pt thin films still present coarsening at working temperatures in the IT range, with drastic consequences on the electrode performance [7,11,12,14]. Promoted by the temperature, the agglomeration of the metal can provoke the breakdown of in-plane percolation, or at least lower the in-plane percolation (metal dewetting into isolated particles), adding an extra (and high) associated resistance and drastically lowering the overall FC performance.

In this work, many efforts were devoted to find an effective way of fabricating reliable Pt thin film electrodes, i.e. with optimized TPB length but ensuring thermal stability. This appendix summarizes the main attempts carried out in this sense (***section B.2***). Pt was used in this work for the electrolyte characterization (see *Chapter IV*) and for current collectors fabrication (see *Chapter III, V and VI*), since (i) the use of EIS has no special needs of good electrode performance for a proper measurement of electrolyte-associated resistance and (ii) the current collection does not require of porous structures or TPB length optimization. However, thin Pt films were found to be inappropriate for their final use as electrodes on micro SOFC systems because of the degradation issues previously mentioned. Typically chosen due to their easy handling, good electronic conductivity and feasibility of microstructural tuning, ***section B.3*** points out Pt's low reproducibility as micro SOFC electrode, due to its quick degradation during working conditions, specially significant on the particular free-standing membrane configuration.

B.2. Fabrication of highly porous Pt films by sputtering

Dense Pt films were deposited by sputtering over dense YSZ thin electrolytic films on bulky Si-based substrates, following the set of deposition conditions described in *Chapter II* (*Section II.2.2*). Film thicknesses were varied from $10\,nm$ to $80\,nm$, in order to study their microstructural evolution when heated up to micro SOFC working temperatures. The evolution of film microstructure was studied for a series of samples with thicknesses of $10\,nm$, $20\,nm$, $40\,nm$ and $80\,nm$, and different annealing

treatments $T_a = 400°C$, $600°C$ and $800°C$ for 6 h. Figure B-1 shows top view SEM images of the different Pt films after each step.

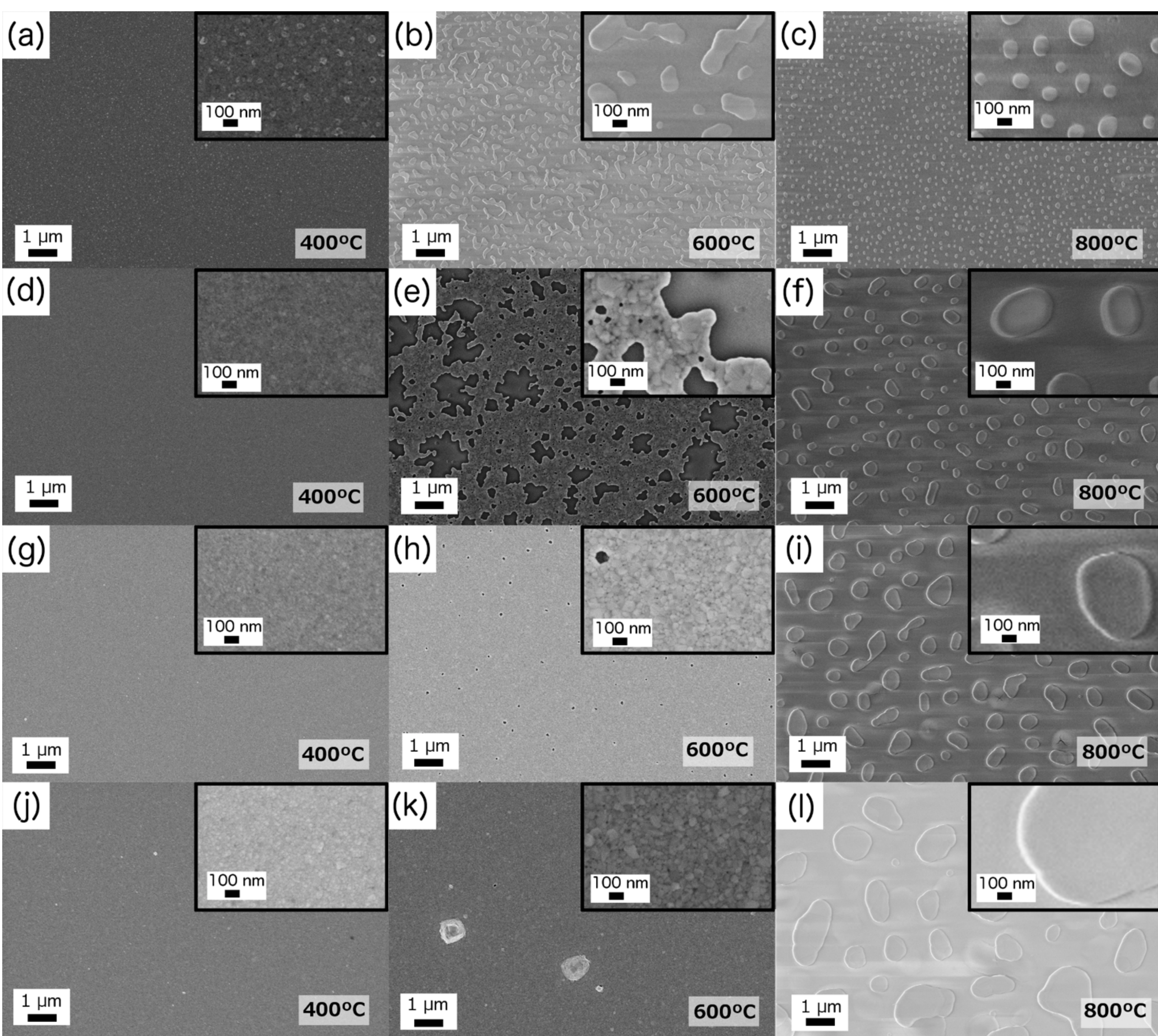

Figure B-1. *SEM top view images of Pt films with varied thickness and thermal treatments, deposited over dense YSZ thin films on Si-based substrates:* $\mathbf{10}\ \boldsymbol{nm}$ *thick (a-c),* $\mathbf{20}\ \boldsymbol{nm}$ *thick (d-f),* $\mathbf{40}\ \boldsymbol{nm}$ *thick (g-i) and* $\mathbf{80}\ \boldsymbol{nm}$ *thick (j-l). The inlets show higher magnification images of the same films, and the annealing temperature is marked for each case.*

Additionally, in-plane conductivity was measured for all the cases in order to check the in-plane percolation of the metallic thin films. By simply probing with two metallic tips on top of the Pt films, DC resistivity was measured and therefore conductivity was calculated according to the specific thickness and distance between tips. Two probe measurements were employed since it was not expected a high contact resistance between metallic tips and Pt layer. Table B-1 summarizes the conductivity for each of the films shown in previous figures. For films annealed at temperatures higher than $400°C$, the expected Pt conductivity at working temperatures, i.e. $T = 500°C$ (ASR target value for YSZ electrolyte reached at $400°C$, see *Chapter IV*), has been calculated considering the reduction of conductivity of metals as a function of temperature[1].

[1] The evolution of in-plane resistance with temperature has been assumed to follow the expression:

***Table B-1.** In-plane conductivity values of Pt thin films as a function of thickness and annealing temperature.*
** n.c. = non-conductive.*

Thickness	As-deposited	$T_a = 400°C$	$T_a = 600°C$	$T_a = 800°C$
$10\ nm$	$3.0 \cdot 10^4\ S/cm$	$3.7 \cdot 10^4\ S/cm$	*n.c.*	*n.c.*
$20\ nm$	$3.2 \cdot 10^4\ S/cm$	$4.3 \cdot 10^4\ S/cm$	RT: $4.1 \cdot 10^4\ S/cm$ 500°C: $1.3 \cdot 10^4\ S/cm$	*n.c.*
$40\ nm$	$3.8 \cdot 10^4\ S/cm$	$4.3 \cdot 10^4\ S/cm$	RT: $6.7 \cdot 10^4\ S/cm$ 500°C: $2.1 \cdot 10^4\ S/cm$	*n.c.*
$80\ nm$	$4.1 \cdot 10^4\ S/cm$	$4.7 \cdot 10^4\ S/cm$	RT: $7.1 \cdot 10^4\ S/cm$ 500°C: $2.2 \cdot 10^4\ S/cm$	*n.c.*

Several conclusions are achieved from these observations. First, it appears clear that agglomeration of Pt films is highly influenced by both the film thickness and the annealing temperature. The influence of the thickness can be clearly identified when comparing films annealed at $T_a = 600°C$ (Figure B-1 (b,e,h,k)). While thinner films either have already lost its in-plane percolation ($10\ nm$-thick film) or appear highly porous (big pores on $20\ nm$-thick film), the thicker ones remain almost fully dense (actually, very thin porosity can be observed on 40 nm and 80 nm-thick films, see inlets on Figure B-1 (h,k)). These results are in perfect agreement with previously published results by Ryll et al. [12], who also identified different types of porosity with film thickness and annealing temperatures, i.e. "microscopic" pores ($20\ nm$, $T_a = 600°C$) and "nanoscopic" pores ($80\ nm$, $T_a = 600°C$). On the other hand, the influence of the annealing temperature can be observed when comparing the $20\ nm$-thick films at different T_a (Figure B-1 (d,e,f)). By the subsequent annealing at higher temperatures, Pt agglomeration is more noticeable. While these films appeared fully dense as-deposited, after annealing at $T_a = 400°C$ local nanoscopic porosity started to appear. Then, "microscopic" pores were already present after next annealing at $T_a = 600°C$ and finally isolated Pt particles appeared after heating up to $T_a = 800°C$.

Regarding the electrical properties of the films, high in-plane conductivity was observed on Pt films $> 20\ nm$-thick under working temperatures (up to $600°C$), while a breakdown of in-plane percolation was observed after thermal treatments at $800°C$, due to the agglomeration of Pt into isolated particles. Therefore, in terms of conductivity, the use of porous Pt films ($\leq 80\ nm$-thick) is restricted to temperatures $< 800°C$. In such case, negligible resistances are expected to appear associated to the current collection (in-plane percolation through the Pt films) on $> 20\ nm$-thick films.

Another conclusion of the study was then the establishment of a maximum temperature affordable by Pt thin films ($\leq 80\ nm$) before loosing in-plane percolation. The complete set of samples prepared and heated up to $800°C$ appeared fully agglomerated into isolated metallic particles, independently of the film thickness. This could be seen on the SEM images (Figure B-1 (c,f,i,l)) where isolated particles of different sizes (thicker the film, bigger the agglomerated particle) were observed in the four cases, and was corroborated by the DC conductivity characterization, always showing null percolation.

From these results, the use of $80\ nm$-thick Pt films appeared as a promising choice for being used as micro SOFC electrode. The high "nanoscopic" porosity observed after $T_a = 600°C$ (see higher magnification

---

$$R = R[1 + a(T - T_0)]$$

where $a(Pt) = 3.92 \cdot 10^3\ °C^{-1}$.

image on Figure B-2), as well as the homogeneous microstructure observed along the sample (opposite to the thinner 40 nm-thick films, where "microscopic" pores appeared on certain zones suggesting a microstructural instability at those temperatures) and the great values of conductivity were considered ideally fitted for their use as electrodes. Therefore, these conditions were chosen for the fabrication of Pt/YSZ/Pt free-standing membranes supported on silicon-based substrates.

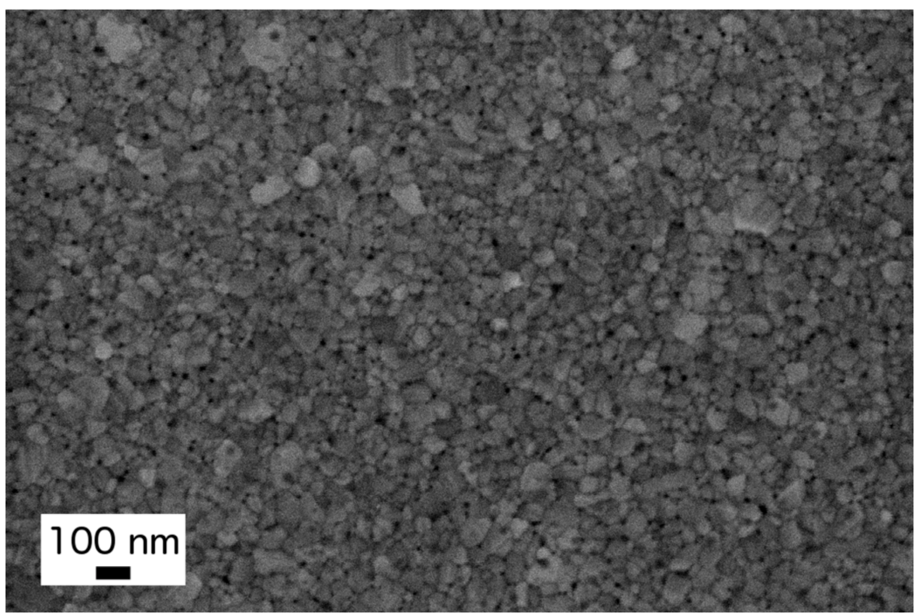

Figure B-2. *High magnification SEM top view image of a $80\ nm$ thick Pt film deposited over dense YSZ thin films on Si-based substrates, after thermal treatment at $T_a = 600°C$.*

B.3. Porous thin Pt films implemented in micro SOFCs

$80\ nm$-thick Pt films were deposited on both sides of free-standing YSZ membranes in order to fabricate symmetrical micro SOFC with Pt as both anode and cathode electrodes. Figure B-3 shows a cross-section image of a Pt/YSZ/Pt free-standing membrane fabricated in this work. The film deposition conditions and thickness were chosen according to the previous study carried out on bulk substrates, and annealing at $T_a = 600°C$ was performed prior to fuel cell test in order to provide the film with the proper porosity.

Electrochemical tests were performed under single atmosphere (EIS of symmetrical membranes for characterization of electrode ASR) and two atmospheres, one at each side of the membrane (measuring the power output and electrode degradation under working conditions). Figure B-4 shows a Nyquist plot corresponding to a Pt/YSZ/Pt membrane ($80\ nm$-thick Pt films) measured at $350°C$ and $400°C$. Two arcs can be differentiated on the figure, one corresponding to the electrolyte associated ohmic resistance (high frequency arc, only seen in the high magnification plot - inlet) and the other to the Pt electrode polarization resistance (low frequency arc, not even closed on the low magnification plot). The high resistance associated to the electrode means an unaffordable source of losses and therefore makes it unreliable for its use as electrode on micro SOFC.

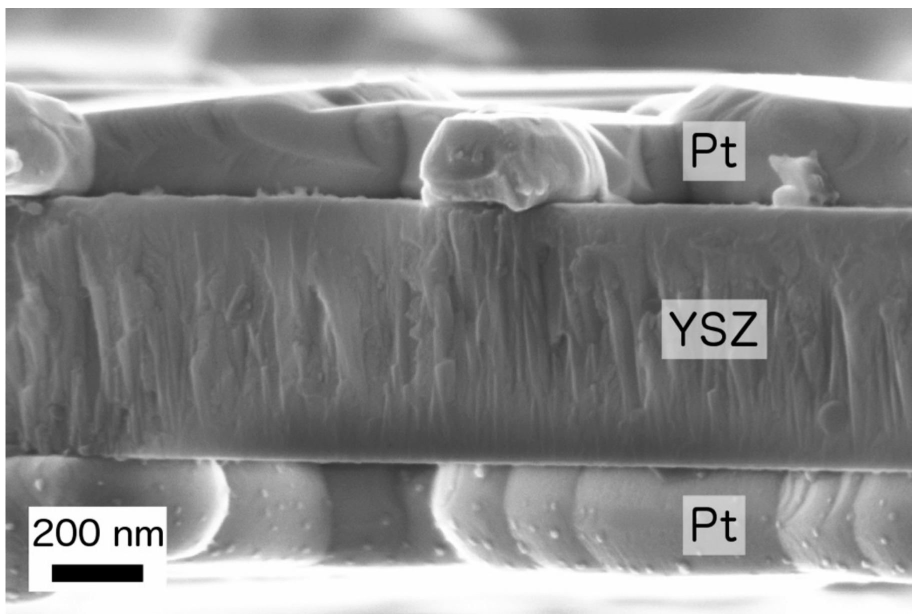

Figure B-3. *Top view and cross-section SEM view of a Pt/YSZ/Pt free-standing membrane fabricated in this work.*

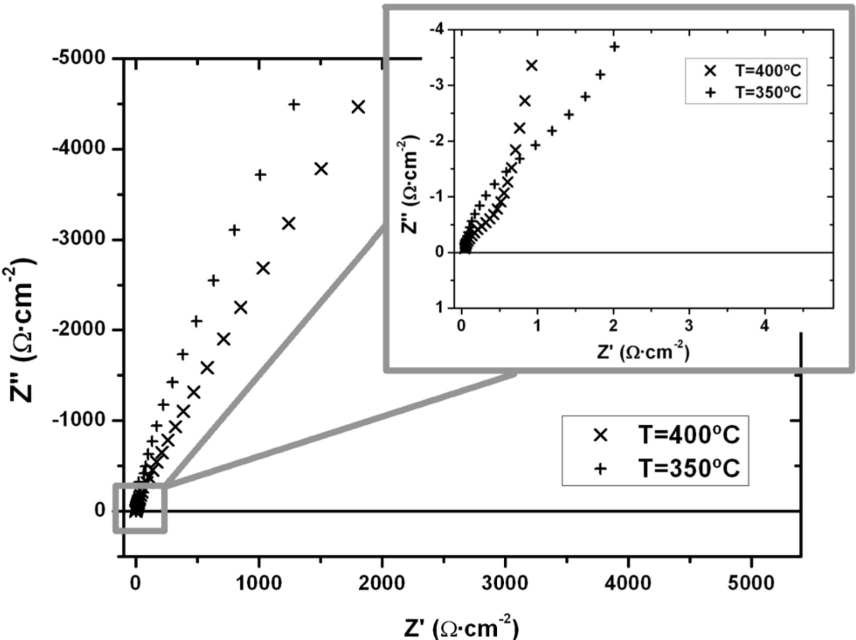

Figure B-4. *Nyquist plot corresponding to a Pt/YSZ/Pt free-standing membrane.*

This figure is only an example of the high resistances typically observed associated to the Pt electrodes. However, it was found impossible in this work to properly characterize the $ASR_{electrode}$ vs. temperature due to the instability of the measurement with time. Already at quite low temperatures such as 400℃ a fast degradation of the electrode performance (low frequency arc making bigger) was observed while measuring, even losing the electrochemical signal after a short period of time (greatly dependent on the sample). Thus, no further studies on the electrode performance variation with temperature were performed.

On the contrary, the following sections show the most important degradation phenomena observed related to the Pt thin film electrodes during operation on real micro SOFC configurations (free-standing membranes) at intermediate temperatures ($300 - 700$℃), namely:

- A *technical* problem related to bad step coverage on the back side of the membranes. In this case the specific design of the micro SOFC system and the high directionality of the sputtering deposition process difficult an effective collection of current from that side.
- A *fundamental* problem related to a drastic thermal dewetting of Pt films on micro SOFC configurations, much higher than that observed on previous studies (performed on bulky substrates). Here, two combined effects are probably accelerating the Pt dewetting, electro-migration and local drastic heating by Joule effect.

B.3.1. Bad step coverage and drastic dewetting on back side

Probably the most important and limiting problem observed in this thesis related to the Pt thin film electrodes and affecting the fuel cell performance was the bad step coverage and subsequent drastic dewetting observed on the back side of the membranes. When fabricating YSZ membranes, Si-based substrate is etched from back side in order to release free-standing YSZ films. Opposed to the anisotropic etching of Si that generates a leaned profile ($54°$, following the 111 plane, see Si wet etching on *Chapter II*), SiO_2 and Si_3N_4 etchings (wet etching with HF and Reactive Ion Etching respectively, see fabrication flow on *Chapter III*) are isotropic, thus generating almost right walls ($90°$). Therefore, trough this process an unavoidable step of $400\ nm$ (SiO_2+Si_3N_4 film thickness) is always created between the YSZ and the leaned Si substrate. Figure B-5 depicts a cross-sectional scheme of the membranes as a reminder of the specific free-standing membrane geometry and pointing out this specific step.

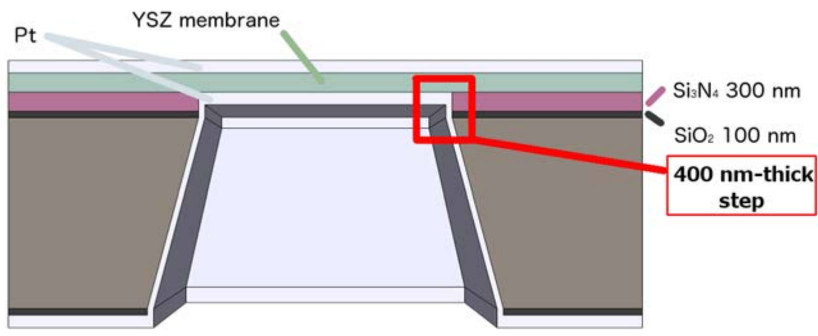

Figure B-5. *Cross-sectional scheme of a Pt/YSZ/Pt membrane*

During the fabrication (deposition) of the back-side Pt electrode, the directionality of the sputtering deposition (similar to other standard metal deposition technique like evaporation) limited the proper coverage of this $400\,nm$ step with Pt, generating a much thinner Pt film on that zone. Although as-deposited films were observed to perfectly cover it (by SEM), when heating samples up to operating temperatures (> 400℃), a drastic dewetting was observed due to the lower thickness of the film there (as shown in previous section, the thermal dewetting is highly influenced by the film thickness). Figure B-6 shows SEM images of some of the membranes after thermal treatment to operating temperatures. As shown in the images, either the Pt film on the membrane appeared completely isolated from the Pt film

covering the bulk substrate or just a few contact points barely avoided the breakdown between them, which enormously increased the associated resistance. This fatal discontinuity, occurred after thermal treatment, perfectly matches with the fast drop of electrochemical signal when measuring free-standing membranes and the impossibility of a reliable characterization of the Pt films.

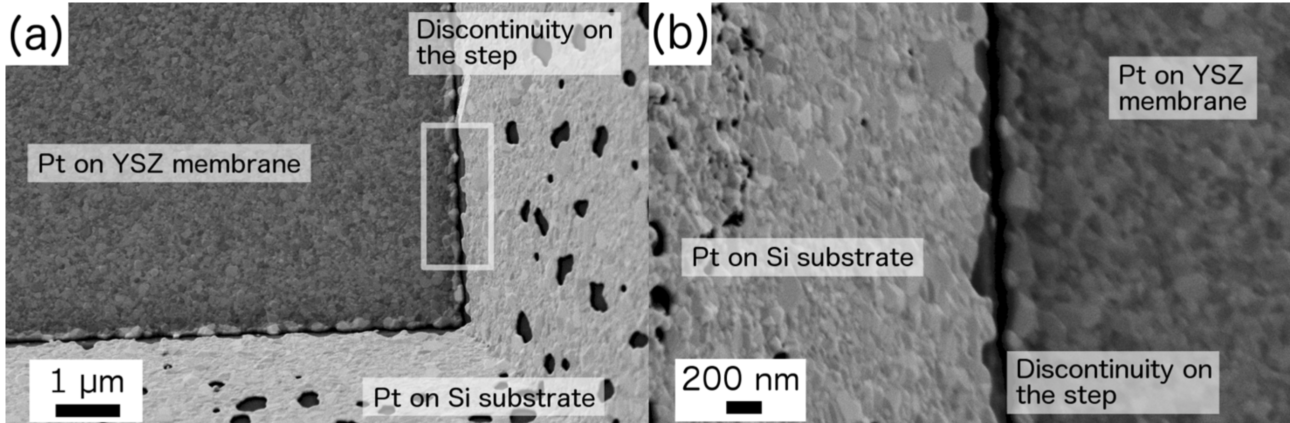

Figure B-6. *SEM images of the step generated on the back side of the membranes.*

B.3.2. Dewetting during working conditions

In addition to the "back-side problem", a faster degradation of Pt thin films was also observed when fabricating Pt/YSZ/Pt membranes after suffering working conditions (compared to that observed on films deposited over bulk substrates). Opposite to previous study on bulk substrates under single atmosphere (air), much severe film degradation was detected here yielding to a rapid loss of percolation after few hours at working temperatures (500℃) and oxidizing (air) and reducing (5%H_2-95%Ar) atmospheres at top and back sides of the membrane respectively. Figure B-7 shows top view SEM images of Pt films on Pt/YSZ/Pt free-standing membranes. The agglomeration was not only found along the $400\ nm$ step on the back side, but also on the rest of the thin film. The drastic film degradation yielded to isolated Pt particles and loss of in-plane percolation. Once the continuity was lost along the film, the electrodes became useless (no current collection).

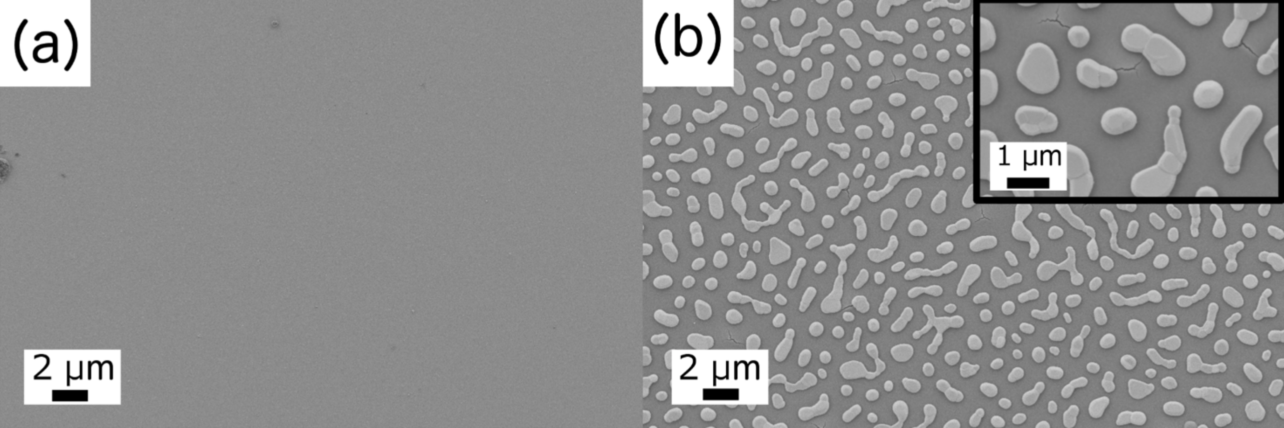

Figure B-7. *Top view SEM images of Pt films before and after measuring.*

Two possible agglomeration sources are suggested here as possible reasons of the drastic dewetting occurred under operation, (i.) the usage of too high current densities and (ii.) the influence of the reducing atmosphere to the metallic film.

First, it is known that when metallic films are heated up electrically (i.e. when applying a current density through it), two parallel effects can happen, namely annealing effects[2] and electro-migration[3] [15]. On one hand, as the structure size decreases, the practical significance of the electro-migration effect increases, due to the higher current densities generated. The typical current density at which this effect occurs in metal interconnects is $10^5 - 10^7\,A/cm^2$ [16]. On the other hand, the dissipation of Joule heating usually sets a limit on the maximum current density that can be carried in thin-film conductors to the range of $10^5 - 10^6\,A/cm^2$ before reaching the melting point of the materials [16]. This values are permitted as thin films are usually deposited on substrates such as silicon, which have good heat conductivities and provide intimate contacts. Thus, the dissipation of Joule heating generated by the electric current passing through the conductor is facilitated. However, in the present case metallic thin films are deposited over free-standing YSZ (thermal conductivity $0.02\ W/(cmK)$ [17], versus the $1.3\ W/(cmK)$ for silicon [18]), thus lowering the heat releasing capabilities of the substrate and probably minimizing the maximum current density affordable by the metallic film.

Taking into account the metallic film thicknesses used in this work ($80\ nm$), it is possible to calculate the current density J going through it as $J = I/A = I/(d \cdot t)$, being t the thickness, d the film dimensions (membrane length, i.e. $d = 0.01 - 0.35\ cm$, see *Chapter III, sections III.2.1* and *III.3.1* for the two different membrane configurations) and I the typical current applied when measuring ($\sim 1 - 10\ mA$, see Figure VII-4 in *Chapter VII*). Direct calculations reflect that J can reach values of $10^3 - 10^5\,A/cm^2$ on the fabricated Pt thin film electrodes.

Under these circumstances, the electro-migration and additional annealing effects starts to be favoured and subsequently the film agglomeration can occur. In addition, it has to be taken in to account that the annealing promotes dewetting and porosification of the film. In this sense, the more porous the film the higher the current density (for a fixed voltage), which therefore accelerates further agglomeration by electro-migration and Joule effect.

Second, it has been reported that thin film dewetting is also favoured under reducing conditions [19], due to a weaker interaction of the metals with oxidized substrates. This could accelerate the dewetting on the anode side, compared to that observed on previous analysis, where thermal treatments were always carried out under oxidizing atmospheres (ambient air).

[2] Annealing occurs by the diffusion of atoms so that a material progresses towards equilibrium. The heat increases the rate of diffusion in the material by providing the energy needed to break bonds causing the movement of atoms, which affects the grain size, grain distribution and density of dislocations.

[3] Electro-migration is caused by the gradual displacement of the metal atoms of a conductor as a result of the current flowing through that conductors. The momentum transfer between conducting electrons and diffusing metal atoms results in material transport. In thin-film conductors, electro-migration-induced damage usually appears in the form of voids and hillocks, and can be caused by inhomogeneities in microstructure, temperature and geometry. Voids can eventually grow and link together to cause electrical discontinuity.

B.4. Conclusions: moving to ceramic-based electrodes

A fast degradation of Pt thin film electrodes has been found under micro SOFC operations. Two main explanations have been found explaining the rapid loss of electrode performance of the Pt films, (i.) a bad step coverage on the back side of the free-standing membranes due to designing and technical considerations and (ii.) a drastic Pt dewetting under micro SOFC working conditions. Therefore, the direct use of porous Pt thin films as electrodes in micro SOFC has been found to be inappropriate in this work.

In this sense, it is important to notice that these problems were solved when using the more thermally stable ceramic-based electrodes proposed in previous chapters. First, the higher stability of these films with temperature with respect to Pt films has been already shown in *Chapter VII* (Figure VII-5). In this case, no electro-migration or other annealing-related effects are expected to happen. Moreover, when moving to ceramic thin film electrodes the step coverage problem was solved. Two main facts eluded the formation of this discontinuity on the ceramic films, (i.) the increased thickness of the ceramic films ($> 200\ nm$) compared to the needed for obtaining porous Pt ($80\ nm$) and (ii.) the better thermomechanical stability of the ceramic components compared to metals at micro SOFC working temperatures. As an example, Figure B-8 shows a cross-sectional SEM image of one of the steps generated on the back side of the membranes perfectly covered by a porous LSC thin film cathode deposited according to the description on *Chapter V*.

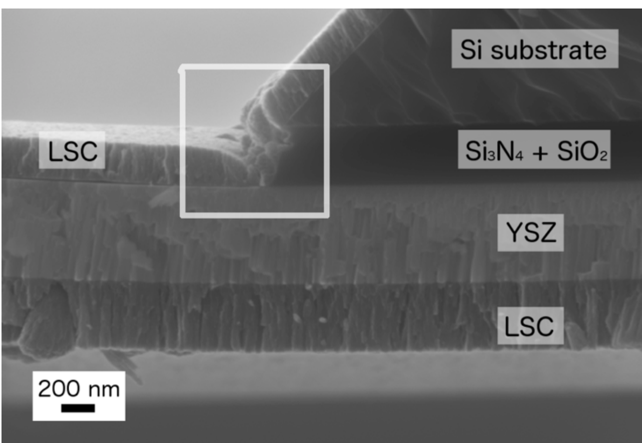

Figure B-8. *Cross-sectional SEM image of the step coverage by a porous LSC ceramic film deposited by PLD, after thermal treatment at* $700°C$*.*

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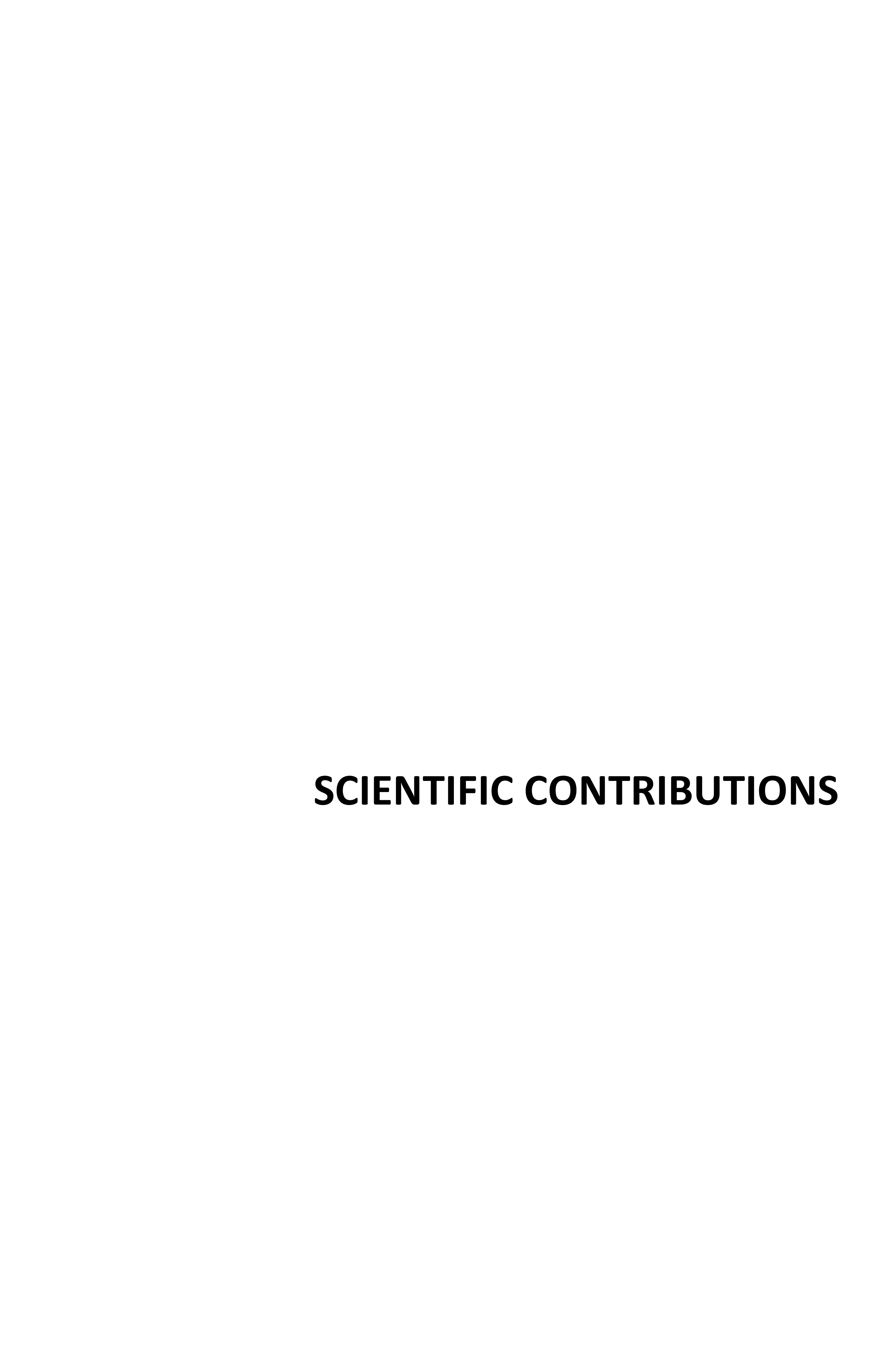

SCIENTIFIC CONTRIBUTIONS

Publications

Peer-reviewed scientific journals:

1. *"Porous $La_{0.6}Sr_{0.4}CoO_{3-\delta}$ thin film cathodes: towards more reliable all-ceramic micro solid oxide fuel cells"*; I. Garbayo, V. Esposito, S. Sanna, A. Morata, D. Pla, N. Sabaté, A. Tarancón; submitted to J. Power Sources in jun 2013 (currently under review).

2. *"Pinhole-free YSZ self-supported membranes for micro solid oxide fuel cell applications"*; I. Garbayo, G. Dezanneau, C. Bogicevic, J. Santiso, I. Gràcia, N. Sabaté, A. Tarancón; Solid State Ionics 216 (2012) 64-68.

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Patents

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3. *"A Micro Solid Oxide Fuel Cell Based Powering System as Energy Source for Portable Devices*"; I. Garbayo, D. Pla, M. Salleras, A. Morata, N. Sabate, A. Tarancon; MRS Spring Meeting, San Francisco, USA, Apr 2013. Oral presentation.

4. *"Large-area micro SOFC based on a silicon supporting grid";* I. Garbayo, M. Salleras, A. Tarancón, A. Morata, G. Sauthier, J. Santiso and N. Sabaté; European Fuel Cell Forum, Lucerne, Switzerland, Jun 2012. Oral presentation.

5. *"$Sr_2Fe_{1.5}Mo_{0.5}O_{6-\delta}$ as symmetrical electrode for micro SOFC"*; I. Garbayo, S. Aruppukottai, G. Dezanneau, A. Morata, N. Sabaté, J. Santiso and A. Tarancón; European Fuel Cell Forum, Lucerne, Switzerland, Jun 2012. Poster presentation.

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