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PH.D THESIS

MONOLITHIC PACKAGING AND TRANSDUCTION
APPROACHES FOR CMOS-MEMS RESONATORS

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Directora: Prof. Núria Barniol Beumala

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CERTIFICA

que la memòria “Monolithic packaging and transduction approaches for CMOS-MEMS resonators” que presenta Eloi Marigó Ferrer per optar al grau de Doctor en Enginyeria Electrònica, ha estat realitzada sota la seva direcció.

Bellaterra, novembre 2012

Dra. Núria Barniol Beumala

Equipped with his five senses
man explores the universe around him
and calls the adventure Science.

Edwin Hubble

AGRAÏMENTS

Arriba un moment a la vida en el que te'n adones que sense gairebé adonar-te'n has arribat molt lluny. Et pares a reflexionar sobre el camí que has escollit i penses en tota la gent que t'ha acompanyat durant el llarg trajecte.

Primer de tot vull agrair el suport i l'estima de la meva família. Als meus pares, sense l'ajut i estima dels quals avui no seria qui soc amb els valors que tinc. Als meus germans, amb els que he crescut, après compartint i ajudant als altres. A la família Marigó per sempre ser-hi en els moments de necessitat fent pinya tots junts. Als meus avis que ja no hi son, els vull agrair haver pogut engendrar una família tant generosa i meravellosa.

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(científiques o no) i festes compartides. Tots vosaltres m'heu fet sentir integrat i part d'un petit però gran grup. Al departament hi ha molta gent que m'ha acompanyat i ajudat. Tots els companys de despatx: Jordi, Miguel, Abdelilah i Alfonso. Tota la resta de becaris: Xavi, Albert, Vanessa, Jordi, Vikas, Simone, Nuria, Albin, Gerard i Paris. I l'ajut i suport de Xio, Toñi, M^a Carmen i Javier, sense vosaltres el departament s'enfonsaria.

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Per acabar només em resta tornar a agrair a tothom (també si m'he deixat a algú) per haver estat amb mi durant aquest camí. Tal i com deia Serrat a la cançó dedicada a Antonio Machado:

*Todo pasa y todo queda
pero lo nuestro es pasar,
pasar haciendo caminos,
caminos sobre la mar.*

*Nunca perseguí la gloria,
ni dejar en la memoria
de los hombres mi canción;
Yo amo los mundos sutiles,
ingrávidos y gentiles
como pompas de jabón.*

*Me gusta verlos pintarse
de sol y grana,
volar bajo el cielo azul,
temblar súbitamente y quebrarse...
Nunca perseguí la gloria.*

*Caminante son tus huellas el camino y nada más;
Caminante, no hay camino se hace camino al andar.
Al andar se hace camino y al volver la vista atrás
Se ve la senda que nunca se ha de volver a pisar.
Caminante no hay camino sino estelas en la mar...*

Eloi

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SUMMARY

The increasingly performance of MEMS and their applicability to a wide range of fields has motivated the research and development of such devices. From the first demonstration of MEMS several applications have grown being the field of sensors their most competitive area.

The present dissertation deals with MEMS devices in radiofrequency domain such as resonators and oscillators with the aim to be used as frequency references. The approach employed in the design and fabrication of all the devices presented in this thesis is based on a $0.35\mu\text{m}$ commercial CMOS technology. The employment of a standard CMOS technology provides the capability to monolithically integrate MEMS devices with CMOS circuits enhancing their performance and reliability.

Related with the fabrication, a package for CMOS-MEMS resonators has been designed, fabricated and characterized. Several approaches have been employed to perform the sealing of the cavity and different resonators were packaged. It is demonstrated that the package provides additional protection to the MEMS devices maintaining their reliability.

The thesis was also focused on two major transduction methods: capacitive and piezoresistive. Different CMOS-MEMS devices with capacitive transduction were fabricated and measured providing resonant frequencies on the HF and VHF range. Some oscillators based on DETF and Free-free mechanical structures were also tested, demonstrating good performance with low biasing signals. From the piezoresistive sensing point of view several resonators were also fabricated and tested, being the measure obtained from a CCB the demonstration of the applicability of piezoresistive transduction to polysilicon CMOS-MEMS resonators.

RESUM EN CATALÀ

El gran increment en el rendiment dels MEMS i la seva aplicació a multitud de camps ha motivat la seva recerca i desenvolupament. Des de la primera demostració d'un MEMS, moltes aplicacions han sorgit, essent el camp dels sensors el seu sector més competitiu.

Aquesta dissertació tracta sobre dispositius MEMS amb aplicacions en el domini de la radiofreqüència, com per exemple ressonadors i oscil·ladors amb l'objectiu d'utilitzar-los com a referències de freqüència. El mètode implementat en el disseny i fabricació de tots els dispositius presentats en aquesta tesi es basa en una tecnologia comercial CMOS de $0.35\mu\text{m}$. La utilització d'una tecnologia CMOS estàndard proporciona la capacitat d'integrar monolíticament els dispositius MEMS amb circuits CMOS incrementant-ne el rendiment i la fiabilitat.

Relacionat amb l'àrea de fabricació, s'ha dissenyat, fabricat i caracteritzat un encapsulat per ressonadors CMOS-MEMS. S'han utilitzat varies aproximacions per aconseguir el segellat de la cavitat. També s'han encapsulat diferents tipus de ressonadors MEMS. S'ha demostrat que l'encapsulat proporciona protecció addicional als dispositius MEMS mantenint-ne la seva fiabilitat.

Aquesta tesi també s'ha centrat en dos mètodes de transducció: capacitiu i piezoresistiu. S'han fabricat i mesurat diferents dispositius CMOS-MEMS amb sensat capacitiu amb freqüències dins de les bandes d'HF i VHF. S'han testejat oscil·ladors basats en diferents estructures mecàniques demostrant unes bones prestacions amb petites senyals de polarització. Des del punt de vista de transducció piezoresistiva s'han fabricat i testejat també diferents estructures mecàniques ressonants, essent la mesura obtinguda amb el pont de polisilici la demostració de l'aplicació del esquema de transducció piezoresistiu a ressonadors CMOS-MEMS.

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1. INTRODUCTION

Three are the main characteristics identified by the acronym *MEMS*¹ (Micro Electro-Mechanical Systems): *Micro* identifying batch processing capabilities (taking profit of the microelectronics semiconductor processing); *Electro-Mechanical* meaning a transduction between motion and electrical signal; and *Systems* which can be related with a functional block instead of a simple device. In the case of CMOS-MEMS, the system has additionally the capability to be monolithically integrated with the CMOS electronics, providing in this sense enhanced signal processing capacities.

As will be summarized in this Ph.D dissertation several groups have been working hard in the integration of MEMS, providing excellent results dealing with sensing, being inertial sensors their paradigmatic example. On the other hand there is a need to find an integrable system able to substitute the bulky quartz crystal as frequency reference sources [VanB11]. Although a big effort has being done in this case of signal processing and several companies are starting to sell MEMS devices as clocks [SiTime, Discera] or RF MEMS [CK]. These systems are integrated in a heterogeneous way with the CMOS circuitry. In this sense the obtention of a CMOS-MEMS oscillator with the required performance for the communications system area is still pending.

In the sensing application area, gravimetric sensors (basically based on resonance frequency changes due to a variation of mass or mechanical stress), MEMS and with higher capabilities their smaller size devices *NEMS* (Nano Electro-Mechanical Systems) has been experienced a big development in different areas [Eki05, Arl11, Boi11, Bar12]. In this case and again the obtention of a very high sensitivity resonator along with their capabilities of being fully integrated as an oscillator with the needed CMOS circuitry, is still pending.

As a consequence we have established the principal motivation of this PhD thesis which consists basically in exploring the possibilities to monolithically integrate MEMS in standard CMOS process trying to obtain an enhanced self-oscillating CMOS-MEMS system for application in the sensing area as well as for RF processing.

Two have been the main challenges to solve: the first one to provide a full-custom CMOS-MEMS system including 0-level packaging of the MEMS device

¹ Microelectromechanical systems

directly in the CMOS die, contributing in this sense to provide a entire batch processing for MEMS. The second challenge has been to explore new transducing schemes optimized in terms of motional resistance and thus requiring less stringent conditions for obtaining a self-excited CMOS-MEMS oscillator. Piezoresistive transduction, with its ability to be also monolithically integrated with CMOS, has been studied as an alternative to capacitive transduction. In both challenges we will pursuit in obtaining a fully CMOS-MEMS self-oscillating as demonstrator.

The present Ph.D dissertation has been written in the core of the Department of Electronic Engineering of the Universitat Autònoma de Barcelona at the ECAS² group. The group is led by Prof. Dra. Núria Barniol and their research framework is based on the development of microelectronic systems. The first projects of the group involved biomedical applications and nowadays the group is focused on integrating microsystems with electronics for sensing purposes and radiofrequency applications. The know-how acquired in the integration of MEMS resonators in CMOS technologies by the ECAS group has been taking as the starting point of this thesis PhD work.

The introduction chapter is divided into six sections: a brief introduction to the MEMS field with several examples of applications, the methods used to induce motion in MEMS, the main sensing techniques, a review of the MEMS fabrication processes, a brief description of the projects under which this thesis has been carried out and the outline and objectives of the dissertation. The detailed explanation of the working principles and technologies of the MEMS involved here will be described in the following chapters.

1.1. MEMS OVERVIEW

MicroElectroMechanical Systems are micron size devices that relates motion with electrical signals. The scaling down of macro mechanical devices to micro mechanical devices provides an improvement in several areas. Obviously as their size is reduced their cost is also reduced by means of using microelectronics batch processes on their fabrication, [Sen01, Kaa09]. The integration of MEMS on standard CMOS technologies also provides enhancement in the size and cost fields areas, [Bal05, NVLSI]. In function of the application the key parameters could be various but there are four major topics which most of the applications have in common: energy efficiency or power consumption, sensitivity, response time and reliability. Concerning the power consumption, MEMS have been demonstrating lower requirements than other electronic circuits [Gra04] even there are MEMS devices capable to extract energy from the

² Electronic circuits and systems

environment [Rou05]. The sensitivity is directly related with the size of the device achieving better sensitivities as dimensions are reduced. See for example the results obtained with carbon nanotubes [Jen08] or with silicon-based nanowires [Yan06]. More recent contributions present promising applications related with mechanical biosensors [Arl11], mass sensing [Fan11, Arc11] and chemical or environmental detection [Boi11, Ver11]. The time between the MEMS device is operated and its response determines the amount of time and the number of measures which the device is capable to perform. It could be also reduced as the mechanical devices are scaled down and the frequency of operation is increased. Understanding the failure mechanisms is a prerequisite for quantifying and improving the reliability of MEMS devices [Hua12]. The common failure mechanisms in MEMS include mechanical fracture, fatigue, stiction, electrical short and open, contamination, etcetera.

1.1.1. HISTORIC PERSPECTIVE

The term MEMS was coined between 1987 and 1988 in a series of three workshops on microdynamics called “Small Machines” developed on Salt Lake City, Hyannis and Princeton respectively [Gab87]. However the first real MEMS device called resonant gate transistor had been fabricated much before (in 1965) [Nat67]. This device shown on Figure 1 has a metal cantilever that works as a moving gate actuated through an electrode above two diffusions on a semiconductor. The motion of the cantilever could be electrically sensed through the semiconductor channel.

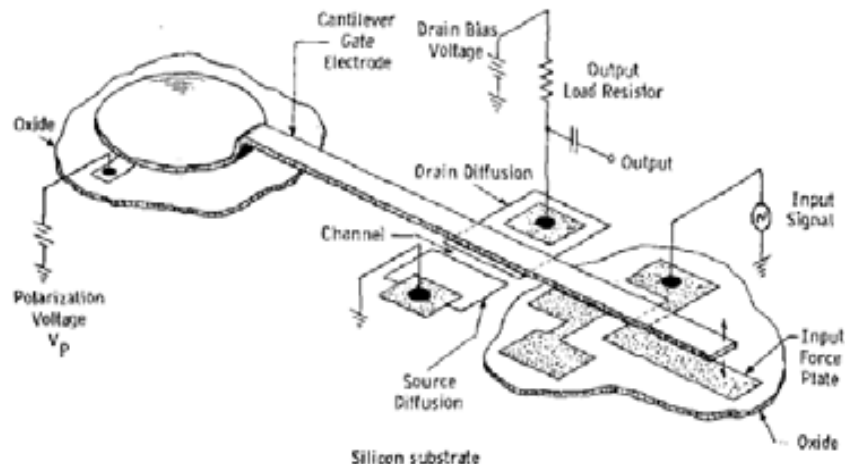


Figure 1.- Geometry and circuit connections of resonant gate transistor [Nat67].

The first mass produced application of MEMS was the pressure sensor in the 1970s decade where a thin diaphragm is deflected due to a pressure difference [Eat97]. The displacement is converted into an electrical signal and the sensing pressure is obtained if the reference pressure is known.

1.1 Introduction to MEMS Technology

Due to the improvement of research and development effort made between 1980s and 1990s new fabrication technologies, applications and potential markets were found [Pet82]. Some of the applications that have increased the MEMS market include AFM³ tips, ink-jet printer heads, airbag accelerometers, micromirrors, silicon microphones, RF switches and RF clock references. The AFM shown on Figure 2 is an instrument used to scan surfaces for imaging, measuring and manipulating matter at the nanoscale [Bin86]. The microscope is composed by a cantilever with a tip, typically of silicon or silicon nitride, the sample surface and a feedback detection system. The tip is placed near the surface and the forces between produce a deflection of the tip which is detected by the detection scheme that produce a feedback signal to maintain a constant distance between the tip and the surface.

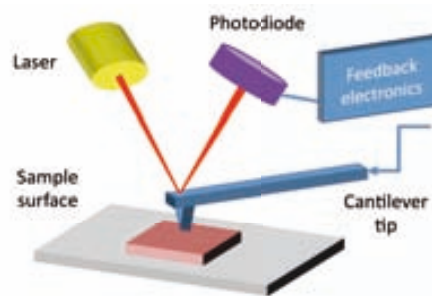


Figure 2.- Main components of an AFM microscope.

Following the timeline, the ink-jet printers have changed radically the printing market making cheaper, faster and smaller devices accessible to the whole consumers and not only the specialized ones. The main improvement that makes this change possible was the application of Microsystems in the heads of ink-jet printers [Kra95]. An example of ink-jet head is shown on Figure 3, where a chamber of ink with a nozzle with a hole of tens of microns is thermoelectrically or piezoelectrically actuated producing single drops of ink.

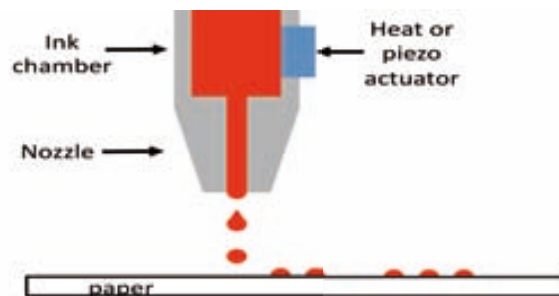


Figure 3.- Ink-jet head based on MEMS actuation technology.

³ Atomic force microscope

One of the most successful MEMS devices constitutes the inertial sensors. Accelerometers and gyroscopes are paradigmatic examples of MEMS in industry, [AnDev, STM]. The sensing of acceleration applied on vehicles provides more safety such as the activation of the airbag in a car. The working concept for the accelerometer is simply, a damped mass attached on a spring suffer displacement when external acceleration is applied. The deflection of the mass is proportional to the acceleration applied. An example of one of the first MEMS accelerometer is shown on Figure 4 [Che80].

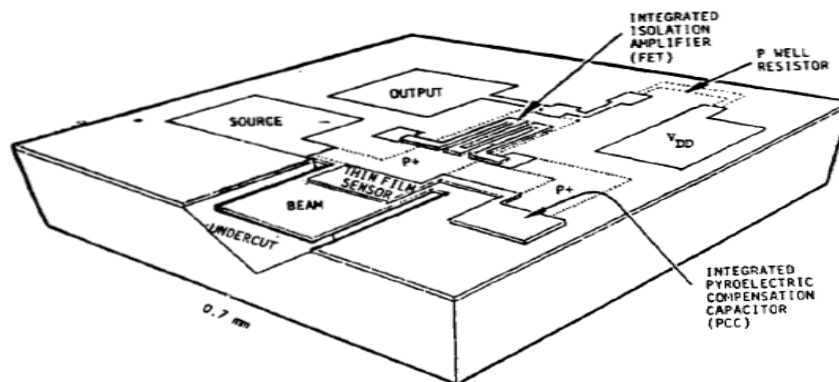


Figure 4.- MEMS accelerometer based on piezoelectric strain-sensing [Che80].

Another remarkable application is micromirror for projectors. The micromirror is typical composed by a square plate with aluminum deposited on top and torsion hinge that produce tilting through electrical signals, Figure 5 [Sam94]. The technology to fabricate arrays of micromirrors enables the production of DMD⁴ projector displays. The high brightness ratio achieved with DMD can compete with standard LCD⁵ projector displays with additional features such as lower heat dissipation, setup time and higher stability [Hor97]. An emerging application for miniaturized DMD are picoprojectors [RoMp11] which are expected to be included as a new feature on smartphones.

⁴ Digital micromirror device

⁵ Liquid cristal display

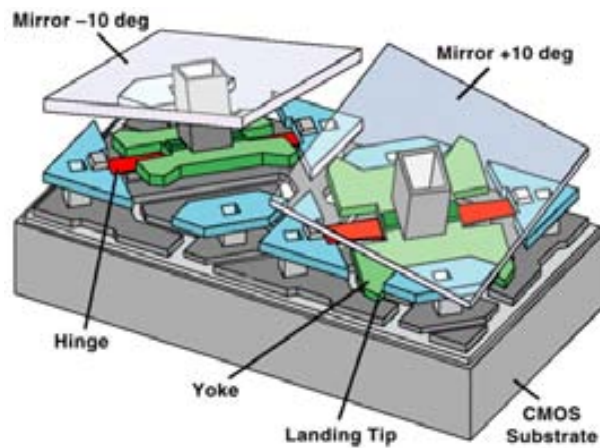


Figure 5.- Main components of a micromirror [Sam94].

The silicon microphones are also rapidly growing their presence in the industry mainly due to their application in electronic portable devices [Yo112]. Those devices are composed by a rigid back plate of silicon, a metalized diaphragm as the upper electrode, an air cavity and silicon dioxide layer between them used as the electret of the microphone, Figure 6 extracted from [Chi12].

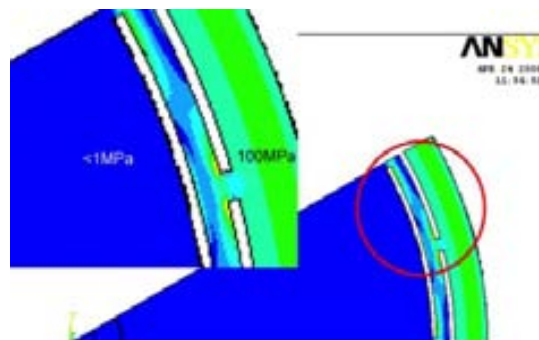


Figure 6.- Cross section of half silicon microphone, [Chi12].

Also several promising applications in the radiofrequency field have been developed including RF switches and RF resonators. The RF switches and resonators are called to replace passive components in high frequency radio transceivers and switching networks [Ngu98]. The biggest challenge in RF MEMS is enhancing reliability and lifetime. In the Figure 7 a typical superheterodyne transceiver is shown where the components suitable to be replaced by MEMS are highlighted. The switches are required, if the transceiver has only one antenna, to select the path of the signal and in the channel selection filter. Whilst the resonators are applicable to filters, matching networks, mixers and oscillators.

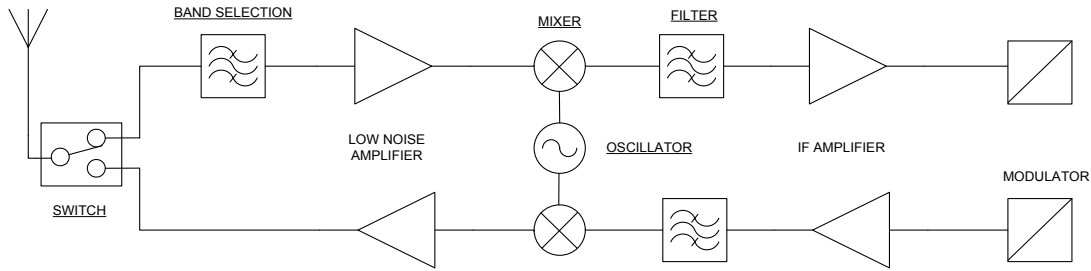


Figure 7.- Superheterodyne transceiver main blocks.

Nowadays the RF switches market is dominated by CMOS⁶ electronics which provide GHz frequency range, supply and control voltages less than 5V, insertion losses in the order of 0.5dB and minimum isolation of 25dB [InfRF]. DelfMEMS propose a RF MEMS switch approach capable to achieve 6GHz with 0.35dB of insertion losses, isolation of 40dB and minimum actuation voltages of 9V [DelfM]. Taking into account the good RF performance, the actuation voltage could be improved reducing the gap size making the device very competitive. The RF switches are divided into capacitive and ohmic switches. The capacitive switches are based on MEMS bridges with a large change in capacitance that modulates the signal transmission [Kaa09] but at frequencies below 1GHz very large capacitance values are needed to obtain low enough impedance. The ohmic switches made of cantilever structure solve this problem with surface contact. However the reliability is lower than the capacitive switches due to repeatedly surface material exchange. An example of RF MEMS capacitive and ohmic switches is shown on Figure 8.

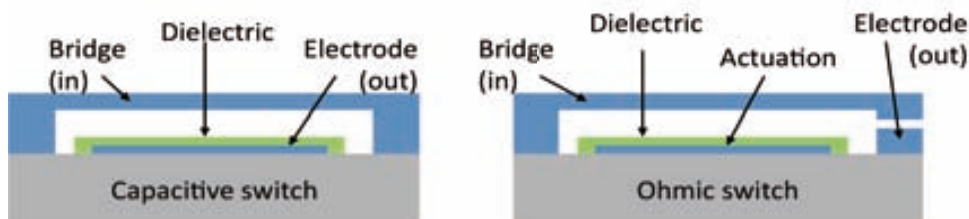


Figure 8.- RF MEMS switch topologies.

In the case of MEMS resonators there are a number of companies trying to displace the traditional quartz oscillator with a Si-based MEMS oscillator for the frequency reference used in clock and timing applications [SiTime, Discera], *Figure 9*. The Si-based MEMS oscillator has the advantages in shock resistance, smaller form factor and are more suitable for mass production, see reference [VanB11] for further information. The MEMS oscillator can be also integrated with the timing circuit into a much smaller package than the Quartz oscillator.

⁶ Complementary metal oxide semiconductor

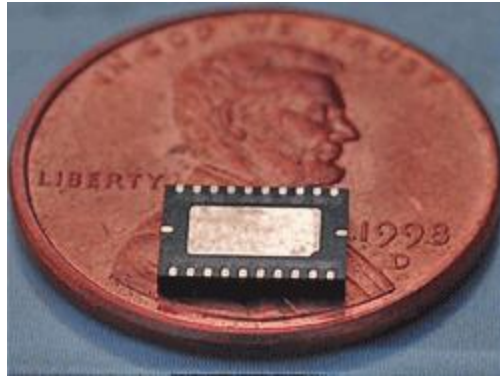


Figure 9.- The SiTime SiT9104 provides six single-ended clock outputs integrated in a small chip which can operate at up to 220MHz, [RoMp11].

Focusing in the Figure 7 on filters, oscillators and mixers, several resonators are mandatory to implement RF transducer topologies. Typical RF filters and oscillators use bulky non integrated passive components increasing the area and the cost of the whole RF transducer. The RF MEMS offer high frequency responses [Rin09], high quality factors [Lin04], *Figure 10* (a), integration solutions and tuning capabilities [Lop09b], *Figure 10* (b). Using MEMS to replace this kind of components will make selective, cheaper, smaller, and reconfigurable devices [VanB11].

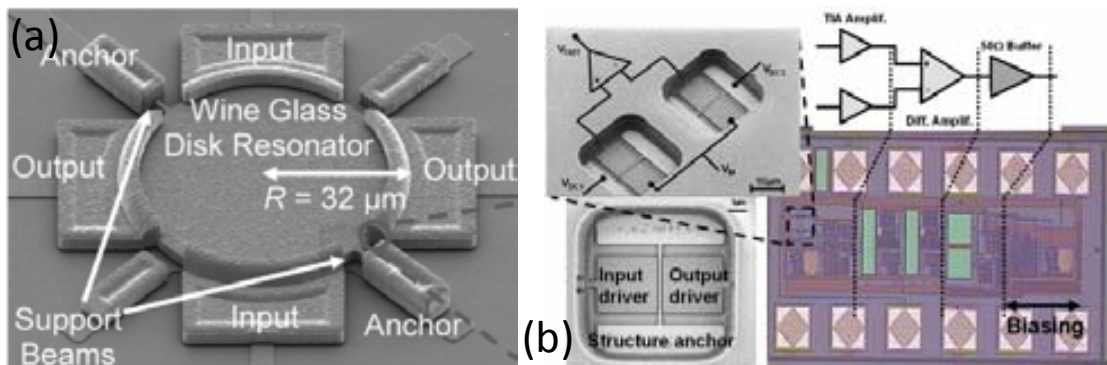


Figure 10.- RF MEMS examples: (a) Wine glass disk resonator with quality factor of 48000 [Lin04], (b) CMOS-MEMS RF tunable bandpass filter [Lop09b].

The capability to monolithically integrate MEMS in a CMOS technology provides the yield and reliability of microelectronics fabrication and the reduction of size and costs with the inclusion in the same die of the MEMS device and the CMOS circuitry. The first attempts to cointegrate MEMS in CMOS technology [Bus94] had provided the basis to adopt different fabrication strategies (pre, intra and post CMOS) [Fed08]. The research in CMOS-MEMS has allowed the appearance of companies like Baolab with his patented technology NanoEMS which is capable to massive manufacture CMOS-MEMS sensors [Baolab]. Cavendish Technologies also reports MEMS devices integrated in the CMOS back-end [CK]. A recent contribution

developed on CEA Leti-Minatec [Arc11] has achieved the fabrication of NEMS resonators in SOI wafer fully compatible with CMOS for multi-gas chromatography purposes.

1.1.3. MARKET PROSPECTIVE

In the last years the extremely growing market of smartphones and tablets has motivated an exponential increase in the demand of inertial MEMS sensors such as accelerometers, compass and gyroscopes. In fact even a specific working group fully dedicated to MEMS has appeared in the ITRS⁷ 2011. On the graph of the Figure 11 it is shown the sales growth from less than 200 millions of dollars in 2008 to 1250 millions of dollars expected on 2012 [RoMp11].

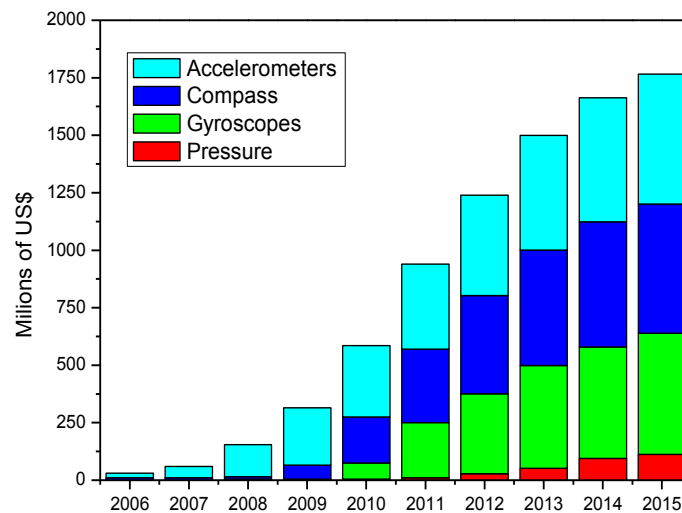


Figure 11.- Sales prospectives for motion sensors in handsets and tablets data extracted from [Mou12].

This tremendous increase in the demand has motivated an improvement on the research effort and an expansion to different areas which in prospective yield to new applications [Yol12]. On the Figure 12 it is shown a timeline graph comparative between the different applications and their correspondingly growth along time. It is remarkable the forecasting emergence on 2014 of the oscillators and the investment on RF-MEMS (the matter of this thesis). Additionally note the increment in other areas as can be microfluidics field and optical MEMS.

⁷ International technology roadmap for semiconductors

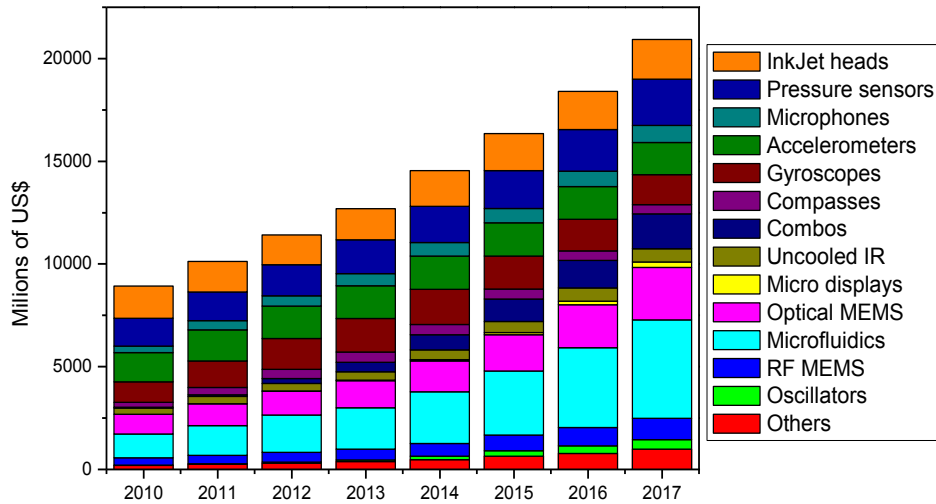


Figure 12.- MEMS market prospective from 2010 to 2017 in millions of US\$, [Yol12].

From the RF-MEMS section of ITRS 2011 the technology requirements are extracted and shown on Table 1. The table is divided into four main characteristics: performance, design & simulation, packaging & integration and testing. In most of the cases on short and middle term manufacturable solutions are known to achieve these requirements. However an improvement in some fields could enhance the proposed RF-MEMS and will allow developing solutions to the long term technology manufacturing requirements.

Year of production	2011	2012	2013	2014	2015	2016	2017
Performance							
Temperature stability (+/- ppm/range, °C)	(+/-15/-20~70)	(+/-10/-30~80)	(+/-4/-30~80)	(+/-2/-30~80)	(+/-1.5/-30~80)	(+/-1.0/-30~80)	(+/-0.5/-30~80)
Phase noise (dBc/Hz@1kHz)	-96	-120	-130	-135	-140	-150	-160
Current consumption (mA)	26	10	3	1.5	1	0.5	0.2
Frequency tolerance (@ 26°C +/- ppm)	20	3	2	1.5	1	0.5	0.2
Ruggedness (kilo G)	12	14	20	25			
Q factor (K)	60	70	80	90			
Jitter (psec-rms)	2	1	0.5	0.4	0.3	0.2	0.1
Design & simulation							
Simulation/estimation of residual stress							
Nonlinear frequency and transient mechanical control circuit modelling							
Packaging & integration							
Minimizing interconnect length and loading							
Integrated inductors with Q>50							
package size (mm x mm x mm)	2.5x2.5x0.75			1x1x0.55			
Testing							
Throughput							
RF precision and repeatability							
Failure respectively before it occurs, during operation of the device							
Validated accelerated life test.							

Table 1.- RF MEMS Resonator Technology Requirements extracted from [RoMp11]. In white manufacturable solutions exist and are being optimized, in yellow

manufacturable solutions are known, in orange interim solutions are known and in red manufacturable solutions are NOT known.

There are two different operating modes for the MEMS: static and dynamic.

In the first mode the device is actuated directly by means of the magnitude to sense and of course there is no need of an additional excitation method. The dynamic approach is based on drive the MEMS in resonance and sense the external magnitude through changes on the characteristics of the resonator (resonance frequency, resonance amplitude, phase at resonance, quality factor...). This approach is more complicated than the static but it provides absolute information regarding the measurand and better sensitivities. The *Figure 13* shows the main blocks in which a MEMS system could be split.

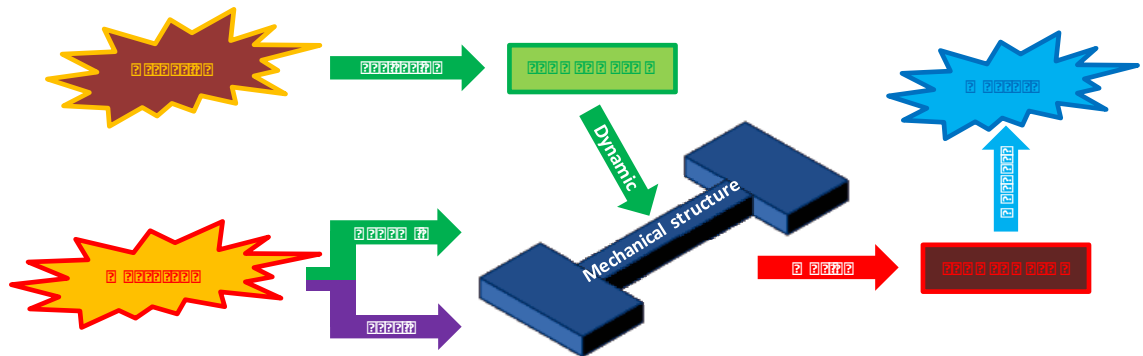


Figure 13.- Schematic representation of the static (purple) and dynamic (green) operation modes. The actuation and measurand are external magnitudes which interact with mechanical structure directly or through a transducer block. The sense of the motion always requires a transducer to translate the movement to an external measurable magnitude.

Focusing on dynamic operation the micro mechanical system must be excited into motion.

There are several different approaches to induce movement to a microsystem. Basically it is required a force source and a medium or material capable to interact with the mechanical device. The most common are electrical or magnetical sources but it is also possible to actuate MEMS with other like thermal sources.

Electrostatic excitation also known as capacitive actuation is based on applying an electrical field through an electrode forming a capacitor between the mechanical structure and the driver.

This is the first one to appear [Nat67] and the large one used technique for this inherent simplicity and applicability over different materials and

topologies. Electrostatic attraction becomes significant at micro-scale however there are limitations imposed by smaller couplings at nano-scale. Usually a continuous electrical signal, an alternate or a combination of both is applied to the electrode that produces an attractive electrostatic force that bends the mechanical structure towards the electrode. Examples of electrostatic actuation are shown on Figure 14. The (a) SEM image corresponds to a RF MEMS varactor from [Pal06]. The (b) SEM image show a clamped clamped beam resonator at 192MHz with a quality factor of 1000 [Tev07].

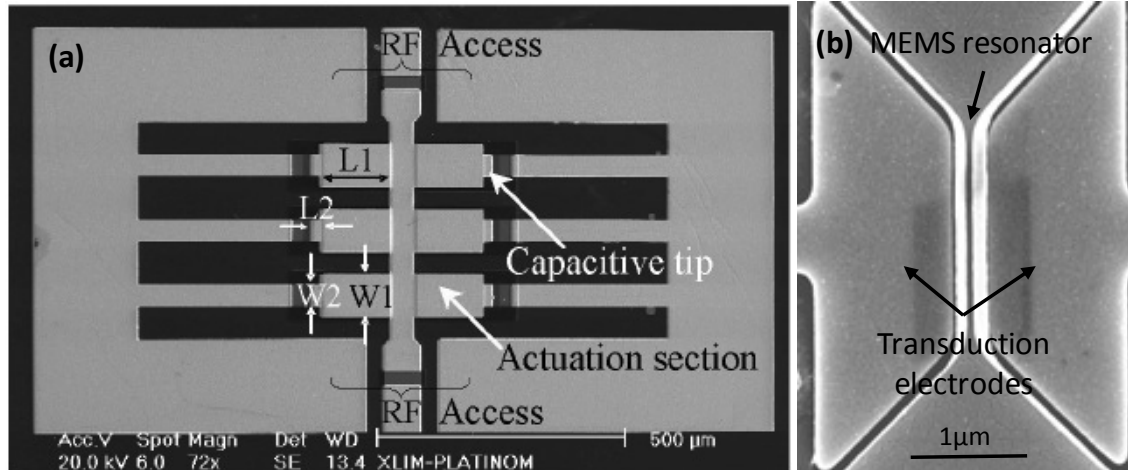


Figure 14.- Examples of capacitive actuated MEMS: (a) switched varactor designed to handle high power RF signals at maximum frequency of 10GHz [Pal06], (b) CMOS-MEMS CCB resonator at 192MHz [Tev07].

1.2.1.2. MAGNETIC

The Lorentz force produced in presence of a magnetic field between moving charged particles or an alternating current applied on the MEMS could also be used to induce motion in a microsystem. To produce a magnetic field a coil or inductor made from metal or a structure of magnetic material is required, the problem is that good coils or inductors are hard to miniaturize and fabricate with standard lithographic techniques. Also, magnetic materials are difficult to integrate with standard foundry process and require extremely low temperatures to generate enough magnetic fields, so magnetic actuation has not found success in MEMS commercial applications. Moreover, in research there are some MEMS actuators based on magnetic actuation as the one shown on the Figure 15, [Guc98].



Figure 15.- Linear magnetic actuator with assembled coil [Guc98].

1.2.1.3. PIEZOELECTRIC

The word piezoelectricity means electricity resulting from pressure. So in piezoelectric materials transient charges are induced in response to a mechanical deformation and vice versa. The piezoelectric actuation force scale well, even better than electrostatic force. Although the achieved displacements are small, in the range of few hundred nanometers, the main drawback is the piezoelectric material requirement increasing the cost and the challenge to integrate with standard foundry processes. The Figure 16 shows an example of a piezoelectric cantilever used as RF MEMS switch with low operation voltage of 2.5V, 0.22dB of insertion losses and isolation of 42dB at 2GHz, [Lee05].

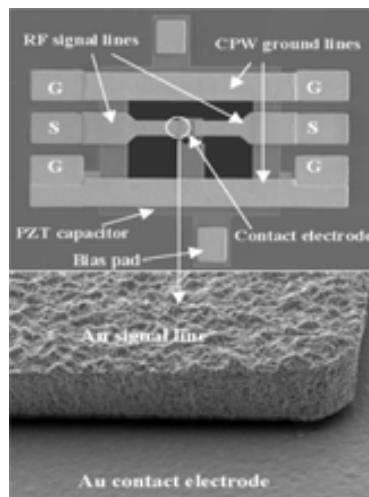


Figure 16.- Piezoelectrically actuated RF MEMS DC contact switch [Lee05].

1.2.1.4. THERMAL

Using thermal expansion of materials it is possible to produce displacements with heating. Typically a flowing current through a resistive structure produce, by means of Joule effect, heat dissipation which induce thermal expansion. This effect can be exploded in bilayer structures with different thermoelastic coefficients to induce bending and movement. The main drawback of this kind of actuators is power

consumption whereas for capacitive or piezoelectric actuators the power consumption is virtually zero. The heating and cooling time constants also limit the response speed of the device. An example of thermal MEMS actuator is shown on Figure 17 where a flowing current through buckling structures of silicon produce perpendicular displacement of the fiber placed in the middle allow aligning them with the other fiber end [Sym04].

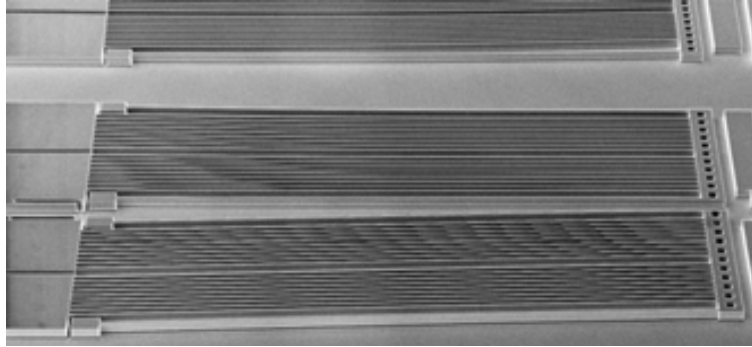


Figure 17.- Electrothermal MEMS actuator for optical fiber alignment [Sym04].

1.2.2. MEMS SENSING

The capability to measure a property or an attribute is called sensing. When a mechanical system is actuated the motion induced produce displacement and this displacement may contain useful information to be extracted through sensing methods. There are, several methods used in certain conditions or applications but in this section the most common ones will be briefly described.

1.2.2.1. CAPACITIVE

As same as an electrode with electrical signal (continuous or harmonic signal) exert some force to a conductive mobile structure that produce displacement, a displacement exert a change of capacitance which could be detected. The capacitive current will be proportional to the change in capacitance between a movable part and electrode. The capacitive sensing depends from the coupling area and from the dielectric between the electrodes and the structure which in most cases is air. So the amount of current is directly related by the coupling area of the electrodes which will be a problem in scaling down devices. Another undesirable effect in capacitive sensing is the so called parasitic current due to the static capacitance and the alternate signal applied on the electrode used to drive the movement in case of resonant devices. This current could completely mask the desired current component and make the measure almost impossible. There are some strategies that could be applied to minimize or subtract these parasitic currents. Despite of these drawbacks the capacitive sensing provides the easiest integrable approach and the less noisy. Some examples of MEMS with standard capacitive sensing are shown on Figure 18: (a) polysilicon disk resonator is fabricated [Cla05], (b) disk resonator with a solid dielectric gap [Lin05], (c,d)

CMOS-MEMS clamped clamped beam resonators fabricated in a standard $0.18\mu\text{m}$ CMOS technology [Lop09].

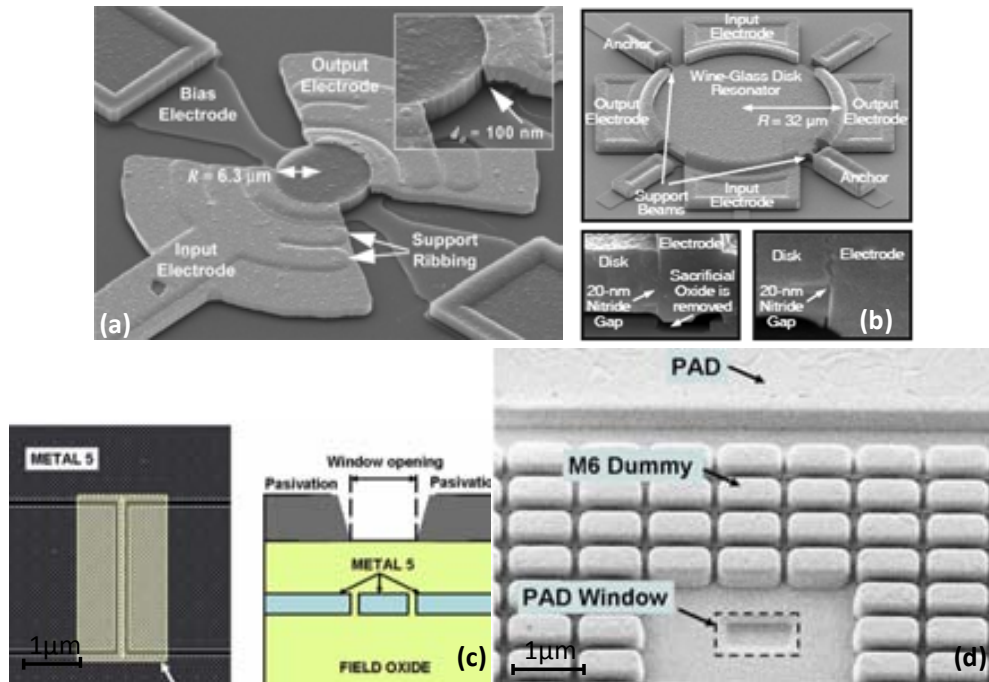


Figure 18.- Examples of capacitive sensing: (a) disk resonator with electrostatic actuation and capacitive sensing with air gap [Cla05], (b) other disk resonator with dielectric gap [Lin05], (c,d) clamped clamped beam resonators fabricated in a standard CMOS technology [Lop09].

1.2.2.2. PIEZORESISTIVE

The piezoresistive effect in metals was first discovered in 1856 by Lord Kelvin but was on 1954 that the large piezoresistive effect on semiconductors was shown [Smi54]. The word piezoresistive comes from change of resistivity for an applied strain which produces material deformations or even mechanical displacements on a movable element. These mechanical deformations or displacements will produce a variation of the resistance capable to be externally measured. This kind of sensing is classically used in many commercial devices including pressure sensors and accelerometers by two reasons: measuring resistance is in most cases easy to implement and a piezoresistor is a shielded structure in comparison to capacitor where environmental variations might induce undesired parasitic. Despite off the benefits, a resistor is intrinsically noisy and consumes a significant amount of power. An example of micromechanical piezoresistive sensing is shown on Figure 19 where four trapezoid cantilevers are micromachined with piezoresistors integrated to sense the drag force induced by fluid flow [Li10].

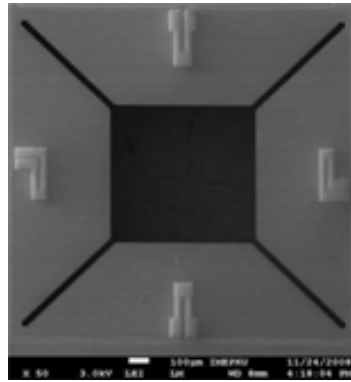


Figure 19.- Fluid flow MEMS sensor with piezoresistive sensing [Li10].

1.2.2.3. PIEZOELECTRIC

The same piezoelectric effect described in actuation section could be used in sensing if a mechanical deformation generates an electrical field capable to be measured. The main advantage that offers is that is self-generating and no requires external bias voltage or current. However, the amount of electrical field produced depend upon the magnitude of the mechanical deformation so detectable signals will require large deformations. Also it is not a suitable method for static measurements because in response to a static deformation the charges are redistributed over the material but remains statically in that position and does not generate current. The main obstacle of this method is that only some specific materials exhibit piezoelectric effect and these materials are not usually compatible with clean room processes. In the Figure 20 there are shown two examples of piezoelectric based MEMS cantilevers for energy scavenging purposes, combining the two different cantilevers the whole device is capable to extract energy from environmental vibrations in a wideband range, [Liu12].

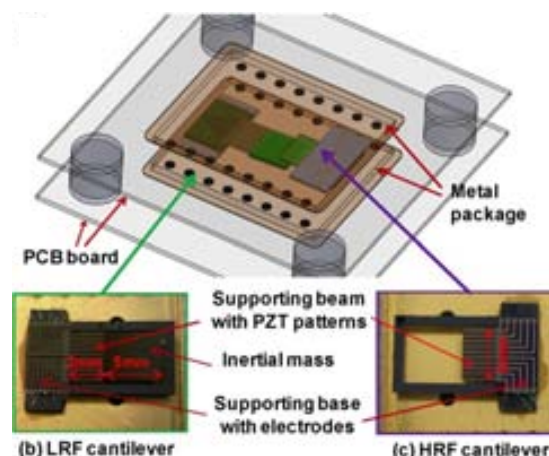


Figure 20.- Piezoelectric MEMS-based wideband energy harvesting, [Liu12].

1.2.2.4. OPTICAL

This sensing method is based on the detection of variations on optical signal that interacts with the mechanical structure. Obviously this method requires some light source such as laser and complex optical set-up: micro mirrors, beam splitters, optical filters, lenses, etc. The additional components make the whole detection system non integrable in a single chip which also increase the whole size and cost in comparison with other methods. Besides, the beam size spot limits the minimum dimensions capable to be measured. On the other hand, this method offers the best noise and parasitic behavior in comparison with the other ones due to the good immunity of light to electrical interferences and parasitics. In the Figure 21 it is shown an accelerometer with electrostatic actuation and optical sensing, the detection scheme is based on integrated nano-gratings that modulate the near-field intensity and polarization of an incident light source, [Kri08].

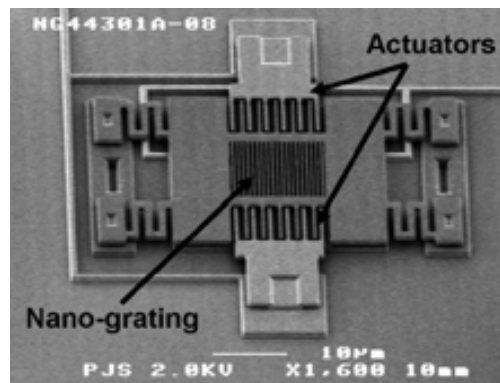


Figure 21.- In-plane MEMS-based nano-g accelerometer with sub-wavelength optical resonant sensor, [Kri2008].

1.3. MEMS DEVICES FABRICATION TECHNOLOGIES

The present section is intended to be a brief introduction to the most common topics in MEMS fabrication technologies and processes. Microfabrication has been developed from the microelectronics industry which is based on planar technologies: constructing the devices on substrates with wafer-based processes. As same as on integrated circuits the fabrication flow is divided into FEOL⁸ processes, BEOL⁹ processes and packaging. The microfabrication flow has similar stages commonly with fewer stages than integrated circuits. Usually in MEMS fabrication there are at least one structural layer and one sacrificial layer. In the first one the movable parts are defined whilst the second one is used to release the structure in order to allow the movement. Depending upon the materials and the dimensions required there are two main

⁸ Front end of line

⁹ Back end of line

microfabrication approaches: surface micromachining and bulk micromachining, [Sen01].

1.3.1. SURFACE MICROMACHINING

Starting from a substrate with a sacrificial layer and a photoresist layer, which was previously deposited, the device is patterned with photolithography process Figure 22 (a,b,c,d) into a deposited structural layer Figure 22 (e) and released using etching process to remove the sacrificial layer Figure 22 (f). The release of polysilicon structures by removing a sacrificial silicon dioxide film using HF¹⁰ acid based wet etching solution is the most popular surface micromachining technique nevertheless sacrificial aluminum etching with dielectric microstructures [Wes96] or sacrificial polymers with metallic microstructures [Sto94] are also processes used in function of the material requirements.

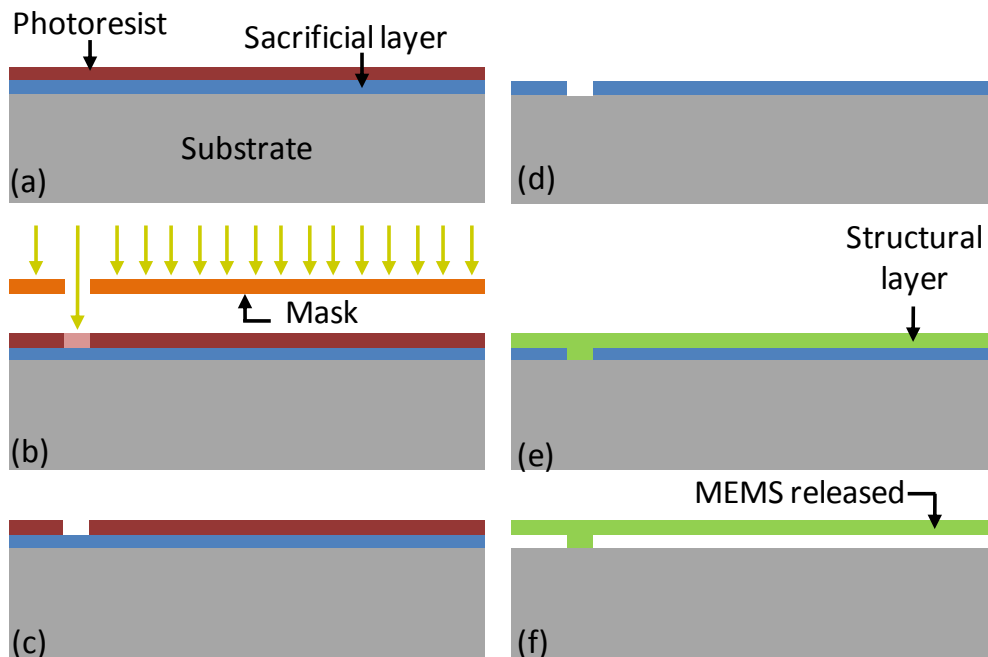


Figure 22.- Surface micromachining processes: (a,b,c) photolithography steps (photoresin deposition, exposing, revealing); (d) patterning; (e) structural layer deposition; (f) MEMS releasing.

1.3.2. BULK MICROMACHINING

This kind of approach is based on the principle that the structural layer is the substrate unlike the surface micromachining that requires a previous deposition of the structural layer material. The use of the substrate in the case of silicon provides a good

¹⁰ Hydrofluoric

mechanical material due to the crystalline lattice of the growth silicon in contrast of the semi crystalline lattices obtained with deposition of silicon (obtaining polycrystalline silicon). The structural layer is patterned by means of photolithography processes, *Figure 23* (a,b,c), and etching processes, *Figure 23* (d). The etching techniques used in bulk micromachining are classified by the directions of etching (isotropic and anisotropic) and by the phase of the etchant (wet for liquids and dry for gases) [Kov98]. The differences between anisotropic and isotropic etching processes are shown on *Figure 23* (d). Anisotropic wet etching of silicon is the most common micromachining technique used and has the characteristic of different etch rates for different crystal planes yielding the typical pyramid-shaped etch grooves.

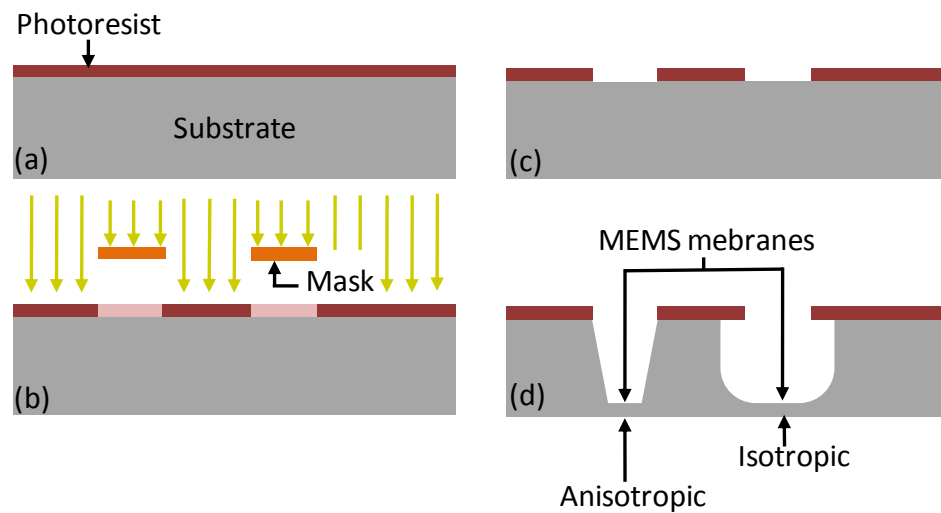


Figure 23.- Bulk micromachining processes: (a,b,c) photolithography steps (photoresin deposition, exposing, revealing); (d) device patterning with anisotropic or isotropic etching.

Examples of etching solutions used in anisotropic wet etching are KOH ¹¹ and TMAH ¹², the first one is very stable and yield reproducible but has relatively high silicon dioxide and aluminum etch rates whereas in TMAH solutions the etching rate of aluminum can be reduced. In anisotropic dry etching the most used method is RIE ¹³ where a plasma etching gas is directed onto the sample by controlling the process parameters. An improved of RIE called DRIE ¹⁴ was developed by Bosch which provides very high aspect ratio microstructures by an alternation of etching and polymer-assisted sidewall protection. In the Figure 24 there are two examples of microstructures fabricated by bulk micromachining processes, [Kla97], [Kov98].

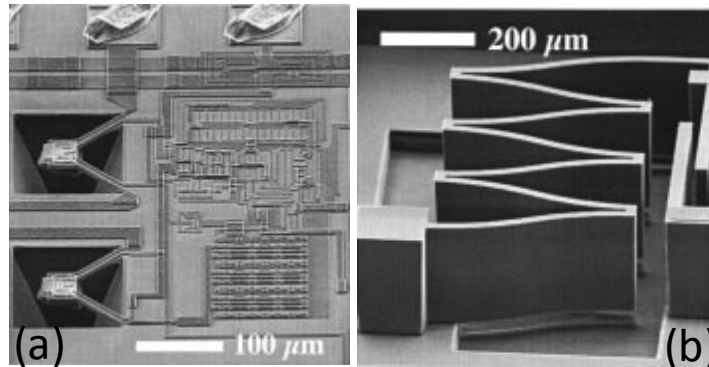


Figure 24.- Examples of anisotropic etching: (a) a suspended silicon n-well microstructure realized using TMAH etching of a CMOS integrated circuit [Kla97], (b) silicon leaf spring of MEMS accelerometer etched by DRIE [Kov98].

1.4. MEMS SYSTEM

Following the process flow of integrated circuits, the next step consists on make the device ready to commercialize. In this sense the signals obtained from MEMS devices must be processed in most of the cases. Huge reduction of costs is reached if the MEMS devices could be interconnected with electronic circuits in the same system. Two main strategies of co integration exist: System-in-Package (SiP) and System-on-chip (SoC).

1.4.1. PACKAGING

There are four major functions that must be provided by the packaging: signal and power distribution, heat dissipation and protection of the fabricated device from the environment (mechanical vibrations, gases, dust, radiation, chemicals...) [Tum97]. Usually it is a critical point between the fabrication of the integrated circuits and the

¹¹ Potassium hydroxide

¹² Tetramethyl ammoniumhydroxide

¹³ Reactive ion etching

¹⁴ Deep RIE

successful commercialization of the product because depending on the packaging the reliability, the lifetime and the total cost will be severely affected. The first two functions (signal and power distribution) are mainly carried by wire bonding between the metal pads of the silicon die and the output pins of the package. The heat dissipation and the protection of the chip will define the materials and the geometry of the package.

Although the packaging is a broad concept which implies a lot of considerations the packaging could be divided into different levels from zero level packaging to third level packaging in function of the requirements of the different levels. The zero level packaging is a post CMOS process directly on the die to protect some exposed parts of the chip capable to be damaged, altered or perturbed by the following steps (for example the quality factor of a MEMS resonator strongly depend of the gas pressure of their surroundings and some kind of vacuum to enhance it is usually required). The first level package term is normally used for all the integrated circuits in a single chip module connecting the metal pads of the chip with the metal pins by means of wire bonding. The second level package includes a group of single chip modules and possible other passive and RF components such as resistors, inductors, capacitors, switches, transmission lines in the same package. The third level and higher packaging corresponds to the outer shell of the product (the cover of a hand-held calculator or a mobile phone, the PCB¹⁵ of a graphics card...). In the Figure 25 there are some examples of the different levels of packaging explained.

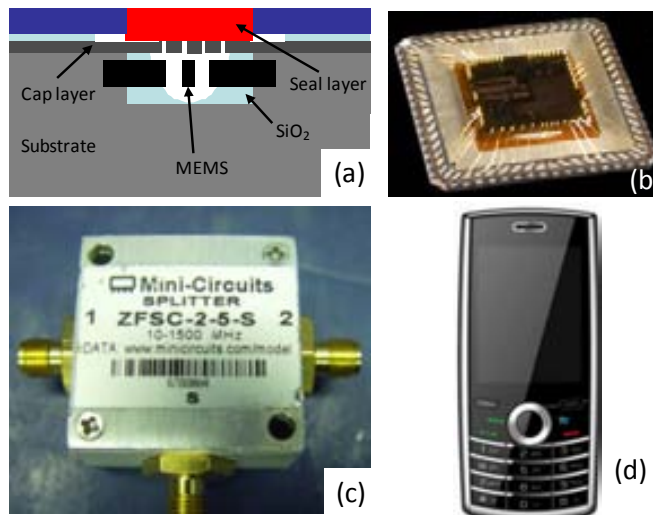


Figure 25.- Examples of different packaging levels. (a) Zero level packaging of MEMS device in order to assure controlled ambient inside them. (b) First level packaging of a single showing also wire bondings. (c) Second level packaging of a power splitter which includes some passive components and transmission lines inside them. (d) A plastic cover of a mobile phone that protects the electronics from the environment.

¹⁵ Printed circuit board

1.4.2. SYSTEM-IN-PACKAGE

The SiP strategy consists on fabricating in different substrates the MEMS devices and the electronic circuits. Separating the fabrication in two batch processes offer better mechanical structures and highest electrical performance of circuits since the materials and processes are not restricted between them. On the other hand, the complexity is transferred to interconnection and packaging of both elements which will also increase the whole cost and reduce the yield of the system. In function of how the substrates are interconnected there are three options available: wire-bonding, flip chip and 3D stacking.

The first one has been the classical option adopted to connect the metal pads of an integrated circuit with the output pins of the package by means of a micron size metal wire [Sil03]. This option is also applicable to the interconnection between different monolithic dies. In fact, this is the easiest technological option since direct observation of the connections is possible through a simple microscope. However, the length and the position of the wire could introduce some sort of parasitic signals especially troublesome on high-frequency applications. An example of wire bonding SiP extracted from [Sil03] is shown on *Figure 26* where a RF-MEMS device and integrated circuit from different substrates are packaged together and interconnected by metal wires.

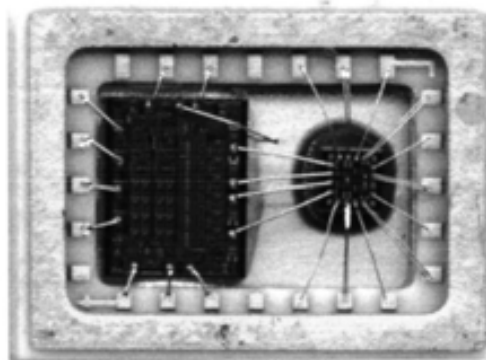


Figure 26.- SiP with RF-MEMS and control integrated circuit interconnected by means of wire bonding, [Sil03].

Flip-chip is an enhancement of wire bonding which takes profit from their advantages and solves the problem of larger and perturbing interconnections mounting one substrate on top of the other [Won01]. The interconnections between the substrates are classically made by solder dots deposited in a similar way than wire bonding. Then, the top chip is flipped and aligned on top of the bottom one and the solder is re-melted. This method is more batch like and provides lower dimensions. Although the alignment

of the two substrates is critical and additional considerations such as thermal expansion or mechanical shock failure must be carefully treated. The *Figure 27* shows an example of flip chip option extracted from [Won01] where the two substrates are attached together using solder bumps.

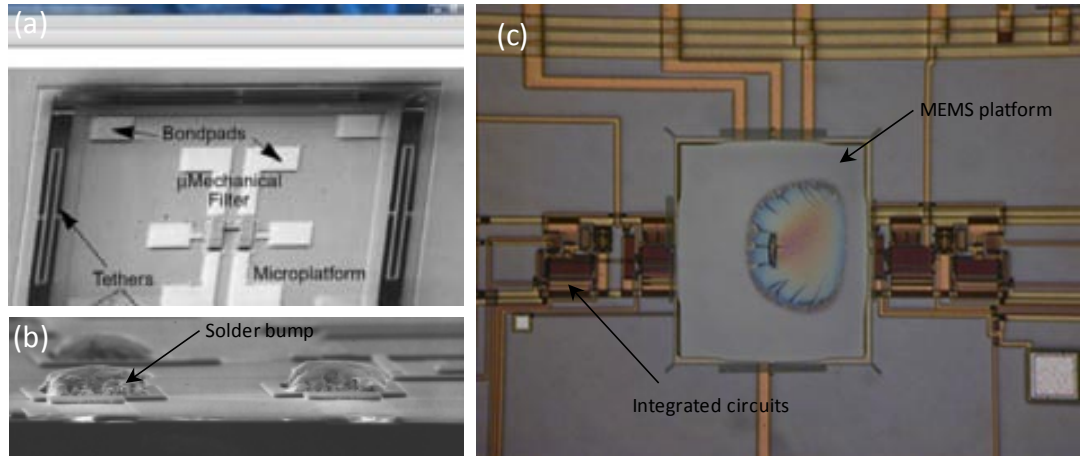


Figure 27.- SiP with flip chip: (a) micromechanical device with embedded bondpads, (b) detail of the solder bumps placed on bondpads, (c) whole system with the MEMS substrate attached on the integrated circuit substrate, [Won01].

From flip chip the 3D stacking is an obvious technological evolution [Bey06]. The improvement consists on make stacks of several substrates in order to obtain high density complex systems. Despite of this is the natural evolution of flip-chip, several additional challenges appear. The most important is related with the substrate dies placed on the middle of the stack which requires interconnection on both sides of it. In this sense TSV (through silicon via) electrical connection provide an efficient solution which moreover reduce the size of an equivalent system with flip-chip [Kni08]. In the *Figure 28* it is shown an example of 3D stacking of six silicon substrates with TSV interconnection.

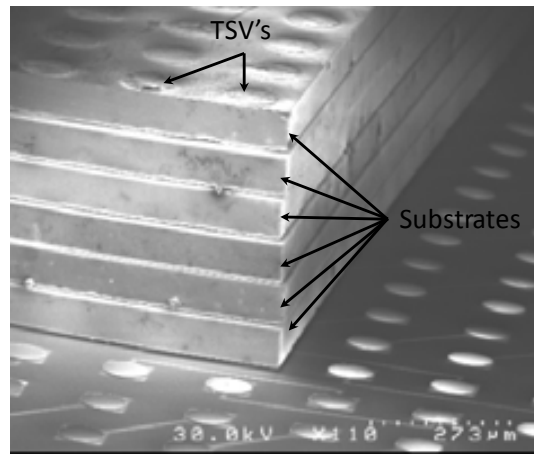


Figure 28.- SiP 3D stacking approach of six high thinned silicon substrates with TSV interconnection, [Kni06].

1.4.3. SYSTEM-ON-CHIP

In System-on-chip option the MEMS devices and electronic circuits are fabricated both on the same substrate. The adoption of this approach must face additional constraints like limitations over the available materials (best mechanical materials may not be suitable for the integration) or processes (normally the restrictions are given by the microelectronic processes) and increase of the complexity of the overall design. On the other hand the advantages provided by monolithic integration such the huge decrease in costs, size and parasitic or the reduction of failure mechanisms makes this kind of approach outstanding. The present thesis is focused into monolithic integration of MEMS devices on commercial CMOS technologies. The available options of SoC will be largely discussed on the third chapter where the fabrication processes and CMOS technologies will be explained.

1.5. RESEARCH FRAMEWORK

In the development of this PhD thesis the ECAS group was involved in two national. The first project developed between 2007 and 2009 was called “Explotación de la aplicabilidad de elementos integrados MEMS-CMOS monolíticos y heterogéneos para sistemas portátiles y autónomos de altas prestaciones (MEMSPORT)” had the objectives of: modelling electromechanically the CMOS-MEMS resonators [Tev06], design and test of different CMOS-MEMS approaches [Lop09], design of filters [Lop09b], mixers [Ura07], oscillators [Ver08], study of different RF transceiver architectures based on CMOS-MEMS subsystems and development of MEMS energy scavengers [Mur09].

The second project developed between 2010 and 2012 is entitled “NEMs/MEms in submicrometric CMOS technologies for RF SYStems and novel applications (NEMESYS)” seeks the goal to go one step beyond the first one and achieve the integration of MEMS/NEMS¹⁶ in advanced CMOS technologies. In particular the objectives of the project are: design of vibrating CMOS-MEMS for signal generation and processing for low power wireless communication systems in the RF range including full system integration [Mar10] and exploitation of alternative transduction schemes [Mar11, Mar12].

Additionally the work developed during this Ph.D. has been granted with three GICSERV projects that had been developed from 2008 to 2011 at the IMB-CNM-CSIC¹⁷. Between 2007 and 2008 a project called “Explotación de la aplicabilidad de elementos integrados MEMS-CMOS monolíticos y heterogéneos para sistemas portables de altas prestaciones” was developed with the aim to seal an integrated zero-level package with a MEMS resonator in a CMOS technology. Between 2008 and 2009 another project called “Realización de perfiles usando FIB¹⁸ y posterior caracterización SEM de sistemas MEMS/NEMS integrados en CMOS” was granted with the objective to acquire the capability to become self service user of the characterization instruments as part of the Ph.D. training. Between 2010 and 2011 the last project called “Sellado y caracterización de dispositivos CMOS-MEMS encapsulados mediante procesos fotolitográficos para la protección de los pads eléctricos” was carried on with the objective of protecting the electrical pads from the wet etching with photolithography process and vacuum seal the package cavity.

1.6. PH.D OBJECTIVES AND OUTLINE

The main goal pursued with the thesis is to develop fabrication approaches and new sensing methodologies that enhance the capabilities of monolithically integrated CMOS-MEMS. With this aim the following specific objectives are established:

- Design, fabricate and characterize an integrated package for CMOS-MEMS devices. In this sense the effort is focused on the design considerations and the additional processes required.
- Design, fabricate and characterize CMOS RF-MEMS with capacitive sensing. Stand alone resonators and self-oscillating CMOS-MEMS devices are characterized and new resonator structures are evaluated in order to push up their sensing capabilities.

¹⁶ Nanoelectromechanical systems

¹⁷ Institut de Microelectrònica de Barcelona – Centro Nacional de Microelectrònica – Consejo Superior de Investigaciones Científicas

¹⁸ Focused ion beam

- Exploit piezoresistive transduction instead of capacitive sensing and evaluate its application in CMOS RF-MEMS. Structures based on this sensing are designed, fabricated and characterized. The polysilicon layer as structural material from the CMOS technology will be used for this kind of sensing.

Considering this introduction chapter, this dissertation has been divided into six chapters:

Chapter 2: This chapter introduces the whole electromechanical theory related with the excitation and motion of MEMS and their specific characteristics.

Chapter 3: In this chapter the CMOS MEMS technology used is described and their application to the packaging is discussed and analyzed. The microelectronics processes involved in the development of the packaging of MEMS are explained and characterized.

Chapter 4: The objective of this chapter is focused on the capacitive sensing CMOS MEMS devices detailing from the whole theory involved to the new CMOS-MEMS devices and systems developed.

Chapter 5: This chapter deals with the CMOS-MEMS devices electrostatic excited and piezoresistive sensed. The main fundamentals together with the new proposed designs and their results are explained.

Chapter 6: The principal achievements and conclusions of this dissertation are explained in this last chapter.

Appendix I contains the information of all of the chips designed during the development of the thesis.

Appendix II contains a brief summary of the electrical characterization set-up used and developed in order to obtain all the electrical measurements on the CMOS-MEMS devices.

2. MICROELECTROMECHANICAL SYSTEMS THEORY

In this chapter the basic principles of the electromechanical fundamentals used in MEMS are explained. The theory and the modeling of mechanical systems are linked and electronic excitation schemes are presented.

2.1. ELASTICITY

A solid material in response to an applied force can be deformed before the breaking point or a permanent shape change. The theory that explains how a particular structure or a material is deformed is called elasticity. The assumption that there will be small and no plastic deformations will allow having linear relations between stress and strain, [Sen01].

The definition of stress is the force per unit area acting on the surface of a differential volume element of a solid body. The unit for stress is the Pascal, defined as one Newton of force per square meter of area. Considering that stress acts uniformly across the entire surface of an element, the normal stresses corresponds to a stresses perpendicular to a differential face and are named with a subscript identifying the direction: σ_x , σ_y and σ_z . The forces that are applied along the faces are called shear forces and the corresponding shear stresses are labeled with a double subscript that relates the face where the force is applied and their direction (τ_{xy} , τ_{xz} , τ_{yx} , τ_{yz} , τ_{zx} , τ_{zy}). In the Figure 1 is shown a differential volume with all these definitions.

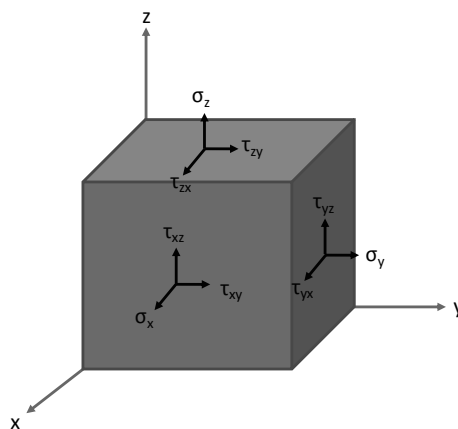


Figure 1.- Normal (σ_x , σ_y , σ_z) and shear (τ_{xy} , τ_{xz} , τ_{yx} , τ_{yz} , τ_{zx} , τ_{zy}) stresses acting in a differential volume.

In order to establish the relation between stress and strain it is assumed that the differential volume is in static equilibrium so there are no net forces or rotational moments on it. To satisfy this fact we will suppose that the forces are balanced adding normal forces. The requirement to avoid rotational moment implies that the shear stresses must be compensated between them so: $\tau_{xy}=\tau_{yx}$, $\tau_{xz}=\tau_{zx}$ and $\tau_{yz}=\tau_{zy}$.

The strain is defined as the differential deformation of a solid body when forces are applied and is expressed as change per unit length. As it is illustrated in the Figure 2 each corner of the volume is moved to a new location. The net motion can be separated into three parts: rigid motion of the original body, rigid body rotation about the center of mass and deformation relative to the displaced and rotated reference.

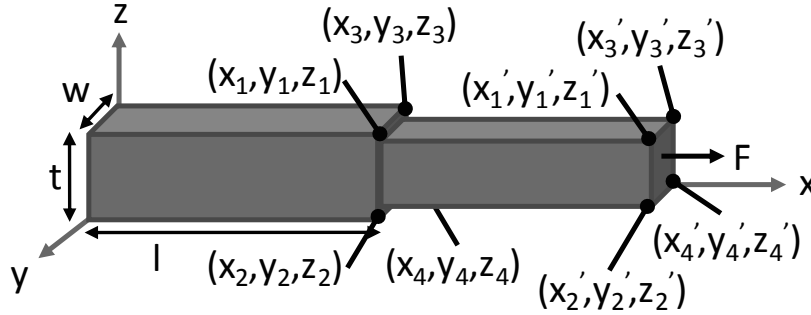


Figure 2.- Deformation of a solid volume in response to an applied force.

As same as for the stress the strain is divided into normal strain and shear strain. Considering the displacement as a function of the original position in x axis, $u(x)$ and a differential length Δx the normal strain ϵ is described by the following equation [2.1].

$$\epsilon_x = \frac{u_x(x + \Delta x) - u_x(x)}{\Delta x} = \frac{\partial u_x}{\partial x} \quad [2.1]$$

For shear strains γ the rigid-body rotation due to the deformation must be suppressed using the symmetric definition of the equation [2.2].

$$\gamma_{xy} = \left(\frac{\Delta u_x}{\Delta y} + \frac{\Delta u_y}{\Delta x} \right) = \left(\frac{\partial u_x}{\partial y} + \frac{\partial u_y}{\partial x} \right) \quad [2.2]$$

Considering an isotropic material (equal mechanical response in each direction) where an uniaxial force is applied the resulting uniaxial stress is proportional to uniaxial strain. The proportionality constant is called Young's modulus E , [2.3], and their units are Pascals due to the dimensionless of the strain.

$$\sigma_x = E \epsilon_x \quad [2.3]$$

The uniaxial strain produces deformation in a free-standing object and contraction in the directions transverse to the uniaxial direction. The relation between the uniaxial strain and the strain in other direction is proportional to the Poisson ratio ν and it is negative, [2.4].

$$\epsilon_y = -\nu\epsilon_x \quad [2.4]$$

The Poisson ratio ν , could take values between 0 and 0.5 which implies that there are materials that when are deformed increase their volume. Taking into account the increase in direction x and the contraction in y and z directions the net change in volume could be expressed as the [2.5].

$$\begin{aligned} \Delta V &= \Delta x \Delta y \Delta z (1 + \epsilon_x)(1 - \nu\epsilon_x)^2 - \Delta x \Delta y \Delta z \xrightarrow{\epsilon_x \downarrow \downarrow} \\ \Delta V &\simeq \Delta x \Delta y \Delta z (1 - 2\nu)\epsilon_x \end{aligned} \quad [2.5]$$

The G constant in elasticity theory is the Shear modulus which linearly relates the shear stress and the shear strain. For a shear stress applied on the x direction plane in the y direction the shear strain is described by [2.6] where if the two subscripts corresponds to the same axis, the equation [2.6] is equivalent to [2.3] (i.e shear strain τ_{xx} is equal to strain in σ_x).

$$\tau_{xy} = G\gamma_{xy} \quad [2.6]$$

The formulation of the linearly dependence of strain, stress and shear components could be extended to anisotropic materials such as crystalline where more than two elastic constants are needed to describe the strain-stress relation. A square 6×6 symmetric matrix of parameters is enough to describe all of the required relations. The subscripts of the stiffness coefficients C are related with the direction of stress and the coordinates axis using short hand matrix notation ($\tau_{xy}=\tau_{yx}$, $\tau_{xz}=\tau_{zx}$, $\tau_{yz}=\tau_{zy}$, $xx \rightarrow 1$, $yy \rightarrow 2$, $zz \rightarrow 3$, $yz \rightarrow 4$, $zx \rightarrow 5$, $xy \rightarrow 6$). However, for a simple cubic material (the atoms are arranged in the vertices of a cube) as it is silicon, there are only three independent quantities and the equation [2.7] describes all of the required relations.

$$\begin{pmatrix} \sigma_x \\ \sigma_y \\ \sigma_z \\ \tau_{yz} \\ \tau_{zx} \\ \tau_{xy} \end{pmatrix} = \begin{pmatrix} C_{11} & C_{12} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{12} & C_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{44} \end{pmatrix} \cdot \begin{pmatrix} \epsilon_x \\ \epsilon_y \\ \epsilon_z \\ \gamma_{yz} \\ \gamma_{zx} \\ \gamma_{xy} \end{pmatrix} \quad [2.7]$$

The three stiffness coefficients for silicon in [200]-crystal axes are [Lid95]:

$$\begin{aligned}
 C_{11} &= 166GPa \\
 C_{12} &= 64GPa \\
 C_{44} &= 80GPa
 \end{aligned}
 \tag{2.8}$$

The stiffness coefficients could be related with the Young modulus in function of the different crystal directions through the following equations [2.9] where the values were extracted from [Sen01].

$$\begin{aligned}
 E_{[200]} &= C_{11} - 2 \frac{C_{12}}{C_{11} + C_{12}} C_{12} = 130GPa \\
 E_{[210]} &= 4 \frac{(C_{11}^2 + C_{12}C_{11} - 2C_{12}^2)C_{44}}{2C_{44}C_{11} + C_{11}^2 + C_{12}C_{11} - 2C_{12}^2} = 170GPa \\
 E_{[211]} &= 3 \frac{C_{44}(C_{11} + 2C_{12})}{C_{11} + 2C_{12} + C_{44}} = 189GPa
 \end{aligned}
 \tag{2.9}$$

Considering a bar with one fixed end with a length l , a cross sectional area $A = w \cdot t$ and uniaxial force F applied on the y axis (Figure 2), the [2.3] can be expressed in terms of the force and the total elongation Δl . The k term is called the spring constant and depends on the Young modulus of the material, the shape of the structure and how the structure is deformed in response of the applied force [2.10]. This last equation corresponds to the well known Hooke's law.

$$\frac{F}{A} = E \frac{\Delta l}{l} \rightarrow F = \frac{E \cdot A}{l} \Delta l \rightarrow F = k \cdot \Delta l
 \tag{2.10}$$

2.2. STATIC DISPLACEMENT IN MEMS

The same bar of the previous section without any end fixed with a force transverse to the neutral axis (axis whose length is unchanged by bending) applied on the tips requires more complex formulation but illustrates how to obtain the differential equation that govern the beam displacement.

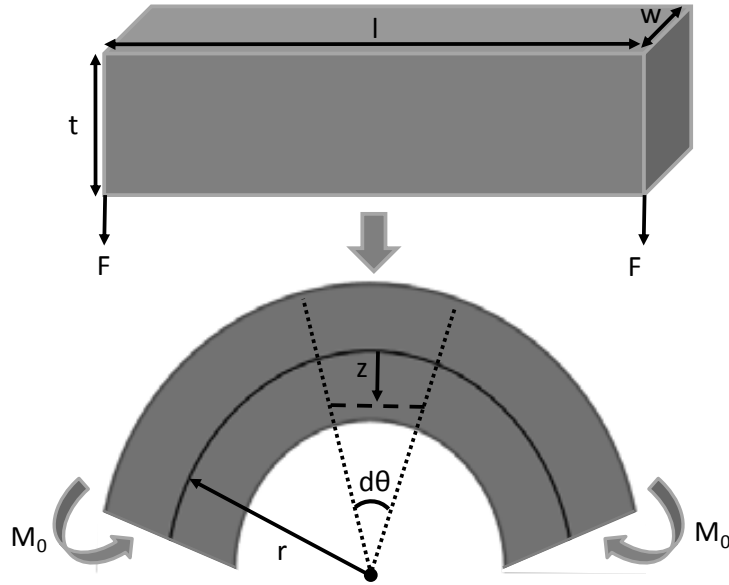


Figure 3.- Segment of a beam in pure bending showing the neutral axis in the middle of the beam. The upper side is in tension whilst the lower side is in compression.

The differential angular segment $d\theta$ has axial length dx when not bent. When the beam is bent the length of an arc segment depends on how far it is from the neutral axis. Considering the length of the dashed segment at position z the relation [2.11] is obtained. The corresponding segment length at the position of the neutral axis when the beam is not bent and considering small angle variation ($\tan d\theta/2 \approx d\theta/2$) is equal to [2.12].

$$dl = (r - z)d\theta \quad [2.11]$$

$$dx = rd\theta \quad [2.12]$$

Then, combining the [2.11] and [2.12] the [2.13] is obtained. Where by definition the strain is clearly the amount represented by [2.14] and the stress could be computed by [2.15].

$$dl = dx - \frac{z}{r}dx \quad [2.13]$$

$$\epsilon_x = -\frac{z}{r} \quad [2.14]$$

$$\sigma_x = -\frac{zE}{r} \quad [2.15]$$

To compute the total internal bending moment, the first moment of the internal stresses distribution is calculated as [2.16] where the moment of inertia I is defined by [2.17].

$$M = \int z(\sigma dA) = \int_{-w/2}^{w/2} z(\sigma_x t dz) = \int_{-t/2}^{t/2} -\frac{z^2 E}{r} t dz = -\frac{w^3 t E}{12 r} = -\frac{E \cdot I}{r} \quad [2.16]$$

$$I = \frac{tw^3}{12} \quad [2.17]$$

So the inverse of the curvature radius is proportional to the moment and inversely proportional to the moment of inertia which depends on the geometry of the beam [2.18].

$$\frac{1}{r} = -\frac{M}{E \cdot I} \quad [2.18]$$

In order to obtain the differential equation for beam bending the geometric displacement of the neutral axis is calculated in function of the angle between the initial and final position of them. The Figure 4 illustrates a beam with one fixed end and one free end named commonly cantilever.

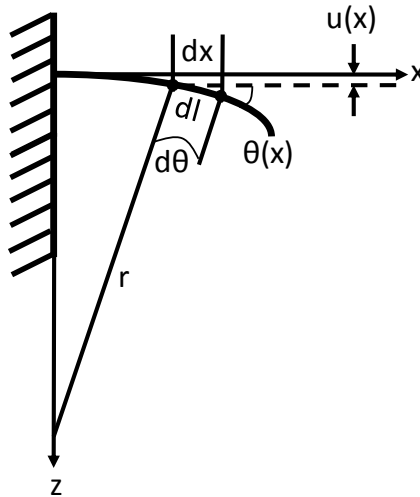


Figure 4.- Cantilever beam with geometric differentials

The increment of beam length along the neutral axis and the slope of the beam at any point $\theta(x)$ are related with the angle deformation θ by the equation [2.19] and [2.20] respectively.

$$dl = \frac{dx}{\cos\theta} \quad [2.19]$$

$$\frac{du}{dx} = \tan\theta \quad [2.20]$$

In addition, for a given radius of curvature r at position x , the relation between dl and the incremental subtended angle $d\theta$ is:

$$dl = rd\theta \quad [2.21]$$

For small deflections the small angle approximation could be assumed obtaining for the equation [2.19] that $dl \approx dx$ and for the equation [2.20] that $du \approx dx \cdot \theta$. Then the equation [2.22] and equation [2.23] are obtained.

$$\frac{d\theta}{dx} \approx \frac{1}{r} \quad [2.22]$$

$$\theta \approx \frac{du}{dx} \quad [2.23]$$

Differentiating the equation [2.23] respect to x and combining with [2.22] the relation between the given radius of curvature and the slope of the beam is obtained:

$$\frac{d\theta}{dx} = \frac{1}{r} = \frac{d^2u}{dx^2} \quad [2.24]$$

Finally, equating the equation [2.18] with equation [2.24] the differential equation for small-angle bending of beams is obtained in the equation [2.25].

$$\frac{d^2u}{dx^2} = -\frac{M}{E \cdot I} \quad [2.25]$$

Considering a point force perpendicular to the beam acting in the free end at position $x=l$, the internal moment is expressed by equation [2.26].

$$M(x) = -F(l - x) \quad [2.26]$$

To solve this equation in the case of the Figure 4 the boundary conditions impose that the displacement and the velocity in the clamped end must be zero so $u(0) = 0$ and $\frac{\partial u(0)}{\partial x} = 0$. The displacement is isolated from equation [2.25] by integrating twice and applying the boundary conditions to the integrating constants obtained in each of the integrals, then the equation [2.27] for the displacement is obtained. In the Figure 5 the equation [2.27] is represented for a cantilever made of polysilicon (considering a Young modulus of 160GPa and mass density of 2330kg/m³) of 13 μ m of length, 350nm of width, 282nm of thickness and a force from 0N to 10nN.

$$u(x) = \frac{F}{E \cdot I} \left(\frac{lx^2}{2} - \frac{x^3}{6} \right) \quad [2.27]$$

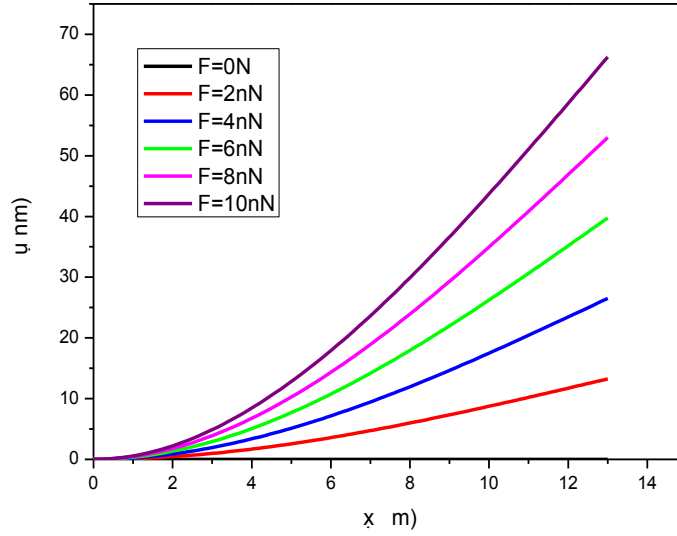


Figure 5.- Displacement along the position for a cantilever with different applied forces.

At the tip end l the displacement equals to equation [2.28] which combined with the Hooke's law $F = k \cdot u(x)$ gives the cantilever effective spring constant of the equation [2.29].

$$u(l) = \frac{l^3}{3E \cdot I} F \quad [2.28]$$

$$k = \frac{3E \cdot I}{l^3} \quad [2.29]$$

The angle of the beam with respect to rest position is obtained taking the partial derivative of the displacement respect the position in the beam, equation [2.30].

$$\theta(x) = \frac{\partial u(x)}{\partial x} = \frac{F}{E \cdot I} \left(lx - \frac{x^2}{2} \right) \quad [2.30]$$

It is convenient to obtain the expressions of the displacement and the effective spring constant for a clamped clamped beam because it is the main mechanical structure used in this thesis. This structure has the two ends fixed so the boundary conditions impose that the displacement and velocity in both ends are zero, $u(0) = u(l) = 0$ and $\frac{\partial u(0)}{\partial x} = \frac{\partial u(l)}{\partial x} = 0$. If the function of the beam is divided in two parts, for lower positions than the middle of the length and for greater positions than the middle of the length, additionally continuity conditions must impose that the displacement and velocity in the middle of the beam have to be the same in each equation, $u\left(\frac{l^+}{2}\right) = u\left(\frac{l^-}{2}\right)$ and $\frac{\partial u\left(\frac{l^+}{2}\right)}{\partial x} = \frac{\partial u\left(\frac{l^-}{2}\right)}{\partial x}$. Applying the moments of the [2.31] and [2.32] to the equation [2.25],

integrating twice and obtaining the integration constants from the boundary conditions, the displacement equations of the [2.33] and [2.34] are obtained.

$$M\left(0 < x < \frac{l}{2}\right) = -\frac{F \cdot l}{8} + \frac{F \cdot x}{2} \quad [2.31]$$

$$M\left(\frac{l}{2} < x < l\right) = \frac{3F \cdot l}{8} - \frac{F \cdot x}{2} \quad [2.32]$$

$$u\left(0 < x < \frac{l}{2}\right) = \frac{F}{E \cdot I} \left(\frac{x^3}{12} - \frac{x^2 l}{16} \right) \quad [2.33]$$

$$u\left(\frac{l}{2} < x < l\right) = \frac{F}{E \cdot I} \left[\frac{x^3}{12} - \frac{x^2 l}{16} - \left(x - \frac{l}{2}\right)^3 \right] \quad [2.34]$$

In the Figure 6 the equations [2.33] and [2.34] are represented for a clamped clamped beam made of the same polysilicon as for the cantilever with $13\mu\text{m}$ of length, 350nm of width, 282nm of thickness and a force from 0N to 10nN . Comparing the graphs of the Figure 5 and Figure 6 it is clearly shown that the cantilever is much softer than the clamped clamped beam.

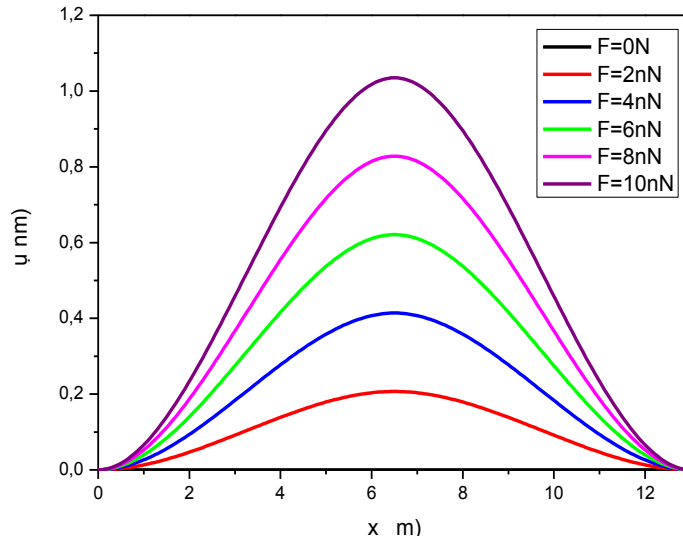


Figure 6- Displacement along the position for a CCB with different applied forces.

The maximum displacement of the beam of the equation [2.35] is produced in the middle and it is obtained from [2.33] or [2.34]. Using Hooke's law analogously to the cantilever case the CCB effective spring constant of the [2.36] is extracted.

$$u\left(\frac{l}{2}\right) = -\frac{(l/2)^3}{48E \cdot I} F \quad [2.35]$$

$$k = \frac{192E \cdot I}{l^3} \quad [2.36]$$

2.3. DYNAMIC BEHAVIOR

In the previous section the mechanical modeling of a resonator was derived obtaining the maximum displacement of a cantilever and a CCB. However, the time dependence is not shown and the dynamic behavior is not shown. To obtain the equation of motion on the beam of Figure 3 the method of dynamic equilibrium is applied with the concepts derived from the previous section, [Ger95]. Before that, the additional consideration that transverse deflections do not result in axial torsion or rotational shear forces must be assumed. The total inertial forces $f_I(x,t)$ acting over a differential section $ds = \rho A dx$ is expressed by D'Alembert's principle shown on [2.37] where $u(x,t)$ is the displacement, ρ is the density of the material and A their cross sectional area. These two last parameters are considered constant over the whole structure.

$$f_I(x,t) = \rho A dx \frac{\partial^2 u(x,t)}{\partial t^2} \quad [2.37]$$

The equilibrium of forces (Newton's first law) in the differential cross section of the beam shown on Figure 7 of [2.38] takes into account the shear forces $V(x,t)$, the distributed load q and the total inertial forces $f_I(x,t)$. Then the dynamic equilibrium equation for forces is depicted on [2.39].

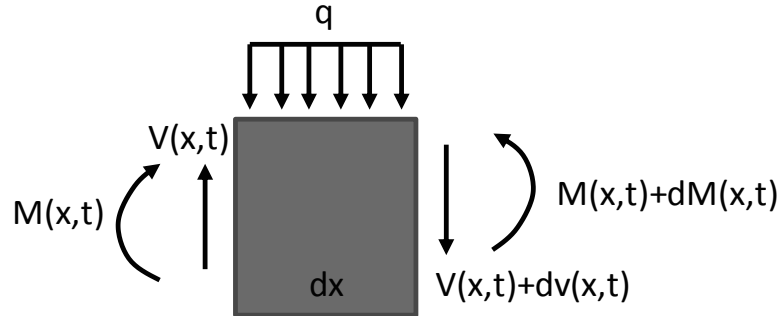


Figure 7.- Differential cross section of a beam with load q , shear forces $V(x,t)$ and bending moments $M(x,t)$. The sign convention establishes that the load is positive when it acts downward on the beam.

$$\sum F = 0 \rightarrow V(x,t) - q dx - (V(x,t) + dV(x,t)) + f_I(x,t) = 0 \rightarrow \quad [2.38]$$

$$\frac{dV(x,t)}{dx} = \frac{f_I(x,t)}{dx} - q$$

$$\frac{dV(x,t)}{dx} = \rho A \frac{\partial^2 u(x,t)}{\partial t^2} - q \quad [2.39]$$

The equilibrium of moments in the differential cross section of the Figure 7 beam is obtained summing moments about an axis at the left-hand side of the element, and taking counterclockwise moments as positive:

$$\sum M = 0 \rightarrow -M(x, t) - qdx \left(\frac{dx}{2} \right) - (V(x, t) + dV(x, t))dx + M(x, t) + dM(x, t) = 0 \quad [2.40]$$

Discarding products of differentials (negligible compared to the other terms), the following relationship is obtained:

$$V(x, t) = \frac{dM(x, t)}{dx} \quad [2.41]$$

Differentiating the shear force and substituting the bending moment $M(x, t)$ by the expression [2.25] obtained in previous section:

$$\frac{dV(x, t)}{dx} = -EI \frac{d^4u}{dx^4} \quad [2.42]$$

Finally equating [2.39] with [2.42] the dynamic Euler-Bernoulli equation for the beam is obtained:

$$EI \frac{\partial^4 u(x, t)}{\partial x^4} + \rho A \frac{\partial^2 u(x, t)}{\partial t^2} = q \quad [2.43]$$

The above equation is dependant over time and position and is difficult to compute, so variable separation is mandatory. To do this the assumption [2.44] that the solution will be in the form of the product of two independent functions is carried out which physically implies that each point of the beam vibrates with an amplitude $U(x)$ and with an angular frequency ω_n dependant on the vibration mode of the beam.

$$u(x, t) = U(x) \cdot \cos(\omega_n t + \theta) \quad [2.44]$$

Substituting the proposed solution [2.44] into [2.43] gives the equation [2.45] which roots are shown on the equation [2.46]. These roots will provide the frequency of each natural mode of the device.

$$EI \frac{\partial^4 u(x)}{\partial x^4} \pm \rho A \omega_n^2 u(x) = 0 \rightarrow \frac{\partial^4 u(x)}{\partial x^4} = \pm \frac{\rho A}{EI} \omega_n^2 u(x) \quad [2.45]$$

Defining the constant k_n as [2.46] the roots of the equation [2.45] are given on [2.47].

$$k_n = \sqrt[4]{\left(\frac{\rho A}{EI} \omega_n^2\right)} \quad [2.46]$$

$$r_1 = k_n ; r_2 = -k_n ; r_3 = j \cdot k_n ; r_4 = -j \cdot k_n \quad [2.47]$$

From the defined k_n the general expression [2.48] for the natural resonant frequencies of beams could be obtained assuming the moment of inertia from [2.17]. This is one of the basic MEMS design expressions which gives the capability to establish the desired operating frequency in function of the mode and the mechanical structure providing the dimensional parameters required.

$$f_n = \frac{(k_n l)^2 w}{2\pi l^2} \sqrt{\frac{E}{12\rho}} \quad [2.48]$$

The general solution of [2.45] could be expressed as a sum of complex exponentials [2.49] or equivalently as a sum of trigonometric functions [2.50].

$$u(x) = C_1 e^{k_n x} + C_2 e^{-k_n x} + C_3 e^{j k_n x} + C_4 e^{-j k_n x} \quad [2.49]$$

$$u(x) = A_n \sin(k_n x) + B_n \cos(k_n x) + C_n \sinh(k_n x) + D_n \cosh(k_n x) \quad [2.50]$$

To obtain the constants A_n , B_n , C_n , and D_n the Dirichlet boundary conditions for the case of the cantilever or the clamped clamped beam have to be applied. For a cantilever there cannot be any displacement or rotation at the fix end (deflection and slope are 0). Since no external moment and force are applied, at the free end of the beam the bending moment and the shear force are also 0. In summary: $u(0) = 0$, $\frac{\partial u(0)}{\partial x} = 0$, $\frac{\partial^2 u(l)}{\partial x^2} = 0$ and $\frac{\partial^3 u(l)}{\partial x^3} = 0$. These boundary conditions applied to [2.50] give the relations of [2.51], [2.52], [2.53] and [2.54].

$$A_n = -C_n \quad [2.51]$$

$$B_n = -D_n \quad [2.52]$$

$$\frac{A_n}{B_n} = -\frac{\cosh(k_n l) + \cos(k_n l)}{\sinh(k_n l) + \sin(k_n l)} = \delta_{cant} \quad [2.53]$$

$$\frac{A_n}{B_n} = -\frac{\sinh(k_n l) - \sin(k_n l)}{\cosh(k_n l) + \cos(k_n l)} \quad [2.54]$$

Combining the relation [2.53] with [2.54] it is possible to obtain the transcendental equation of [2.55] which is graphically computed in the Figure 8 to

obtain the possible solutions which corresponds to the $k_n \cdot l$ constant directly related with the natural modes of the beam.

$$\cosh(k_n l) + \cos(k_n l) = -1 \quad [2.55]$$

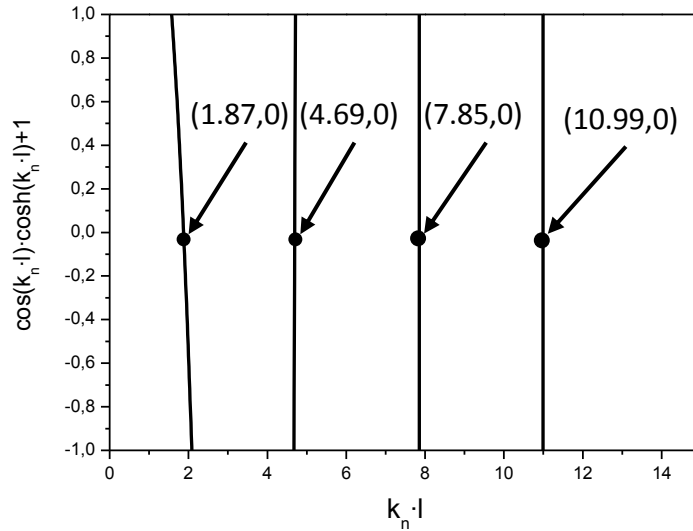


Figure 8.- Possible solutions for $k_n \cdot l$ constants in cantilever structure.

Finally, the deflection profile [2.56] is obtained from [2.50] after substituting the constants and using the definition of δ_{cant} given in equation [2.53]. This function is represented in the Figure 9 for the first three modes where the applicable $k_n \cdot l$ constants are respectively 1.87, 4.69 and 7.85.

$$u(x) = \cos(k_n x) - \cosh(k_n x) + \delta_{cant} (\sin(k_n x) - \sinh(k_n x)) \quad [2.56]$$

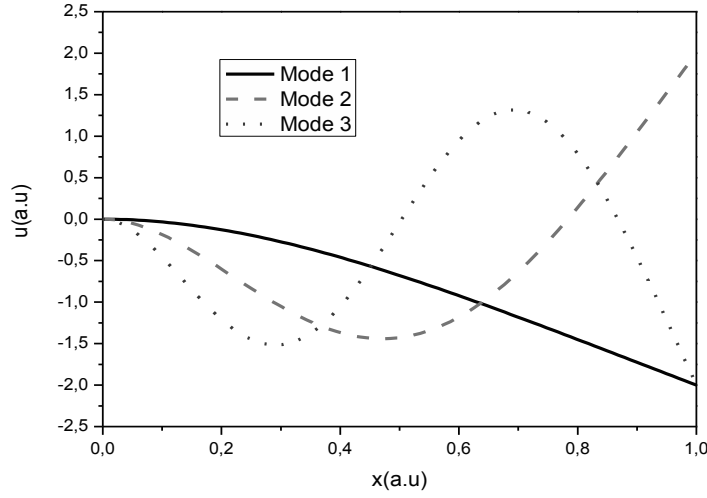


Figure 9.- Deflection profile for a cantilever in the first three resonant modes.

In the case of the CCB the development to get the deflection profile is similar, from the equation [2.45] the boundary conditions of zero displacement and slope at the two fixed ends, $u(0) = 0$, $\frac{\partial u(0)}{\partial x} = 0$, $u(l) = 0$ and $\frac{\partial u(l)}{\partial x} = 0$ impose that the constants in the case of the CCB are [2.57], [2.58], [2.59] and [2.60].

$$A_n = -C_n \quad [2.57]$$

$$B_n = -D_n \quad [2.58]$$

$$\frac{A_n}{B_n} = -\frac{\sin(k_n l) + \sinh(k_n l)}{\cos(k_n l) - \cosh(k_n l)} = \delta_{CCB} \quad [2.59]$$

$$\frac{A_n}{B_n} = -\frac{\cos(k_n l) - \cosh(k_n l)}{\sin(k_n l) - \sinh(k_n l)} \quad [2.60]$$

Equating [2.59] to [2.60] the transcendental function of [2.61] is obtained where different values than the ones found for $k_n \cdot l$ constants for the cantilever are extracted from the graph of Figure 10.

$$\cosh(k_n l) + \cos(k_n l) = 1 \quad [2.61]$$

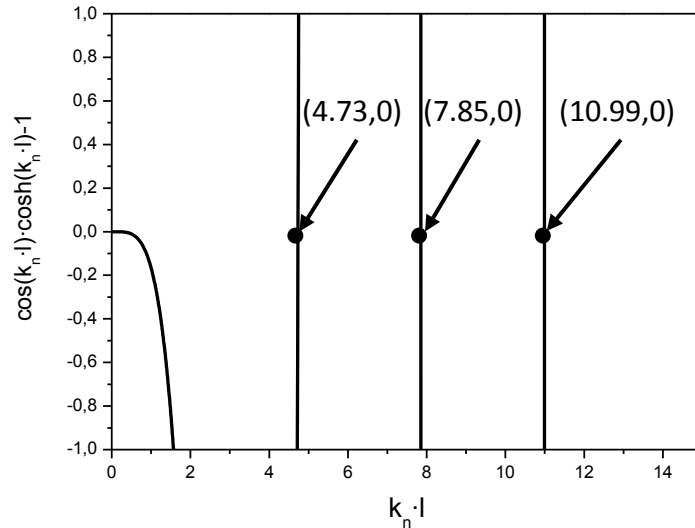


Figure 10.- Possible solutions for $k_n \cdot l$ constants in CCB structure.

At last, the deflection profile for the CCB of [2.62] is found from [2.50] after substituting the constants and using the definition of δ_{CCB} given in equation [2.59]. The deflection profile is represented in the Figure 11 for the first three modes where in the CCB case the $k_n \cdot l$ constants are respectively 4.73, 7.85 and 10.99.

$$u(x) = \cos(k_n x) - \cosh(k_n x) + \delta_{CCB}(\sin(k_n x) - \sinh(k_n x)) \quad [2.62]$$

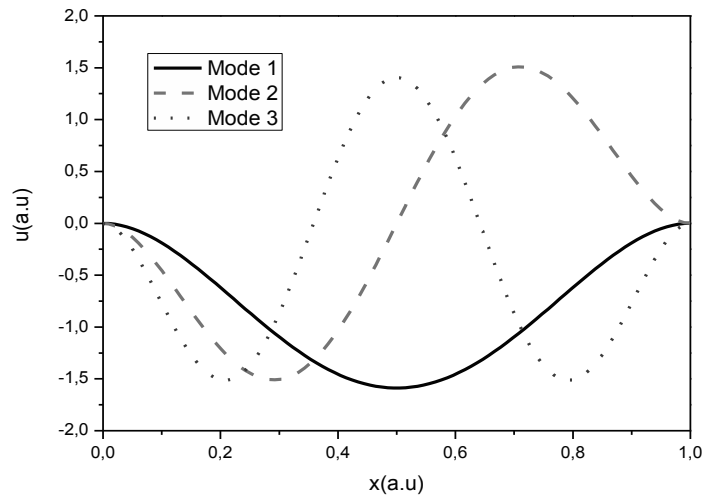


Figure 11.- Deflection profile for a CCB in the first three resonant modes.

2.4. DAMPING

Until now it has been considered that the motion of the MEMS is not restricted by losses of any kind. In this section the different kinds of energy losses and the concepts of damping coefficient and quality factor will be explained. The damping force is proportional to the mass velocity and could be integrated in the motion equation by means of the term γ_{tot} which corresponds to the sum of all damping sources. The quality factor Q is frequency dependant ω_0 and is defined on [2.63], where m_{eff} represents the effective mass of the device which it will be defined on the next section.

$$Q = \frac{\omega_0 m_{eff}}{\gamma_{tot}} \quad [2.63]$$

The first damping mechanism is related with the intrinsic material losses due to the internal friction of the movement at the atomic level that results in heat generation which limits the maximum obtainable quality factor. The material damping is function of temperature, vibration frequency and the vibration mode. At room temperature the viscous damping model [Kaa09] is appropriate for most low loss materials. The equation [2.64] gives the equivalent quality factor from material losses where μ_γ is the viscosity factor of the material and ω_0 the resonance frequency of the structure. In order to compare the intrinsic quality factor of a material independently from the frequency the f·Q product can be computed as a figure of merit. The Table 1 shows the main parameters for different materials and their correspondingly f·Q product. From this table it can be seen that lithium niobate and silicon are the materials which present the lowest material losses. Whilst lithium niobate is rare and cannot be used in standard microelectronic processes, silicon provides good mechanical properties, is the second most abundant element in the Earth's crust and it is suitable for all microelectronic processes.

$$Q_i = \frac{E}{\mu_\gamma \cdot \omega_0} \quad [2.64]$$

Material	E (GPa)	ρ (kg/m ³)	μ_γ (Ns/m ²)	f·Q
Aluminum	11	2700	1.0	1800
Epoxy	9	1210	2300	0.6
Fused quartz	78	2200	3.1	4100
Gold	210	19700	78	420
Lithium niobate	390	7300	0.7	91000
PVC	8	1380	490	2.6
Silicon	160	2320	2.5	10000

Table 1.- Some different material characteristics related with intrinsic damping losses, [Kaa09].

Other important source of energy losses is the anchoring of the device. Whilst in most of the cases the consideration that the anchor is fixed, is enough to obtain the equations of the movement, in a realistic case there are a small portion of the vibration energy that leaks into the support. These losses depend on the location and geometry of the support relative to the vibration mode shape of the device. The lowest quality factors related with the anchors losses are obtained with CCB resonators because their mode shape exerts significant stress in the anchors. Using symmetric geometries such as double ended tuning fork (DETF) in the vibration plane for the movable structure results in net force which is zero at the anchors minimizing the losses due to the anchoring. Modeling this source of losses is extremely difficult so in many cases FEM simulation is more convenient. One approach to estimate the anchor support losses for a cantilever is given by [2.65] from [Hos95] where l is the beam length and t their thickness. It has been considered that the support is an infinitely large elastic body where the stress and strain launches longitudinal and transverse sound waves that propagate into the support.

$$Q_{anchor} \approx 2.17 \left(\frac{l}{t}\right)^3 \quad [2.65]$$

The last contribution to the quality factor discussed in this section is the air damping which is the most important one in air pressure conditions. At the micro-scale the effect of a gas or a liquid where the vibrating body is immersed is extremely important because the size of the particles presents in the fluid limits the free fall velocity of the device and also the losses of the system in this case a gas behaves as a fluid and the quality factor obtained is in the “viscous regime”. When the pressure of the gas drops down the individual molecular collisions dominate the quality factor which is in the “molecular regime”. Lowering more the pressure of the gas the quality factor reaches the “intrinsic regime” which is dominated by the other losses sources explained above. The Figure 12 shows a graph extracted from [New68] which details the well known effect of the pressure of air in the quality factor of a MEMS resonator.

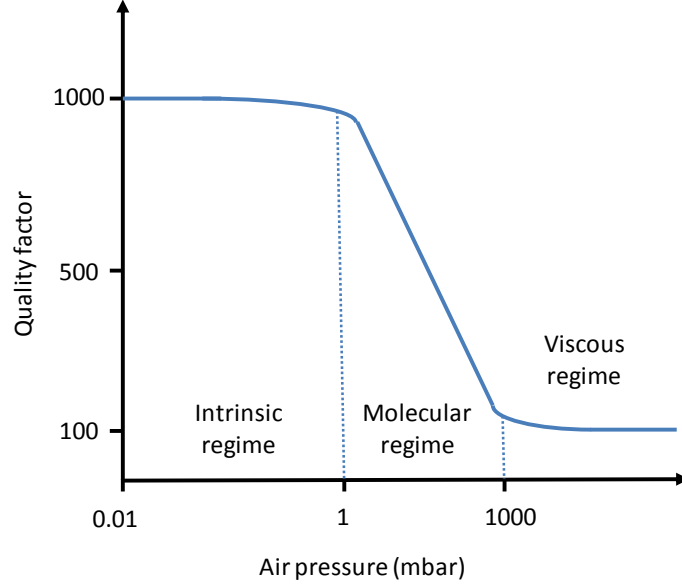


Figure 12.- Effect of the fluid pressure to the quality factor of a micro mechanical resonator. Graph extracted from [New68] with common values from [Ver08b].

Although the gas flow analysis is a challenging problem even at macro-scale, there are some models applicable at micro-scale under certain conditions. First of all the concepts of mean free path λ and Knudsen number K_n must be defined. The mean free path is the average distance that the gas molecules travel before colliding with another molecule and it is given by equation [2.66], where R is the universal gas constant, T is the gas temperature, d_g is the effective diameter of gas molecules, N_A is the Avogadro's number and p is the gas pressure.

$$\lambda = \frac{RT}{\sqrt{2}\pi d_g^2 N_A p} \quad [2.66]$$

The Knudsen number corresponds to the ratio of mean free path to critical device dimensions (commonly the gap) d_c and is given by [2.67]. There are three regimes of gas flow: continuum region ($K_n < 0.1$), transition region ($0.1 < K_n < 10$) and molecular region ($K_n > 10$). Most of MEMS devices work on the transition regime where the molecular effects start to be significant and the continuum models are still valid with some modifications.

$$K_n = \frac{\lambda}{d_c} \quad [2.67]$$

The two major effects of molecular gas collisions are the squeeze film damping and the lateral damping. The first one governs the gas flow between two surfaces moving toward each other [Gri66], [Ble83]. One way to model it semi-empirically in

narrow gaps is to introduce the effective viscosity μ_{eff} defined on [2.68] where in continuum gas flow region the effective viscosity became the standard viscosity μ . The effective viscosity is employed to compute the squeeze number ξ which depends upon the device topology. For a plate with width w lower than the length l , a gap g and a resonance frequency ω , the squeeze number ξ is given by [2.69]. Finally, the squeeze film damping coefficient is extracted from [2.70] where m and n are odd integers, [Ble83, Vei95]

$$\mu_{eff} = \frac{\mu}{1 + 9.638K_n^{1.159}} \quad [2.68]$$

$$\xi = \frac{12\mu_{eff}w^2}{pg^2}\omega \quad [2.69]$$

$$\gamma_{gas_squeeze} = \frac{64\xi pA}{\pi^6 g\omega} \sum_{m,n \text{ odd}} \frac{m^2 + c^2n^2}{(mn)^2 \left[(m^2 + c^2n^2)^2 + \left(\frac{\xi}{\pi^2} \right)^2 \right]} \quad [2.70]$$

The squeeze film damping effect is strongly reduced in laterally moving structures because the gas below the device is dragged with the movement. In such case the lateral damping effect produced by the shear force between the plate and the substrate prevails. The effective viscosity and damping coefficient for a plate with an area A and a distance with the substrate d are depicted on [2.71] and [2.72], [Vei01] where it is assumed that the gas velocity distribution is linear.

$$\mu_{eff} = \frac{\mu}{1 + 2K_n} \quad [2.71]$$

$$\gamma_{gas_lateral} = \frac{\mu_{eff}A}{d} \quad [2.72]$$

Most of the models presented are based on empiric measurements and they are applicable in only some specific cases, for more accurate results is convenient to employ FEM simulators instead of analytic equations.

Another possible source of energy loss in long and thin microstructures is Thermo Elastic Damping (TED). Thermoelastic energy dissipation is caused by irreversible heat flows across the thickness of the resonator as it vibrates. This mechanism of energy loss becomes less relevant as thickness is decreased, being intrinsic and anchoring losses the main mechanism that limit the quality factor in vacuum. The quality factor for TED for a cantilever can be expressed by means of equation [2.73] from [Sri02]. The Q_{intra} is referred to the damping associated with the rapid thermal relaxation due to intracrystalline heat conduction. The Zener term Q_z corresponds to the special case where the grain size is small and there is an estimated

maximum error in the temperature proportional to the grain size, relative to the maximum temperature change, incurred by approximating a smooth continuous curve by stepped temperature gradient. Finally, the intercrystalline damping Q_{inter} is related with the lateral and transverse strains of the grain boundaries which are constrained to be equal to maintain continuity. This constraint leads to additional dilatational stress and temperature inhomogeneities on the scale of the average grain size.

$$\frac{1}{Q_{TED}} = \frac{1}{Q_{intra}} + \frac{1}{Q_z} + \frac{1}{Q_{inter}} \quad [2.73]$$

The computation of the total quality factor is computed in [2.74] where only the main energy losses considered important in this section are shown.

$$\frac{1}{Q_t} = \frac{1}{Q_i} + \frac{1}{Q_{anchor}} + \frac{1}{Q_{gas_squeeze}} + \frac{1}{Q_{gas_lateral}} + \frac{1}{Q_{TED}} \quad [2.74]$$

2.5. MECHANICAL MODELLING SPRING-MASS LUMPED MODEL

Assuming the linear behavior formulated by Hooke's law most of the mechanical structures used in MEMS could be described in terms of mass-spring modeling through the Newton's second law, equation [2.75].

$$F = ma = m_{eff} \frac{\partial^2 u(x)}{\partial t^2} = -k \cdot u(x) \rightarrow m_{eff} \frac{\partial^2 u(x)}{\partial t^2} + k \cdot u(x) = 0 \quad [2.75]$$

The model assumes that all the mass is concentrated in a certain point and there is an equivalent of the spring constant and an effective mass of all the structure, Figure 13.

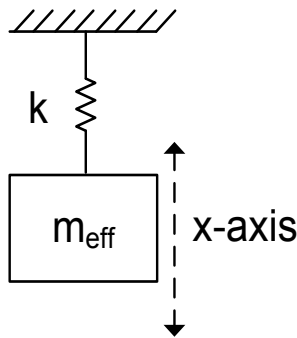


Figure 13.- Basic spring-mass model for mechanical systems.

The spring constant is given by the expressions found on section 2.2 (equation [2.29] for the cantilever and equation [2.36] for the CCB) and the effective mass is computed through the resonance frequency found on section 2.3 (equation [2.48]) which

depends on the resonance mode and their modal shape. Employing the definition of the natural resonance frequency of the [2.76], the effective mass is calculated for the cantilever [2.77] and CCB [2.78] structures respectively.

$$\omega_0 = \sqrt{\frac{k}{m_{eff}}} \quad [2.76]$$

$$m_{eff_cant} = \frac{3l\rho}{(k_n l)^4} \left(\frac{t}{w}\right)^3 \quad [2.77]$$

$$m_{eff_CCB} = \frac{192twl\rho}{(k_n l)^4} \quad [2.78]$$

The general solution of the differential equation of [2.75] is the sine wave depicted on the [2.79] which leads to the harmonic oscillator concept applicable to different physic systems (mechanics, electronics, pneumatics...).

$$u(t) = U(x)\sin(\omega t + \phi) \quad [2.79]$$

The Hooke's law allows the simplification of springs which are in series or in parallel as is shown in Figure 14, equation [2.80] for springs in parallel and equation [2.81] for springs in series.

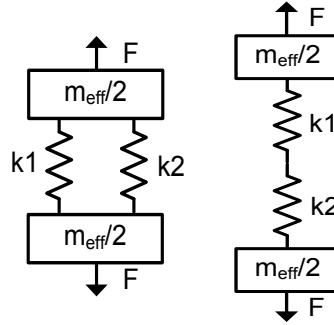


Figure 14.- Springs in parallel and in series.

$$F_{parallel} = k_1 u(x) + k_2 u(x) \rightarrow k_{tot} = k_1 + k_2 \quad [2.80]$$

$$F_{series} = k_1 u(x_1) = k_2 u(x_2) \rightarrow x_{tot} = x_1 + x_2 = \left(\frac{1}{k_1} + \frac{1}{k_2}\right) F \rightarrow \quad [2.81]$$

$$\frac{1}{k_{tot}} = \frac{1}{k_1} + \frac{1}{k_2}$$

Adding a damping term γ_{tot} to the equation [2.75] which represents the energy losses of the system and a harmonic force of amplitude F and frequency ω , the dynamic

motion equation of [2.82] is obtained. The Figure 15 shows the mechanical model which is called forced harmonic oscillator with damping.

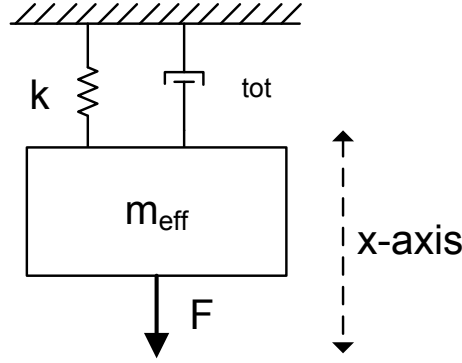


Figure 15.- Spring-mass system model with damping and actuation force.

$$m_{eff} \frac{\partial^2 u(x)}{\partial t^2} + \gamma_{tot} \frac{\partial u(x)}{\partial t} + k \cdot u(x) = F e^{j\omega t} \quad [2.82]$$

To solve the second order differential equation of the motion it can be assumed that the solution for x is a complex exponential which depend upon time and frequency, and calculate the partial derivatives as is shown in equation [2.83] and equation [2.84].

$$m_{eff} \frac{\partial^2}{\partial t^2} (u(x) e^{j\omega t}) + \gamma_{tot} \frac{\partial}{\partial t} (u(x)) + k \cdot u(x) e^{j\omega t} = F e^{j\omega t} \quad [2.83]$$

$$-\omega^2 m_{eff} (u(x) e^{j\omega t}) + j\omega \cdot \gamma_{tot} (u(x) e^{j\omega t}) + k \cdot u(x) e^{j\omega t} = F e^{j\omega t} \rightarrow \quad [2.84]$$

$$u(x) = \frac{F}{k - \omega^2 m_{eff} + j\omega \cdot \gamma_{tot}}$$

The modulus of the equation [2.84] gives the maximum displacement in function of the frequency which is maximum at the resonant frequency of the device. From the definition of the quality factor of [2.63] the equation [2.84] transforms to the equation [2.85] taking their modulus. The Figure 16 represents a frequency sweep of the modulus and phase of the displacement from the equation [2.84] for a first mode of a cantilever and a CCB made of polysilicon (young modulus of 160GPa and 2330kg/m³) of 13 μ m of length, 350nm of width, 282nm of thickness, a force of 1nN and a quality factor range from 1 to 10.

$$|u(x)| = \frac{F/m_{eff}}{\sqrt{(\omega^2 - \omega_0^2)^2 + \left(\frac{\omega \cdot \omega_0}{Q}\right)^2}} \quad [2.85]$$

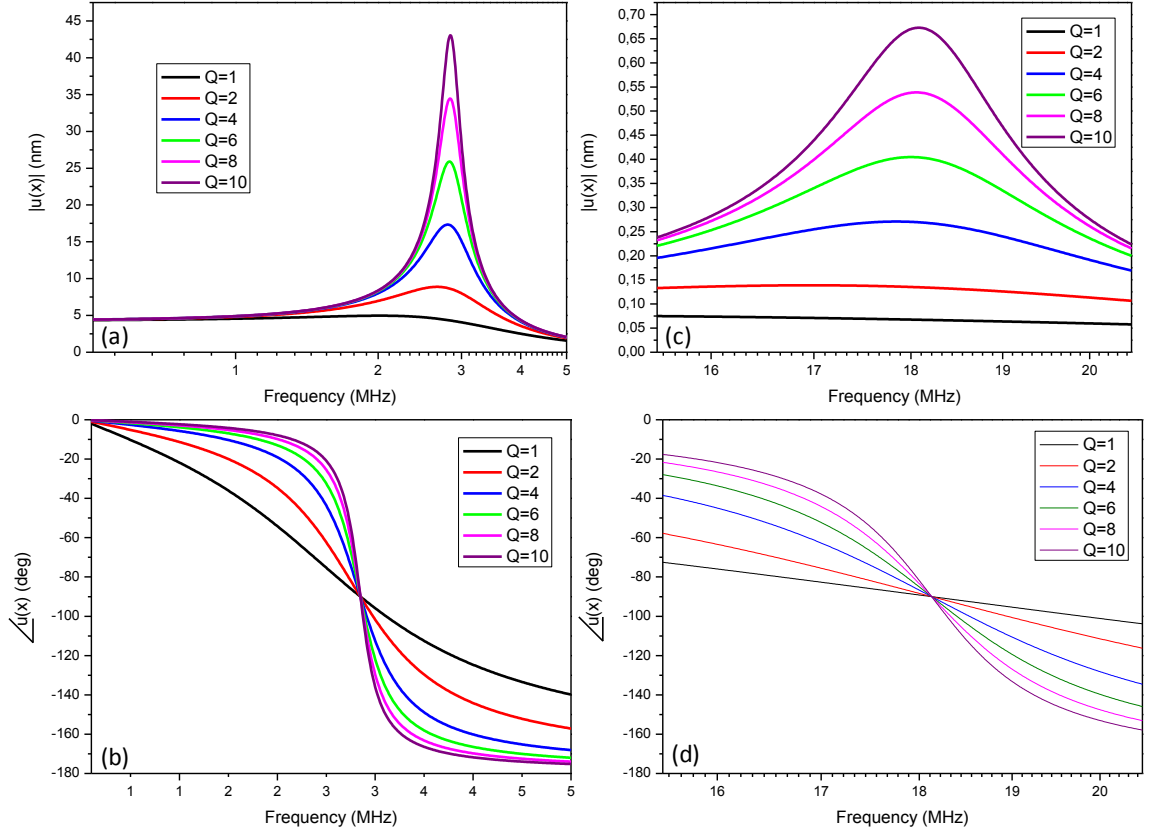


Figure 16.- Magnitude and phase of the maximum displacement of MEMS in function of the frequency with increasingly quality factor: (a,b) displacement for a cantilever at their free end ($x=l$); (c,d) displacement of a CCB at the middle of the beam ($x=l/2$).

At resonance the maximum displacement is given by [2.86] for a known applied force. Increasing the quality factor for a given resonator will represent that the same amount of displacement will be reached by a smaller force reducing the required power to actuate it.

$$|u(x)|_{max} = \frac{F \cdot Q}{m_{eff} \cdot \omega_0^2} = \frac{F \cdot Q}{k} \quad [2.86]$$

The frequency selectivity provided by the quality factor represents that the mechanical energy is concentrated at a certain frequency or is spread into a certain bandwidth. The computation of quality factor from the frequency response of a MEMS device could be done by means of the magnitude or the phase [2.87]. From the magnitude the relation between the resonance frequency f_0 and the bandwidth BW_{3dB} at -3dB from the maximum define the quality factor. From the phase the slope of the graph $\delta\phi/\delta f$ near the resonance frequency f_0 is employed to compute their quality factor.

$$Q = \frac{f_0}{BW_{3db}} = f_0 \frac{\pi}{360} \frac{\delta\phi}{\delta f} \quad [2.87]$$

2.1.1 Electrostatic Excitation

As has been detailed in the previous chapter there are several different ways to actuate a micromechanical device: electrostatic, magnetic, piezoelectric, thermal, etc. This section will focus on electrostatic transduction which is the method chosen due to their inherent benefits for a monolithical integration.

2.1.1.1 Electrostatic Excitation

The basic principle of operation for an electrostatic excitation is the force exerted by an electric field between two conductive surfaces separated by a dielectric. If the electrical field is time varying the corresponding force is time varying also so if the frequency of the excitation is close to a mode vibration frequency of the mechanical device the electrical signal could excite the resonator. The most simple electrostatic actuation scheme is composed by a fixed electrode and the movable structure. Including another electrode on the other side of the device will decrease the parasitic signal obtained by means of the capacitive read-out which will be explained in subsequent chapters. So the analysis of the electrostatic actuation is focused to the two electrodes configuration as is shown on the Figure 17 where a CCB with two electrodes is represented. On the figure there are represented the two variable capacitors that will exert the forces into the system, two different signals V_1 and V_2 are added to elaborate a more detailed analysis which will be useful in following chapters. The grounding of one electrode represents the reading path where the output current will flow and it will be discussed afterwards.

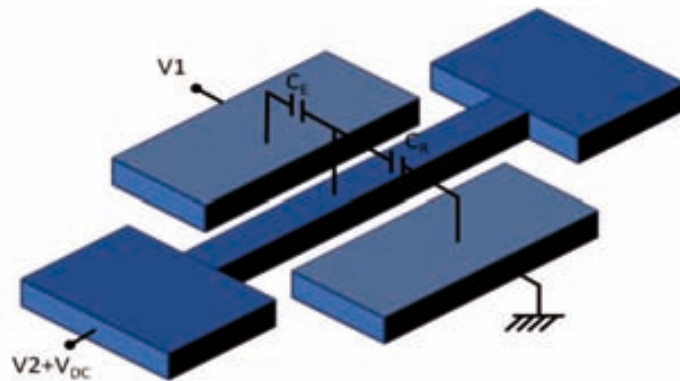


Figure 17.- CCB with two electrodes, two AC signals and one DC signal.

Considering the electric potential in each of the electrodes the equivalent potentials on the capacitors will be the equation [2.88] for the left electrode and the equation [2.89] for the right electrode.

$$V_E = V1 - V2 - V_{DC} \quad [2.88]$$

$$V_R = V2 + V_{DC} \quad [2.89]$$

To take into account that the capacitance is dependent with the position of the beam the equations [2.90] and [2.91] are used for each capacitor where the value g corresponds to the gap between the electrodes and the beam and this one is considered symmetric for each side. The coupling area A is given by the product of the coupling length and the layer thickness ($A = l_{electr} \cdot t$) and ε represents the dielectric constant.

$$C_E = \frac{\varepsilon \cdot A}{g + x} \quad [2.90]$$

$$C_R = \frac{\varepsilon \cdot A}{g - x} \quad [2.91]$$

The force exerted by the capacitors is obtained taking the derivative of the energy stored in the capacitors in function of the position of the beam as it is shown in the [2.92].

$$F_x = -\frac{dE}{dx} = -\frac{d}{dx} \cdot \frac{1}{2} (C_E \cdot V_E^2 + C_R \cdot V_R^2) \quad [2.92]$$

Developing the equation [2.92] using the potentials defined by [2.88] and [2.89] the force in function of the applied signals is obtained:

$$F_x = -\frac{1}{2} \left[\frac{dC_E}{dx} V1^2 + \left(\frac{dC_E}{dx} + \frac{dC_R}{dx} \right) V2^2 + \left(\frac{dC_E}{dx} + \frac{dC_R}{dx} \right) V_{DC}^2 + \left(\frac{dC_R}{dx} \mp \frac{dC_E}{dx} \right) 2V2 \cdot V_{DC} - \frac{dC_E}{dx} 2V1 \cdot V2 \pm \frac{dC_E}{dx} 2V1 \cdot V_{DC} \right] \quad [2.93]$$

The applied force has several terms which depend upon the excitation signals. The development of the force in function of the two AC signals is done because the term where the two AC signals are multiplied will be used in mixing measurements which will be explained in following chapters. Assuming in this case that the signal $V2=0$ and the signal $V1=V_{AC1} \cdot \sin(\omega_0 t)$ is a sinusoidal with a frequency equal to the resonance frequency of the MEMS resonator ω_0 , the equation [2.93] is equal to the equation [2.94] where the only term that will induce vibration at the resonance frequency is the last one.¹⁹

¹⁹ Note that $V1^2 = (A_1 \sin(\omega_0 t))^2 = \frac{A_1^2}{2} (1 - \cos(2\omega_0 t))$ and the second term has no AC signal.

$$F_x = -\frac{1}{2} \left[\frac{dC_E}{dx} V_1^2 + \left(\frac{dC_E}{dx} + \frac{dC_R}{dx} \right) V_{DC}^2 + \frac{dC_E}{dx} 2V_1 \cdot V_{DC} \right] \quad [2.94]$$

Finally, substituting the derivatives by the first Taylor expansion term and considering that there will be small displacements (the vibration amplitude x will be much lower than the defined gap g) the equation [2.90] and [2.91] could be expressed as the equation [2.95] and [2.96].

$$\frac{dC_E}{dx} = -\frac{\varepsilon \cdot A}{g^2} \left(1 - 2\frac{x}{g} \right) = -\frac{C_0}{g} \left(1 - 2\frac{x}{g} \right) \quad [2.95]$$

$$\frac{dC_R}{dx} = \frac{\varepsilon \cdot A}{g^2} \left(1 + 2\frac{x}{g} \right) = \frac{C_0}{g} \left(1 + 2\frac{x}{g} \right) \quad [2.96]$$

Taking the third term of equation [2.94] and substituting the capacitor derivatives by [2.95] and [2.96] the equation [2.97] is found which gives the exerted force in function of the position of the beam and the applied AC and DC signals. Assuming that there will be small displacements ($x \ll g$) the second term given by the resonator displacement will be much lower than the unit term.

$$F_x = \frac{1}{2} \left[\frac{C_0}{g} \left(1 - 2\frac{x}{g} \right) 2V_1 \cdot V_{DC} \right] \cong \frac{C_0}{g} V_{DC} V_{AC1} \sin(\omega_0 t) \quad [2.97]$$

From the above expression the eletromechanical excitation coupling factor which relates the electrical excitation signal with the force exerted is quantified on [2.98].

$$\eta_e = \frac{F_x}{V_1} = \frac{C_0}{g} V_{DC} \quad [2.98]$$

2.6.2. ELECTRICAL SPRING SOFTENING

The electrical spring softening effect comes from the linear dependence with the resonator displacement of [2.94] after substituting the Taylor approximations of the capacitor derivatives and rearranging the terms into equation [2.99].

$$F_x = \frac{C_0}{g} \left(\frac{V_1^2}{2} + V_1 \cdot V_{DC} \right) - \frac{C_0 \cdot x}{g^2} (V_1^2 + 2V_{DC}^2 + 2V_1 \cdot V_{DC}) \quad [2.99]$$

Comparing the dependence with the position of the force equivalence with the Hooke's law for electrical stiffness could be obtained taking the derivative of [2.99] respect the position obtaining equation [2.100].

$$k_{el} = \frac{dF_x}{dx} = -\frac{C_0}{g^2} (V_1^2 + 2V_{DC}^2 + 2V_1 \cdot V_{DC}) \quad [2.100]$$

Substituting the signal V_1 by their sinusoidal expression $V_1 = V_{AC1} \sin(\omega t)$ the equation [2.101] is found.

$$k_{el} = \frac{dF_x}{dx} = -\frac{C_0}{g^2} \left[\frac{V_{AC1}^2}{2} (1 - \cos(2\omega t)) + 2V_{DC}^2 + 2V_{AC1} \cdot V_{DC} \sin(\omega t) \right] \quad [2.101]$$

It is remarkable that there are two terms with time dependence but considering the mean values of the voltage components, the electrical elastic constant expression is:

$$|k_{el}| = -\frac{C_0}{g^2} \left[\frac{V_{AC1}^2}{2} + 2V_{DC}^2 \right] \xrightarrow{V_{AC1} \ll V_{DC}} |k_{el}| \cong 2V_{DC}^2 \frac{C_0}{g^2} \quad [2.102]$$

Then, the resulting effective spring constant results in:

$$k_{eff} = k - |k_{el}| \quad [2.103]$$

The resulting resonant frequency taking into account the electrical spring constant is equation [2.104] where it can be seen that applying a constant voltage could be used to tune electrically the natural resonance frequency of the device. The Figure 18 shows a simulation of the effect that an increase on the continuous voltage produce over the frequency response of a cantilever and a CCB structures respectively.

$$\omega = \sqrt{\frac{k_{eff}}{m_{eff}}} = \sqrt{\frac{k - |k_{el}|}{m_{eff}}} = \omega_0 \sqrt{1 - \frac{|k_{el}|}{k}} \cong \omega_0 \left(1 - \frac{1}{2} \frac{C_0}{k g^2} V_{DC}^2 \right) \quad [2.104]$$

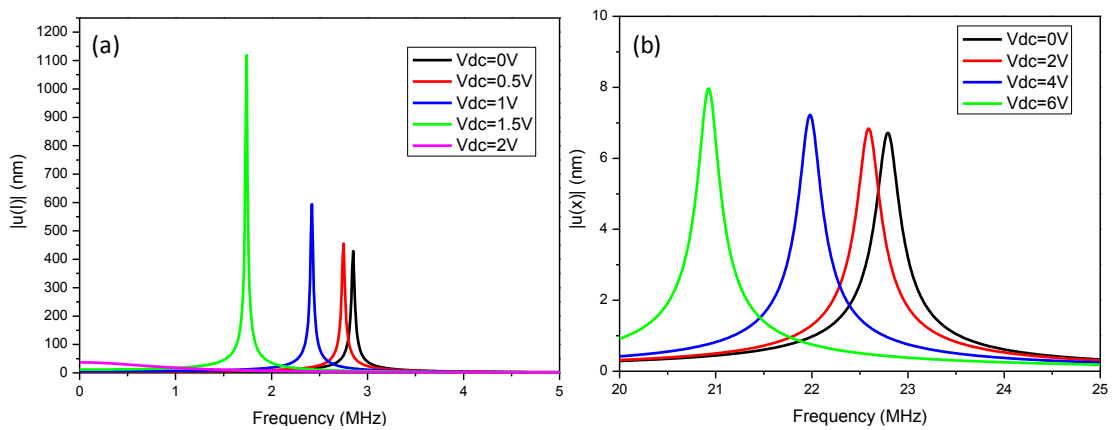


Figure 18.- Electrical spring softening effect for a cantilever (a) and for a CCB (b) respectively.

2.6.3. SNAP-IN VOLTAGE

At this point it has been considered that the actuation voltage has no limits, but actually exist some unstable point between the applied electrical force and the elastic recovering force when the system becomes unstable and the beam will collapse with the electrode. The voltage required to get this point is called the snap-in voltage. Considering one electrode transduction and the beam the total force of the equation [2.98] is obtained.

$$F_t = F_{electrical} + F_{mechanical} = \frac{1}{2} \left(\frac{\varepsilon A}{(g-x)^2} V^2 \right) - k \cdot x \quad [2.105]$$

Equating the equation [2.98] to 0 will give the equilibrium point between the electrical and mechanical forces and allow computing the actuation voltage as a function of plate displacement as it is shown on the equation [2.99].

$$F_t = 0 \rightarrow \frac{1}{2} \left(\frac{\varepsilon A}{(g-x)^2} V^2 \right) - k \cdot x = 0 \xrightarrow{x=x_0} V^2 = k \cdot x_0 \frac{2(g-x_0)^2}{\varepsilon \cdot A} \quad [2.106]$$

The pull-in displacement is calculated from the stability of the equilibrium point deriving the total force in function of the displacement and equating the result to 0, [2.107]. Then the actuation voltage of [2.106] is substituted on [2.107] obtaining [2.108]. Above the displacement point obtained, the stiffness becomes positive and the system is unstable. In the Figure 19 the stiffness dF_t/dx in function of the normalized displacement is represented for a cantilever in dashed line and for a CCB in solid line.

$$\frac{dF_t}{dx} = 0 \rightarrow \frac{\varepsilon A}{(g-x_0)^3} V^2 - k = 0 \quad [2.107]$$

$$\frac{\varepsilon A}{(g-x_0)^3} k \cdot x_0 \frac{2(g-x_0)^2}{\varepsilon \cdot A} - k = 0 \rightarrow \frac{2k \cdot x_0}{g-x_0} = k \rightarrow x_0 = \frac{g}{3} \quad [2.108]$$

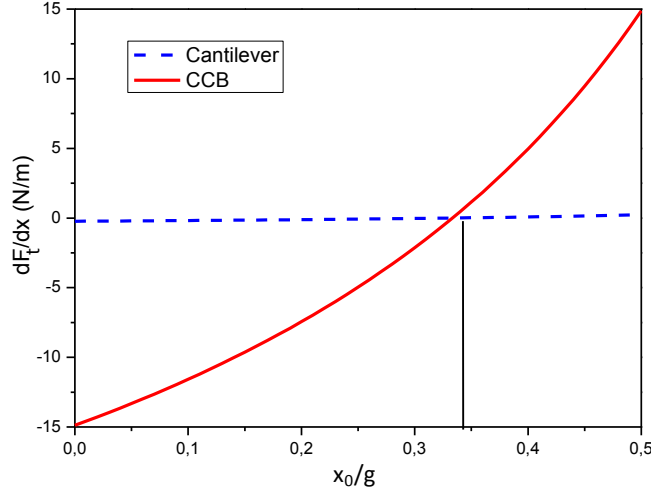


Figure 19.- The stiffness as a function of equilibrium point. The equilibrium point is obtained at $x_0/g=1/3$.

Finally, substituting the pull-in displacement of [2.108] to the voltage equation of [2.106] gives the DC pull-in voltage:

$$V^2 = k \cdot \frac{g}{3} \frac{2 \left(g - \frac{g}{3}\right)^2}{\varepsilon \cdot A} \rightarrow V_{\text{pull-in}} = \sqrt{\frac{8k \cdot g^3}{27\varepsilon \cdot A}} \quad [2.109]$$

Representing the equation [2.106] in the Figure 20 shows the dependence of the DC voltage respect the normalized position. The black lines establish the boundary DC voltage known as the pull-in voltage calculated by [2.109] for the spring constant of the cantilever [2.29] and for the spring constant of the CCB [2.36].

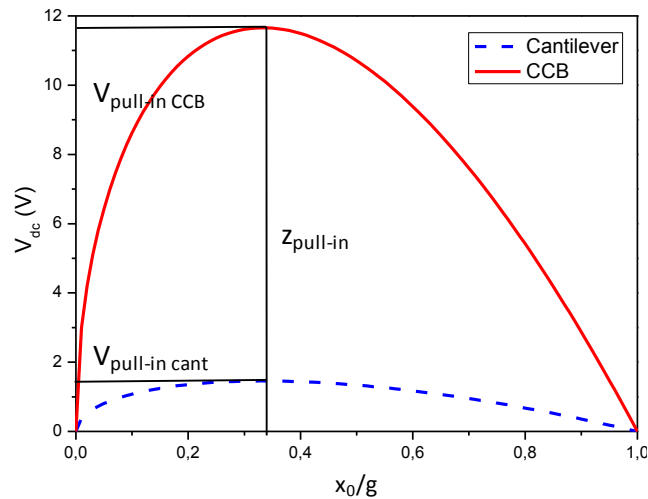


Figure 20.- Relationship between equilibrium plate displacement and V_{DC} for a cantilever and a CCB with a length of $13\mu\text{m}$, a width of 350nm , a thickness of 282nm , a gap of 100nm and a coupling length of $9\mu\text{m}$.

3. CMOS-MEMS PACKAGING FABRICATION

The fabrication of MEMS and integrated circuits has been intrinsically linked from the beginning of the semiconductors industry. Many processes developed in the field of electronics have been borrowed to fabricate MEMS in batch production which allows the reduction of fabrication costs by massive production. The MEMS fabrication has improved some of the techniques of the IC industry and has also developed new processes capable to produce synergies between semiconductors and MEMS industry. Most of these processes are divided into three different steps: etching (KOH, TMAH, RIE, DRIE), lithography (optical, EBL²⁰, based on AFM, FIB patterning) and deposition (PVD²¹, LPCVD²², PECVD²³).

In general MEMS are commonly fabricated separately from the electronic circuits which increase the system size and furthermore their cost. Nowadays there are known different approximations to integrate in the same silicon die both microsystems and electronics [Bal02], [Fed08], [Che12], [Zal10]. In ECAS group there are several contributions reported [Ver06], [Ura07], [Tev08], [Lop09] which are focused in the employment of a standard CMOS technology to fabricate together MEMS and circuits. In this chapter there will be detailed the methods and the processes required to fabricate CMOS-MEMS.

Due to the small size of MEMS resonators they suffer from low quality factors. The quality factor described in the previous chapter could be increased by adopting some optimized mechanical structures or materials and reducing the air pressure of the surroundings of the structure. In this sense the vacuum packaging is a major issue to improve the capabilities of MEMS. In this chapter there are presented some designs of zero level packaging of CMOS-MEMS using the layers available in the CMOS technology.

One of the major topics in the development of this thesis involves the processes and techniques used in microelectronics fabrication for a successful MEMS integration in a CMOS process. In this sense the main objectives of the present chapter consist on develop a vacuum sealing package for CMOS-MEMS resonators to protect the device structure and increase their quality factor. The topics covered in this chapter imply from

²⁰ Electron-beam lithography

²¹ Physical vapor deposition

²² Low pressure chemical vapor deposition

²³ Plasma enhanced chemical vapor deposition

the package design to their fabrication and characterization. In the last section of the chapter it is presented a method based on the knowledge obtained which allow the fabrication of nanochannels applicable in many different fields (chemistry, biology, medicine...).

3.1. APPROACHES FOR CMOS-MEMS INTEGRATION

As it is explained in the introduction chapter there are two main methods to fabricate MEMS: surface micromachining and bulk micromachining. The fabrication approach of surface micromachining require similar processes than the ones used in standard CMOS fabrication whilst employing bulk micromachining imply that additional processes or modifications must be made over the CMOS flow fabrication processes. There are three major ways to integrate micromachining processes with CMOS technology in function of their order in relation of the CMOS sequence: pre-CMOS, intra-CMOS or post-CMOS. The main advantage of pre-CMOS and post-CMOS approaches is that the processes to fabricate MEMS are not restricted to the available layers and materials of CMOS technology unlike intra-CMOS approach which use these layers and their restrictions. However there are also drawbacks over pre-CMOS and post-CMOS approaches: the interconnection between MEMS and CMOS is challenging and the stringent thermal budget for all process steps following standard CMOS technologies excludes high temperature processes for post-CMOS approach. The main feature of intra-CMOS fabrication approach is that the inherent reliability and performance of CMOS processes can be exploited.

3.1.1. PRE-CMOS MICROMACHINING

The fabrication flow begins with the MEMS processes, after that the structures are buried and sealed to protect them from the subsequent CMOS processes. After the microstructures are fabricated and protected the wafer surface is planarized in order to be used as starting material for the next CMOS processes. In this way any kind of CMOS technology may be compatible with this approach with some minor modifications such as the interconnection vias between MEMS and circuitry areas. All of these CMOS-MEMS co integration processes require post-CMOS releasing with wet or dry etching.

One of the first demonstrations of this kind of fabrication approach was developed at Sandia National Laboratories and was called M³EMS (modular, monolithic MEMS) [Smi95], [Bus98]. This consist on built the microstructure with multi-layer polysilicon in a trench previously etched into the bulk silicon wafer with anisotropic wet etchant and after that refilling the trench with LPCVD (low pressure

chemical vapor deposition) silicon oxide and planarizing the wafer with CMP (chemical mechanical planarization). A cross section of the technology is depicted on Figure 49.

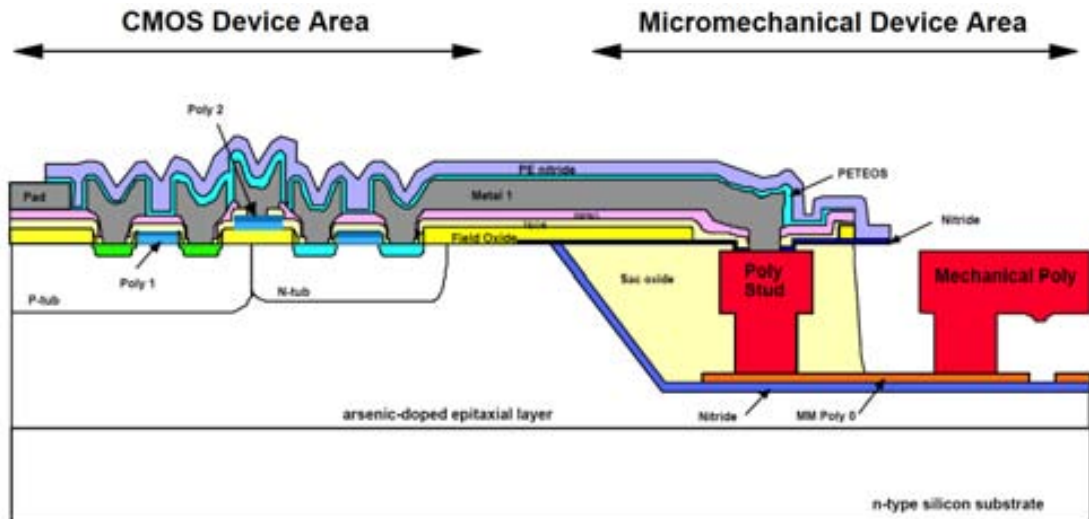


Figure 49.- A cross-sectional schematic of the subsurface, embedded MEMS integrated technology from M^3EMS technology [Smi95].

The Mod MEMS process developed by Analog Devices [Yas03] provides thicker polysilicon structures with sub- μm CMOS circuitry. The polysilicon structures are built on top of the wafer and protected by isolation trenches, then a capping oxide/nitride sandwich is deposited and finally the MEMS regions are passivated by thermal oxidation. After that an epitaxial silicon growth provides the CMOS device area whilst the MEMS devices are surrounded and protected by oxide. The last step is to planarize the surface with CMP and proceed with the CMOS processes.

It is well known that a single crystalline material has better mechanical behavior than a polycrystalline one so some approaches use mechanization of bulk silicon in conjunction of CMOS processes. The SOIMEMS technology developed also by Analog Devices offers thicker structural layers with more advanced BiCMOS technology [Lem99], [Jud04]. This technology begins with the separation with trenches of the MEMS area from the circuitry area, then the trenches are refilled, the surface is planarized and the CMOS process sequence is executed.

Another different pre-CMOS micromachining approach developed by MIT consist on fabricate sealed cavities and use wafer bonding to incorporate them into the CMOS process [Par95], [Par97]. The cavities are etched into a handle wafer and sealed

by silicon fusion bonding the device wafer on to the handle wafer. Then, the surface is planarized to the desired thickness and the CMOS sequence applied.

Recently, a co-integration of NEMS on the front-end processes of CMOS-FDSOI²⁴ technology has been achieved [Oll12]. The process is based on a SOI substrate with top silicon layer and bottom silicon layer of 40nm and 200nm respectively. The NEMS are patterned with EBL and dry plasma etching and the silicon dioxide with a thickness of 145nm between silicon layers is removed with HF-vapor etching. The NEMS device is then oxidized controlling the thickness and the shape of the nanowire and encapsulated in a conformal polysilicon layer. Before proceed with the FEOL²⁵ processes a 200nm thick HTO²⁶ layer is deposited to protect the encapsulated device. After the CMOS flow which includes the interconnection of NEMS and CMOS circuits the releasing is performed in two steps, the HTO layer is removed by means of anisotropic etching and then the polysilicon which surrounds and protects the NEMS device is removed with selective isotropic chemical etching. This approach is able to reach NEMS thickness of 25-40nm, widths of 40-100nm, gaps of 60-180nm and lengths of a few microns, Figure 50.

²⁴ CMOS fully depleted SOI

²⁵ Front end of line

²⁶ High thermal oxide

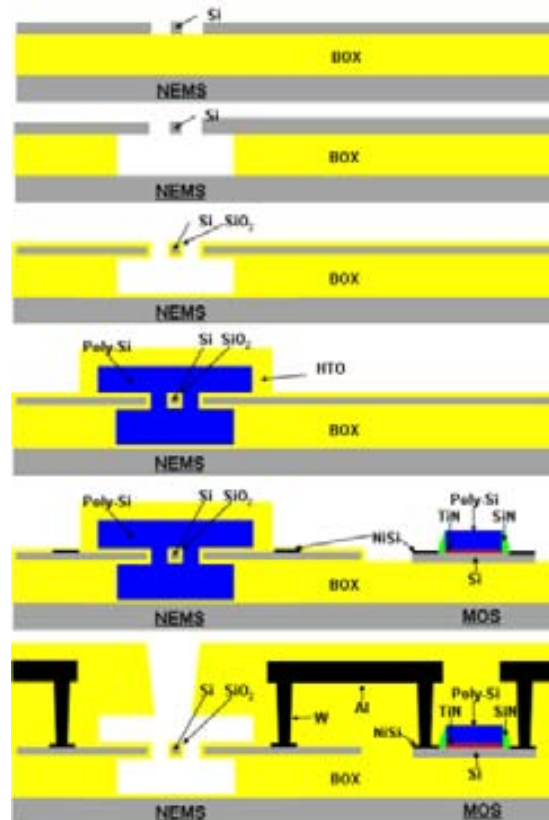


Figure 50.- Schematic of the process flow for single-crystal NEMS co-integration with CMOS-FDSOI technology, [Oll12].

3.1.2. INTRA-CMOS MICROMACHINING

This approach consists on fabricate the microstructures between the FEOL and BEOL²⁷ processes of the CMOS sequence. Actually this fabrication sequence ensures process compatibility with the polysilicon deposition and anneals (limited to non affect the doping profiles of the FEOL processes).

Infineon Technologies employs the standard polysilicon capacitor module of a 0.8 μm BiCMOS process as the structural layer of MEMS, [Sch98]. Before the back-end processes a single micromachining step is inserted in the whole process flow. A doped well is used as lower electrode; the field oxide serves as sacrificial layer and the capacitor polysilicon as structural layer and top electrode. The devices are released and sealed in low pressure conditions and the regular BiCMOS back-end processes are continued.

²⁷ Back end of line

Another intra-CMOS approach proposed by [Fed96] employs stacks of aluminum and silicon dioxide using HP 0.8 μm three-metal n-well CMOS technology, *Figure 51*. The top metal layer is used as the etch-resistant mask which protects the CMOS circuits from the anisotropic etching with RIE that defines the laminated metal/oxide structures. Finally an isotropic silicon dry etching is performed to release the structural stacks.

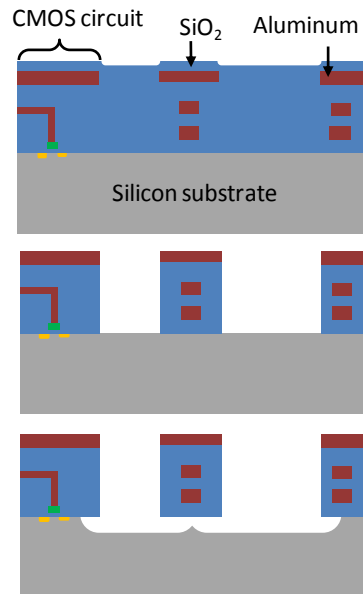


Figure 51.- Stacked via process to define CMOS-MEMS with metal layer protection, anisotropic silicon dioxide etching and isotropic silicon etching to release the structure, [Fed96].

Analog Devices inserts a micromachining module between the front-end and the back-end of the BiCMOS process flow [Cor93] which is based on: LPCVD of nitride and BPSG (borophosphosilicate) to protect the circuitry area, LPCVD nitride layer as etch-stop during the sensor release, sacrificial oxide, polysilicon deposition, doping and annealing of the polysilicon with phosphorus implantation. After removing the sacrificial oxide from the circuitry areas the FEOL processes are resumed. This approach is employed to fabricate integrated gyroscopes [Gee02] with the same process that is used to produce tens of millions of single-chip integrated airbag accelerometers.

Our group approaches are based on the use of conducting layers (metals or polysilicon) as structural layers, [Ver06, Lop09]. The dielectric layers patterning definition (vias and pad) are smartly placed in order to let open the top passivation layer and reduce the amount of silicon dioxide. After the CMOS process flow, a single mask-less wet etching process is performed to release the mechanical structures from their silicon dioxide surroundings. This method employed in the fabrication of MEMS is the

approach which our group is focused on that allows a minimization of the number of additional steps required and exploits the feature size of the CMOS technology used.

Baolab Microsystems [Baolab] released on 2010 NanoEMS™ technology which propose the co-integration of MEMS structures using standard mask techniques on the BEOL metal layers. The inter-metal dielectric is then etched away through the pad openings in the passivation layer using dry etching based on HF. The etching uses equipment that is already available for volume production and takes less than an hour, which is insignificant compared to the overall production time. The holes are then sealed and the chip packaged as required. Employing this technology Baolab Microsystems fabricates a CMOS 3D Compass which includes the MEMS sensor, analog and digital electronics with low power consumption (2mW) and good resolution (0.3μT).

Lately, another composite stack approach in TSMC 0.35μm two polysilicon and four metals CMOS technology was described, [Che12]. Defining the structures in the metal layers and employing the intermetal vias as the stack walls it is capable to obtain thicker structures with embedded silicon dioxide. Combining the negative and positive temperature compensation coefficients of aluminum and silicon dioxide respectively it is capable to obtain MEMS devices with low frequency drift due to temperature variations, Figure 52.

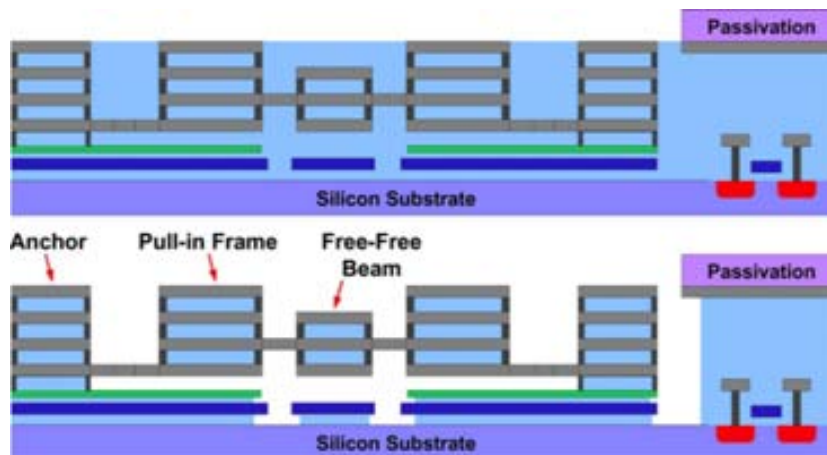


Figure 52.- Metal-SiO₂ composite resonator with passive temperature compensation capability, [Che12].

3.1.3. POST-CMOS MICROMACHINING

This kind of approach probably provides the higher compatibility with standard CMOS processes than the other two approaches because the fabrication of MEMS is

placed at the end of the BEOL processes. So the CMOS processes are not altered and any foundry could provide them whilst the MEMS are fabricated in specific laboratories. The main problem of this approach is the CMOS layers itself as they cannot endure higher temperatures than 450°C excluding high-temperature deposition (for example LPCVD) and annealing steps. However PECVD, sputtering, electroplating and most wet and dry micromachining processes are compatible with the post-CMOS approach.

Texas Instruments has developed a DMD on top of a CMOS SRAM cell using low-temperature processes [VanK98]. The circuitry is fabricated in 0.8µm double-metal CMOS process and the final dielectric is planarized using CMP and vias are integrated for interconnecting the mirror with the underlying circuitry. The mirror structure requires six photolithographic steps to define four metal layers and two sacrificial resist layers. The aluminium layers are sputter-deposited and are used to fabricate the yoke address electrodes and the bias/reset bus, the torsional hinges, the mirror address electrodes, yoke and hinge support posts and the mirror, Figure 53. The releasing is done by etching the polymer sacrificial layers in a plasma etcher. Finally, a coating is applied to prevent stiction between the micromirrors and the landing pads.

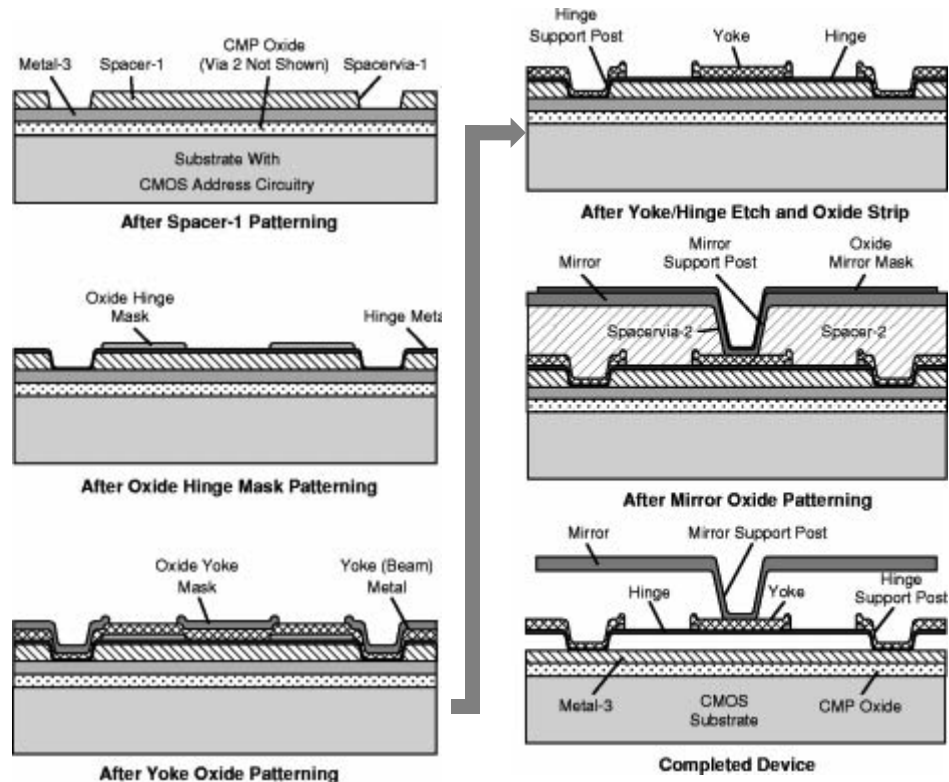


Figure 53.- DMD superstructure process flow developed by Texas Instruments, [VanK98].

Rather than depositing additional layers on the CMOS substrate the CMOS layers or the substrate itself could be employed as MEMS structural layers with micromachining techniques. An example of this approach is a mass-sensitive nanocantilever [Dav03], [Ver05] fabricated into a nanoarea, Figure 54. During the CMOS sequence a rectangular area is defined with the two polysilicon layers. After that the passivation layer is opened and the nanoarea is exposed to the following aluminum deposition. This aluminum is used as a mask through laser lithography which pattern is transferred to the gate polysilicon with dry etching. Finally the structure is released by locally removing the field oxide using buffered etching solution. With this approach the thickness of 600nm is given by the CMOS process. However the post CMOS patterning with laser gives the final resolution of 700nm for the definition of the width and the gap which after the fabrication are of 840nm and 1.3 μ m respectively.

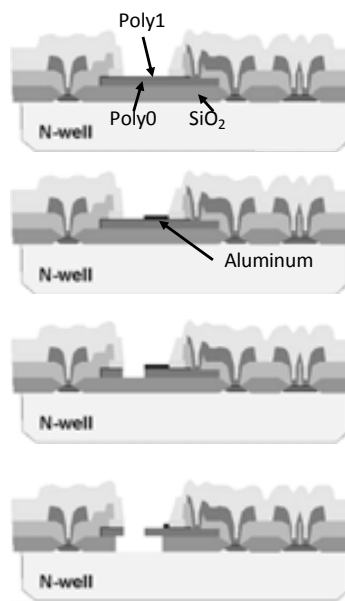


Figure 54.- Nanocantilever post-CMOS definition in an embedded nanoarea using a 2.5 μ m twin well, two polysilicon and two metals CMOS technology, [Ver05].

3.1.4. CMOS-MEMS APPROACHES SUMMARY

The Table 3 summarizes the main fabrication characteristics of the different CMOS-MEMS approaches reported. Specifically there are highlighted the structural material employed, the additional fabrication steps required to include MEMS in the CMOS flow, the feature size and thickness of the MEMS. There are important conclusions that can be extracted. By one side the pre-CMOS approaches have the capability to choose the structural material and thickness, obtaining better mechanical performance than the other approaches which limit the material (either because the material of the layer is given by the CMOS technology or the stringent thermal budget imposed by CMOS processes). However this approach requires several additional processes including some photolithography, deposition and etching steps. Another

common requirement in pre-CMOS is that the final substrate must be smooth enough to allow the following CMOS processes (CMP or wafer bonding solve or avoid this problem). The benefits of intra-CMOS approach are their fabrication simplicity with few additional fabrication steps and their feature size provided by the gate size of the CMOS technology which is usually competitive to even fabricate NEMS. Also the yield and reliability of CMOS is exploited in MEMS fabrication by means of this approach. At last the main advantage of post-CMOS approach consists on their compatibility with all the CMOS technologies since the MEMS fabrication takes no effect over the CMOS circuits. So this approach is capable to be made in different foundries or MEMS specific laboratories.

References	Approach	Structural material	Additional MEMS fabrication steps	CMOS feature size (μm)	MEMS feature size (μm)	Minimum gap (μm)	Thickness (μm)
[Smi95], [Bus98]	pre-CMOS	poly-Si	L+D+E+CMF+A	2	1	1.6	2
[Yas03]		poly-Si	L+D+I+E+CMF+A	2.5	6	-	6
[Lem99], [Jud04]		Si	L+E+CMF	0.6	3	4	10
[Par95], [Par97]		Si	L+E+WB+A	2	50	-	10
[Oll12]		Si	L+E+D	0.05	0.1	0.18	0.04
[Sch98]	intra-CMOS	poly-Si	L+E	0.8	70	0.6	0.4
[Fed96]		Al+SiO ₂	E	0.8	1.2	1.2	4.8
[Cor93], [Gee02]		poly-Si	L+D+I+E	3	-	-	4
[Ver06]		Al	E	0.35	0.6	0.6	0.85
[Lop09]		poly-Si	E	0.35	0.35	0.04	0.282
				0.18	0.28	0.28	0.58
[Baolab]		Al	E	-	-	-	-
[Che12]		Al+W+SiO ₂	E	4	0.6	0.11	0.925
[VanK98]	post-CMOS	Al	L+D+E	0.8	16	-	-
[Dav03], [Ver05]		poly-Si	L+D+E	2.5	0.84	1	0.6

Table 3.- Summary of the main fabrication characteristics over the different CMOS-MEMS fabrication approaches. The additional fabrication steps acronyms are: L (lithography), D (deposition), E (etching), A (annealing), I (implantation), WB (Wafer Bonding).

3.2. AMS C35B4C3 CMOS TECHNOLOGY DESCRIPTION

The EURORACTICE IC [EUP] service brings ASIC design and manufacturing capability through Multi Project Wafer (MPW) offering different IC technologies from different foundries such as ON semiconductor, Autriamicrosystems (AMS), IHP, LFoundry, TSMC, UMC, etc. In previous studies ECAS group has worked with two

specific foundries, AMS and UMC. In this thesis the whole of the devices have been fabricated in AMS foundry.

The AMS foundry offer a family of CMOS processes which have in common the CMOS core module. The C35 core module is based on a p-substrate wafer, a pseudo twin-well, stacked contacts, polysilicon gate layer, minimum feature size of $0.35\mu\text{m}$ and supply voltage of 3.3V. There are available specific modules which add some additional layers or modify some of the core layers. These modules are:

- CPOLY capacitor: Additional polysilicon layer above of the core polysilicon in order to form high integrated capacitances due to small dielectric layer between them.
- 5-Volt: Specific NMOS and PMOS transistors with different gate oxide thickness optimized to operate at 5V instead of 3.3V of the core module.
- High resistivity: Design of integrated resistances with low doped polysilicon.
- Metal-4: Addition of a fourth metal layer to increase the connectivity capabilities between devices.
- Thick metal: A thickness of $2\mu\text{m}$ of top metal instead of $1\mu\text{m}$ to fabricate integrated inductors.
- MIM capacitor: Additional metal layer between metal 2 and metal 3 intended to be used to integrate capacitances (similar than CPOLY module).

There are two main modules which add useful layers in the fabrication of CMOS-MEMS: the CPOLY capacitor and the Metal-4 modules. The only process available that include these two modules is the C35B4C3 and is also one of the processes more scheduled in the calendar of EURO PRACTICE (seven times on a year) allowing different RUNs over a year with high regularity. The Figure 55 shows a cross section of the technology detailing all the layers. The Table 4 shows the main parameters of each layer available in the technology.

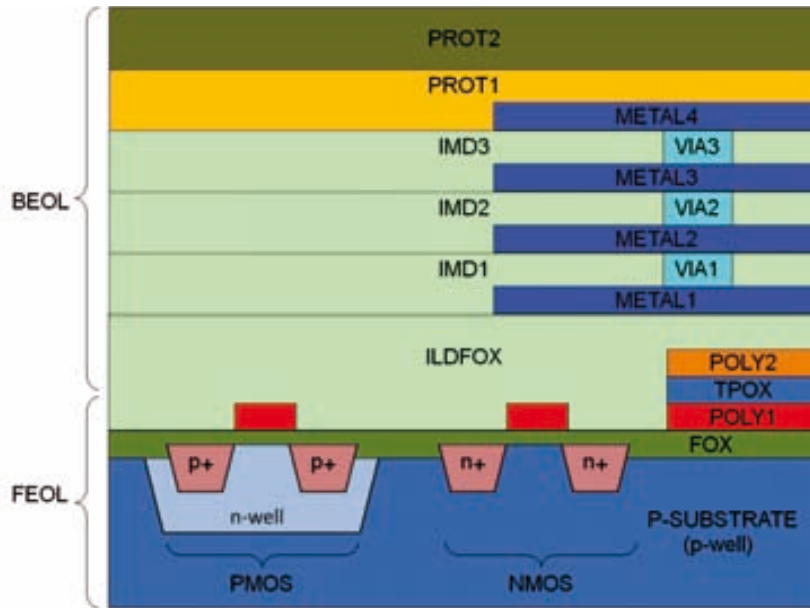


Figure 55.- AMS C35B4C3 CMOS technology layers.

Layer parameter	Source	P1	P2	M1	M2	M3	M4
<i>Material</i>	technology	poly-si	poly-Si	Al ²⁸	Al ⁹	Al ⁹	Al ²⁹
<i>Thickness (nm)</i>		282	200	665	640	640	925
<i>Maximum density current (mA/μm)</i>		0.5	0.3	1.0	1.0	1.0	1.6
<i>Resistivity (Ω·μm)</i>		4.23	10	0.09	0.09	0.09	0.09
<i>Minimum size (nm)</i>		350	800	500	600	600	600
<i>Minimum distance between conductors (nm)</i>		450	500	450	500	600	600
<i>Density (kg/m³)</i>	typical	2330	2330	3000	3000	3000	3000
<i>Young modulus (GPa)</i>		160	160	131	131	131	131

Table 4.- Mechanical and electrical parameters of the layers provided in the C35B4C3 technology.

The design with this technology is done through a design kit installed with CADENCE software. The design kit includes all the layers available in the technology and libraries with pre designed blocks such as transistors, capacitors, inductors, resistors, digital circuits, etc. The FEOL processes include the growth of the gate dielectric, patterning of the gate the drain and the source regions, implantation and diffusion of dopants. The FEOL layers of AMS C35B4C3 are depicted in Figure 55. The BEOL are composed by deposition of different metal layers separated by dielectrics which will interconnect the terminals of the transistors. In this stage a passivation layer is also deposited to protect and isolate the whole chip. The FEOL layers of the technology are shown on Figure 55.

²⁸ Actually it is a stack of TiN + Al + TiN

²⁹ The top metal is made of a stack Al + TiN

3.2.1. CMOS-MEMS DESIGN IN AMS C35B4C3

The CMOS technology has several design rules for each layer that must be followed to ensure a correct fabrication of the electronic circuit devices. However, to allow the fabrication of MEMS with this CMOS technology some design rules have to be skipped or modified with our requirements. The foundry allows some design rules violation for prototype purposes but the last responsible if the fabrication fails is the designer. From top layers to bottom the following list explains all the layers of the CMOS technology main design rules modifications mandatory for CMOS-MEMS fabrication:

- PAD: This layer defines the opening hole on the passivation layer which is intended to accommodate the metal contact pads of the chip. The opening hole has a minimum square size of 15 μ m and below them all metals and vias must be placed.
- VIA 3 & 2: The vias are used to define the contacts between metal layers and have a square size of 500nm and a separation of 1 μ m. The vias must be placed between metal layers.
- METALS 4, 3, 2 & 1: The metals are used to interconnect the transistors and circuits between them and with the output pads of the chip. The metal layers are composed by a sandwich of TiN with aluminum between them. The metals have design rules related with minimum sizes, distances between edges and relations with via layers.
- CONT: It is a layer with design rules requirements similar than the other vias but the contact is made between metal 1 and FEOL layers (polysilicon or active regions).
- POLY 2: The second polysilicon layer is available in the CPOLY module for integrated capacitor purposes so a design requirement is that below them must be placed the first polysilicon layer in order to make the two plates separated by thin silicon dioxide layer. The minimum feature size of POLY2 is 650nm and the distance between two edges is 500nm.
- POLY1: The first polysilicon layer is primarily used to make the gates of the transistors with a feature size of 350nm and distance between edges of 450nm.
- NPLUS & PPLUS: These layers define the regions where the doping impurities which define the source and the drain regions of the transistors will be placed.
- DIFF: This layer is used overall NPLUS and or PPLUS to define the active regions of the transistors.

- NTUB: Finally, this layer defines the N-WELL region where the PMOS transistors will be placed because the wafer is originally doped with p-type impurities making the P-WELL of the NMOS transistors.

From the previous layers the modifications over the design rules to allow our CMOS-MEMS fabrication approach are listed below:

- PAD: To allow the releasing of MEMS with wet etching this layer is employed to let the passivation opened in top of the MEMS. The design rule violated consist on put below them only the structural layer (polysilicon or metal) and not adding the metal stack required as in the case of the output pads.
- VIAS: In MEMS fabrication the placement of these vias without their corresponding metal layers is used to reduce the amount of silicon dioxide, reducing the etching time required. The shape and dimensions of these vias are also modified to adapt their shape to the MEMS profile and dimensions.
- METALS: All the metals could be used as structural layers for MEMS. It is common to use only the metal 4 because the other metals have more dielectric layers in top of them which increase the etching time. However in case of metal stacks all the metals are employed.
- POLYSILICONS: The polysilicon layers could be used also as structural layers to fabricate MEMS devices due to better mechanical properties of polysilicon regarding metals. The first polysilicon layer is mainly used to implement the MEMS structure whilst the electrodes are made of second polysilicon layer. In this case the rule violated consists on skip the first polysilicon placement below the second polysilicon as in the CPOLY module. Taking advantage of the inter oxide layer through spacer technique [Lop09] the polysilicon layers could be used to achieve smaller gaps such as 40nm.

The technology provides two different materials as structural layers, a sandwich of metals and polysilicon. The second one has better mechanical properties and better feature size allowing smaller devices and smaller transduction gaps. Despite of this, the polysilicon is buried into more oxide than metal layers requiring larger etching times.

Independently from the shape of the MEMS resonator there are common definition steps of the whole layout. The structure and the electrodes are defined using

polysilicon or metal layers trying to follow the maximum design rules. The vias and the PAD opening are defined and adapted to the resonator shape. A grounded well is placed below the MEMS in order to fix the voltage to a constant value and control the electrostatic vertical force to a known value. Then the CMOS circuitry, previously designed is placed and connected. Finally the external metal pads are distributed over the chip and connected to each of the MEMS terminals. In the Figure 56 it is shown a composition of two images from the same layout of a CCB separated by red dashed line. In the middle of the resonator there are shown the vias and PAD openings whilst in the other middle the polysilicon beam and electrodes are shown.

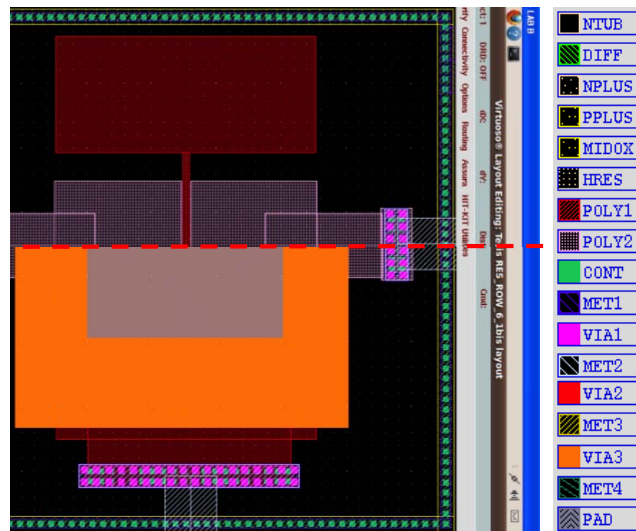


Figure 56.- Modified layout of a CCB in AMS C35B4C3 CMOS technology design kit for CADENCE. The image is divided by a dashed line to show the polysilicon layers which in the real layout will be hidden by the vias and pad layers.

3.2.2. POST CMOS RELEASING

Once the testing chips are fabricated by the foundry post CMOS processes must be performed to correctly release the resonators buried in silicon dioxide. There are two different etching approaches to remove the silicon dioxide dry and wet etching. Our group has performed some tests with dry etching and the releasing of the mechanical structures has not been possible. However, the wet etching process after controlling their parameters has provided good repeatability and correct releasing of the structures. So this is the standard process employed to release our MEMS with our fabrication approach.

The wet etching of silicon dioxide is typically done by Hydrofluoric Acid (HF) which reported etching rate between 43nm/min to 680nm/min [Wil96] depending upon the type of silicon dioxide and the method used to grow or deposit it. One of the problems of HF is that it is a highly corrosive acid, capable of dissolving many

materials such as aluminum of the pads. In order to prevent this drawback a buffered solution of HF (BHF) is employed. This BHF is composed by ammonium fluoride, acetic and HF acid and works slowing down the etching rate of aluminum preserving the etching rate of silicon dioxide. The experimental etching rate of BHF is 100nm/min requiring around 4 minutes of etching in metal resonators and 28 minutes of etching in polysilicon resonators as they are surrounded by 360nm and 1.6 μ m of silicon dioxide respectively. The difference between the predicted and real etching time is due to the degradation of the etching rate in large processes. In fact, the BHF effective etching time is established on 18 minutes. So the releasing of polysilicon resonators requires two etching steps (18+10 minutes) in order to rebuild the BHF solution. The Figure 57 shows optical and SEM images of a CCB before and after wet etching process. The optical image gives a quick look over the amount of silicon dioxide present below the resonator considering the color observed. In Figure 57 (a) the resonator is fully covered by silicon dioxide and the electrodes are yellowish green. After the wet etching process, Figure 57 (c), a purple ring appears on the corners of the electrodes and the smooth substrate is revealed.

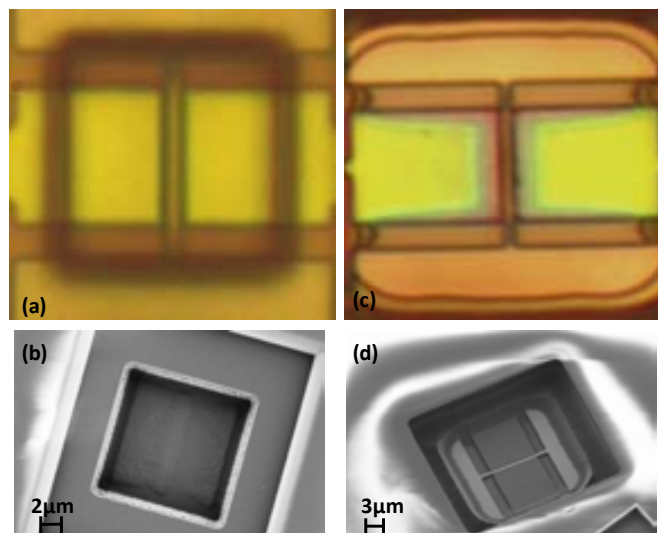


Figure 57.- (a,b) optical and SEM images respectively of a polysilicon CCB before releasing process; (c,d) same resonator after 28 minutes of BHF wet etching.

SEM image or in some cases a FIB cut and further SEM image are mandatory to check if there are remaining silicon dioxide. Figure 58 shows a FIB cut where it is clearly seen that the resonator was correctly released. The FIB cuts provide useful information but destroy some parts of the structure so the requirement of these tests must be considered carefully.

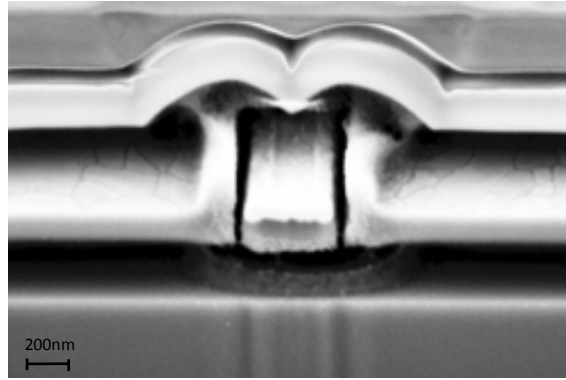


Figure 58.- SEM image of a FIB section made on a polysilicon CCB ($l=13\mu\text{m}$, $w=350\text{nm}$, $t=282\text{nm}$ and $g=40\text{nm}$). A 2 minutes wet etching process was done in order to remove silicon dioxide from the surroundings of the beam to increase the contrast between layers on the SEM imaging after the FIB processing.

3.3. APPROACHES FOR MEMS PACKAGING

The packaging is a key step in the fabrication of microelectronics as involves important topics in the final product as performance, capabilities and cost. As it has described in the introduction there are different levels of packaging, from zero to third level, covering from the protection of the IC die to the outer shell of the product with specific requirements in function of the desired application. Some examples of these requirements are listed below:

- Devices, such as transmit/receive switches, must exclude moisture to prevent deterioration or corrosion and might require an inert atmosphere to remain stable.
- Pressure sensors must be open to atmospheric pressure but not be susceptible to moisture damage.
- Optical devices, such as camera modules, must exclude particles, must not have organics that can condense on optical surfaces over time, require optical windows and must maintain optical chain alignment over the product life.
- Devices that analyze fluids require containment of those liquids and must not leak.
- Devices requiring ESD protection greater than that required by CMOS devices.
- Devices requiring controlled atmosphere to enhance their response (MEMS resonator encapsulated in vacuum) or protect the layer materials with inert gas.

3.3.1. PACKAGING APPROACHES

There are different methods used for encapsulating MEMS at the device level. In this section we will focused on two of them: attachment of a separate lid on top of the walls of the package; deposition of some sort of encapsulation layer directly on the device (integrated package). The first method provides good throughput as it can be

applied to entire wafers, packaging all of the devices. The main challenges within this method correspond to the election of the lid material and the bonding techniques. The second method is based on a smartly design of both the device and the package, requiring only some additional processes to close the package. This method provides the higher yield and the lowest cost but has some limitations over the materials of the package.

The work developed by [Wan06] is based on the first approach: fabricate separately the device wafer and the cap wafer, *Figure 59*. The silicon wafers have a thickness of $350\mu\text{m}$ and are hermetically sealed with each other through a closed square loop of Au-Sn eutectic solder. The cap wafer is etched with TMAH to accommodate a cavity where a seed layer composed by Cr/Au for the incoming electroplating process is deposited. Through-hole vias are fabricated with RIE process and the electroplating of Cu is performed. Finally a sealing line of $70\mu\text{m}$ for the bonding is deposited onto the patterned seed layer of Cr/Au. The RF-MEMS devices are patterned on a Ti-Ni-Au layer in the device wafer and the two wafers were eutectic bonded during 20 minutes with a temperature profile with a peak of 280°C . The whole package with the device has a final size of 1mm by 1mm.

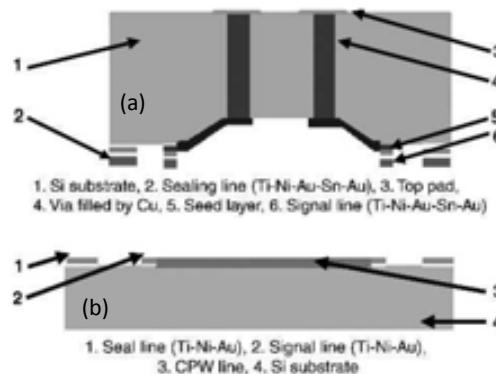


Figure 59.- MEMS and package fabrication approach based on bonding a cap (a) and device (b) wafers, [Wan06].

The [Can03] presents a device and package fabrication method based on the second method, *Figure 60*. The process begins with a SOI wafer with trenches etched on the device layer with the patterns of the MEMS, *Figure 60* (a). Then a thin LPCVD deposition of silicon dioxide is performed to cover the trenches and let opened electrical contacts, *Figure 60* (b). A cap silicon layer with a thickness of $20\mu\text{m}$ is deposited and additional vent trenches are etched in this cap layer to allow the releasing of the device, *Figure 60* (c). Then the MEMS device is released through dry etching based on HF, *Figure 60* (d). Finally the cap layer trenches are sealed with another layer of silicon dioxide deposited with LPCVD, *Figure 60* (e). As the LPCVD furnace is under vacuum, the cavities are also under vacuum when sealed.

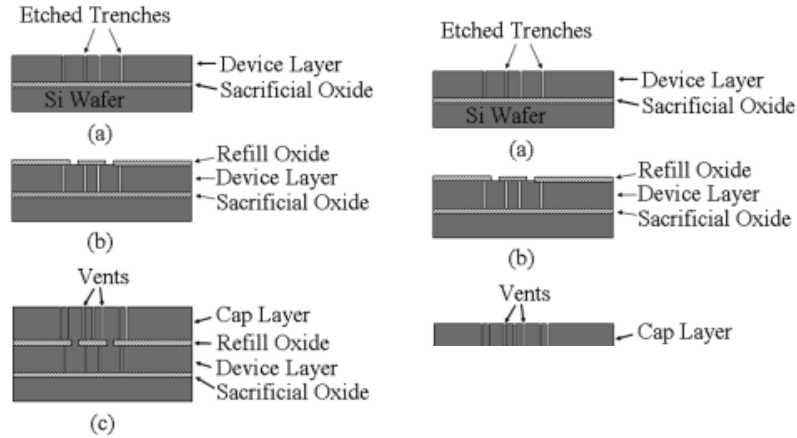


Figure 60.- MEMS and 0-level package co-fabrication approach by [Can03].

An alternative on integrated packaging is presented in [He06] where the packaging material is $1\mu\text{m}$ thick porous alumina (Al_2O_3). The concept of using a porous material is based on a releasing process of plasma dry etching which vapors can penetrate into the cavity. After that the cap layer is sealed with a PECVD deposition of silicon nitride with a thickness of $2.5\mu\text{m}$. The whole device package has a size of $160\mu\text{m}$ by $300\mu\text{m}$ and a vacuum of 10.6mbar is sustained over the initial month.

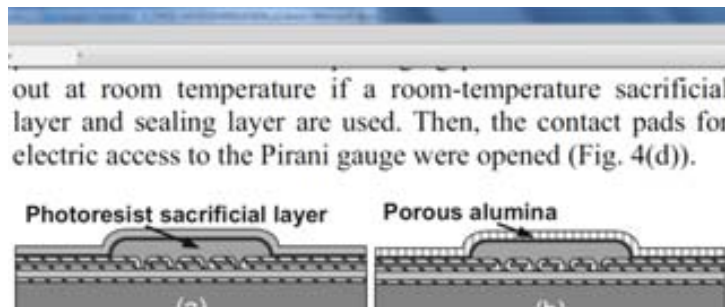


Figure 61.- Process flow of vacuum encapsulation of a metal Pirani gauge, [He06].

Another approach based on capping with porous material is demonstrated on [Verh08]. The Figure 62 shows the concept process route. The MEMS device is micromachined with a sacrificial spacer layer and silicon dioxide layer is deposited and patterned in such a way that only SiO_2 is present where the cavities have to be created. This step is followed by the deposition of the supporting cap layer to avoid collapsing of larger cavities. In this shell, releasing holes are patterned, followed by a deposition of a SiOC cap layer. Through the SiOC layer the sacrificial SiO_2 is removed by vapor HF, releasing the mechanical micro structures. The cavity is evacuated achieving $8 \cdot 10^{-3}\text{mbar}$ and the release channels are sealed by the deposition of a hermetic seal layer. The whole MEMS packaged size is $50\mu\text{m}$ by $50\mu\text{m}$.

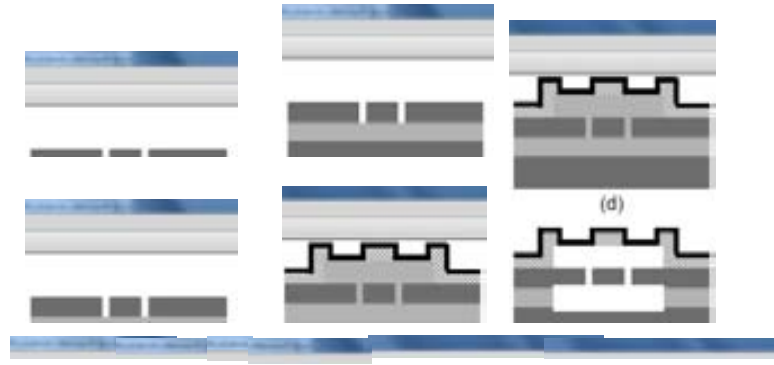


Figure 62.- Schematic drawing of the process route for encapsulating a MEMS device using a permeable SiOC layer, [Verh08].

MEMS design, Package design, Fabrication, Releasing, Sealing, Test, MEMS packaged

The present thesis presents a novel method to develop a package of MEMS resonators which takes a step further the integrated package concept using the metal layers available on the CMOS technology. [Mar10]. The process flow concept (Figure 63) is simple: design the MEMS resonator, design the packaging, send the whole layout to the foundry, release the resonator and seal the package. Between the releasing and the sealing steps the resonator must be electrically tested to check that it is correctly released because the metal layer covers the entire structure and obscures from SEM imaging what lies beneath.

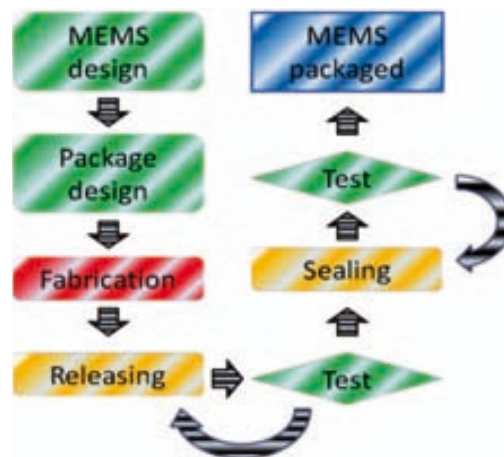


Figure 63.- Process flow for co-integration of MEMS and 0-level packaging.

The package itself could be made by one single metal layer on top of the resonator following their size and adding releasing holes along the structure of the resonator. The problem of one single layer is that the sealing process required could damage the resonator adding material on top of them. This problem is solved adding an additional metal layer with releasing holes misaligned between the two metal layers in

order to allow the releasing process through the two layers and protect the resonator from the subsequent deposition. The conceptual idea is shown on **¡Error! No se encuentra el origen de la referencia.:** the material of the walls of 0-level package are from the silicon dioxide deposited between the metal layers on CMOS flow process; the MEMS resonator is released through the holes; a mask to protect the metal pads is aligned; the sealing deposition is performed through the mask.

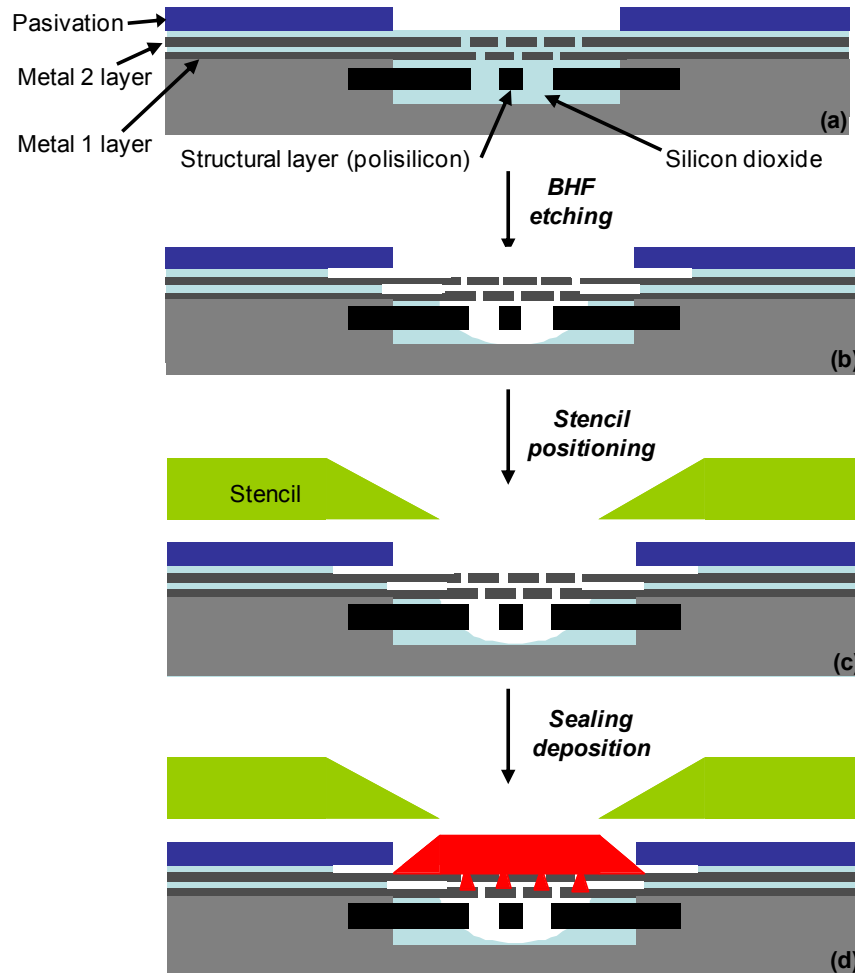


Figure 64.- Conceptual package and sealing process of our CMOS-MEMS 0-level packaging approach: (a) the two metal layers with misaligned releasing holes, the silicon dioxide walls and the silicon substrate make the package cavity which contains the MEMS resonator; (b) the post CMOS releasing process is performed; (c) a mask is placed and aligned on top of the die; (d) the selective deposition in vacuum conditions is done to seal the package and maintain low pressure inside the cavity whilst the rest of the remains protected from that deposition.

In the described approach there are some major challenges that must be solved to obtain the packaged resonator under vacuum conditions. By one side the correct releasing is predicted to be more difficult with two metal layers above the resonator.

The sealing process requires a correct alignment of the mask at chip level, and the sealing deposition must be thicker enough to cover entirely the holes.

3.4.1. PACKAGE DESIGN

The package cover is composed by first and second metals with 500nm misaligned square holes with 500nm of side. In the first version of the package the covers are adapted to the size of the MEMS resonator and do not increase their total size taking into account the anchors and the electrodes. Between them several vias have been placed to actuate as pillars and sustain the top metal layer. The opening square PAD of $15\mu\text{m}$ is maintained but only the via 3 is placed below the PAD to respect the definition of metal 2 cover. The **¡Error! No se encuentra el origen de la referencia.** shows the layers of the MEMS separately from the package layers and the whole layout including the opening PAD window. The MEMS resonator corresponds to a CCB ($l=13.2\mu\text{m}$, $w=350\text{nm}$, $g=150\text{nm}$) with the structural layer from first polysilicon layer and the electrodes from the second polysilicon layer. In this case the rectangular cover size is of $25\mu\text{m}$ by each side.

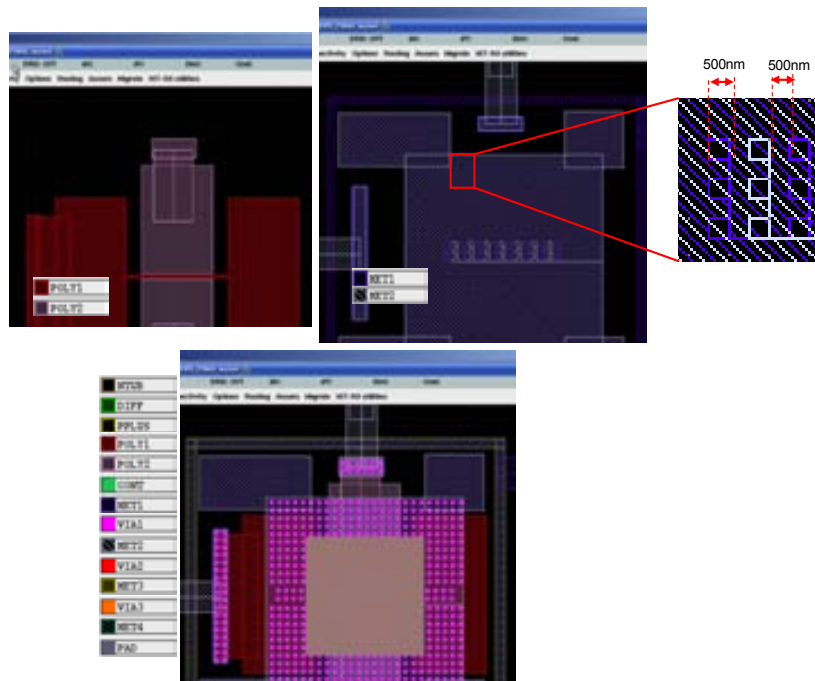


Figure 65.- Layout of CCB packaged with metal layers from AMS C35B4C3 technology. The rectangular cover size is of $25\mu\text{m}$ and the releasing holes of 500nm of side are misaligned 500nm between the two metal layers.

Another version of the package (Figure 66) increases the size of each side of the metal covers to $45\mu\text{m}$, regarding the size of the resonator. The size of the opening PAD window is maintained to a square of $15\mu\text{m}^2$.

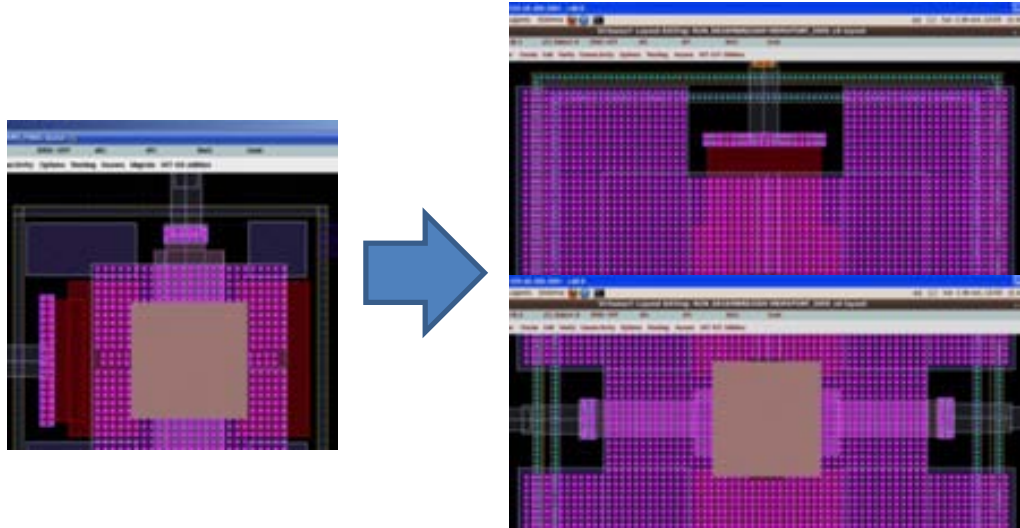


Figure 66.- Comparison between two different size package design covers with the same MEMS resonator below them.

One challenge from covering MEMS resonator with metal is that the penetration of the etching solution will be more difficult even though placing releasing holes on it. So in order to decrease the etching time required two different strategies were proposed and applied (Figure 67) to different package versions: increase the size of the holes maintaining the number of them or increase the density of holes over the metal covers.

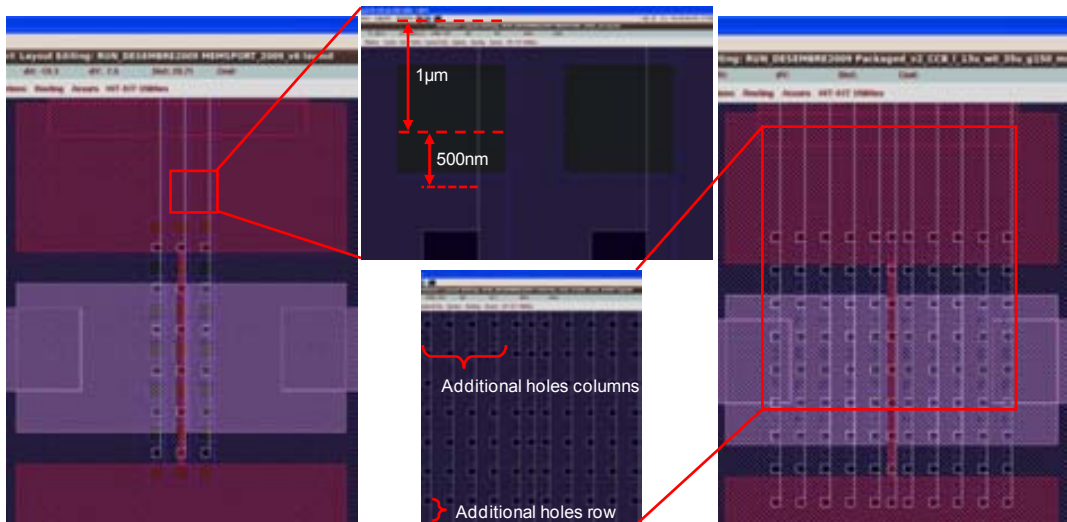


Figure 67.- Metal covers with bigger holes ($1\mu\text{m}$ instead of 500nm) and additional holes columns.

Other kind of MEMS structures could be also packaged. In particular the Figure 68 shows the layouts of Free-Free and DETF resonators with their corresponding metal covers. The Free-Free structure has three main beams (two parallel and one

perpendicular) so holes were placed on top of all of them. The DETF has two main beams in parallel but holes were added on all the metal cover to apply the etching enhancement of increasing the holes density described above.

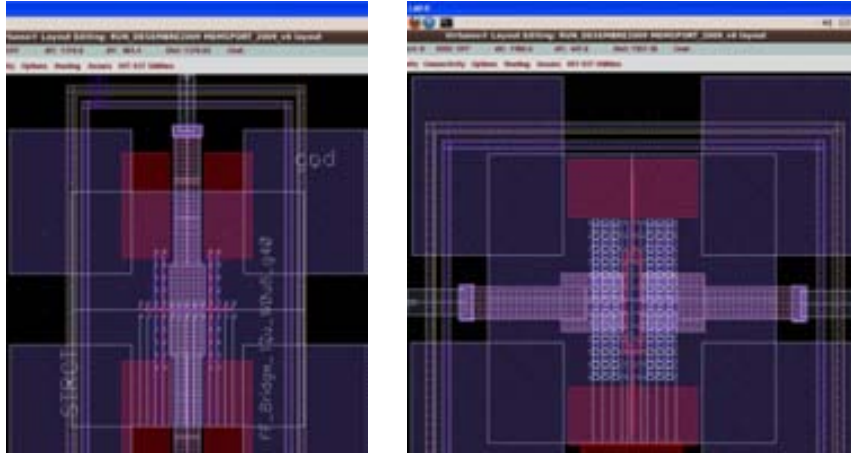


Figure 68.- Packaging layouts for a Free-Free ($l=17\mu\text{m}$, $w=800\text{nm}$) and DETF ($l=15.8\mu\text{m}$, $w=500\text{nm}$) resonators. The size of the package and the placement of the holes were dimensioned considering the shape of these MEMS structures.

In the Table 5 it is shown a summary over the main parameters of the metal covers from the different packages designed.

Parameter	CCB packaged v1	CCB packaged v2	CCB packaged v3	Free-free packaged	DETF packaged
Material	TiN+Al+TiN	TiN+Al+TiN	TiN+Al+TiN	TiN+Al+TiN	TiN+Al+TiN
Cover length (μm)	25	45	45	45	45
Cover width (μm)	25	45	45	45	45
Metal 1 thickness (nm)	665	665	665	665	665
Metal 2 thickness (nm)	640	640	640	640	640
Hole size (nm)	500	1000/500	500	500	500
Distance of decorrelation (nm)	500	500	500	500	500
Holes rows and columns	8x3	7x3	9x11	13x3	13x11

Table 5.- Main package parameters for each different version.

3.4.2. RELEASING

The next step of the process flow after fabrication is the releasing of the MEMS devices. To release packaged MEMS the HF based solution is employed however in this case the metal covers of the package obstruct the direct microscope checking of this process. Two characterization approaches are performed, one based on physical characterization with SEM imaging and FIB cutting and the other based on electrical measuring the response of the MEMS resonator.

A. PHYSICAL CHARACTERIZATION

The physical characterization consists on employ microscopy tools to check the package and the resonator status. These tools include optical or electronic microscopes and also a FIB instrument to make cross sections of the package with the resonator. The use of FIB implies that the device studied is damaged and the package is broken, but their results could provide important information over the amount of remaining silicon dioxide and the effects of the etching on the metal covers.

Using the same BHF solution than the one described previously for a period of 28 minutes the SEM images of the *Figure 69* are obtained, where the (a) image corresponds to a device before releasing, the (b) image after releasing and the (c) is a zoom of the releasing holes. The releasing holes are circular instead of square due to the resolution of the photolithography process during the metal patterning, because the 500nm holes are below the 650nm feature size of metal 1 and metal 2. The diameter of 430nm is smaller than the 500nm side of the layout but it is expected as we are pushing down the design rules of the technology.

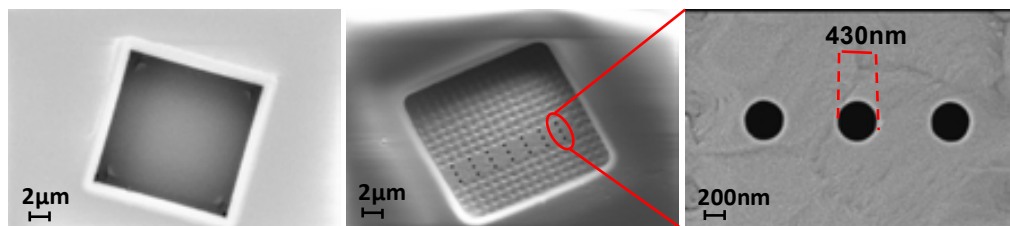


Figure 69.- SEM images of CCB packaged before (a) and after(b,c) BHF releasing process.

In order to check the proper releasing of the packaged MEMS some FIB cross sections are made. In the *Figure 70* there are shown two images from the same resonator of two different dice. The *Figure 70* (a) image is obtained from a chip which has been etched during 22 minutes of BHF solution and the resonator remains buried

into silicon dioxide. It is also noteworthy to see the two metal layers made with a sandwich of TiN and aluminum with the misaligned holes between layers and the via pillars that hold on the top cover. The *Figure 70* (b) image corresponds to a CCB device successfully released where the beam and the lateral electrodes are clearly observable.

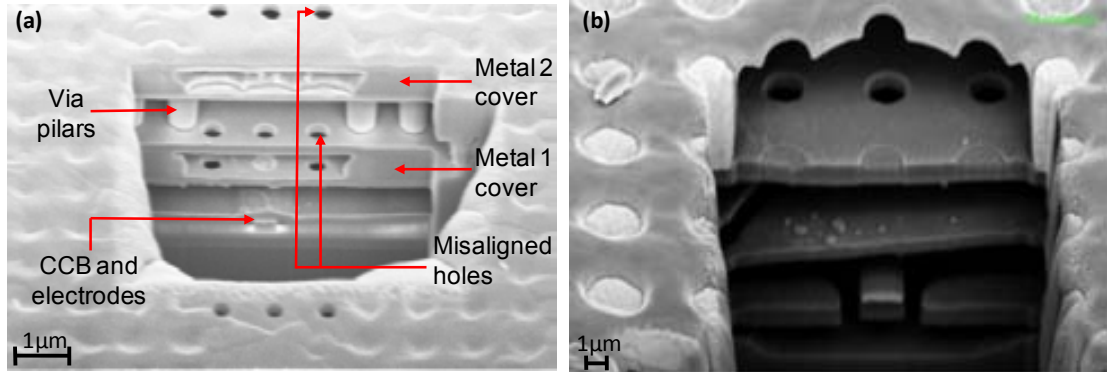


Figure 70.- SEM images cross sections from CCB packaged devices: (a) image with resonator buried in silicon dioxide; (b) image with resonator correctly released.

From the wet etching process there were detected some undesirable effects. By one side the rectangular PAD which let the passivation open is enlarged by the wet etching process. If the edges of the metal covers were reached during the etching step the package is destroyed as it is shown on *Figure 71* (a). Additionally, it has been detected that the metal tracks which connect the MEMS resonator with the output PADS of the chip acts as etching catalyst making tunnels between them that could destroy the vacuum package capability, *Figure 71* (b).

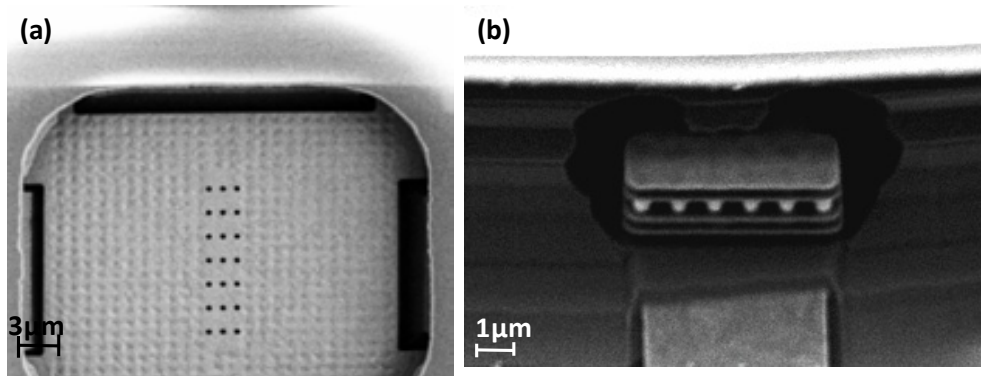


Figure 71.- Examples of problems encountered with the package design: (a) the wet etching process has enlarged the opening window of the passivation letting opened the edges of the metal covers; (b) etched tunnels had been appeared in the metal tracks which connects the PADS with the different parts of the MEMS.

In order to check the tunnels around metal tracks additionally FIB sections are performed. Because the wet etching is performed without using a mask protection, there

is a non-desired etching around the electrical pads which are not protected by the passivation layers. With this etching and considering that the metal paths act as a catalyst for the wet etch solution we must prove that the metal layer is not etched around the resonator and that there is no tunnel for the reactive agents. *Figure 72* (a) shows an optical image and SEM images of this metal path. The metal path close to the pad ((b) image from *Figure 72*) clearly shows aluminum degradation, while the metal path close to the resonator ((c) image from *Figure 72*) is not affected. From these images we can conclude that the reactive agents will release the resonator and the cavity formed by the package will remain close except for the corresponding releasing holes.

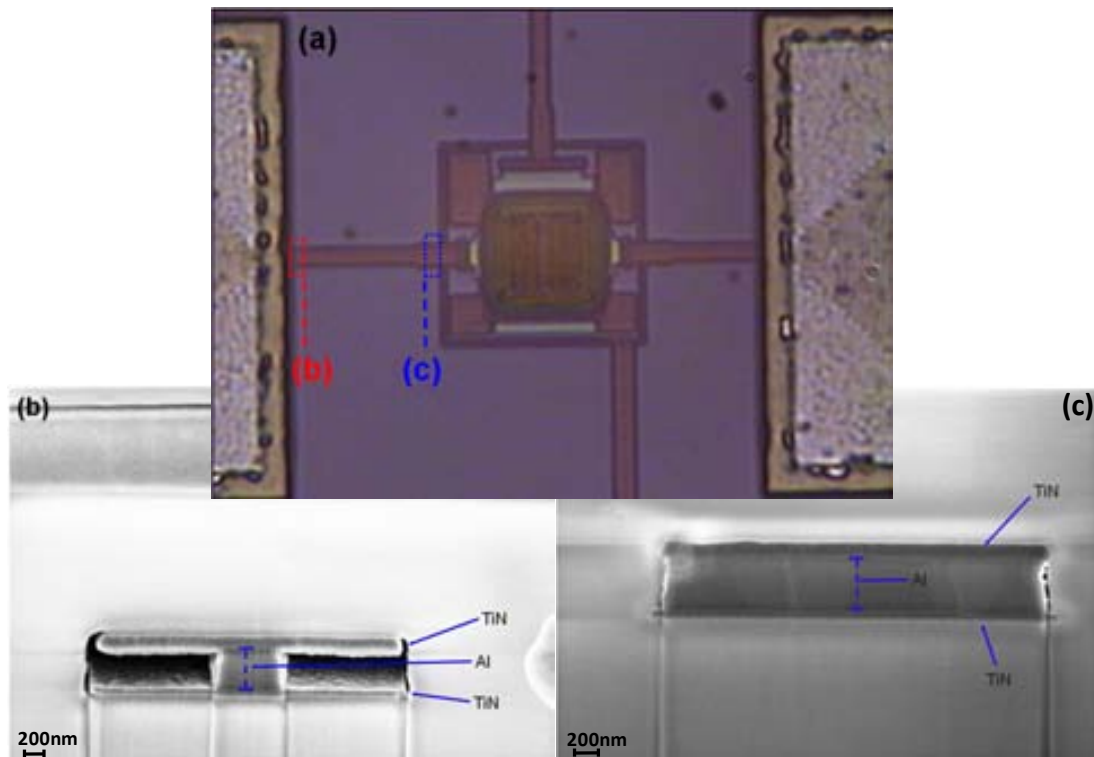


Figure 72.- (a) Optical image of the packaged resonator with electrical pads and metal paths; (b) SEM image of a cross section of the beginning of one metal line where the aluminum is highly etched; (c) SEM image of a cross section near the end of the metal line where the etching agent has stopped.

The other package versions were also inspected with electron microscopy after releasing process. The improved packages for the CCB with bigger holes (a) and high density holes (b) approaches are shown on SEM images of the *Figure 73*. From the images it can be shown that the top metal cover has been disappeared (in the bigger holes package the CCB is visible through them) after the etching process. After checking the layout we can conclude that this effect is produced by an error in it. With the PAD and VIA3 openings there had been added a VIA2 opening (rectangular metal ring) which in the fabrication overrides the deposition of the metal 2 cover. Despite of

this error, the layout enlargement of the metal covers has been maintained the package cavity avoiding the etching till the corners of the cover.

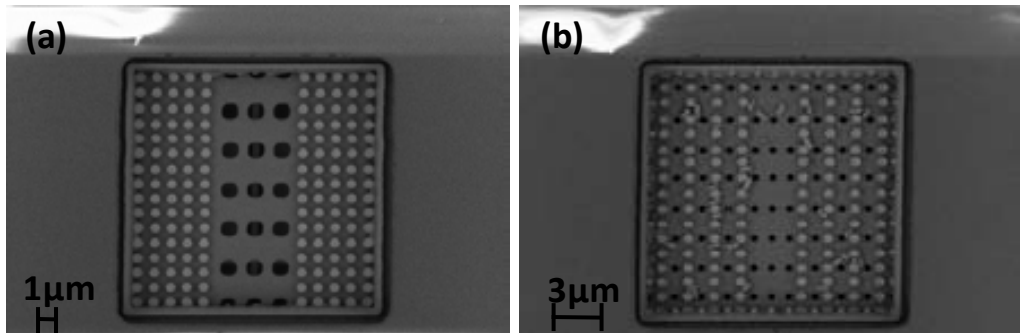


Figure 73.- SEM images of the two strategies employed to ease the penetration of the wet etching solution. In the (a) the holes are enlarged from 500nm to 1 μ m. In the (b) six additional columns of holes were added.

The other resonator packages are depicted on Figure 74. The Free-Free resonator with bigger holes corresponds to (a) and the DETF with more releasing holes is shown on (b). The same VIA2 layout error was produced in these package versions and only the metal 1 cover remains covering the MEMS resonators.

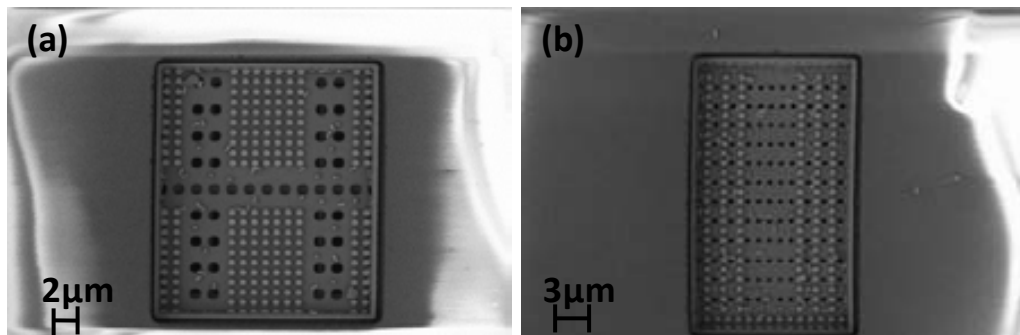


Figure 74.- (a) Image corresponds to a Free-Free resonator packaged with the bigger holes enhancement. (b) Image represents a DETF resonator packaged with the high density holes enhancement.

B. ELECTRICAL CHARACTERIZATION

The functional electrical characterization consist on induce the MEMS resonator into motion and detect their output current through capacitive sensing. The capacitive sensing principles are detailed in their corresponding chapter so for the moment the importance remains on detecting a resonance peak and their corresponding quality factor.

The first electrical test to be performed is done after the post-CMOS etching process which allows checking if the device is correctly released. In the *Figure 75* it is shown a graph with the electrical measures (magnitude and phase) over the packaged CCB resonator of the *Figure 65*. The resonance found around 22.2MHz and the quality factor of 40 extracted similar than without packaging (see chapter 4) gives the evidence that the device is successfully released.

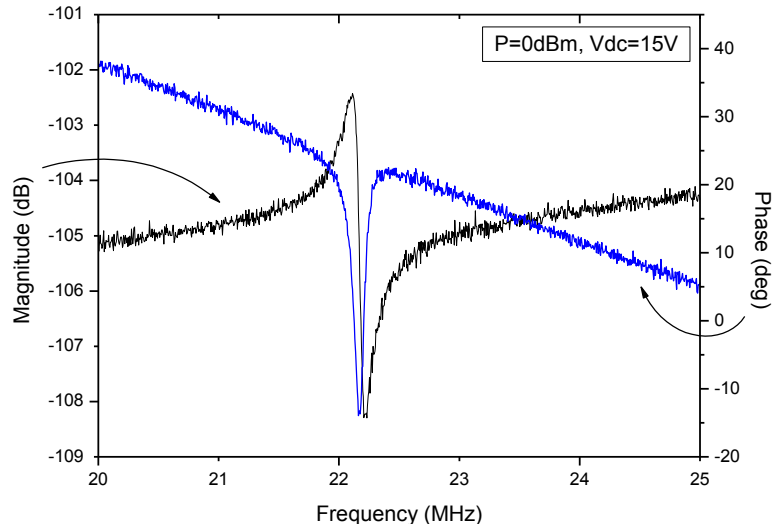


Figure 75.- Magnitude and phase of the electrical measures done for a CCB packaged and correctly released.

The next electrical test to be performed corresponds to the measures under vacuum conditions which will give us the evidence through the increase of the quality factor that the package is correctly sealed. Before proceed to seal the package, the device is tested in a vacuum chamber to obtain the electrical measures which will be used to compare the device behavior when the sealing will be performed. The chip is bonded in a PCB and the device is electrically tested before and after achieve vacuum conditions of $6 \cdot 10^{-3}$ mbar. Comparing the electrical measures of *Figure 75* and *Figure 76* under air pressure there is a huge increase of parasitic current, passing from a level of -105dB (extracted parasitic capacitance of 895aF) to -67.5dB (parasitic capacitance of 63fF). The graph of the *Figure 76* also shows the measure under vacuum conditions (pressure of $6 \cdot 10^{-3}$ mbar) where the quality factor is clearly increased but cannot be computed due to the high amount of parasitic current which almost masks the motional current. It is remarkable that the resonator is working in non linear regime due to the large displacement achieved by the highly excitation signals, however the change in quality factor in function of the air pressure as it was expected is clearly shown. A similar polysilicon resonator has been measured on [Lop09] in air and vacuum conditions increasing the quality factor from 227 to 4400 demonstrating that the mechanical and electrical responses are enhanced in low pressure ambient and could be employed to test the sealing of the package.

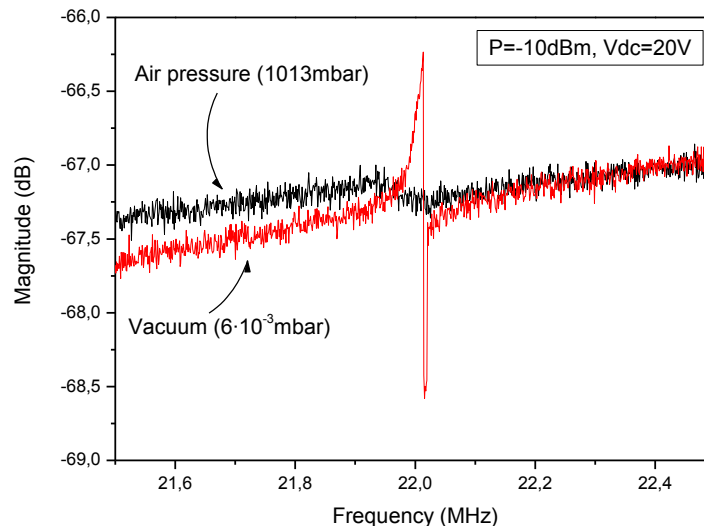


Figure 76.- Magnitude response of the released CCB packaged and bonded before and after vacuum conditions of $6 \cdot 10^{-3}$ mbar.

3.4.3. REQUIREMENTS FOR THE VACUUM SEALING

The deposition process which will seal the package must be completely defined: the most suitable type of deposition has to be established, the deposited material has to be chosen and the minimum thickness to cover the holes has to be studied.

To obtain the required deposition thickness a homogeneous deposition of aluminum over the whole chip is performed. The main advantage is that the alignment with a mask is not required greatly reducing the complexity of the sealing in exchange for shortcutting all the pads. Two homogeneous PVD aluminum evaporation depositions (Univex 450 from Leybold) with thicknesses of 250nm are done in order to establish the total thickness required to seal the holes of the package. In the **¡Error! No se encuentra el origen de la referencia.** are shown three SEM images corresponding to a package after releasing the MEMS (a), the first 250nm deposition (b) and the second 250nm deposition (c). The diameter size of the holes is greatly reduced from 430nm to 128nm, but a thicker deposition will assure the whole sealing.

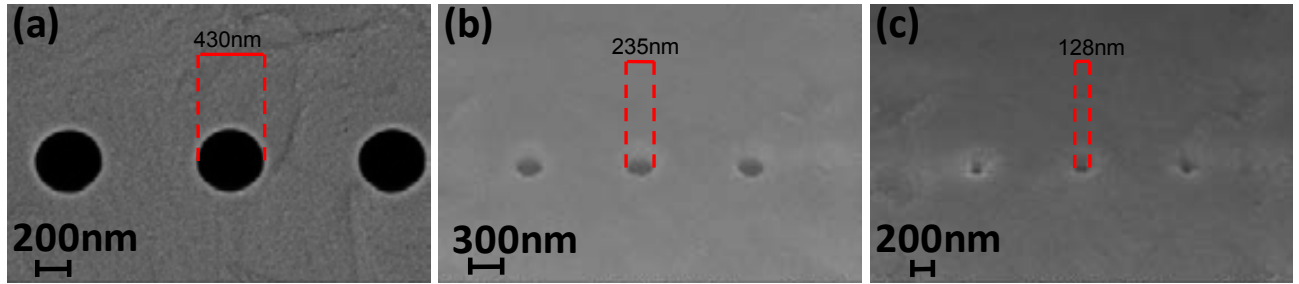


Figure 77.- SEM images showing the reduction of diameter of package holes due to two PVD evaporation depositions of aluminum of 250nm thick.

A FIB section from one packaged CCB is performed and shown on *Figure 78* where the deposited aluminum layer is clearly observable on top of the passivation layer in the (a) image and on top of the metal 2 layer on the package on image (b).

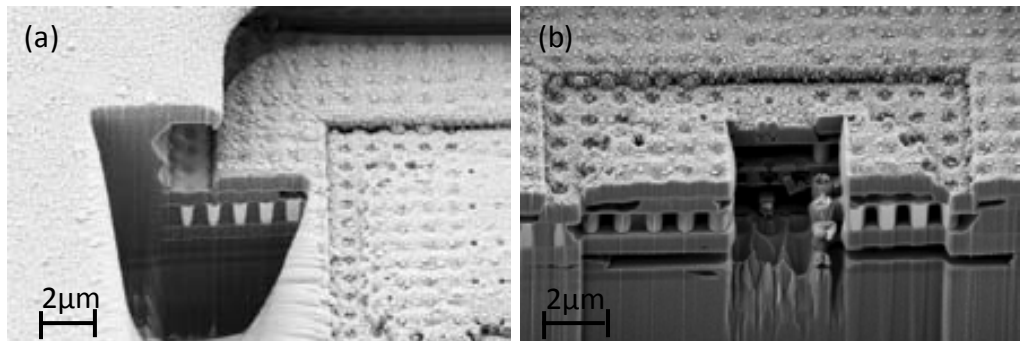


Figure 78.- SEM images of FIB sections made on a packaged CCB after depositing two layers of 250nm of aluminum.

In order to correctly establish the correct thickness another deposition is performed onto the same device of another chip. This time a PVD sputtering deposition (Sputtering Leybold Heraeus Z 550) of aluminum with a thickness of 700nm is made. A cross section SEM image with the result obtained is shown on *Figure 79*. This time the thickness of 700nm is enough to completely seal the releasing holes. However the surface is rougher than in the case of the deposition with PVD evaporation.

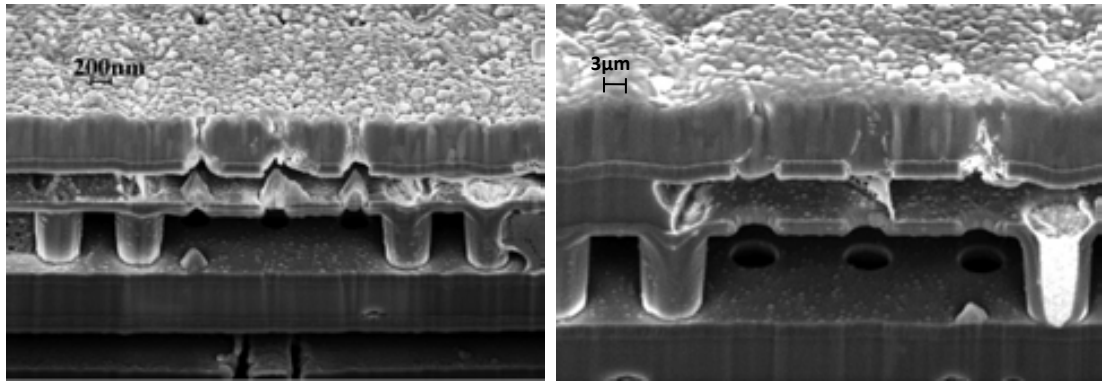


Figure 79.- SEM image cross sections made with FIB from a packaged resonator with 700nm of PVD sputtering deposition. The images had been taken in different parts of the same package during the FIB cutting.

The deposition processes applied has allowed setting a required thickness of at least 700nm to fully seal the releasing holes. The comparison between PVD evaporation and sputtering shows that a rougher surface is obtained for sputtering. A rough surface implies metal grains instead of continuous surface which could let gases penetrate into the package. For this reason the selected deposition method is PVD evaporation. The material selected for all the cases is aluminum which is an available metal on the two methods and provides good adherence onto the top metal cover.

3.4.4. SEALING APPROACHES

After that the parameters for the deposition are well known the sealing process could be performed. There are five different sealing approaches that had been developed during the thesis. The main concept which all of them have in common is that some kind of mask is placed above the chip to protect the metal pads from the deposition. Some of the techniques used provide resolutions much lower than the ones required to seal the package. However, we take advantage of their capability to align the patterns with the chip samples, which is one of our main challenges.

A. AUTOALIGNMENT METHOD WITH SOI STENCIL

After the resonator is correctly fabricated, released and works properly the next step consists on sealing the package by a selective deposition of some material to cover the releasing holes without covering the full chip which will produce shortcircuits between metal pads. The first approximation was the use of a stencil similar than [Savu2008], where a SOI wafer is used as a mask for the subsequent deposition. The use of a SOI wafer is required due to the fact that one layer acts as a mask and the other

contains the die of the chip. The masks of the stencil will be designed to provide self alignment between the patterns of the mask and the packaged MEMS to be sealed.

The fabrication of the stencil is done in a project entitled “*Explotación de la aplicabilidad de elementos integrados MEMS-CMOS monolíticos y heterogéneos para sistemas portables de altas prestaciones*” in collaboration with IMB-CNM through a program called GICSERV offered by Ministry of Science. Two different fabrication approaches (*Figure 80*) for the stencil are referred: KOH for thicker SOI layer plus RIE for thinner silicon layer or RIE plus RIE respectively.

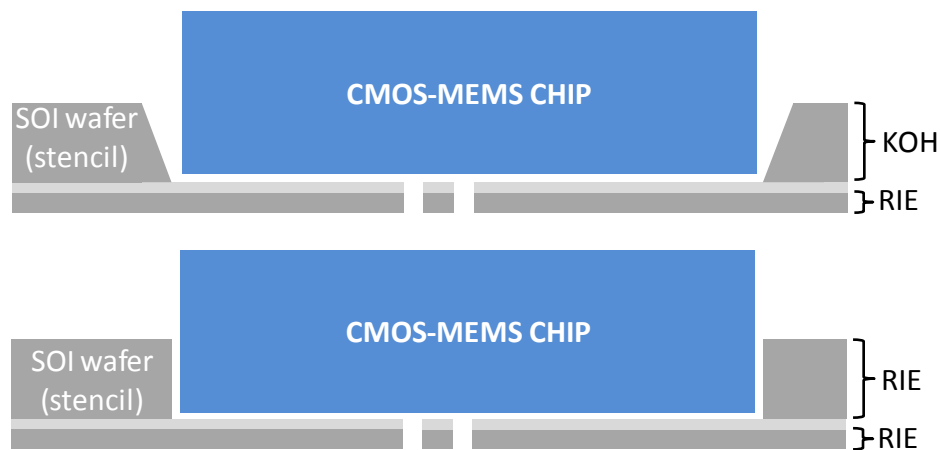


Figure 80.- Fabrication approaches of the stencil masks: KOH or RIE for chip placement and RIE for the deposition windows. An additional etching step based on HF is required to remove the silicon dioxide of the SOI wafer. The design of the stencil is based on place the chip within it and the deposition windows are self aligned with the 0-level packages MEMS.

The fabrication process of each stencil requires two photolithographic processes (two masks) one for each silicon layer of SOI wafer, *Figure 81*. The silicon of each layer is etched through the patterns defined by the resin with KOH or RIE depending upon the layer. The KOH solution stops when the silicon dioxide layer is reached. On contrary the RIE etching is controlled by time allowing higher control over the depth despite of critical stopping. The middle silicon dioxide remaining is etched through standard HF solution.

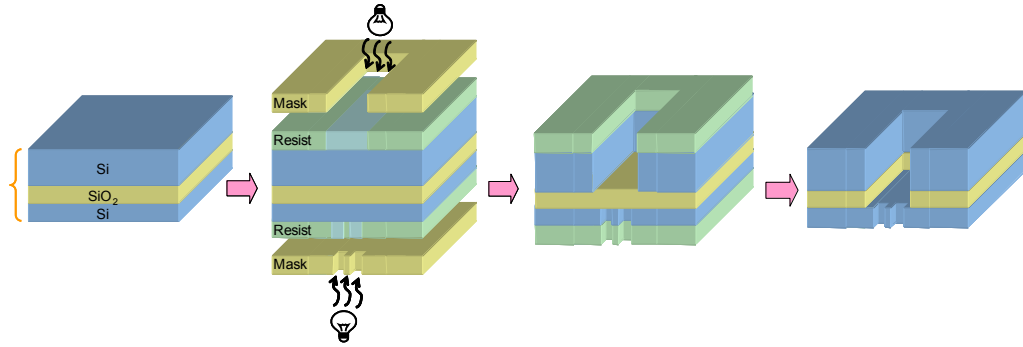


Figure 81.- Fabrication process of the stencils. In the third step the top silicon is etched with KOH or RIE.

In the *Figure 82* it is shown an example of the stencil mask on top of the chip layout, the stencil represented by solid green grease, protect the whole chip from the deposition process leaving only the sealing window devices opened.

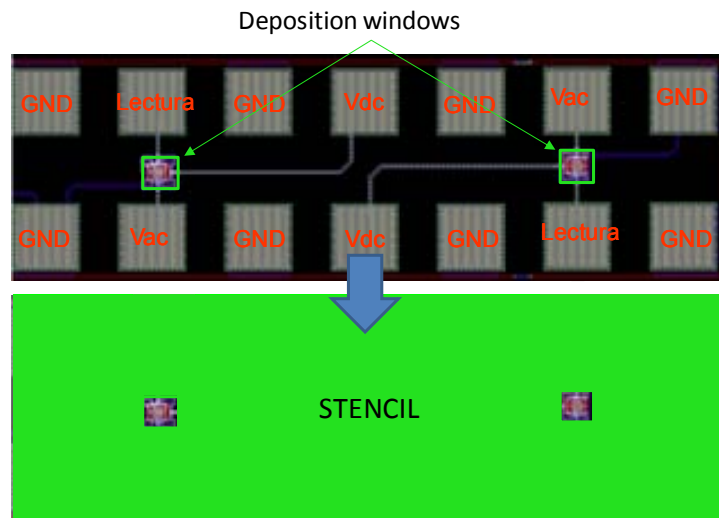


Figure 82.- The stencil represented by solid grease is positioned on top of the chip layout leaving only the deposition windows opened.

The two masks which will be used in the fabrication of the stencil must contemplate for one side the size of the whole chip and for the other the size and the position of the deposition windows, the mask is the same for the RIE and KOH stencil allowing enough space to include several versions of different windows. In order to obtain the size of the chip, some samples are measured with a microscope with 20X lens through measuring software. The mean of length side is $3916.14\mu\text{m}$ and for the width side is $2972.84\mu\text{m}$, the standard deviation is $3.57\mu\text{m}$ and $1.67\mu\text{m}$ respectively. As one of the stencils is fabricated with KOH which is anisotropic silicon etchant the angle of the etching in the wafer must be taken into account in the design of the stencil layout. The SOI wafers available are 100 crystallographic orientated with bulk silicon of

475 μm thick, so the etching angle is 54.74° and the over side chip windows is equivalent to 581 μm . Then the size of the chip windows are 2972 μm by 3916 μm and 3553 μm by 4391 μm for RIE and KOH stencils respectively. For the standard deviation obtained in the sizes of the chips, the established tolerances of the chip windows are $\pm 3\mu\text{m}$, $\pm 6\mu\text{m}$ and $+9\mu\text{m}$. Regarding the deposition windows the PAD opening in the chip layout is equal to 15x15 μm^2 however the post CMOS wet etching process increase the size of the opening PAD. Then different deposition window sizes of 30x30 μm^2 , 35x35 μm^2 , 40x40 μm^2 , 45x45 μm^2 and 50x50 μm^2 are included in the corresponding mask to assure a whole covering of the opening PAD and seal the package. The two masks superposed with the alignment marks are shown on *Figure 83*.

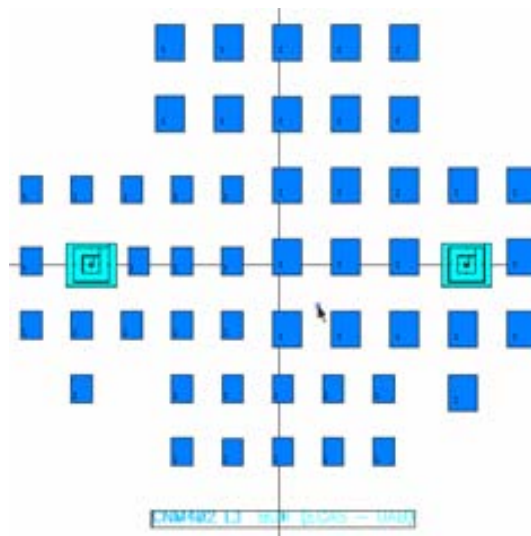


Figure 83.- Chip mask and opening window mask to fabricate the stencil.

During the fabrication of the KOH stencils a problem with the solution has produced enlargement of the chip windows destroying the auto alignment capability of these stencils. On the contrary the RIE stencils were correctly fabricated. The chip window that fits the size of the testing chip is the bigger one (2981 μm by 3925 μm) with opening deposition windows of 50x50 μm^2 . The chip is placed on the stencil and a deposition of 1 μm of aluminum is done with PVD sputtering. After the deposition the optical characterization shown that the deposited aluminum is placed at the opposite end of the desired position due to a mirror defect in the opening window mask. Furthermore, SEM analysis (*Figure 84*) has displayed that the size of the deposited aluminum is bigger than the opening window designed (70x70 μm^2 instead of 50x50 μm^2) because the chip does not fit perfectly producing a small space between the chip and the stencil which enhance the size of the deposited aluminum. Additionally the relative position of the square aluminum deposited has been displaced 50 μm in both axes respectively from the desired position, (a, b) *Figure 84*. So if there had not been mirroring effect the opening windows neither had been well aligned. This effect critically in this approach is produced by the differences in cutting the chip samples. Although the mean size of the

chip is approximately the same for all samples (taking into account the standard deviation), the position of the fabricated layout with respect to the edges of the chip is different enough to not allow the auto alignment capability. This problem is easily solved working with entire wafers (as massive production works) but in our case for research purposes a chip process has to be made.

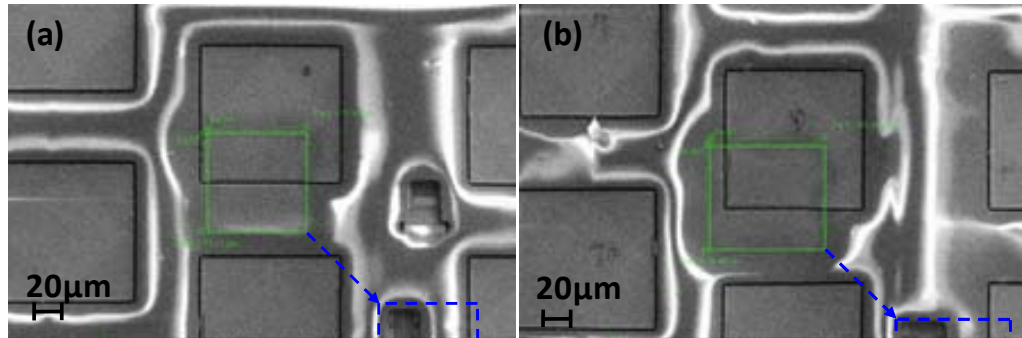


Figure 84.- (a,b) SEM images of the oversized deposited square aluminum in solid line and their theoretical position in dashed line.

B. SEALING WITH STENCIL AND MANUAL ALIGNMENT

The stencil has not been useful in their initial purpose, but the deposition windows are correctly fabricated and can be exploited in a different way. The manual alignment concept is based on the positioning through a microscope of the stencil windows on top of the packaged MEMS, fix the chip with the stencil and proceed with a metal deposition to seal the package.

The stencil is mounted on two probe holders which have three axis positioning capability. The chip is fixed on a piece of a wafer and placed on the holder of a probe table which also has three axis of movement and a vacuum sucker to let fixed the sample. The probe table has a microscope with three lenses with magnifications of 10X, 50X and 100X. The alignment process begins with the positioning of the stencil windows in relation with the microscope field so that the vision through them is possible. Then the chip is positioned at 5mm of vertical distance from the stencil and with the XY micrometers of the holder the correct position of the package is found as it can be seen on the (a) image of the *Figure 85*. After that the stencil and the piece of wafer with the chip are stuck together with silicone melt which is vacuum compatible and can withstand temperatures below 100°C. The alignment is checked again and the prototype is ready for the deposition of 700nm of aluminum with PVD evaporation.

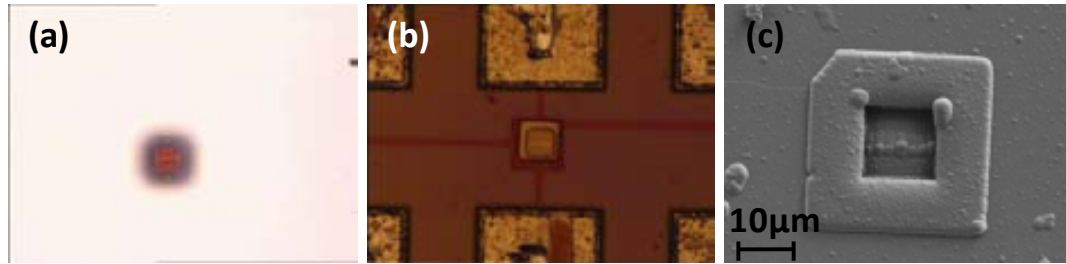


Figure 85.- (a) Optical image of the stencil (in white due to light reflection of the silicon surface) with the package correctly aligned below them; (b) Optical image of the selective deposition of the 700nm layer; (c) SEM image of the package.

After the deposition of the metal layer has been made the stencil and the piece of wafer are separated with a hot air gun and the result is checked optically and with a SEM microscope, (b, c) of Figure 85. The alignment of the deposited metal layer has been successful and the holes are completely covered.

C. SEALING WITH ELECTRON-BEAM LITHOGRAPHY (EBL)

After testing the two previous approaches a more complex process is adopted, using lithography process to protect the electrical pads during metallization. Standard lithography techniques require alignment between the mask and the sample, the same problem as we had previously. Using lithography based on electron beam devices allow to align directly on the sample with resolutions on the nanometers range. In the previous paragraph it was demonstrated that a thickness larger than 500nm is required to completely seal the holes of the package. The fabrication process is depicted on the Figure 86, first some different layers of resin are deposited, the resin is exposed with electron beam, the resin is revealed, the metal is deposited and finally a lift-off of the resin let only the metal layer.

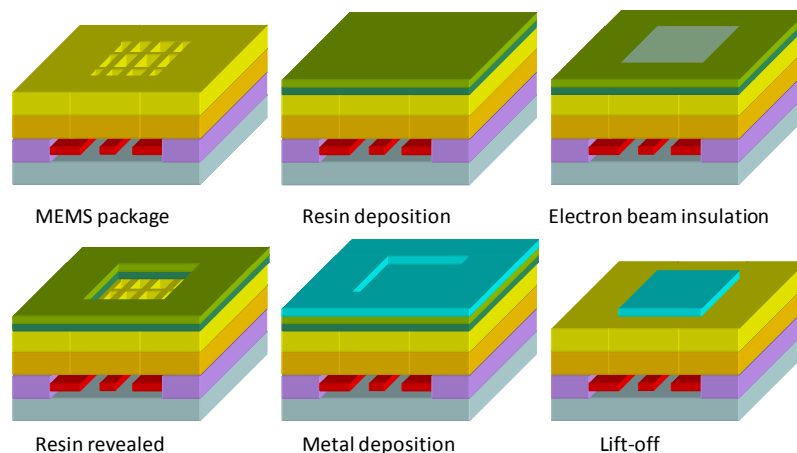


Figure 86.- Package sealing process with EBL techniques.

The whole process is done at the clean room of the CNM through the GICSERV project called “Sellado y caracterización de dispositivos CMOS-MEMS encapsulados mediante procesos fotolitográficos para la protección de los pads eléctricos”. The required thickness of the metal layer implies that more of one layer of resin must be used. There are two different resins available from MicroChem, PMMA (polymethyl methacrylate) and MMA (methyl methacrylate) with the deposition film thickness versus spin speed graphs of the Figure 87. The total thickness is established to 700nm and taking into account a spin speed of 1500rpm three layers of MMA and two of PMMA are required, [MChem].

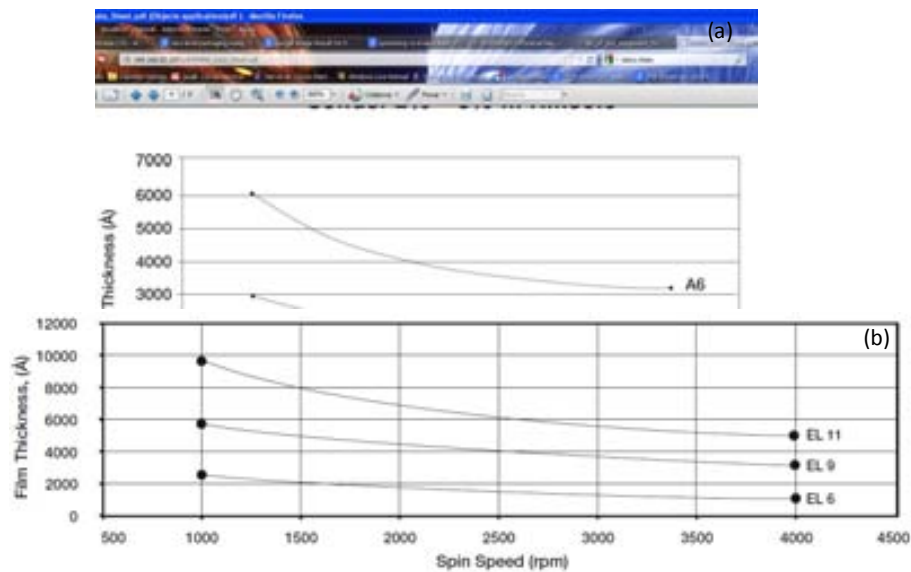


Figure 87.- Resins films thickness versus spin speed graphs for resins [MChem]: (a) 495PMMA A2; (b) MMA8.5 EL 6.

The resins are deposited in a spinner at 1500rpm during 60 seconds and the drying is done in a hot plate at 180° during 60 seconds. After that the samples are placed on the SEM vacuum chamber and square windows of 15 μm^2 are insulated with voltage acceleration of 15kV and a current of 192 μA . Later the resin is revealed with MIBK (methyl isobutyl ketone). Then the layer of 700nm of aluminum is deposited with PVD sputtering. Finally the lift-off process is applied which consists on a solution of hot acetone with ultrasonic vibrations. In the Figure 88 there are shown optic (a) and SEM (b) images of the result obtained on the sample. The window is correctly aligned on top of the package however their size is 40% smallest than the opening pad. Also there is still some resin not enough revealed (on the optical image is transparent) and the remaining aluminum from the lift-off is around it. The total thickness of the resin plus the metal deposited makes the lift-off process very challenging with the class of resins available.

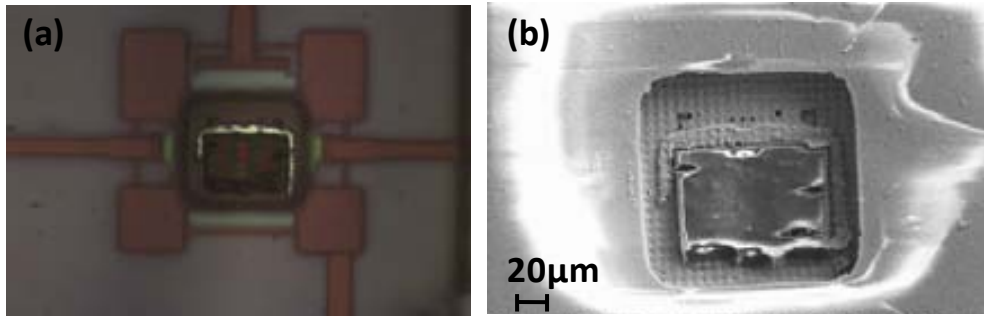


Figure 88.- Optical and SEM images of the deposited aluminum with EBL lithography.

D. SEALING WITH ELECTRON-BEAM INDUCED DEPOSITION

This other approach is based on the use of electron beam in a cavity filled with some precursor gas to induce the deposition of material on the sample with a resolution in the range of nanometers. The use of electron beam tools allows a perfect alignment. The instrument with EBID³⁰ capability is the same that has the FIB tool, and the induced deposition could be made with electrons or ions. Nevertheless the ions sputter the surface and may alter our package. The SEM image (a) of the Figure 89 shows packaged CCB resonator before proceed to seal the first row of holes, the perpendicular direction of deposition with respect to the MEMS resonator avoid the secondary electrons deposition on the first metal layer. The material deposited is 40% aluminum from an organic molecule. The final top view result is shown on (b) image of the Figure 89 where the holes are perfectly sealed and the package has not suffered any damage.

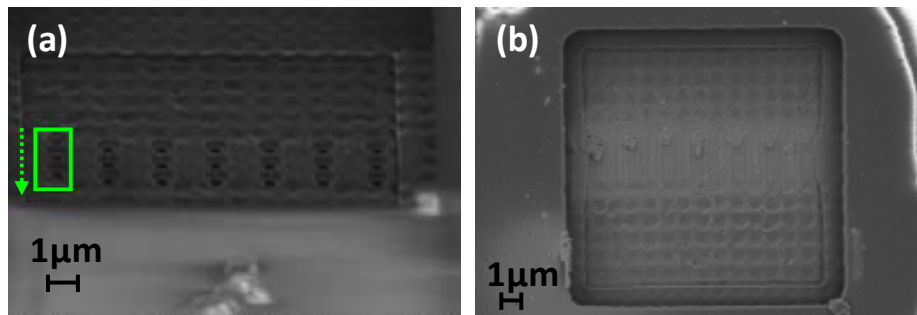


Figure 89.- (a) SEM image of the package with green detail of the direction of deposition. (b) Package correctly sealed with EBID method.

³⁰ Electron-beam induced deposition

E. SEALING WITH LASER LITHOGRAPHY

The last method employed to try to seal the package includes the use of a laser micro writer from Durham Magneto Optics LTD [DMO] which is capable to optically align the sample with a mask with a resolution of $1\mu\text{m}$. The patterns are drawn in a software GDSII mask, the same format as the masks used in CMOS fabrication. The resolution is much lower than the resolution provided by EBL method but is highly enough for the purpose of sealing the package with a rectangular metal window. The micro writer laser is property of ICMAB (CSIC) and is placed in the photolithography laboratory of the clean room operative since January 2011.

The process begins with the chip sample sticked with the same resin of the photolithography process in a piece of wafer because the smallest chuck of the spinner is higher than the size of the chip. After that the positive photoresist Microposit Shipley S1813 [MShip] is deposited and spun with 7500 rpm/s of acceleration reaching 5000rpm of speed during 25 seconds to obtain a thickness of $1\mu\text{m}$. Then the resin is soft baked at 95°C during 1 minute and the sample is placed on the micro writer sample plate. The micro writer tool has 19 different semiconductor lasers, 17 of which are used for exposing the sample and 2 are used for focus and alignment. The GDSII mask employed is composed of two different layers: one corresponding to the metal pads to perform the alignment and the other with the rectangular windows on top of the MEMS packages.

In order to correctly align the mask with the sample three pads of the edges of the chip are used and the alignment is checked. The laser tool provides three different laser resolutions to insulate the sample, $1\mu\text{m}$, $5\mu\text{m}$ and $10\mu\text{m}$ and allow different exposing doses. The election of these parameters will affect to the total exposition time and the shape of the exposition. After the laser exposition the resin is revealed with Microposit developer MF-319 solution during 45 seconds. Then the rectangular windows are checked with optical microscope and the process is repeated until the correct parameters are found. The final opening windows revealed on the resin for different packaged resonators are depicted on (a, b, c, d, e) images of the Figure 90. It is remarkable that in most cases the opening windows larger than the opening PAD window are correctly revealed. However in the (b) picture of the Figure 90 the size of the window does not cover the entire package and additionally around the opening the surface is rough indicating that higher dose or more exposing or revealing time are required. This fact comes from the tremendous difficulty to deposit a constant thickness resin layer over a small chip with different heights (passivation, metal pads, metal cover packages...) which makes vary the optimal conditions in function of the region of the chip.

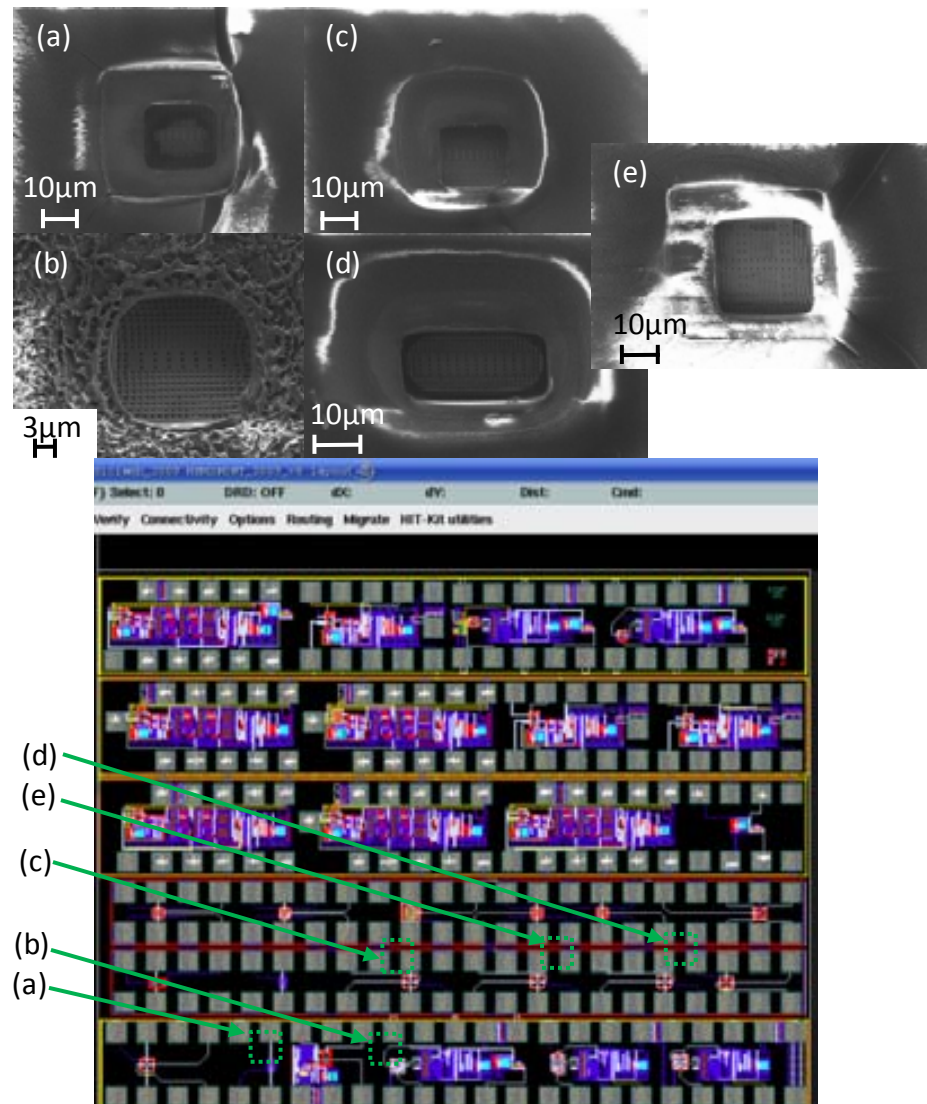


Figure 90.- SEM images of the windows revealed on the deposited resin layer and their corresponding position on the chip layout: (a, b, c) packaged CCB resonators, (d) packaged DETF, (e) packaged Free-Free.

The next step consists on depositing an aluminum layer with a thickness of 750nm and performs the lift-off as it was explained in previous sections. The obtained rectangular metal windows on top of the packages are observed in the *Figure 91*. It is remarkable that finally the sealing of the package has been accomplished with photolithographic methods with critically alignment problem. Unfortunately the sealed resonators have been tested and no results were obtained so the devices which have been working previously to the sealing process could be collapsed during the lift-off process.

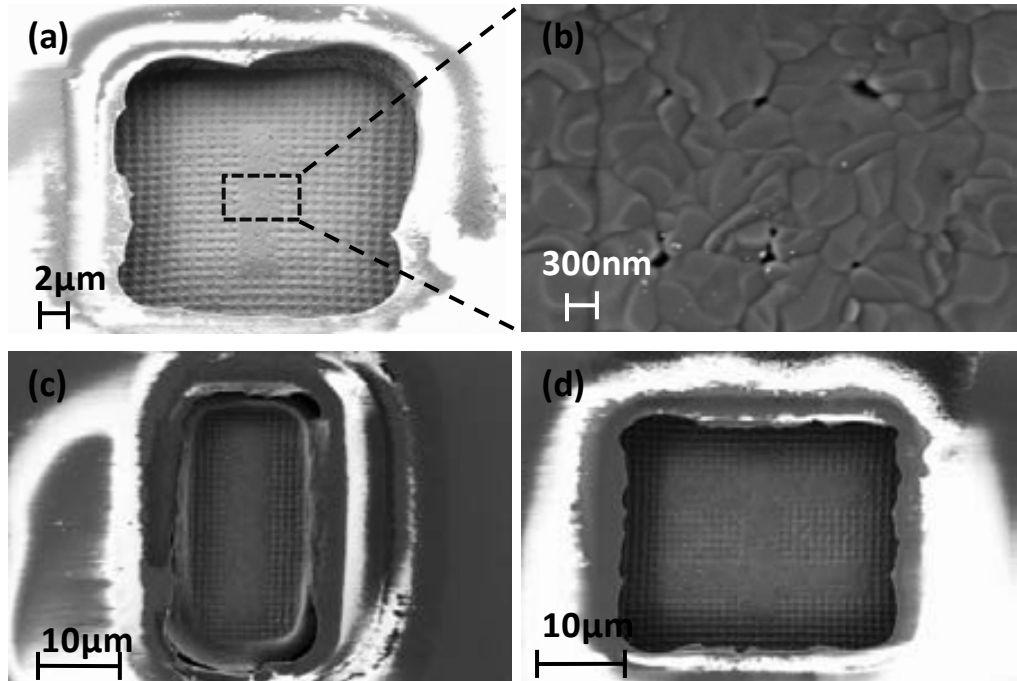


Figure 91.- SEM images of the deposited metal windows on the packaged resonators: (a,b) CCB packaged sealed with a zoom detail of the apparently remaining holes, (c) DETF packaged sealed, (d) Free-Free packaged sealed.

3.4.5. SEALING VALIDATION

From the successful sealing deposition approaches FIB cuts are performed and shown in the Figure 92. The metal layer of a final thickness of 790nm in the center of the window is correctly deposited on top of the second metal layer completely sealing the holes. It is also noteworthy that the aluminum has not been penetrated to the first metal layer and so on over the resonator. In this device the resonator is still covered with silicon dioxide and no vibration could be excited.

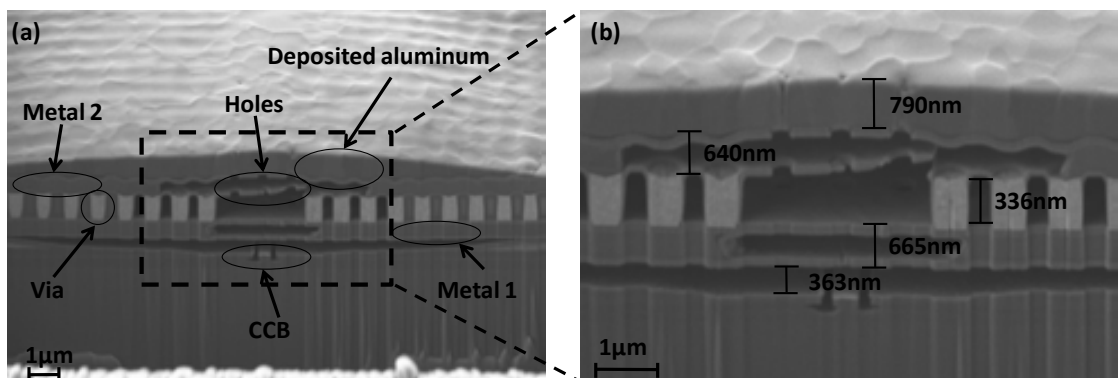


Figure 92.- SEM images of a FIB cut from the packaged and sealed CCB. (a) The metal layer of 790nm is clearly observable on top of the second metal layer. (b) The holes are completely sealed and there is no metal contamination inside the package cavity although the resonator is not fully released.

Another sealed CCB resonator was electrically tested (Figure 93) and keeps working but no vacuum is still present in the cavity because the quality factor around 40 corresponds to standard air pressure. The graph of Figure 93 gives a comparison between the same resonator before and after sealing demonstrating that the resonance frequency has not changed so no sealing material has been pass through the first metal cover layer.

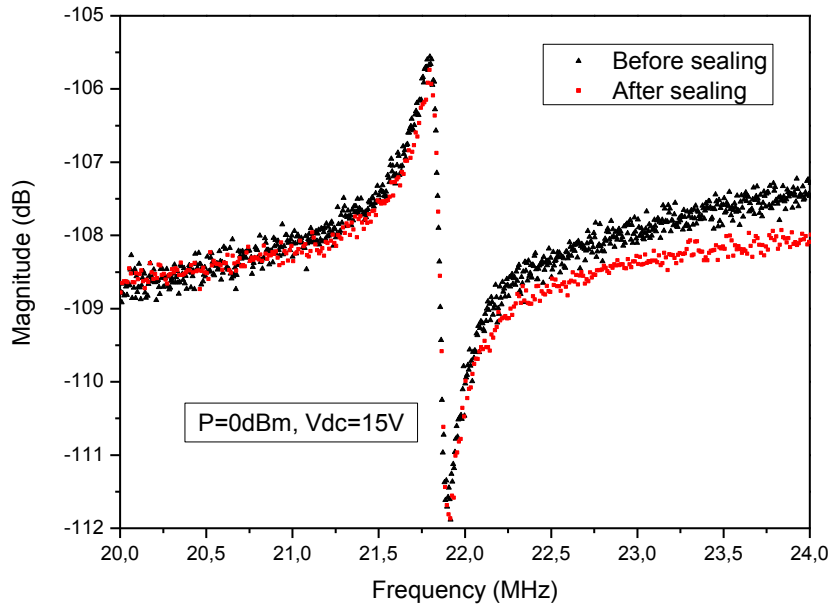


Figure 93.- Magnitude response of the CCB packaged and sealed.

Despite of vacuum is not sustained inside the package cavity we can state that the CMOS-MEMS resonator is packaged and protected for further wafer processing such as dicing and first level or chip-scale packaging. Additionally the proposed method avoids the use of RF feedthroughs on the vacuum sealing enhancing [Che09] the performance for RF MEMS resonators. The compact volume and simple additional post-CMOS processes needed with vacuum capability give very competitive value to our approach in order to be introduced in the market. The following *Table 6* gives the summary of the different packaging approaches presented, highlighting the capping material, the packaging approach, the additional processes to fabricate the package (regardless the fabrication or releasing of MEMS) and the final size of the whole MEMS device with the package. Our package approach can get the best volume size with metal material and can be applied to different MEMS resonator structures (cantilever, tuning fork, disk, etc) and to different structural layer materials used in standard CMOS technologies (i.e. metal).

Reference	Capping material	Approach	Additional processes	Size (μm)
[Can03]	Si	Integrated package	L+D+E	300 x 200
[Wan06]	Si	Separate lid	L+D+E+WB	1000 x 1000
[He06]	Al_2O_3	Integrated package	L+D+E	1325 x 975
[Verh08]	SiOC	Integrated package	L+D+E	50 x 50
[Fed08]	Si	Integrated package	L+D+E	500 x 100
This work	Al	CMOS integrated package	L+D	25 x 25

Table 6.- Comparison between different package fabrication approaches. The additional fabrication processes for the package are: L (lithography), D (deposition), E (etching), WB (Wafer Bonding).

3.5. NANOCANNELS

From the experience obtained working in the design and characterization of MEMS packages a totally different concept has been matured using metal layers from the CMOS technology. The idea is to use two metal layers in conjunction with strategically shaped and placed vias to develop integrated nanochannels for microfluidics. These nanochannels could be also integrated on a MEMS resonator and could provide a different way for sensing purposes on a liquid medium, *Figure 94*. In fact recently some examples of resonators with built-in μ channels have been already presented [Bur07, Bar10, Lee10, Arl10]. Mainly the goal for these approaches is to overcome the low quality factor achieved when the resonator is in a liquid media and thus the low frequency stability which degrades the final resolution in bio and chemical sensors. Nanomechanical resonators operating in vacuum are capable of detecting and weighing single biomolecules, but their application to the life sciences has been limited by viscous forces that impede their motion in liquid environments. A promising approach to avoid this problem, encapsulating the fluid within a mechanical resonator surrounded by vacuum, has not yet been tried with resonant sensors of mass less than $\sim 100\text{ng}$, despite predictions that devices with smaller effective mass will have proportionally finer mass resolution. In our case, in which an electrostatic excitation and capacitive detection are employed, the use of CMOS integrated small size resonators with embedded μ channels will allow the sensing in liquids without the problem of the damping and thus providing a quality factor only dependant over the air pressure being capable to operate in vacuum conditions with highest quality factors. The method is also capable to provide higher thickness resonators composed by stacking different layers similar than the approaches presented by the Taiwan group [Che11].

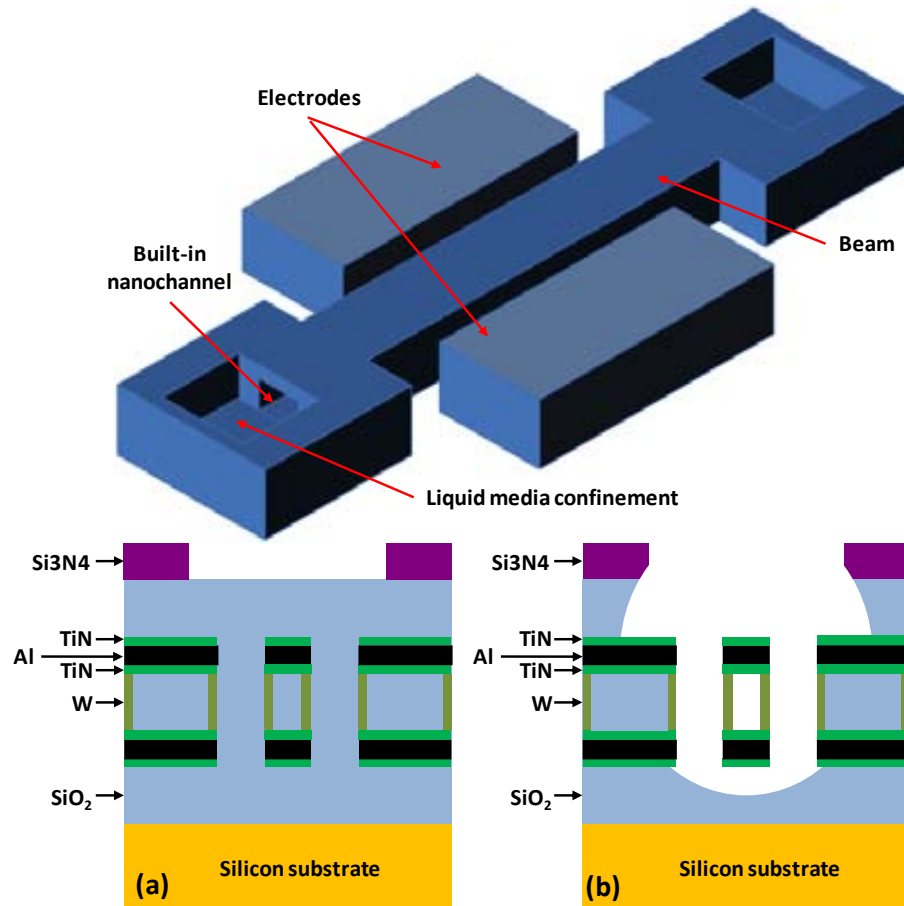


Figure 94.- Conceptual diagram and fabrication process of the built-in nanochannel in a CCB resonator with electrodes for actuation and detection of the first flexural in-plane mode. In the process before (a) and after (b) releasing, the resonator and electrodes are composed by two metal layers and via walls. The metals are composed by a stack of TiN, Al and TiN whilst the vias are from W. The releasing process etch the silicon dioxide from the surroundings of the beam and also the silicon dioxide from the channel due to the openings placed on the anchors which confine the wet etching solution.

From the concept two different test approaches without electrodes were designed and fabricated. The difference between the two layouts depicted on image (a) from Figure 95 is related with the shape of the intermetal via: filled rectangular or ring rectangular. The SEM image (b) of Figure 95 corresponds to both fabrication approaches after wet etching process of 28 minutes. Both CCB have a length of $32\mu\text{m}$, a width of $5\mu\text{m}$ and expected channel width of $4\mu\text{m}$.

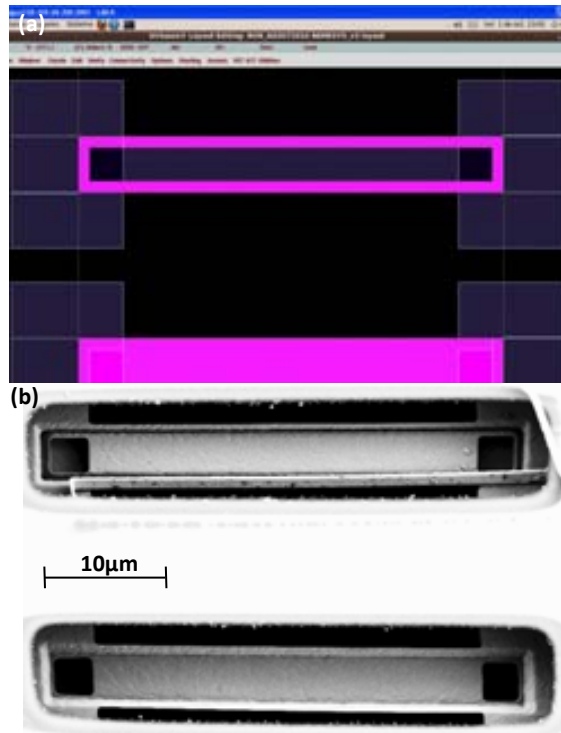


Figure 95.- (a) CCB (length of $32\mu\text{m}$ and width of $5\mu\text{m}$) with built-in channel (width of $4\mu\text{m}$) test layouts, the two metals are bonded through different via shapes; (b) fabricated and released test designs.

In order to check the final fabricated devices a FIB cut is made on a sample chip and after that a wet etching is performed to remove the surrounding silicon dioxide. The SEM images of the two nanochannel approaches are shown on the *Figure 96*. In (a) image placing a filled rectangular via has removed the silicon dioxide between the two metal layers during the CMOS process. So the two metals are in contact without a separation. In the second approach shown on (b) image there is a channel made from the two metals and via walls with $4\mu\text{m}$ width and 780nm of height.

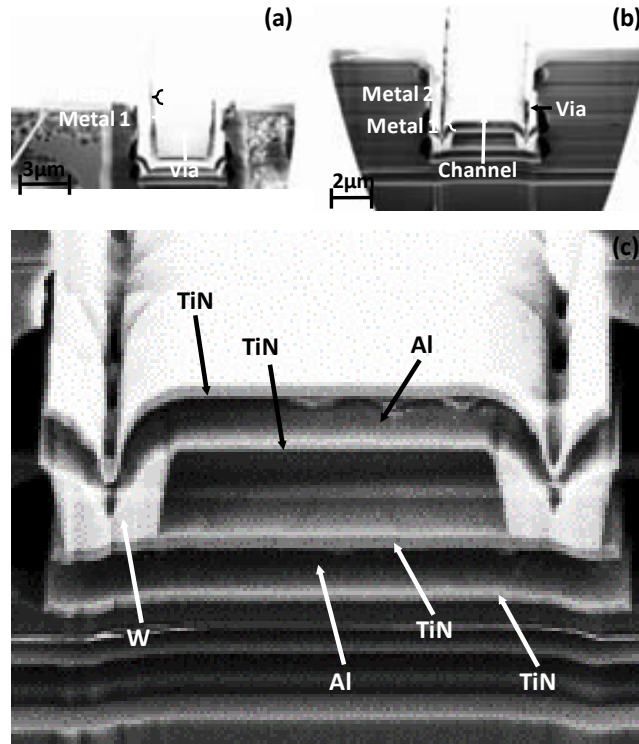


Figure 96.- SEM images from FIB sections made on both CCB with built-in nanochannel test devices: (a) rectangular filled via, (b) ring rectangular via, (c) zoom detail showing the materials of each layer.

After the fabrication approach has been tested and the shape of the via has been established another chip was fabricated. In this one the second approach of the shape of the via is applied on CCB structures with driving and sensing electrodes. In the same RUN there were included several different metal CCB design test layouts with built-in nanochannel (decreasing width, length, gaps, metals, etc) only for fabrication testing purposes (without driving electrodes) in order to establish the most suitable combination of metals and dimensions of the beam and channel. The layout of the *Figure 97* present the two designs: (a) CCB made by metal 1 and metal 2 with a length of $20\mu\text{m}$, a width of $4\mu\text{m}$, a channel width of $3\mu\text{m}$ and a gap of 650nm ; (b) CCB composed by metal 3 and metal 4 with a length of $10\mu\text{m}$, a width of $1.45\mu\text{m}$, a channel width of 450nm and a gap of 650nm . The image (c) shows a detail zoom where the thickness of TiN and Al could be extracted obtaining 100nm . From the dimensions and thickness of each layer the computed frequencies for first lateral in plane mode are 6.1MHz for the larger CCB and 5.5MHz for the shorter. It has been assumed that the channel is filled with silicon dioxide and the young modulus and density for each layer (the same for all metals) are: $E_{\text{METAL}}=131\text{GPa}$, $E_{\text{VIA}}=411\text{GPa}$, $E_{\text{SiO}_2}=73\text{GPa}$, $\rho_{\text{METAL}}=3000\text{kg/m}^3$, $\rho_{\text{VIA}}=19250\text{kg/m}^3$ and $\rho_{\text{SiO}_2}=26340\text{kg/m}^3$.

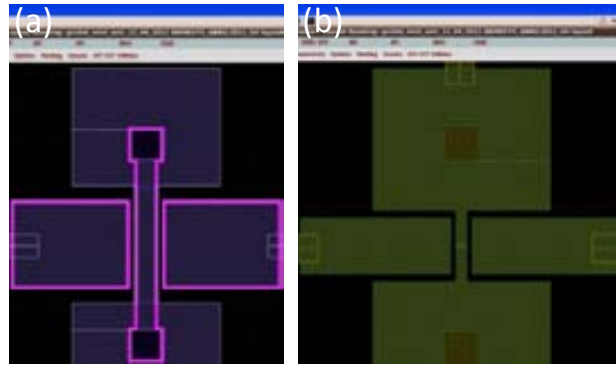


Figure 97.- Metal MEMS resonators with embedded nanochannels: (a) metal 1/metal 2 CCB with a length of $20\mu\text{m}$, a width of $4\mu\text{m}$ and a gap 650nm ; (b) metal 3/metal 4 CCB with a length of $10\mu\text{m}$, a width of $1.45\mu\text{m}$ and a gap of 650nm .

In the Figure 98 there are depicted the SEM images obtained from the two resonators after BHF wet etching process of 54minutes. The longest resonator has 700nm via walls width and the embedded nanochannel has $3\mu\text{m}$ width and 900nm channel height. The shortest resonator has 320nm channel width and 900nm channel height. In the resonator of the Figure 98 (c,d) the electrodes have been disappeared during the wet etching process. The smallest resonator has a channel width lower than the 450nm designed making a submicron channel fully fabricated with standard CMOS technology.

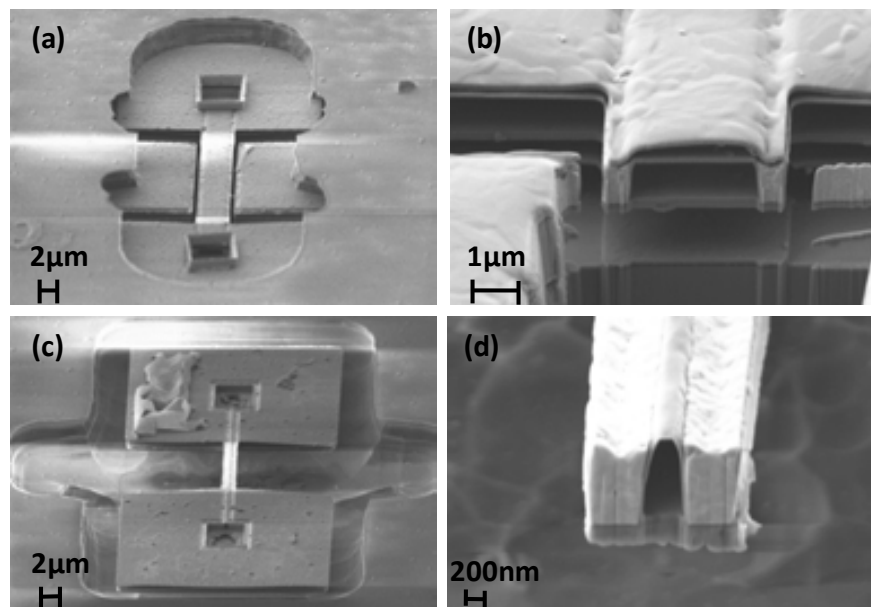


Figure 98.- CCB with driving electrodes and built-in channel: (a, b) metal 2 with metal 3 with a length of $20\mu\text{m}$, a width of $4.4\mu\text{m}$, channel width of $3\mu\text{m}$, channel height of 900nm and gap of 650nm ; (c, d) metal 3 with metal 4 with a length of $10\mu\text{m}$, a width of $1.72\mu\text{m}$, channel width of 320nm , channel height of 900nm and gap of 650nm .

An additional cross section cut was performed on one side of the largest CCB, *Figure 99*. In the middle of the resonator there is still some remaining silicon dioxide. However it has been demonstrated that the approach is capable to confine and guide the HF based solution through the channel and the whole releasing is only a matter of additional etching time.

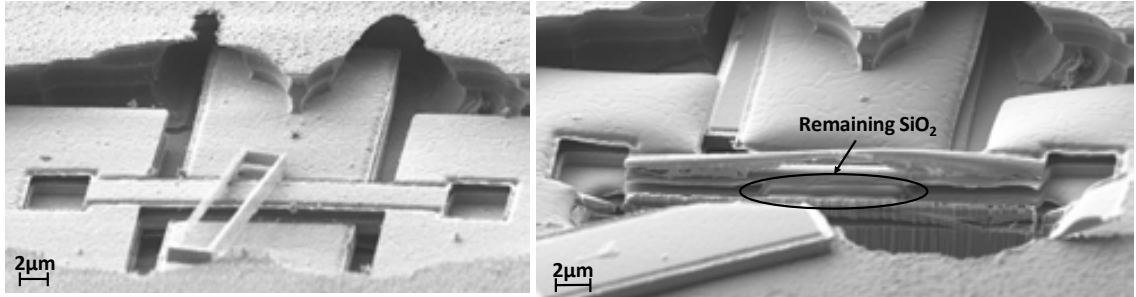


Figure 99.- Lateral cross section from CCB with built-in channel showing that it is not fully etched from SiO₂.

In order to corroborate the materials involved in the nanochannel, EDX³¹ spectroscopy is performed. The result shown on *Figure 100* provides the evidence that the material is tungsten with a 60.8% of concentration. There is also detected a 13.2% of titanium and a 3% of aluminum from the top and bottom metals. Finally, some traces of gallium (3.4%) implanted during the FIB cutting are detected.

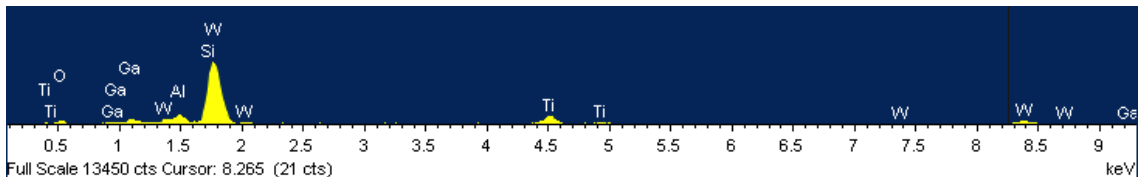
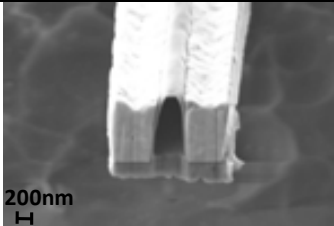




Figure 100.- EDX spectroscopy result made on one wall of the smallest nanochannel.

Knowing all the materials from which the resonator is made and the dimensions extracted from the SEM images, the total mass of the resonator could be computed in order to compare our approach with other designs. The total mass for the shortest resonator is 309pg, composed by 242pg from the wolfram walls and 67pg from the metal covers. From the cross section (d) of *Figure 98* it appears that the inner channel is composed only by TiN, so supposing that the wolfram walls could be removed the final mass for a TiN channel (thickness of 100nm and $\rho_{\text{TiN}}=5220\text{kg/m}^3$) of 320nm width and 900nm height will be of 13pg. This huge reduction could provide extremely low mass resolution with CMOS integration capability.

³¹ Energy-dispersive X-ray spectroscopy

The following *Table 7* gives a comparison between three different built-in channel approaches. Our approach provides a mass on the order of 100pg with TiN material (biological compatible) integrated in a CMOS technology with the easiest resonator transduction. The calculated resonator masses for the other approaches were made assuming a length of 10 μ m

Device		Materials	Built-in channel			Resonator transduction	Integration capabilities
			width (nm)	height (nm)	resonator mass* (pg)		
This work		TiN (all around), W (walls)	320	900	309	Electrostatic and capacitive readout. Monolithically integrated in CMOS	Standard CMOS
[Bar10]		Si ₃ N ₄ (all around)	650	107	16	Optothermal actuation and optical detection	Difficult
[Bur07, Lee10]		Si	2000	700	50000	Electrostatic actuation and optical-lever detection	Difficult

*Table 7.- Summary over the parameters of different MEMS resonators with built-in nanochannel. *The mass was computed assuming a resonator length of 10 μ m, $\rho_{Si_3N_4}=3200\text{kg/m}^3$ and $\rho_{Si}=2330\text{kg/m}^3$.*

3.6. CONCLUSIONS

In this chapter the fabrication of CMOS-MEMS was presented, detailing state of the art approaches. The fabrication method employed by our group is also explained, highlighting the challenges to face up and the provided capabilities. The main goal of the present chapter was to design, fabricate and characterize a vacuum sealing packaged for CMOS-MEMS resonators. Some design and fabrication strategies had been showed being our integrated package the smallest one with only few additional processes required. Different MEMS devices were packaged and had been successfully tested, demonstrating the reliability of the method. It has also been introduced the concept and design of MEMS resonators with built-in channels which could have good performance sensing capabilities in microfluidic related applications.

The transduction method used to sense the motion of micromechanical system is a key issue regarding subjects such as size, power handling, cost, etc. The objective of the present chapter is to establish the limits for capacitive sensing due to both the dimensions reduction and the increase of resonance frequency. We will find the transduction gain for our capacitive transduction system emphasizing the problems associated with read-out system. The chapter includes an explanation of the capacitive sensing method in MEMS and exposes the electrical measures obtained for different topologies of resonators. The MEMS resonators presented in this chapter were fabricated on standard CMOS technology AMSC35B4 using the two polysilicon layers as it has been explained in the previous chapter.

Figure 101.- CCB with two electrodes capacitive sensing.

Capacitive transduction has some similarities compared to electrostatic actuation, an electrode is placed on a side of the structure in order to obtain a variable capacitor which will induce a current dependant with the motion of the MEMS. The Figure 101 illustrates the two driver configuration for electrostatic actuation through the right electrode and capacitive sensing through the left electrode. Capacitive sensing is also possible with only one actuation electrode monitoring the current generated in the structure of the MEMS however the one port configuration has the serious drawback that the same excitation signal is directly coupled to the flowing current of the structure through the capacitor.

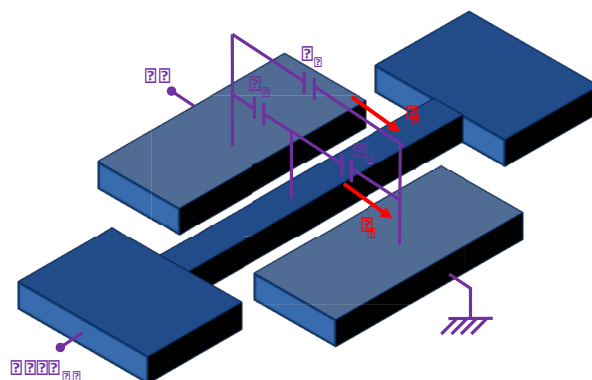


Figure 101.- CCB with two electrodes capacitive sensing.

Using the same definitions of the second chapter for the capacitors and voltages, [2.88-2.91] the current in a capacitor is defined as the time derivative of the product of the voltage and the capacitance, [4.112]. For standard electrostatic excitation and

capacitive sensing the V2 signal is set to 0 and the motional current obtained will be reduced to the third term only dependant over the DC voltage, the capacitance C_R variation (which in small displacements is approximated by C_0/g as same as on [2.97]) and the variation of the movement, [4.111].

$$I_m = \frac{\partial(C_R \cdot V_R)}{\partial t} = C_R \frac{\partial V_2}{\partial t} + V_2 \frac{\partial C_R}{\partial u(x)} \frac{\partial u(x)}{\partial t} + V_{DC} \frac{\partial C_R}{\partial u(x)} \frac{\partial u(x)}{\partial t} \quad [4.110]$$

$$I_m = V_{DC} \frac{\partial C_R}{\partial u(x)} \frac{\partial u(x)}{\partial t} \cong V_{DC} \frac{C_0}{g} \frac{\partial u(x)}{\partial t} = \eta_r \frac{\partial u(x)}{\partial t} \quad [4.111]$$

Where η_r is the electromechanical coupling factor for sensing expressed as [4.112] like the ratio between motional current and variation of movement with the units of C/m.

$$\eta_r = \frac{I_m}{\partial u(x)/\partial t} = V_{DC} \frac{C_0}{g} \quad [4.112]$$

As it was explained in previous chapters for $V_2=0$ the most important term of the [2.94] force, is the last one which depends on the signal V1 and V_{DC} enabling excitation force at the same frequency than the electrical signal V1 with a magnitude bigger than the first term as the two signals are multiplied and $V_{DC} \gg V_1$. This force term is rewritten in equation [4.113] with the equivalent approximation for small displacements and using the electromechanical coupling factor of [2.98].

$$F_x = -V_1 \cdot V_{DC} \frac{\partial C_E}{\partial u(x)} \cong -\eta_e \cdot V_1 \quad [4.113]$$

From equation [2.86], near to the natural resonance frequency ($\omega=\omega_0$) it can be demonstrated that the equation [4.114] is applicable. Then, the time derivative of the position is computed obtaining a time derivative of the applied force [4.115].

$$k \cdot |u(x)| = Q \cdot F_x \rightarrow |u(x)| = \frac{Q}{k} F_x \rightarrow \frac{\partial u(x)}{\partial t} = \frac{Q}{k} \frac{\partial F_x}{\partial t} \quad [4.114]$$

$$\frac{\partial u(x)}{\partial t} = \frac{Q}{k} \frac{\partial F_x}{\partial t} = -\frac{Q}{k} \eta_e \frac{\partial V_1}{\partial t} \quad [4.115]$$

Substituting the result of [4.115] in the equation [4.111] the equation [4.116] for the output current is obtained. From the defined electromechanical coupling factors on [2.98] and in [4.112] it can be seen that for symmetric electrodes both of them are equal.

$$I_m = -\eta_r \eta_e \frac{Q}{k} \frac{\partial V_1}{\partial t} \quad [4.116]$$

Thus the maximum motional current if $V1 = V_{AC1} \sin(\omega_0 t)$ is:

$$I_m = -\eta^2 \frac{Q}{k} \frac{\partial V1}{\partial t} = \eta^2 \frac{Q}{k} V_{AC1} \cdot \omega_0 = \left(V_{DC} \frac{C_0}{g} \right)^2 \frac{Q}{k} V_{AC1} \cdot \omega_0 \quad [4.117]$$

From the electromechanical sensing coupling factor of [4.112] and setting the vibration signal as $u(x) = x_0 \sin(\omega_0 t)$ a new parameter called transduction gain [4.118] is defined. The transduction gain gives figure of merit in A/m units to bring a comparison between different resonator MEMS structures.

$$\eta_e = \frac{I_m}{\partial u(x)/\partial t} = \frac{I_m}{x_0 \omega_0 \sin(\omega_0 t)} \rightarrow \left(\frac{I_m}{x_0} \right)_{max} = \omega_0 \cdot \eta_r = \omega_0 \cdot V_{DC} \frac{C_0}{g} \quad [4.118]$$

The capacitive sensing method with electrostatic actuation has the major drawback that the capacitive coupling between the excitation electrode and the sensing electrode will produce a direct current proportional to the excitation signal, called parasitic current. The parasitic capacitive coupling comes from different contributions: lateral capacitances and fringing fields between conductors. In the electrical modeling section all the contributions will be described but at this point it will be considered that all the terms are combined on an equivalent parasitic capacitor C_p . The parasitic current obtained is shown on equation [4.119] where it is remarkable the frequency proportional term of this current which means that for devices with high resonant frequencies the parasitic current could easily mask the motional current.

$$I_p = C_p \frac{\partial(V1 - 0)}{\partial t} = -C_p V_{AC1} \omega_0 \cdot \sin(\omega_0 \cdot t) \quad [4.119]$$

The previous expression for the parasitic current is applicable in one or two electrodes configuration, but the configuration of the Figure 101 will have lower parasitic capacitor than the one driver configuration which will have a direct capacitor. The reason is that the beam biased to V_{DC} will attract the field lines from the parasitic signal shielding the output electrode from the parasitic signal. Actually there is still parasitic capacitance in two ports configuration between the two electrodes produced mainly by the fringing fields and from the coupling between output metal pads. Computing the relation between motional and parasitic current, the relation [4.120] is obtained.

$$\frac{I_m}{I_p} = \frac{V_{AC1} \frac{\eta^2 Q}{k} \omega_0}{C_p V_{AC1} \omega_0} = \frac{\eta^2 Q}{k C_p} \quad [4.120]$$

4.2. ELECTRICAL MODELLING

To establish an electrical model for the MEMS resonator the electromechanical coupling factor η is used to relate the mechanical motion with the motional current and the actuation voltage to the excitation force. Then the equation of motion for a forced lumped resonator of the equation [2.82] (rewritten on [4.121] for simplicity) is transformed into equation [4.122] by means of electromechanical coupling factor of [4.112].

$$m_{eff} \frac{\partial^2 u(x)}{\partial t^2} + \gamma_{tot} \frac{\partial u(x)}{\partial t} + k \cdot u(x) = F e^{j\omega t} \quad [4.121]$$

$$\frac{m_{eff}}{\eta} \frac{\partial I_m}{\partial t} + \frac{\gamma_{tot}}{\eta} I_m + \frac{k}{\eta} \int I_m dt = \eta \cdot V_{AC} \rightarrow \quad [4.122]$$

$$\frac{m_{eff}}{\eta^2} \frac{\partial I_m}{\partial t} + \frac{\gamma_{tot}}{\eta^2} I_m + \frac{k}{\eta^2} \int I_m dt = V_{AC}$$

In the previous equation the three left terms could be related to an equivalent inductance, resistance and capacitance respectively due to their dependence with the motional current as it is shown on the equation [4.123].

$$L_m \frac{\partial I_m}{\partial t} + R_m \cdot I_m + \frac{1}{C_m} \int I_m dt = V_{AC} \quad [4.123]$$

So the mechanical motion of the MEMS for each of the couplings could be represented by an RLC series circuit with the equivalent values of the equation [4.124], [4.125] and [4.126].

$$R_m = \frac{\gamma_{tot}}{\eta^2} = \frac{\omega_0 m_{eff}}{Q \eta^2} = \frac{\sqrt{k \cdot m_{eff}}}{Q \eta^2} = \frac{1}{Q} \sqrt{\frac{L_m}{C_m}} \quad [4.124]$$

$$C_m = \frac{\eta^2}{k} \quad [4.125]$$

$$L_m = \frac{m}{\eta^2} \quad [4.126]$$

As it has been detailed in the previous section the output current is composed by two terms: the motional current described by the RLC circuit and a parasitic current from the parasitic capacitances present between the conductors. In order to model this current the different capacitances have to be described. In the Figure 102 it is shown a section of a CMOS technology with the different layers and the capacitances between all conductors. The resonator is represented in red color with two electrodes on the both sides which are connected through contacts and metals to the output pads. The C_{pp} capacitor represents the coupling between the excitation pad and the sensing pad, as same as the C_{dri} represents the capacitor between the excitation and sensing electrodes.

Between the pads and the beam the capacitors are C_{pc} and between the electrodes and the beam is C_{dc} . Finally there are capacitors C_{ds} between the substrate and the electrodes and between the substrate and the beam is C_{cs} . It has been considered that the coupling between the electrodes or pads and the beam are symmetric.

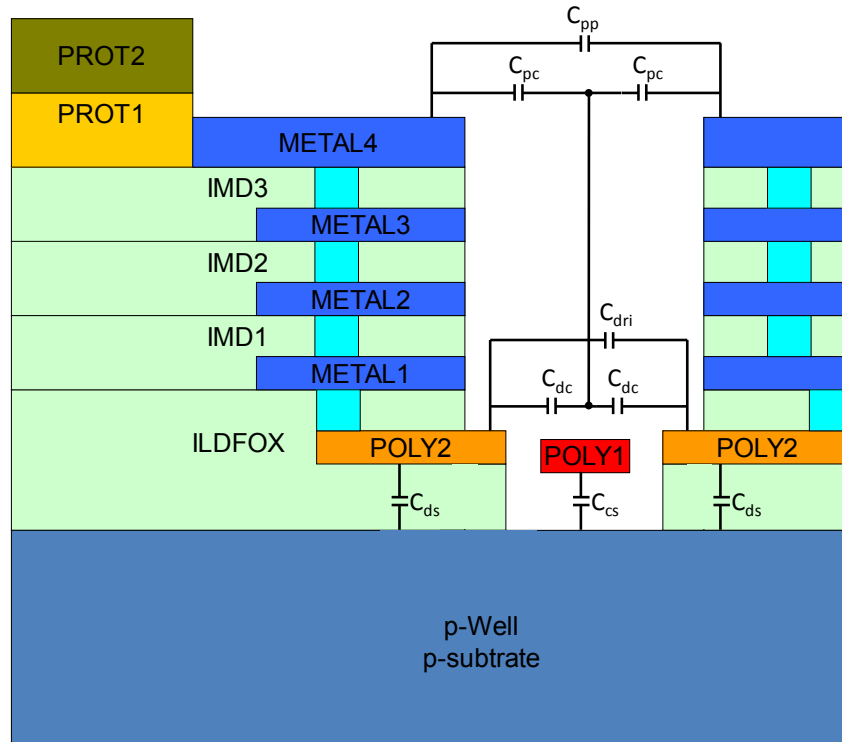


Figure 102.- CMOS-MEMS technology equivalent capacitors extracted from [Muñ11].

Considering that one electrode is an input, the other is the output and the beam is connected to a DC voltage the small signal equivalent model of the two electrodes resonator [Ngu99] is shown on the Figure 103, where the grounding of the beam comes from the grounding of the DC source in small signal analysis. The capacitors C_{oe} and C_{or} represent the equivalent parallel of C_{ds} , C_{dc} and C_{pc} seen between each driver and the beam. The capacitor C_{cs} is cancelled since the beam and the substrate are at the same potential in small signal model.

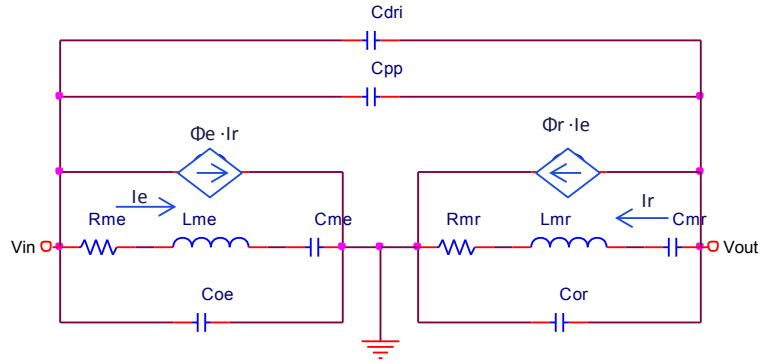


Figure 103.- Small signal model of the two electrodes resonator.

The dependant current sources modelize the electromechanical couplings in the excitation and the sensing electrodes (the input signal actuates mechanically the structure which induce a current at the output). The Φ_e and the Φ_r are defined in the equation [4.127].

$$\phi_e = \frac{\eta_e}{\eta_r} = \frac{V_{DC} \frac{\partial C_e}{\partial x}}{V_{DC} \frac{\partial C_r}{\partial x}} \frac{\frac{\partial C_e}{\partial x} = -\frac{\partial C_r}{\partial x}}{\frac{\partial C_e}{\partial x} = -\frac{\partial C_r}{\partial x}} \quad \phi_e = \phi_r = -1 \quad [4.127]$$

The model shown on the Figure 103 could be simplified to the Figure 104 by assuming symmetric couplings between resonator and the two electrodes ($Z_{me} = Z_{mr} = Z_m$). From the input current of the Figure 103 the equation [4.128] could be developed to demonstrate that the model of the Figure 104 describe the same behavior.

$$I_{in} = I_e + \phi_e \cdot I_r + I_{C_{dri}} + I_{C_{pp}} + I_{C_{oe}} \rightarrow \quad [4.128]$$

$$I_{in} = \frac{V_{in} - V_{out}}{Z_m} + I_{C_{dri}} + I_{C_{pp}} + I_{C_{oe}}$$

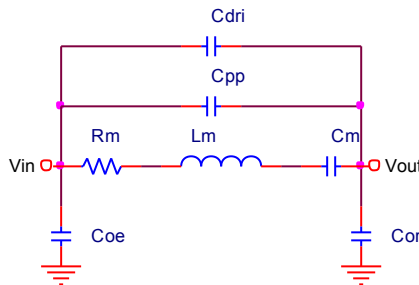


Figure 104.- Equivalent small signal model for symmetric couplings.

The RLC equivalent model is computed and the magnitude and phase of the response are extracted and showed on the Figure 105 for a CCB resonator with $13\mu\text{m}$ of length, 350nm of width, a thickness of 282nm of polysilicon, gap of 150nm , quality

factor of 200 and total parasitic capacitance of 250aF (parallel of C_{dri} and C_{pp}). The value of the impedances, electromechanical coupling factor and transduction gain for each DC voltage value are depicted on *Table 8*.

V_{DC}	C_m (aF)	L_m (H)	R_m (M Ω)	η ($\cdot 10^{-9}$ C/m)	I_m/x (A/m)
5	1.75	46.34	25.68	4.991	0.55
10	7.02	11.58	6.42	9.949	1.10
15	15.81	5.15	2.85	14.97	1.66

Table 8.- Equivalent impedances for the small signal model of a 17.6MHz CCB with $l=13\mu m$, $w=350nm$, $t=282nm$, $g=150nm$ and $Q=200$. The electromechanical coupling factor and the transduction gain are also computed.

Comparing the graph of the Figure 105 and the graph of the displacement versus the frequency shown on chapter 2 on Figure 16 allows concluding that the model is consistent with the mechanical theory explained previously. The differences in the out of resonance coupling levels without parasitic capacitance are explained by the limited sweep bandwidth, at the limit the motional current tends to 0.

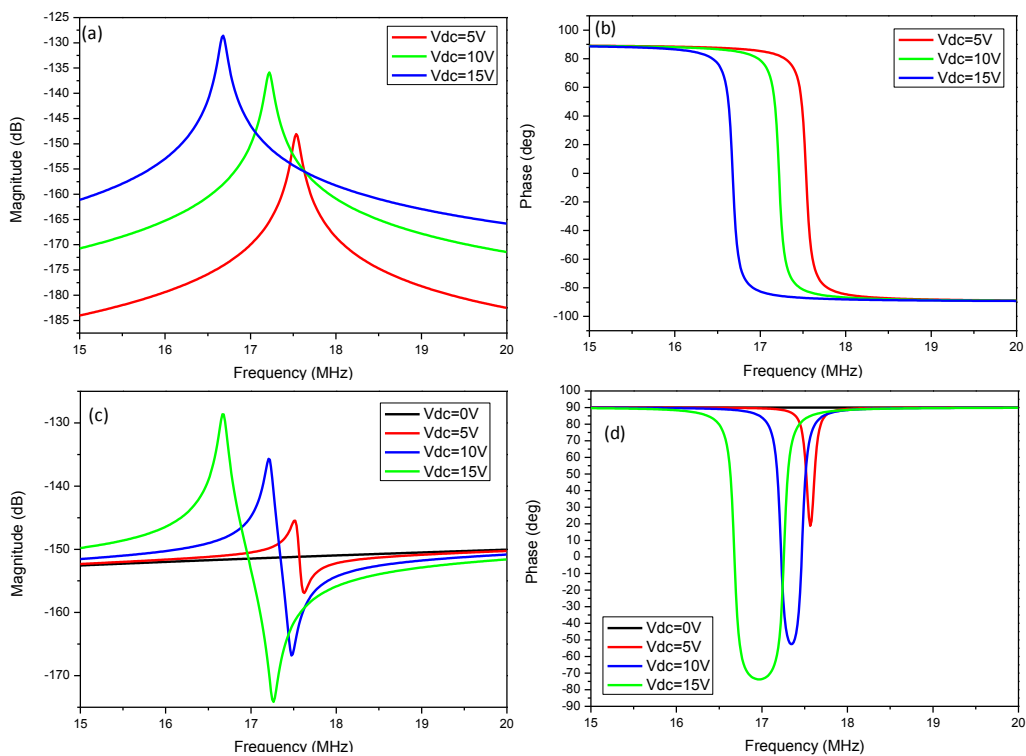


Figure 105.- Magnitude and phase response of the electrical model of a CCB resonator: (a,b) without parasitic capacitance, (c,d) with $C_p=250aF$.

4.3. METHODS TO DECREASE PARASITIC EFFECTS IN CAPACITIVE TRANSDUCTION

There are other measurement methods based on electrostatic actuation and capacitive sensing that reduce the amount of the parasitic current. They could be divided into: mixing methods (excite and read at different frequencies or by combining signals), differential measurements (subtract the parasitic contribution from the whole current) or by smarter layout design.

MEMS resonators as mixers

MEMS resonators could act as mixers [Lop09d], translating up or down the frequency of the output signal. Depending on where the product between two signals takes place, there are two different mixing mechanisms: force and current. On both mixing types, the RF signal is applied in the excitation electrode and the LO signal (plus the DC voltage is connected to the resonator as it is shown on Figure 106.

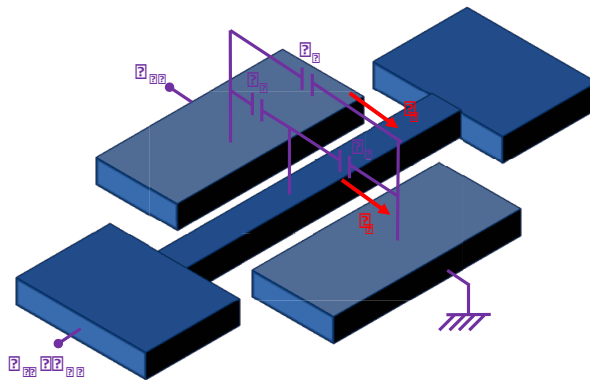


Figure 106.- Signals applied for sensing with mixing.

The electrostatic force exerted by an electrode to a beam could be expressed in terms of both signals:

$$F = \frac{1}{2} \frac{\partial C}{\partial x} \left[\frac{1}{2} (V_{RF} + V_{DC})^2 + \frac{1}{2} (V_{RF} - V_{DC})^2 \right] \quad [4.129]$$

Expanding the different terms from the previous equation, the applied force becomes:

$$F = \frac{1}{2} \frac{\partial C}{\partial x} \left(\frac{1}{2} (V_{RF}^2 + 2V_{RF}V_{DC} + V_{DC}^2) + \frac{1}{2} (V_{RF}^2 - 2V_{RF}V_{DC} + V_{DC}^2) \right) \quad [4.130]$$

From [4.130] the second term corresponds to current mixing and the fourth to force mixing. Note that the term $V_{RF} \cdot V_{LO}$ is already performing the mixing and therefore the frequency of this force is $f = f_{RF} \pm f_{LO}$. The $V_{RF} \cdot V_{DC}$ with $f_{RF} = f_1$ is the same

that was found on second chapter. The MEMS resonator must be excited with forces near the natural resonance frequency (f_0) whilst other force components do not produce movement and are filtered. So, for force mixing f_{RF} and f_{LO} must be chosen so that $f_{RF}+f_{LO}=f_0$ or $f_{RF}-f_{LO}=f_0$, depending if we want up or down conversion. For current mixing the input frequency must meet $f_{RF}=f_0$. Considering only the force frequency terms for each kind of mixing from [4.130], the [4.131] and [4.132] are found.

$$F_{x_force_mix} = V_{RF} \cdot V_{LO} \frac{\partial C_E}{\partial x} \quad [4.131]$$

$$F_{x_current_mix} = V_{RF} \cdot V_{DC} \frac{\partial C_E}{\partial x} \quad [4.132]$$

Therefore, the displacement associated as those forces is:

$$u(x)_{force_mix} = \frac{Q}{k} V_{RF} \cdot V_{LO} \frac{\partial C_E}{\partial x} \quad [4.133]$$

$$u(x)_{current_mix} = \frac{Q}{k} V_{RF} \cdot V_{DC} \frac{\partial C_E}{\partial x} \quad [4.134]$$

The general output current expression for the MEMS resonator depicted on Figure 106 is:

$$\begin{aligned} I_0 &= C_R \frac{\partial(V_{DC} + V_{LO})}{\partial t} + (V_{DC} + V_{LO}) \frac{\partial C_R}{\partial t} \\ &= C_R \frac{\partial V_{LO}}{\partial t} + V_{LO} \frac{\partial C_R}{\partial x} \frac{\partial x}{\partial t} + V_{DC} \frac{\partial C_R}{\partial x} \frac{\partial x}{\partial t} \end{aligned} \quad [4.135]$$

The second term is used in the current mixing and the third one is used in force mixing. Finally the output current expression considering each particular force excitation will become:

$$I_{0_force_mix} = V_{DC} \frac{\partial C_R}{\partial x} \frac{\partial C_E}{\partial x} \frac{Q}{k} \left(V_{LO} \frac{\partial V_{RF}}{\partial t} + V_{RF} \frac{\partial V_{LO}}{\partial t} \right) \quad [4.136]$$

$$I_{0_current_mix} = V_{DC} \frac{\partial C_R}{\partial x} \frac{\partial C_E}{\partial x} \frac{Q}{k} V_{LO} \frac{\partial V_{RF}}{\partial t} \quad [4.137]$$

It can be concluded that both methods have similar expressions, although the force mixing presents an additional term that increases the amount of output current. The final output current will be similar but the magnitude of the applied force, and thus the displacement, will be greater in current mixing. Note that the input and output signals have different frequencies, so that the parasitic current will be outside of the desired output frequency band, and therefore does not affect the resonance measurement. An example of both methods applied to a CCB is detailed on [Ura07]

where the device could operate as an up or down conversion mixer of radiofrequency signals. The enhancement of resonator current response in application of mixing method is demonstrated on [Lin10].

4.3.2. DIFFERENTIAL MEASUREMENTS

This method is based on the use of two equal MEMS devices which are connected to a differential amplifier. Then both resonators are excited by means of the same V_{AC} signal and the V_{DC} is set to 0V in one of them and swept in the other. So only one of the resonators will provide motional current but both of them will have the parasitic current contribution which will be subtracted by the differential amplifier. This method requires double MEMS area with equal resonators and additional circuitry in comparison with the mixing method. But it requires an easier set-up (one single network analyzer is enough) and provides good performance in CMOS-MEMS devices. An example of the application of this method is shown on [Lop09b, Ura09] where two CCB are fabricated together with a differential amplifier in a standard CMOS technology and the parasitic effect is completely removed from the output signal.

4.3.3. SMART LAYOUT

If the contributions to the total parasitic capacitance are well known a smart layout design could be certainly enough to decrease it. From the design of MEMS the election of larger widths maintaining the gap will reduce the direct capacitor electrodes whilst the actuation and sensing performance will be unaffected. The placement, the size of the electrodes or the reduction of the thickness of metal pads are well known solutions to reduce the amount of parasitic capacitance. Some specific layouts with added electrodes which allow the tuning of the gap in flexural resonators has also been successfully reported [Gin12b]. The placement of polarized walls or some kind of Faraday cages will shield the motional signal from the undesired parasitic currents [Dew11] enhancing the response obtained.

4.4. MEMS TRANSDUCTION CHALLENGES FOR HIGH FREQUENCY RESONATORS

The design and fabrication of high frequency resonators with capacitive sensing faces some challenges mainly related with the coupling between the structure of the resonator and the transduction electrodes. Employing the transduction gain defined on equation [4.118] the different challenges faced by different resonators could be compared.

The size scaling down of mechanical resonators leads to the development of smaller devices with increasing capabilities such as better mass sensitivity, lower power consumption, faster response time or higher resonant frequencies. Instead of the powerful enhancements provided the scaling down of MEMS devices must face some important challenges [Eki05b]. Focusing on MEMS with electrostatic excitation and capacitive sensing the Table 9 summarizes the important parameters and how each one scales down assuming uniform scaling in the three dimensions (except for the transduction gap). The effective mass and the electromechanical transduction factor (considered equally for the excitation and for the sensing) are severely scaled down making challenging the transduction of small devices. The spring constant and the transduction gain scales down proportionally with the size. Finally, the resonance frequency and the motional resistance magnitudes are increased with homogenous scaling down of the MEMS device providing by one side higher frequencies but also higher motional resistances. Related with the parasitic current a higher frequency also increases their value. Moreover a reduction on the width size also increases the direct capacitor between electrodes C_{dri} raising the total parasitic capacitance. We include here the scaling of the mass sensitivity to highlight the importance of small dimensions and high frequency MEMS resonators as this parameter provides the highest improvement.

Magnitude	Equation	Scaling factor
Effective mass	$m_{eff} = \frac{192twl\rho}{(k_n l)^4}$	λ^3
Spring constant	$k = \frac{16Et w^3}{l^3}$	λ
Resonance frequency	$f_n = \frac{(k_n l)^2 w}{2\pi l^2} \sqrt{\frac{E}{12\rho}}$	λ^{-1}
Electromechanical transduction factor	$\eta = V_{DC} \frac{\varepsilon \cdot A}{g^2}$	λ^2
Motional resistance	$R_m = \frac{\sqrt{k \cdot m_{eff}}}{Q\eta^2}$	λ^{-2}
Transduction gain	$\left(\frac{I_m}{x_0}\right) = \omega_n \cdot \eta$	λ
Mass sensitivity	$\frac{\delta m}{\delta f} \approx \frac{2 \cdot m_{eff}}{f_0}$	λ^4

Table 9.- Scaling factors for some important magnitudes of a CCB assuming that $\lambda < 1$. The approach could be applied to other MEMS topologies with similar scaling factors.

4.5. STATE OF THE ART

The capacitive sensing method provides a powerful integrated solution which in the CMOS-MEMS field is crucial. In function of the pursued application the requirements for resonators based on capacitive sensing may vary. However there are some characteristics which could be taken in order to establish some criteria. As the

method is based on capacitive coupling it is convenient to assume that the coupling area (mainly limited by transduction gap, g on Table 10) it is an important parameter which will determine how much current will flow and could be detected. Indirectly related with the coupling is the resonance frequency of the device because the size of the resonator scales with the amount of coupling available. Assuming the electrical model given by Figure 104 the motional resistance depends upon the electromechanical coupling factor, the resonance frequency and the quality factor so their value summarize the performance of the sensing method and the benefits of the resonator (f_0 , Q , R_m and η on Table 10). The motional resistance also affects to the amount of output current if additional circuitry or measurement tools are connected due to unmatched impedances. The transduction gain (I_m/x on Table 10) gives the amount of current for certain vibration amplitude and provides a magnitude to compare how scalable is the device. If the resonator is used in an oscillator topology the output amplitude signal and the phase noise (P_N at 1kHz on Table 10) were the key parameters.

Other important parameters in capacitive sensing are: parasitic current, spring softening effect or electromechanical nonlinearities. The quantification of these parameters provides by one side the amount of motional current detectable, the tunability of the resonator and their dynamic range.

There are a lot of contributions on CMOS-MEMS capacitive sensing along the past twenty years: from the first efforts to integrate MEMS in a CMOS technology with a pressure transducer [Sch91] or an inertial sensor [Yun92] to nowadays with a mature technology and processes which have been enabled the diversity of applications. In the references field application of MEMS the reduction of motional resistance and the increase of resonance frequency are desired.

The Kaajakari's group contribution [Ran05] explains a square extensional mode resonator made of silicon on a SOI wafer and bonded to the circuitry die. Despite the resonator is not monolithic CMOS-MEMS it is employed on oscillator topology achieving good performance on phase noise. The use of crystal silicon allows the high quality factor and the separation of the fabrication of MEMS from circuits provides the small gap and consequently the low motional resistance obtained.

Fedder and Lo in [Lo07] employ the metals from a CMOS technology as masks for micromachining Silicon-Fin resonators integrated with a differential amplifier. The use of the silicon from the substrate allows thicker structures instead of the thickness achieved by single available CMOS layers. Despite of the large transduction gap the

higher thickness provides an increase over the coupling area and the motional resistance is reduced.

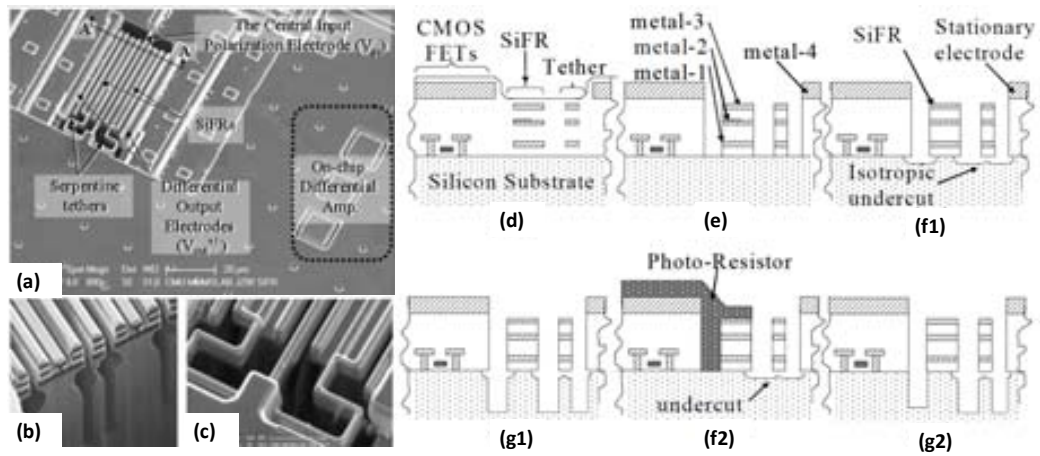


Figure 107.- SEM images of SiFR and fabrication process: (a) top view, (b) FIB cross-section view along the A-A' line from (a), (c) close-up view showing the release of the serpentine tethers, (d) after foundry CMOS processing, (e) after SiO₂ etch, (f1) after isotropic etch to release tethers, (g1) after anisotropic etch to define the length of resonator structures, (f2) after an alternate PR protection step and an isotropic tether releasing etch, and (g2) alternate process after removing PR and anisotropic silicon etching.

Nguyen group developed a flexural mode nickel disk resonator array at 11.1MHz on top of a CMOS circuit in closed loop configuration [Hua08]. The size of the disks and the small transduction gap gives a reasonable motional resistance. However the employment of flexural mode instead of bulk mode (the array is composed by a number of disks mechanically coupled with beams and only anchored at both ends) provides low quality factor and not so good phase noise.

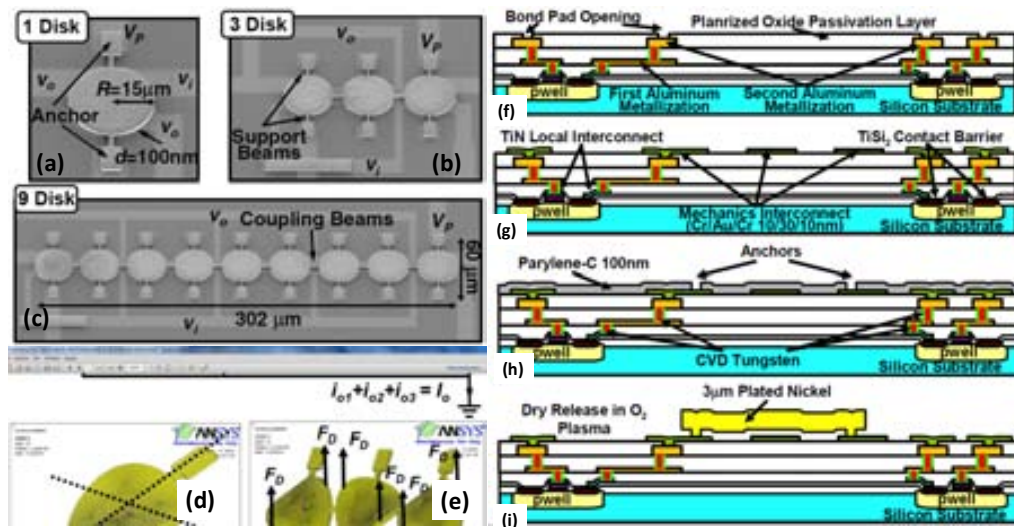


Figure 108.- (a,b,c) SEM images of flexural-mode disk-array resonators using varying numbers of mechanically-coupled disks; (d) mode shape of a constituent disk;

(d) flexural-mode shape of the disk array selected by properly phased electrostatic driving forces induced; (f, g, h, i) cross sectional fabrication process flow for the fully monolithic nickel flexural-mode disk-array oscillator.

The flexural structure made by Zalalutdinov in [Zal10] called dome resonator made by polysilicon is thermally actuated and capacitive sensed. The fabrication approach is easier as it only requires a post CMOS etching step to release the structure obtaining the short transduction gap of 120nm and thus providing reasonable motional resistance despite of the lower size.

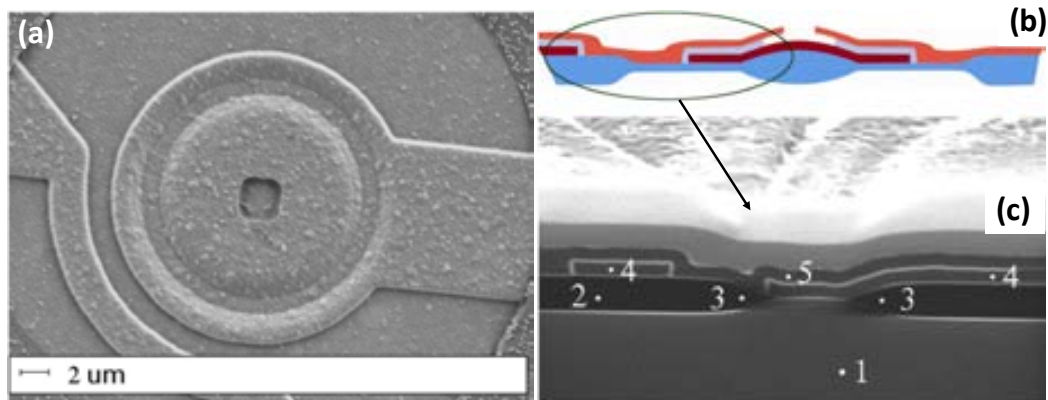


Figure 109.- (a) SEM image of the dome resonator with radius larger than the BB length. A thermoelastic actuator implemented as a poly1 heater is seen in parallel to the resonator's circumference; (b) Schematic view of the cross section of the double-poly dome resonator. The part of the cross section encircled in (b) is shown on SEM image (c) with Si substrate marked as (1), FOX as (2), BBs as (3), poly1 as (4), and poly2 as (5).

In Taiwan in collaboration with TSMC foundry several examples of CMOS-MEMS resonators appeared over the last years. The approach shown on [Che11] is based on flexural stacks of metal with confined silicon dioxide, Figure 110. The high motional resistances obtained are limited by the transduction gap allowed between metal layers.

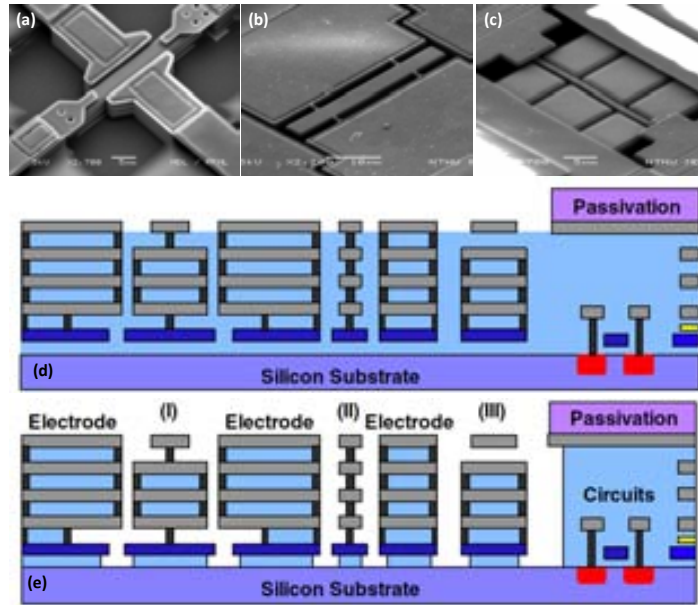


Figure 110.- SEM views of fabricated CMOS-MEMS resonators and fabrication process: (a) In-plane via-supported free-free beam; (b) out-of-plane metal Free-free beam; (c) in-plane via-supported pinned-pinned beam; (d, e) cross-sections depicting the fabrication process used to achieve CMOS-MEMS resonators in this work. (d) After the standard CMOS process, (e) after the wet release process.

Employing a different approach from similar CMOS technology ($0.18\mu\text{m}$ instead of $0.35\mu\text{m}$) based on [Liu11], the contribution [Che12b] shows a whole square plate resonator made from silicon dioxide (the metals are only employed to conduct the electrical signals), Figure 111. The employment of low mechanical loss material and a bulk vibration mode results in the high quality factor achieved by the square resonator. The transduction gap is also improved in comparison with the previous approaches.

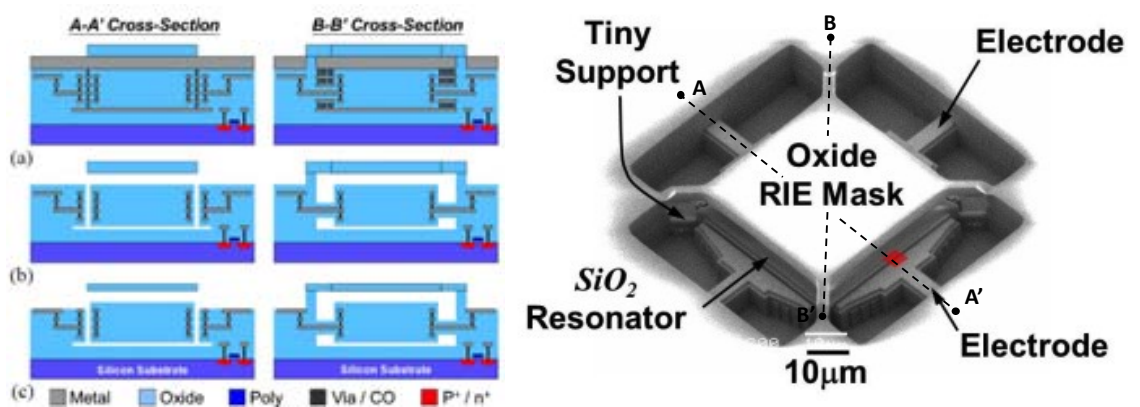
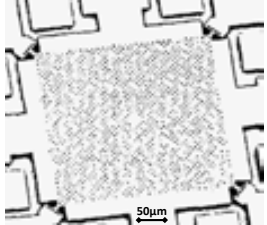
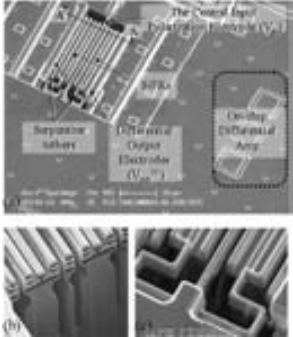
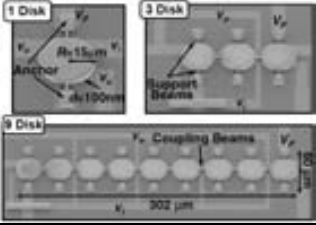
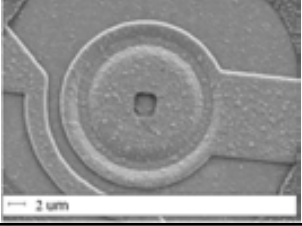
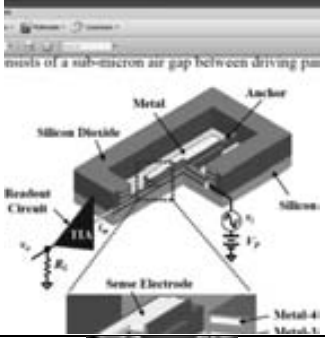
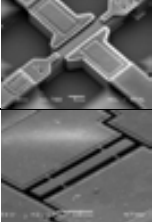
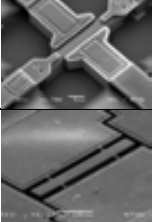


Figure 111.- Cross-sectional views depicting the fabrication process used to achieve the proposed CMOS-MEMS resonators. (a) After standard $0.18\mu\text{m}$ CMOS process. (b) After removal of sacrificial metal and VIAs using metal wet etching technique. (c) After removal of passivation using an RIE dry etching (i.e., maskless process). The SEM image of the fabricated square plate resonator includes the cross section lines A-A' and B-B' shown on the fabrication flow.

The following table gives a summary over the most important parameters in capacitive sensing for MEMS devices applicable to resonators and frequency references.

Ref.	Device	g (μm)	f_0 (MHz)	Q^*	R_m (Ω)	η ($\cdot 10^{-9}$ C/m)	V_{DC} (V)	I_m/x (A/m)	S_ϕ (dBc/Hz) @1kHz
[Ran05]		0.18	12.9	100000	0.5k	62220	20	5043.12	-130
[Lo07]		1.45	8.04	3589	183.9k	38.7	46	1.95	-
[Hua08]		0.1	11.1	1092	5.8k	1537	5	107.2	-80
[Zal10]		0.12	51.36	1020	740k	174	3.6	56.07	-
[Liu11]		0.64	3.11	4454	21.63k	808	170	15.79	-
[Che11]		0.5	14.5	1590	5.26M	190	70	17.32	-
		1.0	3.64	1770	8.22M	43	60	0.98	-

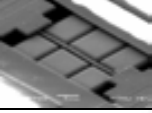
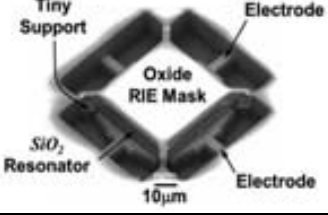
		0.5	1.46	810	7.08M	105	25	0.96	-
[Che12b]		0.38	47.9	10920	250k	829	70	249.45	-

Table 10.- Comparison between some state of the art CMOS-MEMS resonators with capacitive sensing. The motional resistance, electromechanical coupling factor and transduction gain, not given in most cases, are computed taking into account each particular device coupling area and gap. *All the quality factors were extracted in low pressure conditions except for [Ram05] which the depicted value is assumed in the simulations.

4.6. FINAL ELECTRONIC READ-OUT FOR THE CAPACITIVE TRANSDUCTION

Once the motion is transduced to an electrical signal, it is necessary to measure it. In this section we will explain the different configurations employed on our CMOS-MEMS resonators. The resonator could be designed and fabricated in stand-alone configuration or thanks to the monolithically integration with CMOS, an electronic amplifier can be added between the sensing electrode and the output pad, decreasing in this way the parasitic contribution. Finally our MEMS resonator has been fabricated with a CMOS amplifier in a closed loop, providing a self-oscillating CMOS-MEMS system. We will evaluate the main parameters of the final detected signal in three configurations. On all the cases the amount of parasitic current also affects the transduction gain and will be taken into account.

4.6.1. STAND-ALONE MEMS

In this case a direct read-out of the transduced signal will be performed with the network analyzer. This technique is known simply as transmission detection technique. In the following figure an electrical schematic of the set-up is shown:



Figure 112.- Schematic electrical set-up for measuring stand-alone MEMS with capacitive transduction with a network analyzer. The optical image of a CCB with the output pads and zoom of the resonator are also depicted.

From the electrical model (Figure 104) at resonance, the MEMS resonator could be represented as single motional impedance. Then, considering the input impedance of network analyzer (typically of 50Ω), the detected output voltage will depend from the two series impedance R_m+R_L . In capacitive transduction the value of R_m is usually large than R_L and the impedances are unmatched. The challenge to decrease R_m till R_L value will provide a matched network with maximum power transference between network analyzer and MEMS resonator. Combining both motional I_m and parasitic currents I_p the final output voltage at the input of network analyzer will be:

$$V_{out} = \frac{I_m R_L}{R_m + R_L} \quad [4.138]$$

Taking into account the frequency response of the MEMS, we can compute the final signal S to background B ratio at resonance which will be simply the ratio between the motional current and the parasitic current (it was already established in [4.120] and repeated on [4.139]).

$$\frac{S}{B} = \frac{I_m}{I_p} \quad [4.139]$$

Finally the voltage transduction gain can be computed as:

$$\frac{V_{out}}{V_{in}} = \frac{I_m}{I_p} \left(\frac{R_L}{R_m + R_L} \right) \left(\frac{R_m}{R_m + R_L} \right)^2 \quad [4.140]$$

Note that if the relation between the motional and parasitic current is much lower than the unity the effect of parasitic capacitance on the transduction gain can be neglected.

Just to clarify, and taking into account the parameters given in the Table 8, we can compute the S/B ratio and the final transduction gain (see Table 11).

V_{DC}	$\eta \cdot 10^{-9} \text{C/m}$	S/B	$V_{out}/x \text{ (V/m)}$
5	4.991	1.41	47.17
10	9.949	5.62	64.79
15	14.97	12.72	89.28

Table 11.- Equivalent signal to background ratio and voltage transduction gain for a 17.6MHz CCB with $l=13\mu\text{m}$, $w=350\text{nm}$, $t=282\text{nm}$, $g=150\text{nm}$, $Q=200$ and $C_p=250\text{aF}$.

The motional resistance could be experimentally extracted through [4.141], where R_L corresponds to the input impedance of the network analyzer of 50Ω and S_{21} is the peak magnitude in dB.

$$R_L = \frac{1}{|S_{21}|^2} \cdot \frac{1}{|Z_{in}|^2} \quad [4.141]$$

NON

In this case we were using a CMOS amplifier in its capacitive detection scheme (see Figure 113).

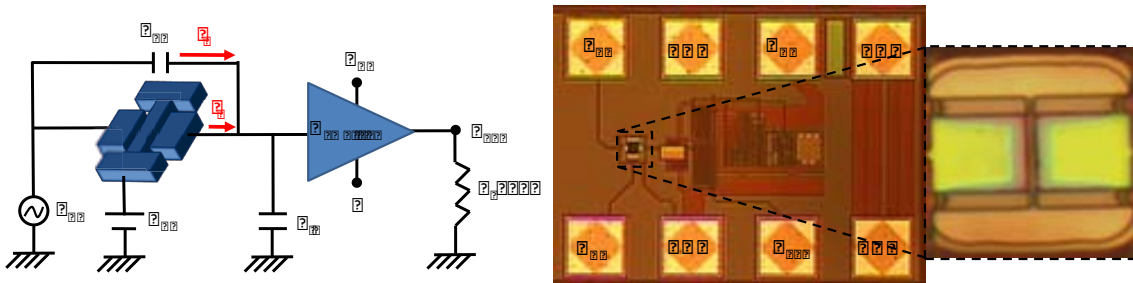


Figure 113.- Schematic electrical set-up for measuring MEMS with on-chip CMOS amplifier with capacitive transduction using a network analyzer. The optical image of a CCB with CMOS amplifier, the output pads and a zoom of the resonator are also depicted.

In this case C_{IN} represents the total input capacitance to the unity-gain CMOS buffer amplifier. Note that there will still be a parasitic contribution coming from any electrical coupling between the input and output electrodes. However, the CMOS pre-amplifier reduce a lot this parasitic capacitance because cancels any direct connection between the electrical output pads of the circuit. The design of this CMOS amplifier is out of the scope of this thesis and simply it has been used the one reported in [Ver08, Ver08b]. For this CMOS amplifier the final input capacitance is $C_{IN} \approx 13\text{fF}$. Knowing the final voltage, the transduction gain can be easily computed as:

$$\frac{V_{out}}{x} = \frac{I_m}{x} \cdot \frac{1}{\omega C_{in}} \quad [4.142]$$

The contribution of this parasitic capacitance has to be also considered, being in this case much smaller than with the stand-alone configuration, as we have already explained. This parasitic capacitance can be computed from the magnitude measurements out of the resonance peak with [4.143] where S_{21} is the background level of the magnitude, f_{oor} is the frequency out of resonance from B_1 and $G_{amplifier}$ is the transimpedance gain of the CMOS amplifier (being in our CMOS amplifier of 150dB Ω).

$$C_{pp} \cong \frac{10^{(S_{21}/20)}}{2\pi f_{oor} \cdot G_{amplifier}} \quad [4.143]$$

Comparing the transduction gain of these CMOS-MEMS with on-chip amplification with the stand-alone MEMS resonator, a difference of $1/(\omega C_{IN})$ multiplying factor is found. Which is equal to a multiplying factor of $6.9 \cdot 10^5$ at 17.6MHz, enhancing in this way the transduction capability. Considering the same CCB from the Table 11 with a CMOS amplifier, the following table gives the equivalent voltage transduction gain.

V_{DC}	$\eta (\cdot 10^{-9} C/m)$	$V_{out}/x (V/m)$
5	4.991	$32.55 \cdot 10^6$
10	9.949	$44.71 \cdot 10^6$
15	14.97	$61.60 \cdot 10^6$

Table 12.- Equivalent signal to background ratio and voltage transduction gain for a 17.6MHz CCB ($l=13\mu m$, $w=350nm$, $t=282nm$, $g=150nm$, $Q=200$ and $C_p=250aF$) with CMOS amplifier ($C_{IN}=13fF$).

4.6.3. SELF-OSCILLATING CMOS-MEMS

The basic blocks to develop an oscillator are a resonator and an amplifier connected in closed loop configuration. The operation begins with enabling the circuit power which produces electrical white noise that is feedback to the resonator. The resonator filters the white noise and only allows the pass of the signal at their resonance frequency. Then the amplifier increase the amplitude of this signal and the process is repeated until stability is reached if the Barkhausen criterion is met. The Barkhausen criterion gives two conditions related with the loop gain magnitude and phase shown on [4.144] and [4.145].

$$|G(j\omega_0)| \geq 1 \quad [4.144]$$

$$\angle G(j\omega_0) = 2\pi n \quad n \in 0, 1, 2, \dots \quad [4.145]$$

Employing the electrical model of the resonator given in the *Figure 104* and considering the equivalent oscillator impedance Z_A the oscillator circuit model corresponds to the *Figure 114*, [Vit88].

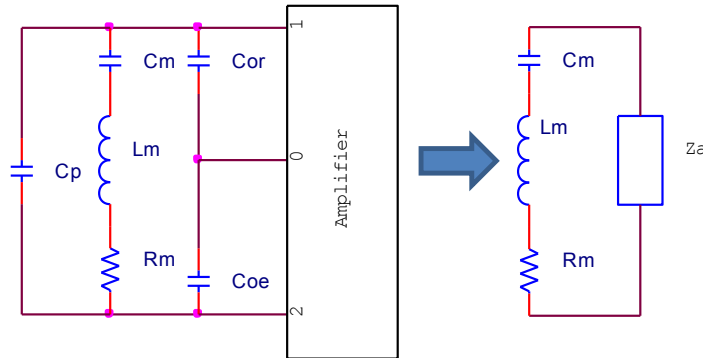


Figure 114.- Equivalent model for the oscillator given by the RLC||C resonator model and amplifier equivalent impedance.

From the mechanical resonance frequency ω_m of the resonator circuit [4.146] the motional impedance of the resonator Z_m could be expressed as equation [4.147]. Considering that the frequency ω of the oscillator will be close to the resonator frequency ω_m and defining the relative amount of frequency pulling p above the mechanical resonant frequency [4.148], the motional impedance is approximated by equation [4.149].

$$\omega_m = 1/\sqrt{LC} \quad [4.146]$$

$$Z_m = R_m + \frac{j}{\omega_m C_m} \left(\frac{\omega}{\omega_m} - \frac{\omega_m}{\omega} \right) \quad [4.147]$$

$$p = \frac{\omega - \omega_m}{\omega_m} \ll 1 \quad [4.148]$$

$$Z_m = R_m + j \frac{2p}{\omega C_m} \quad [4.149]$$

From the Barkhausen criterion it can be demonstrated [Vit88] that the critical condition for oscillation can be expressed as [4.150]. Splitting this equation into the real and imaginary components gives the two conditions [4.151] and [4.152]. From the real condition it can be extracted that the amplifier gain must compensate the motional resistance of the resonator. So it is mandatory to design resonators with low motional resistances (high quality factor and high electromechanical coupling factor) in order to decrease the complexity of the required CMOS circuit and thus their power consumption and noise. On the other side from the imaginary part the contribution of parasitic capacitors increase the frequency pulling, and therefore the resonator controlled oscillation. Then for a good performance oscillator the monolithic integration

of mechanical resonator and CMOS circuit will provide a smaller parasitic capacitance compared with non monolithic approaches.

$$Z_m + Z_c = 0 \quad [4.150]$$

$$-Re[Z_c] = R_m \quad [4.151]$$

$$-Im[Z_c] = \frac{2p}{\omega C_m} \quad [4.152]$$

Once the oscillator stability is reached an output periodic signal is obtained. From this periodic signal their amplitude, frequency and shape will give the performance of the oscillator. The short-term stability is limited by random fluctuations in the phase of the waveform $\phi(t)$ in [4.153] which spread their spectrum. In this sense this phase noise is computed by means of power spectral density $S_\phi(\omega_m)$ according to Lesson's model equation [4.154] extracted from [Lee66]. The model assumes that the feedback oscillator has an effective noise figure F and the additive noise is white at a certain temperature T. The k corresponds to the Boltzman constant, the P_s to the power signal level of the oscillator and the α parameter is determined by the level of flicker noise of the amplifier.

$$v(t) = A\cos(\omega_0 t + \phi(t)) \quad [4.153]$$

$$S_\phi(\omega_m) = \left(\frac{\alpha}{\omega_m} + \frac{2kTF}{P_s} \right) \left[1 + \left(\frac{\omega_0}{2Q\omega_m} \right)^2 \right] \quad [4.154]$$

From Lesson's model three regions could be identified in function of the offset frequency from the carrier ω_m : the low frequency spectral density is dominated by the flicker noise with a slope of -60dB/dec; before the feedback loop half-bandwidth the slope of -20dB/dec is mainly dependant over the quality factor; for large frequencies the spectral density is flat and limited by the thermal noise of the amplifier and their corresponding output power signal. The Figure 115 gives a schematic plot of the phase noise regions of an oscillator. The reduction over the phase noise of an oscillator will be obtained with high output power and high quality factor. However the increase of the output power could also increase the flicker noise of the oscillator and the non linearity of the resonator.

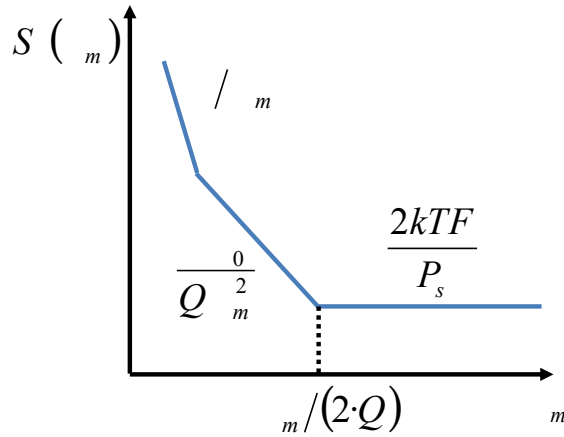


Figure 115.- Power spectral density versus offset carrier frequency given by Lesson’s model [Lee66].

For these self-oscillating CMOS-MEMS the same CMOS amplifier explained in last section has been used. The closed-loop has been implemented directly on chip to reduce the parasitic effects due to the bonding pads which degrade the total gain and change the loop phase, Figure 116. In this sense the output of the oscillator will be defined by the non-linear properties of the MEMS because there is no possibility to change the loop gain.

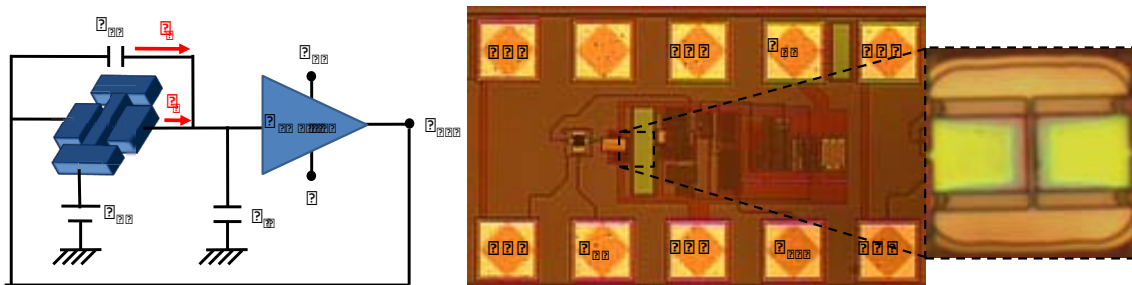


Figure 116.- Schematic electrical set-up for self-oscillating CMOS-MEMS with capacitive transduction. The optical image of a CCB with CMOS amplifier in closed loop configuration, the output pads and a zoom of the resonator are also depicted.

In order to characterize the electrical non-linear properties the terms of the force must be derived. From the force F_x between the two electrodes from [2.92] and considering a Taylor expansion in x :

$$F_x = \frac{Q^2}{2C} \left(\frac{2Q^2}{2C} \frac{2Q^2}{2C} \frac{2Q^2}{2C} \right) \frac{Q^2}{2C} \tag{4.155}$$

$$F_x = \frac{2Q^2}{2C} \left(\frac{2Q^2}{2C} \frac{2Q^2}{2C} \left(\frac{2Q^2}{2C} \right)^2 \frac{2Q^2}{2C} \right)$$

The first term in this equation is a force that is independent on the AC component of the voltage, but is dependent on the resonator displacement and can therefore be considered a spring force. This term adds to the mechanical spring force, which is typically much higher in value, and can be used to fine tune the mechanical resonance frequency. The second term can also be considered a spring force, but with a spring constant that depends on x . This implies that according to the motional capacitance C_m and resonance frequency ω_0 are functions of the resonator amplitude x . In [VanB12] it is shown that this term can increase Q_{loaded} , and thus the near-carrier phase noise can be decreased. The third term in [2.92] comprises the product of two time-varying signals: V_{AC} and x . If the resonator is excited by a noisy voltage $V_{AC}+V_n$, where V_n represents the noise term, then the product $x \cdot (V_{AC}+V_n)$ contained in the third term will result in upconversion of the V_n spectrum around the oscillation frequency. This mechanism can result in the upconversion of flicker noise in the oscillator loop leading to a $1/\omega^3$ instead of a $1/\omega^2$ of the near-carrier noise roll-off thereby causing a deterioration of the near-carrier phase noise [Kaa05]. This simple analysis shows that different nonlinearities in the resonator can result in an improvement as well as a deterioration of the near-carrier noise.

4.7. ELECTRICAL CHARACTERIZATION OF FLEXURAL CMOS-MEMS RESONATORS

In this section there are presented the obtained results for different resonators topologies based on electrostatic actuation and capacitive sensing. CMOS-MEMS resonators are measured in stand-alone configuration, with amplifier and in closed-loop configuration. From the less to high mechanical complexity a CCB, DETF, Free-Free and Cross-Beams are revised.

4.7.1. CLAMPED CLAMPED BEAM RESONATOR

A clamped clamped beam is a well known mechanic structure. It is stiffer than a cantilever but it is also more robust in front of stiction and residual stresses. A frequency around 25MHz and a width of 500nm are established, obtaining a design length of 13 μ m. The transduction gap is set to 100nm. The SEM image of *Figure 117* shows the CCB resonator after being released.

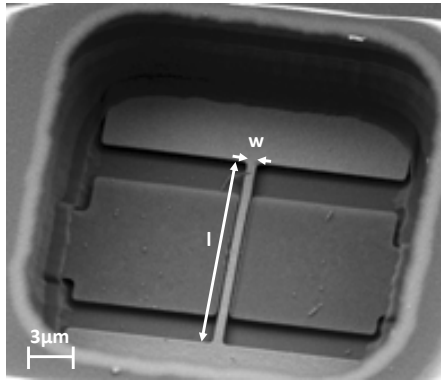


Figure 117.- SEM image of a CCB resonator after releasing process fabricated on CMOS technology with main dimensional design parameters.

The CCB structure is simulated with finite elements software (COVENTOR³²) to check their properly operating mode and resonance frequency. The *Figure 118* represents the first lateral mode at 25.5MHz with a spring constant of 43.8N/m and an effective mass of 1.7fg.

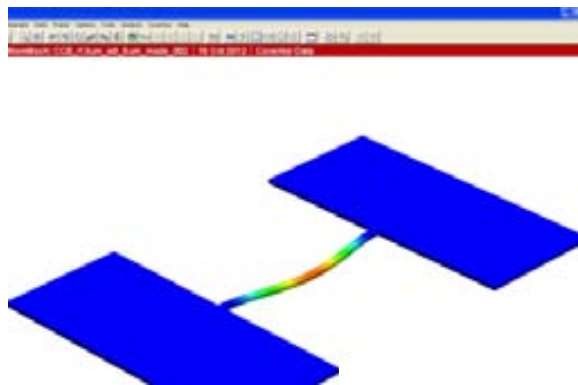


Figure 118.- Simulation of the CCB with $l=13.2\mu\text{m}$ in their first lateral mode by finite elements software.

From the stand alone set-up shown in Figure 119 with electrostatic actuation and capacitive sensing the magnitude and phase measures in air conditions were performed for different biasing conditions. The fixed parameters are the frequency band of 10MHz centered at 27.5MHz with 1601 points, an IF filter of 100Hz and an excitation AC power of 0dBm. The DC voltage is swept from 0 to 15V and the Figure 120 is obtained.

³² A Young modulus of 160GPa and mass density of 2330kg/m^3 has been used for all the polysilicon resonators.

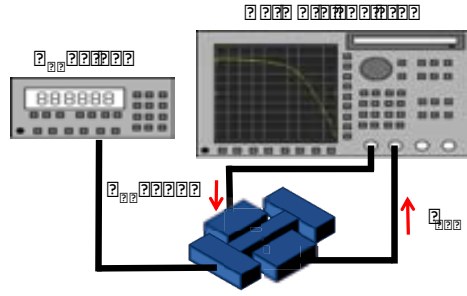


Figure 119.- Electrical set-up for measuring stand-alone CCB resonator.

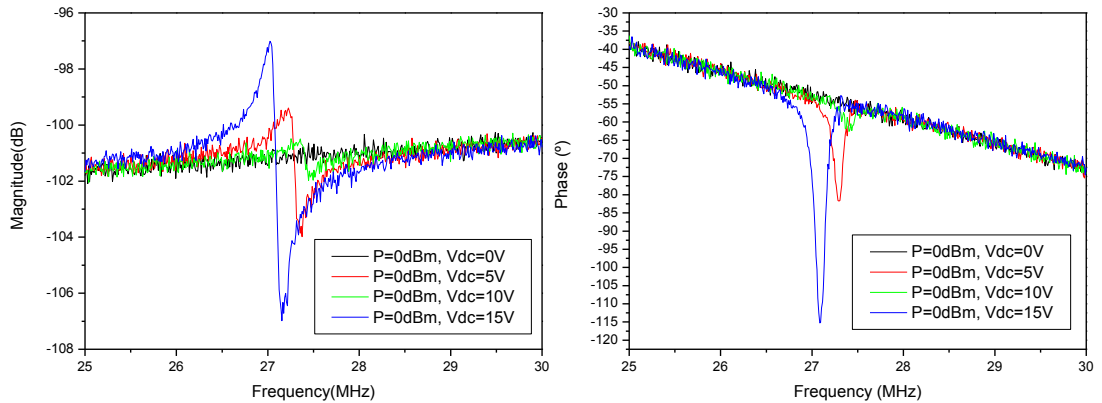


Figure 120.- Magnitude and phase obtained from network analyzer applying an input power of 0dBm and different DC voltage biasing conditions.

The resonance around 27.2MHz is clearly measured and the electrical spring softening behavior is also observed. Increasing the DC voltage the resonance frequency is also reduced and separated from the antiresonance due to the parasitic capacitance. The extracted quality factor is 67 and the spring softening slope is -1.65kHz/V^2 . Computing the electromechanical coupling factor and the motional resistance from the electrical model for V_{DC} voltage of 15V gives a value of $34 \cdot 10^{-9}\text{C/m}$ and $3.4\text{M}\Omega$ respectively. The experimentally motional resistance and the extracted parasitic capacitance are extracted using [4.141] and [4.143] with $G_{\text{amplifier}}$ set to 1, obtaining $3.5\text{M}\Omega$ and 50.5fF .

Increasing the power delivered to the excitation electrode produce an increase of the exerted force and their nonlinear terms are enhanced. In addition to this geometrical nonlinearity there are material effects which produce nonlinearities [Kaa04]. This non linear point gives the dynamic range of the resonator which in last instance will limit the maximum signal amplitude in oscillators and filters.

In order to drive the resonator to nonlinearity and find the non linearity bifurcation point some sweeps are performed maintaining the AC power to the

maximum output which the network analyzer is capable to provide (18dBm which corresponds to $5V_{pp}$ for a load of 50Ω) and sweeping the DC voltage.

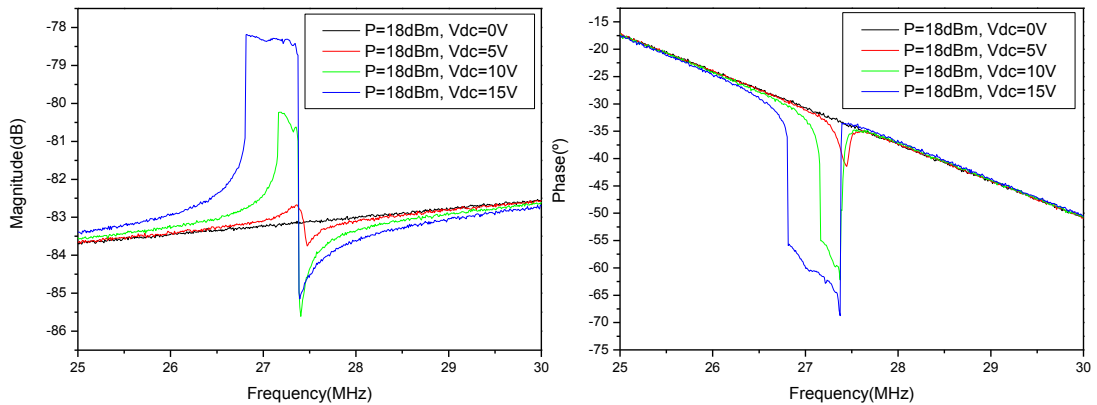


Figure 121.- Magnitude and phase of a CCB with maximum AC power and DC voltage sweep.

From the measures of Figure 121 it could be seen that for the maximum excitation the peak has a flat response instead of a lorentzian. This is produced by a hard-contact between the beam and the electrodes similar than the hard-contact shown on [Lin08] employed in “reswitching”. Extracting the parasitic capacitance gives a value of $401.7fF$. Comparing the previous value obtained of $50.fF$ with $401.7fF$ it has been a huge increase in parasitic capacitance despite of the CCB resonator is the same. This could be explained considering the fringing field contribution to the total parasitic capacitance. So the increase of the AC power from $0dBm$ to $18dBm$ also enhances the fringing fields between the actuation and sensing electrodes.

In order to avoid the hard-contact and reach the nonlinearity point the excitation power is maintained to lower levels and the DC voltage is increased until the shape of the measured signal becomes nonlinear. On the Figure 122 it is shown this correspondingly experiment where the response begins to be nonlinear from $20V$ of DC voltage with an actuation AC power of $-10dBm$ ($200mV_{pp}$ for a load of 50Ω). In this case the parasitic extracted corresponds to $62.41fF$ in good agreement with measures of Figure 120.

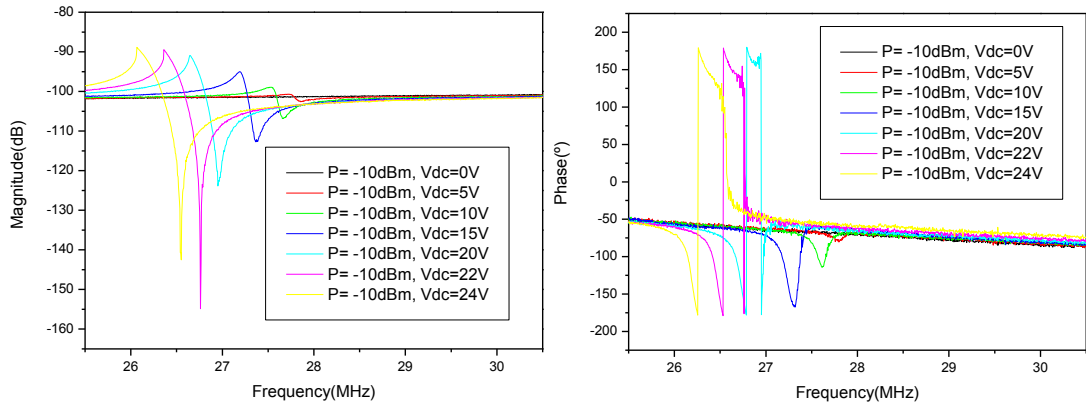


Figure 122.- Magnitude and phase with AC power of -10dBm with DC voltage sweep until the spring softening nonlinearity point is reached.

The same resonator is integrated in another row of the same RUN with CMOS amplifier in closed loop configuration. One electrode of the device is connected to the input of the circuit whilst the other is connected to the output acting as signal feedback path. If the Barkhausen conditions are accomplished self sustained oscillation of the compound of resonator plus amplifier may be reached. The only output requirements are by one side the biasing voltage of the CMOS amplifier (the current consumed is around 3.5mA) and the DC voltage on the resonator structure to allow the motional current. The output signal could be detected by means of a simple oscilloscope and two DC sources, set-up shown on Figure 123.

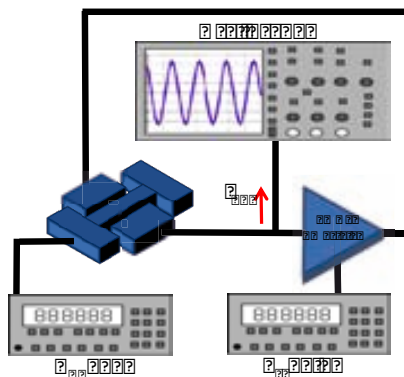


Figure 123.- Electrical set-up for measuring self-oscillating CMOS CCB resonator.

The obtained measure for a DC voltage of 15V is depicted on the graph of Figure 124. The gap of 100nm makes necessary this value of DC voltage to obtain the resonance peak of 6dB shown on Figure 122 in order to have enough current which amplified through the CMOS circuit is capable to excite the resonator closing the loop. The shape of the periodic signal is not purely sinusoidal due to energy given to higher modes. The computed resonance frequency is 28.03MHz with amplitude of 338mV_{pp} in

good agreement with the previous single resonator measures. Note that with this AC signal and DC voltage, the actuation will force a non-linear operation of the MEMS resonators (we have already shown in *Figure 122* that an AC actuation voltage of 200mV_{pp} produces an electrical non-linear behavior for DC voltages higher than 10V).

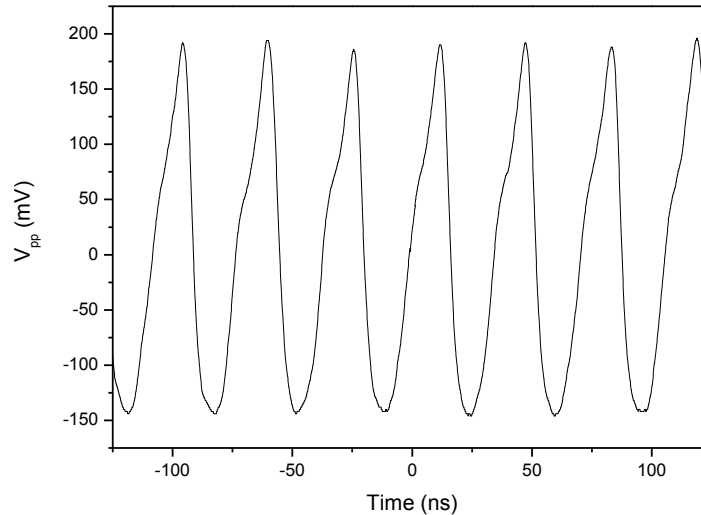


Figure 124.- Electrical measure of the sine wave signal obtained by the CCB resonator in closed loop configuration for a DC voltage of 15V .

In the same RUN there was also included an oscillator with the same CCB resonator with the smallest gap of 40nm which this CMOS technology is capable of [Lop09]. The same set-up of Figure 123 is repeated obtaining the periodic sine wave signal of the Figure 125 with a DC voltage of 5V . Achieve self sustained oscillation with this lower voltage is significant since the CMOS circuits of this technology are biased with 3.3V . In this case the frequency of the obtained signal is also around 28.07MHz with peak to peak amplitude of 372mV_{pp} . Although the DC bias has decreased, a nonlinear behavior is also found on [2.92] due to a decrease on the gap distance.

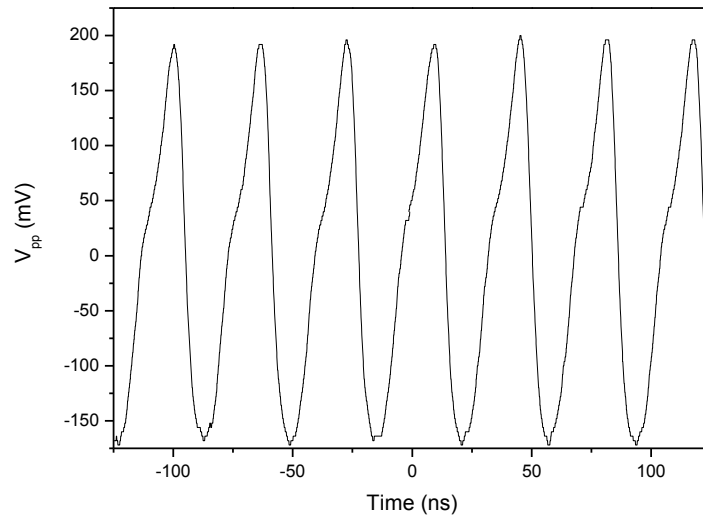


Figure 125.- Periodic signal obtained for the same CCB CMOS oscillator with transduction gap of 40nm applying 5V of DC voltage.

A shorter CCB is designed to resonate around 48MHz with a length of $9.4\mu\text{m}$ a width of 500nm and a gap of 40nm. The FEM simulation of the Figure 126 gives a resonant frequency of 48.2MHz with a spring constant of 117.7N/m and an effective mass of 1.3fg.

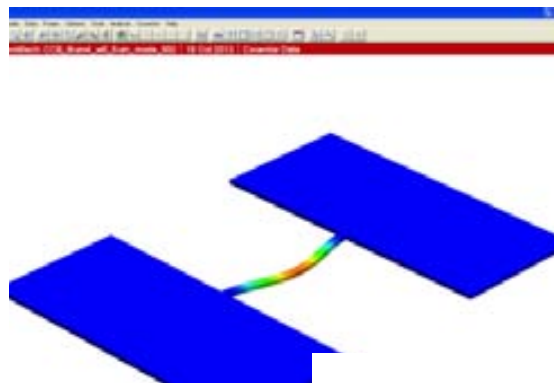


Figure 126.- Simulation of the CCB with $l=9\mu\text{m}$ in their first lateral mode by finite elements software.

The stand-alone resonator is electrically measured by means of the same electrostatic excitation and capacitive sensing set-up of the other CCB. The measures shown on the graphs of the Figure 127 are obtained for an AC power of -5dBm and a voltage sweep from 0V to 10V. The resonance frequency is around 49MHz, the extracted quality factor is 82 and the spring softening has a value of -30.5kHz/V^2 . In this case the nonlinear point is reached for DC voltages higher than 6V when the shape of the peak of the magnitude measure begins to be left curved. Their computed electromechanical coupling factor, extracted motional resistance and extracted parasitic

capacitance have the values of $62 \cdot 10^{-9} \text{C/m}$, $3.75 \text{M}\Omega$ and 26.5fF respectively for a DC voltage of 6V . Despite of the coupling length is shorter than the beam of Figure 118, the smallest gap provides higher electromechanical coupling factor. Otherwise the shorter coupling length reduces the amount of fringing fields between electrodes decreasing the parasitic.

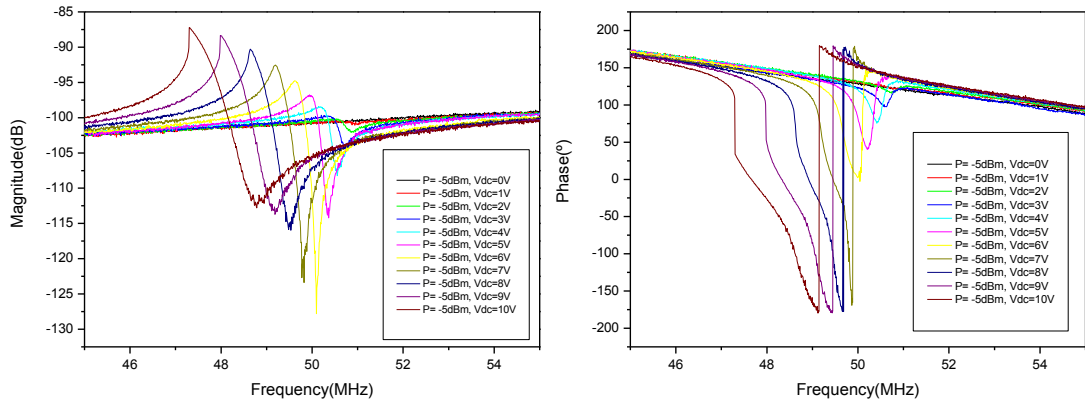


Figure 127.- Magnitude and phase for shorter CCB with a gap of 40nm.

As a summary of this section the Table 13 shows the main parameters and measures of the CCB resonators.

V_{DC} (V)	l (μm)	w (μm)	g (nm)	f_0 (MHz)	k (N/m)	m (fg)	Q	η (10^{-9}C/m)	R_m (Ω)	I_m/x (A/m)
15	13.2	0.5	100	27.01	43.8	1.7	67	34	3.4M	5.98
5	13.2	0.5	40	28.07	43.8	1.4	67*	70	754k	12.34
6	9.4	0.5	40	49.64	117.7	1.3	82	62	3.75M	19.83

Table 13.- Main dimensions and extracted parameters for the measures of CCB resonators. The frequency and electromechanical coupling factor were taken for a certain DC voltage value. *Assumed equal quality factor for both same resonators.

4.7.2. DOUBLE ENDED TUNING FORK RESONATOR

The DETF are basically two beams mechanically coupled in parallel by means of two short supports. These particular structures present two lateral vibration modes in function of the singular movement of each beam which are in phase or out of phase. The separation frequency of the two lateral modes is dependent on the length of the coupling supports which also allow the presence of torsional modes which transfer lateral displacement to higher harmonics. In the Figure 128 it is shown a SEM image of this structure with the main dimensional parameters. The out of phase lateral vibration mode is interesting as the coupling supports actuates as zero displacement nodes minimizing the energy loss through the anchors and increasing the quality factor of the resonator.

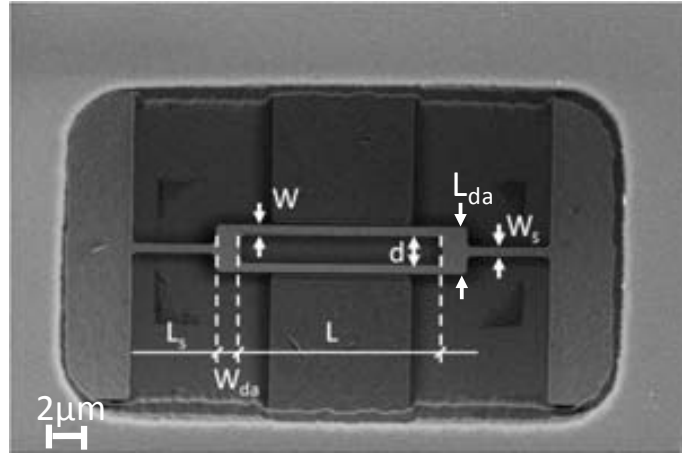


Figure 128.- DETF SEM image after releasing process with main dimensional parameters indicated.

The DETF resonator follows the analytical expression of the [4.156] extracted from [Bus89] where the eigenvalue α_n for the out of phase mode is 4.73.

$$f_o = \frac{1}{2\pi} \frac{(\alpha_n)^2}{L^2} \sqrt{\frac{E \cdot W^2}{12\rho}} \quad [4.156]$$

For a resonance frequency of 25MHz the design parameters established are shown on Table 14. The DETF is fabricated in single resonator configuration, with CMOS amplifier and in closed loop configuration for oscillator purposes.

Dimension	W (μm)	L (μm)	d (μm)	W _{da} (μm)	L _{da} (μm)	W _s (μm)	L _s (μm)	g (nm)	Mass (fg)
Value	0.5	12.8	2	1.5	3	0.5	5.3	40	17.81

Table 14.- Dimensional parameters for the DETF resonator.

Previously to the electrical characterization some simulations are performed in order to check the vibration modes which this resonator is capable of. In the Figure 129 there are shown three modal shapes of the first lateral modes. The first mode is excited at 11.86MHz with spring constant of 82.7N/m and effective mass of 14.9fg. The modal shape exhibit is the same than the first lateral mode of a single beam. The second mode known as the out of phase, resonate at 25.85MHz with spring constant of 141.2N/m and effective mass of 5.3fg. In the simulation is clearly shown the fact that the coupling supports are zero displacement nodes making this mode the desirable one for high Q resonators. The third mode is the in phase lateral mode excited at 35.26MHz with spring constant of 383.9N/m and effective mass of 7.8fg. In the simulations if the length of the coupling support L_{da} is increased the frequency distance is reduced controlling the bandwidth for filter applications.

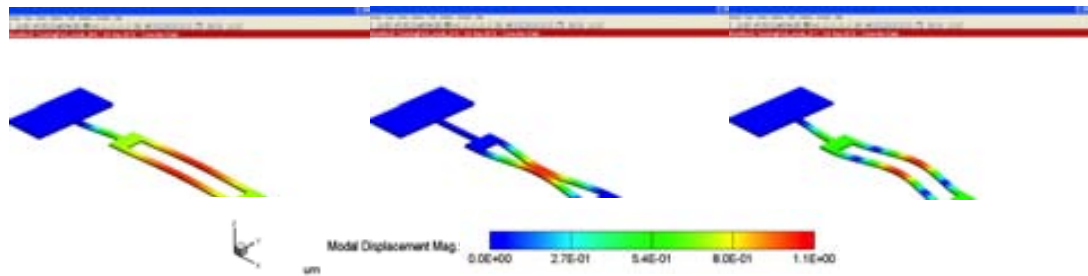


Figure 129.- FEM simulations of the DETF principal lateral vibration modes.

After the DETF resonator is correctly released (see the SEM image of the Figure 128) the same set-up with electrostatic excitation and capacitive sensing of the Figure 119. Frequency sweeps are performed keeping the excitation power and DC voltage constant to 0dBm and 4V respectively in order to detect the different modes.

In the graphs of the Figure 130 there are shown the measures of the magnitude and phase of the three modes described above. The (a) graph shows the first lateral mode with a resonance frequency of 11.15MHz and a quality factor of 39. The (b) graph corresponds to the second lateral out of phase mode with a resonance frequency of 26.16MHz and a quality factor of 41. The electrical response a resonance valley instead of a peak because the excitation force and the motional current are out of phase in this particular mode. The third mode of the (c) graph has a frequency of 35.04MHz and a quality factor of 35. It is remarkable that the quality factor of the second mode is only slightly higher than the other modes in contraposition of the theoretical increase due to the reduction of the anchor losses. The reason is related with the different contributions to the total quality factor as it was explained on the second chapter. The losses due to fluid energy mask the other losses sources making unappreciable in air conditions the effect of the anchors.

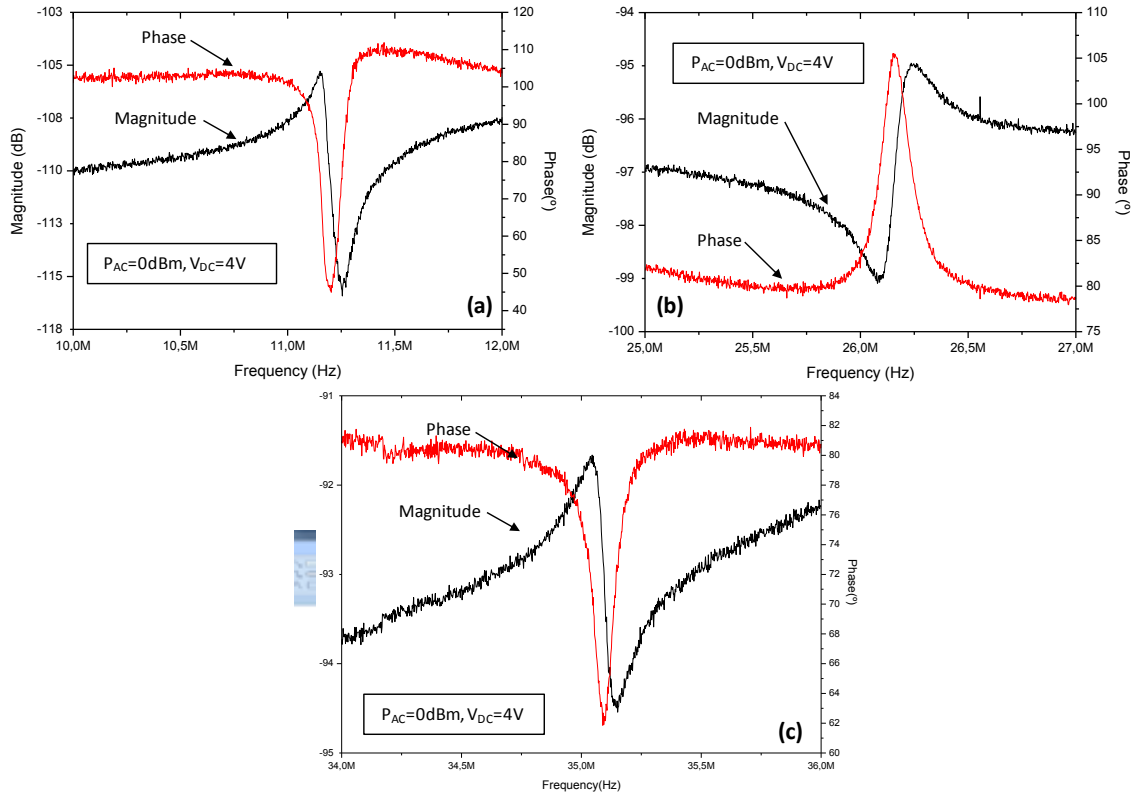


Figure 130.- Electrical measures of the DETF resonator: (a) graph corresponds to the first lateral mode, (b) graph to the out of phase lateral mode and (c) graph corresponds to the in-phase lateral mode.

Computing the electromechanical coupling factor and the motional resistance from the electrical model for V_{DC} voltage of 4V for each mode gives the values shown on the Table 15. From the measures of Figure 130 the extracted motional resistance and parasitic capacitance are: $8.9M\Omega$ and $50.3fF$ for first lateral mode, $2.8M\Omega$ and $89.9fF$ for the second out-of phase lateral mode, $1.9M\Omega$ and $98.9fF$ for the second in-phase lateral mode.

Lateral mode	f_0 (MHz)	k (N/m)	m (fg)	Q	η ($10^{-9}C/m$)	R_m (Ω)	I_m/x (A/m)
First	11.86	82.7	14.9	39	56.1	9.04M	4.18
Second out-of-phase	25.85	141.2	5.3	41	56.1	6.70M	9.11
Second in-phase	35.26	383.9	7.8	35	56.1	15.71M	12.43

Table 15.- Main dimensions and extracted parameters for the measures of each mode of DETF resonators. The frequency and electromechanical coupling factor were taken for a certain $V_{DC}=4V$.

From the first mode a DC sweep till 4V (higher voltages may produce stiction of the beams due to the small gap) is performed on (a) graph of the Figure 131. The spring softening of $-12.5kHz/V^2$ is extracted from the slope of (b) graph of Figure 131.

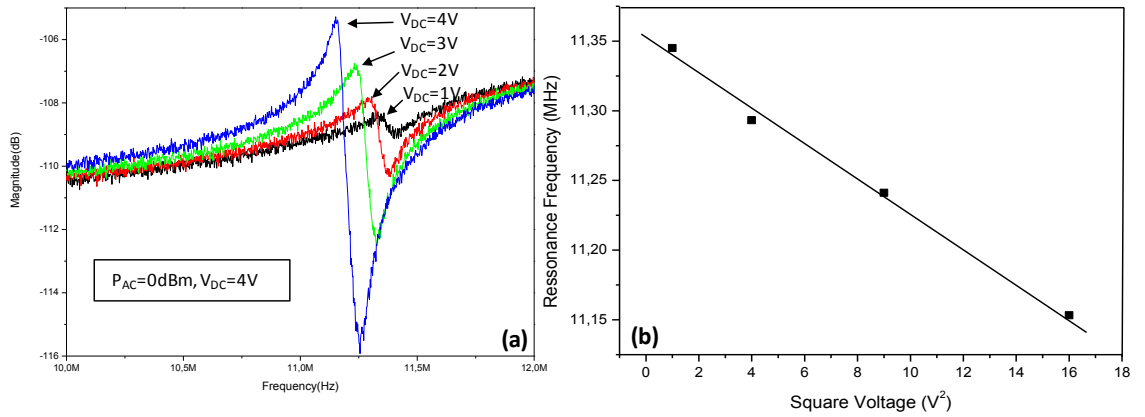


Figure 131.- (a) DC sweep from 1V to 4V magnitude measures of the first lateral mode; (b) computed spring softening graph.

In order to establish the effective dynamic range non linear measurements were also made. In the magnitude graph (a) of Figure 132 with a constant 4.2V of DC voltage it is shown that the resonator begins with nonlinear behavior between 0dBm (632mV_{PP} at 50Ω) and 2.5dBm (843mV_{PP} at 50Ω) of AC power. So the magnitude of output signal in the oscillator configuration cannot be higher than that value (the amplifier gain must be evaluated) to prevent nonlinear signals.

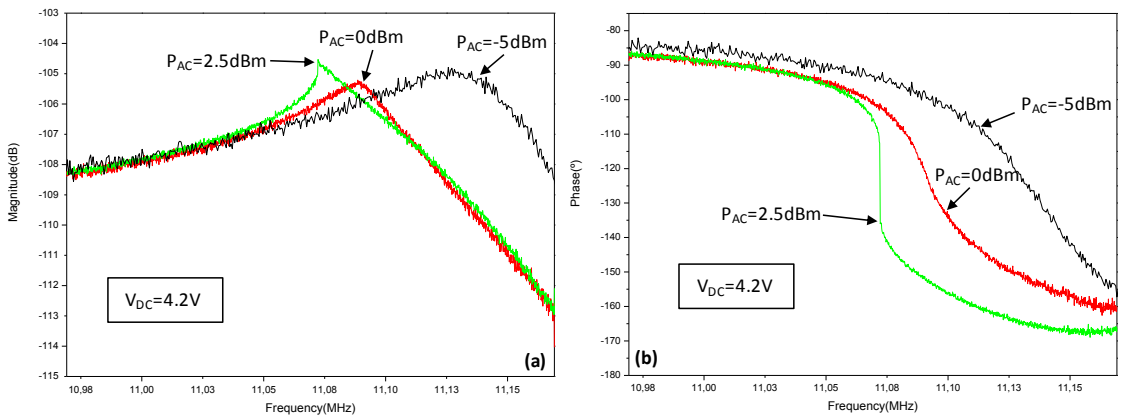


Figure 132.- Magnitude (a) and phase (b) electrical AC sweep performed on DETF resonator.

The DETF resonator is also integrated with a on-chip CMOS amplifier [Ver08b]. The set-up of the Figure 133 is employed. In this configuration one electrode is connected to metal PAD whilst the other electrode is connected to the input of the amplifier. The circuitry requires constant 3.3V biasing so additional DC voltage source is mandatory. The output of the circuit is connected to the output metal PAD which is directly connected to the input port of the network analyzer.

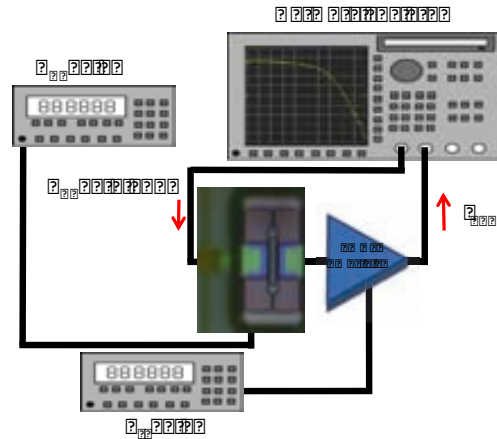


Figure 133.- Electrical set-up for measuring DETF resonator with on-chip CMOS amplifier.

The DC sweep measure performed, depicted on (a) graph of Figure 134, shows the magnitude response from AC power excitation of 0dBm and DC sweep from 0V to 3V. There are some remarkable observations on the measure. First of all the measured level around -65dB higher than the value obtained for single resonators fits with the additional amplifier stage attached to the DETF resonator. The strange effect of the magnitude response as the DC voltage is swept can be explained considering that the CMOS amplifier has a constant DC voltage of 2.5V on the output electrode due to the biasing of the first stage of the whole amplifier. This constant voltage introduces an asymmetry on the DETF resonator biasing introducing a shift on the phase of the motional current and inverting the resonance peak (similar than the behavior of the second lateral out of phase mode). As the voltage is increased the excitation force is also increased enhancing the vibration amplitude. When the voltage reaches the 2.5V the inversion effect disappears and the magnitude response behaves the standard one. The resonance frequency is 11.3MHz and the computed quality factor is 78. The higher quality factor could be explained taking into account that the resonance peak has higher magnitude than the peak in the stand-alone resonator configuration which difficult their computation if the peak is lower than 3dB. The extracted motional resistance and parasitic capacitance are 39.7k Ω and 33.3aF respectively. This huge increase is provided by the gain from the transimpedance amplifier integrated with the resonator. In (b) graph of Figure 134, the resonance frequency versus the square of the applied effective voltages between electrode and resonator is shown. The linear behavior is clearly derived from the straight line region allowing the characterization of the spring softening effect with a slope of 19kHz/V², which is in the same range than the stand-alone resonator. For effective voltages bigger than 1.6V a non linear behavior is found.

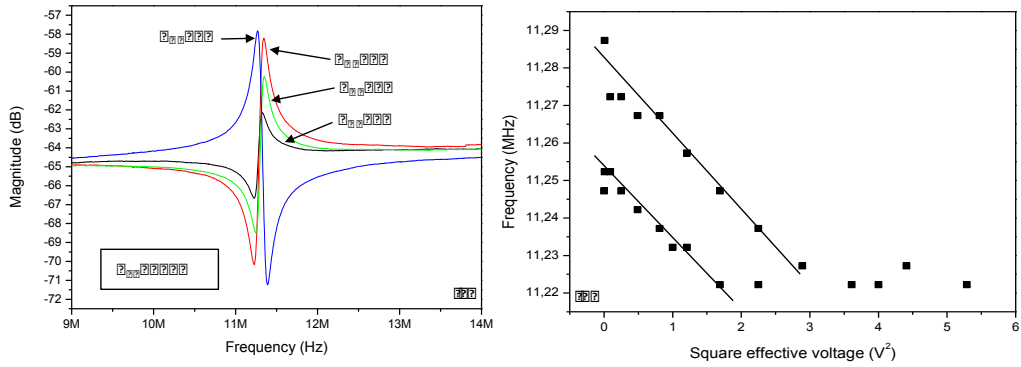


Figure 134.- First mode electrical magnitude response DC sweep from DETF resonator with CMOS amplifier and computed spring softening graph.

The last DETF measures performed corresponds to the self-oscillating configuration which set-up is depicted on Figure 135. The circuit is also biased with 3.3V through a current source and the whole device has 4mA of current consumption. In this case there are not excitation signal because the feedback takes care of excite the resonator and the output signal could be detected by means of an oscilloscope.

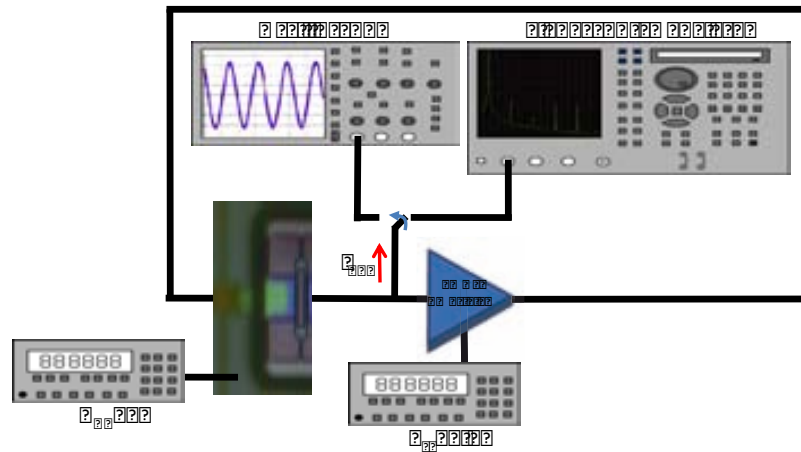


Figure 135.- Electrical set-up for measuring self-oscillating CMOS DETF resonator.

The device is bonded into a PCB and placed inside the vacuum chamber where a pressure of $4.6 \cdot 10^{-3}$ mbar is achieved. When the power of the circuit is switch on, applying 0V on the resonator the output signal of the Figure 136 is obtained. The oscillation is produced due to the effective voltage between the output electrode, polarized at 2.5V, and the resonator which in low pressure conditions is capable to enable enough motional current to produce self-sustained oscillations. The obtained signal has amplitude of 380mV_{pp} with almost sinusoidal shape. The best shape of the waveform in comparison with self-oscillating CCB is attributed to the fact that in the case of DETF the resonator is driven into the linear regime (the non-linear bifurcation

point is found between 632mV_{PP} and 843mV_{PP} . The frequency of 11.5MHz is slightly different from the one obtained in previous experiments because the low pressure decreases the damping forces as well as the forces required for a certain vibration amplitude. However the higher resonance frequency with lower applied signals match with the spring softening behavior studied for the DETF resonator.

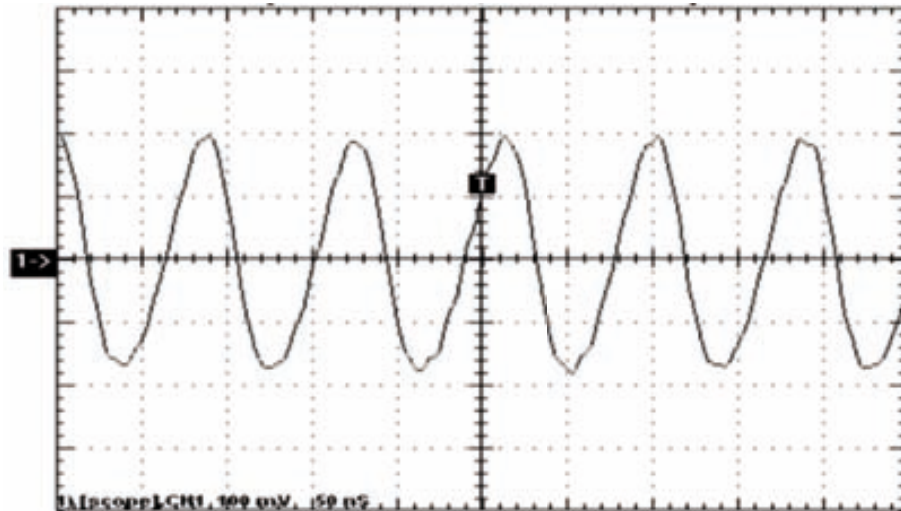


Figure 136.- DETF oscillator signal output detected by an oscilloscope with $V_{\text{DC}}=0\text{V}$ in vacuum conditions of $4.6 \cdot 10^{-3}\text{mbar}$.

In order to fully characterize the oscillator the signal source analyzer set-up of Figure 135 is adopted. This tool has the capability to obtain the spectrum of the signal and compute their corresponding phase noise. In the graph of the Figure 137 there are shown the frequency spectrum at the left side and the phase noise at the right side. There are three graphs superimposed with different DC voltages applied. The measures of 0V and 0.2V have a peak of -10.8dBm at 11.45MHz and at 11.47MHz respectively with a phase noise with an approximately slope of -20dB per decade and -98.9dBc/Hz at 10kHz . The interesting result corresponds to the measure at 0.4V which has a resonance frequency of 11.46MHz with a peak of -20.3dBm and phase noise slope of -60dB per decade which allows to reach around -100dBc/Hz at 1kHz , a value two frequency decades before than the other voltage values and one decade better than other reported CMOS-MEMS oscillators [Hua08]. The explanation of this large difference remains on the kind of operation of the resonator, linear or nonlinear. As there are a 2.5V DC voltage in one electrode the effective voltage between the DETF structure and the electrode is reduced when higher values were applied. In vacuum conditions the resonator without applying DC voltage begins working in nonlinear regime so increasing the applied voltage, the effective voltage is reduced and linear regime is achieved [Mar10b]. The improvement of the phase noise provided by the change between linearity and non-linearity is in good agreement with [Kaa05].

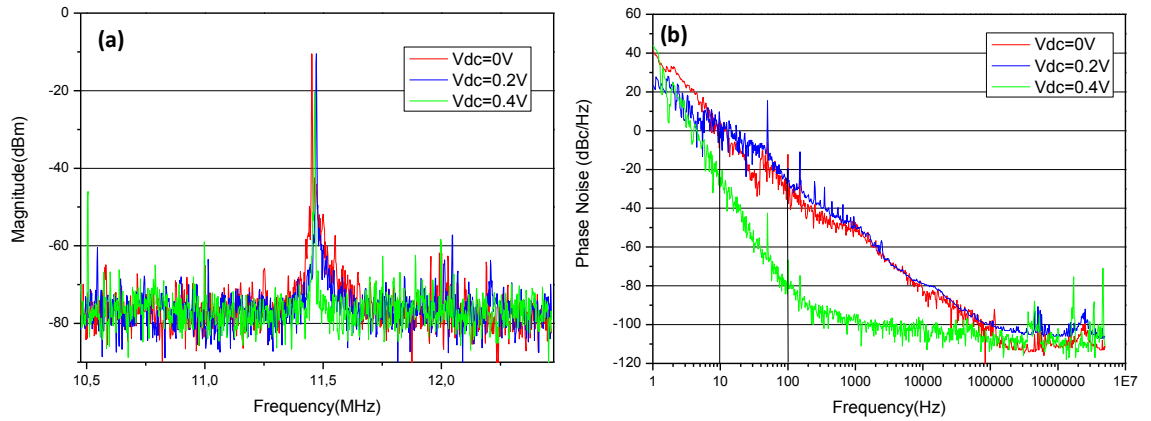


Figure 137.- Signal source analyzer measures for three DC voltages: (a) graph corresponds to the output oscillator signal spectrum and (b) graph is their computed phase noise. These measures were taken into the vacuum chamber with a pressure of $4.6 \cdot 10^{-3}$ mbar.

4.7.3. FREE-FREE RESONATOR

Another mechanical topology which reduces the anchor losses is the free-free resonator depicted on Figure 138. The structure is constructed by one main thicker beam supported by two thinner beams. The support beams are operated at their second lateral mode whilst the main beam is excited to their first lateral mode introducing nodal points with virtual zero displacement in the junctions and reducing the losses of the resonator.

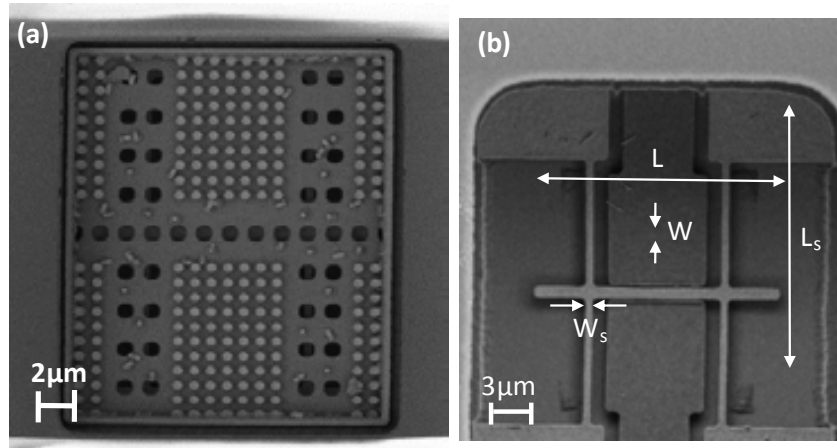


Figure 138.- (a) SEM image of a Free-free packaged after releasing process; the same Free-free resonator without package with main dimensional parameters indicated.

The analytical expression is obtained through the same process than the followed in the second chapter for the cantilever or the CCB. From the Euler-Bernoulli equation the boundary conditions are established to allow the free movement of both ends of

free-free resonator and thus obtaining the resonance frequency equation of [4.157]. The eigenvalues α_n for each mode are the same for free-free and for CCB as well as their corresponding resonance frequency.

$$f_o = \frac{1}{2\pi} \frac{(\alpha_n)^2 W}{L^2} \sqrt{\frac{E}{12\rho}} \quad [4.157]$$

In order to obtain the resonator length a frequency of 24MHz and a main beam width of $0.8\mu\text{m}$ are fixed obtained by means of the previous equation a length of $17\mu\text{m}$ is required. The dimensioning of the supports is made considering that the second lateral mode of CCB is set to 24MHz and their width to $0.4\mu\text{m}$ obtaining a length of $20\mu\text{m}$. Finally the transduction gap is set to 40nm . The device is simulated with FEM software obtaining the modal behavior depicted in Figure 139 with a resonance frequency of 23.93MHz, a spring constant of 97.3N/m and an effective mass of 4.3fg . The free-free resonator is fabricated with a CMOS amplifier in closed loop configuration.

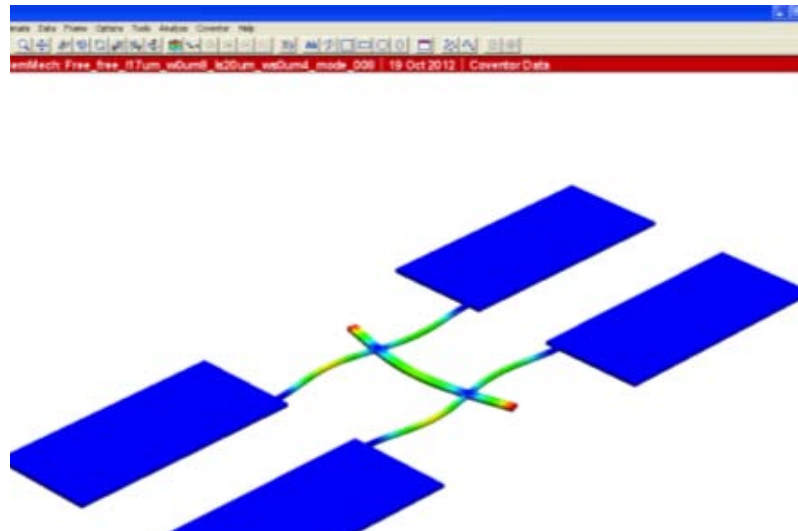


Figure 139.- Simulation of the free-free in their first lateral mode made by finite elements software.

Computing the electromechanical coupling factor and the motional resistance from the electrical model for V_{dc} voltage of 12V for each mode gives the values shown on the Table 16.

Parameter	L (μm)	W (μm)	L_s (μm)	W_s (μm)	g (nm)	f_0 (MHz)	k (N/m)	m (fg)	Q^*	η ($\cdot 10^{-9}$)	R_m (Ω)	I_m/x (A/m)
Value	17	0.8	20	0.4	40	24	97.3	4.3	197	131	4.8 M	19.8

Table 16.- Dimensional parameters and computed values for the Free-free resonator. *Assumed from the measure over the same structure found in [Lop10].

The packaged device was released by wet etching and the self-oscillating set-up of the

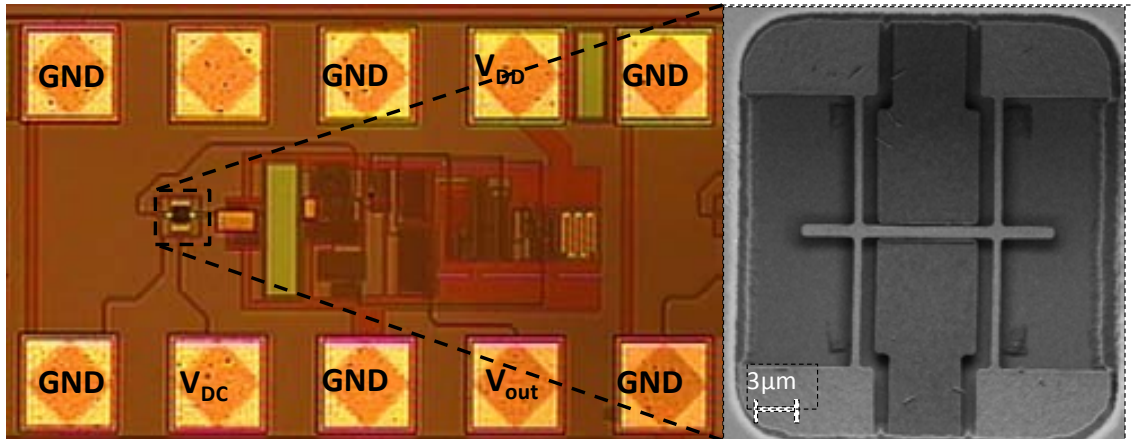


Figure 140 is adopted where the output signal is detected by means of an oscilloscope.

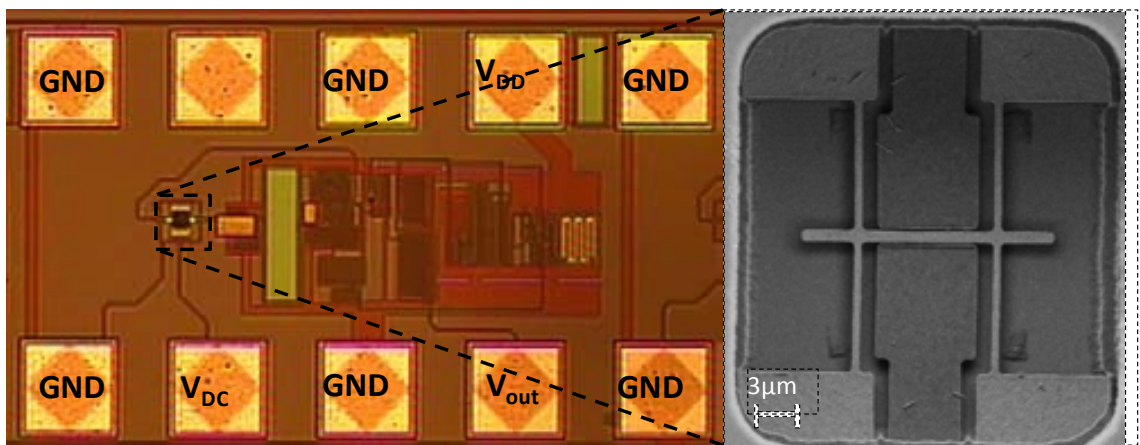


Figure 140.- Free-free resonator in self-oscillating configuration.

A sweep over the DC voltage is performed and shown on Figure 141: at 6V the output current is low to give stable oscillations but increasing beyond 7V it produces a clearly sinusoidal signal of 25.6MHz with amplitude of 400mV_{pp}.

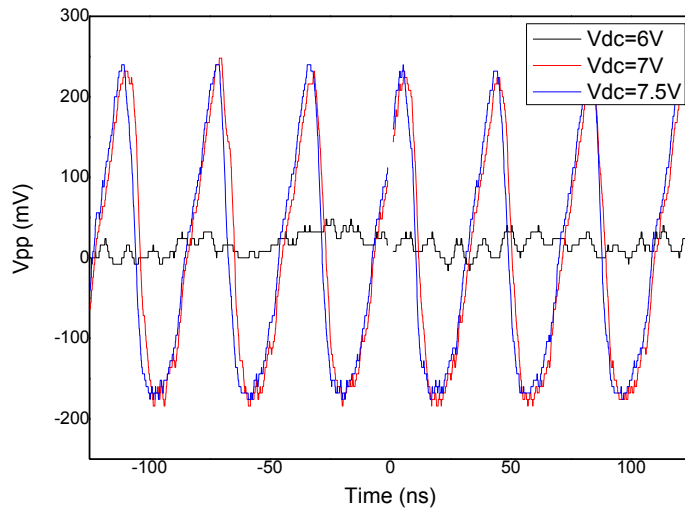


Figure 141.- Free-Free packaged oscillator sinewave periodic output signal for different biasing DC voltages.

4.7.4. CROSS BEAMS RESONATOR

Obtain smaller MEMS resonators with capacitive sensing is a major challenge due to the scaling down of the couplings that decrease the amount of output current and the increase of frequency that raise the parasitic capacitance. The structure called cross beams resonator is designed by two reasons: operate at higher frequencies and maintain enough capacitive coupling [Mar11]. The device, conceptually depicted on Figure 142, consist of two equally CCB coupled perpendicularly with four electrodes in each side. The second flexural mode of each CCB is excited obtaining a zero displacement point in the center of the resonator so each of the fourth small beams could be considered as single CCB operated at their first lateral mode. In summary higher frequency resonator is obtained with at least four times more coupling between the structure and the electrodes (two electrodes are used in excitation and the other two to sense the current).

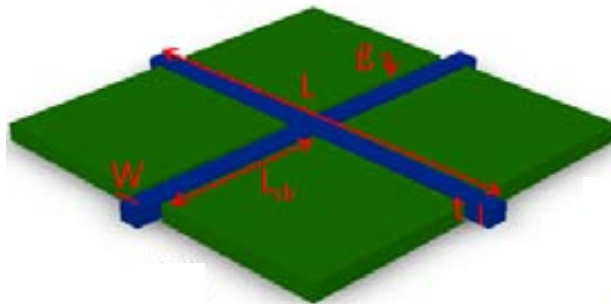


Figure 142.- Cross beams resonator concept and main dimensional parameters.

To design the device the resonance frequency expression obtained from the Euler-Bernoulli formulation of a single CCB is employed and repeated on [4.158] for completion.

$$f_n = \frac{(\alpha_n)^2 W}{2\pi L^2} \sqrt{\frac{E}{12\rho}} \quad [4.158]$$

To compare the coupling area between the cross beams (C_{CB}) and the CCB resonator (C_{CCB}) each driver coupling length have to be considered. The length of the CCB resonating at 250MHz is equal to each arm of the Cross Beams ($L_{CCB} = L_{arm_CB} = \frac{L}{2}$) because the modal profile of the first in plane mode of the CCB is the same as one of the arms of the Cross Beams. The equation [4.158] takes into account the minimum separation distance of the technology ($0.35\mu\text{m}$ for AMS C35B4) and the gap. For large lengths the cross beams structure offers a minimum of 4 times more coupling area, enhancing in this way the capacitive transduction in high frequency and thus increasing the electromechanical coupling factor by means of equation [4.160]. Then, the equivalent motional impedance of [4.161] decreases quadratically with the increasing coupling area in comparison with the CCB.

$$\Delta C_{area} = \frac{C_{CB}}{C_{CCB}} = \frac{4 \left(L_{arm_CB} - \frac{W}{2} - g - 0.35 \right)}{L_{CCB} - 2 \cdot 0.35} \xrightarrow{L_{arm_CB}=L_{CCB}\uparrow} \Delta C_{area} \cong 4 \quad [4.159]$$

$$\eta_{CB} = \Delta C_{area} \cdot \eta_{CCB} \quad [4.160]$$

$$R_m = \frac{\sqrt{k/m_{eff}}}{Q \cdot \eta^2} = \frac{\sqrt{k/m_{eff}}}{Q \cdot (\Delta C_{area} \cdot \eta_{CCB})^2} \quad [4.161]$$

Considering the minimum dimension allowed in the CMOS technology for the beam width and fixing a resonance frequency of 250MHz the resonator length is computed. The transduction gap is established at 100nm. With the first dimensioning the device is simulated with FEM software to obtain the finally dimensions shown on Table 17. To maximize the driver coupling length it is considered the length of each arm ($L/2$), the gap and a fixed separation of 350nm between anchors and electrodes given by the design rules of the CMOS technology. The mechanical modeling parameters and equivalent motional resistance are also computed assuming a quality factor of 200 and a DC voltage of 15V.

Parameter	W (μm)	L (μm)	t (nm)	L _{dr} (μm)	g (nm)	α_n (1 st mode CCB)	α_n (2 nd mode CB)	f ₀ (MHz)	k (N/m)	m _{eff} (fg)	ΔC_{area}	Q*	η (10 ⁻⁹ C/m)	R _m (Ω)	I _{m/x} (A/m)
Value	0.35	7	282	2.875	100	4.730	9.593	250	2968	1.2	4.1	67	44.1	4.84M	69.3

Table 17.- Main design parameters and computed electromechanical coupling factor, motional resistance and transduction gain for the cross beams resonator. *Assumed from the quality factor of single CCB.

The simulations of the Figure 143 represent the different modes that could be excited with the four electrodes with the properly configuration of signals. The first two

modes of Figure 143 are excited at 239MHz and could be enabled connecting the electrodes in parallel in such a form that only one of the arms is oscillating. The interesting mode is the third one excited at 250MHz connecting the electrodes with mirror symmetry respect to the middle of the cross.

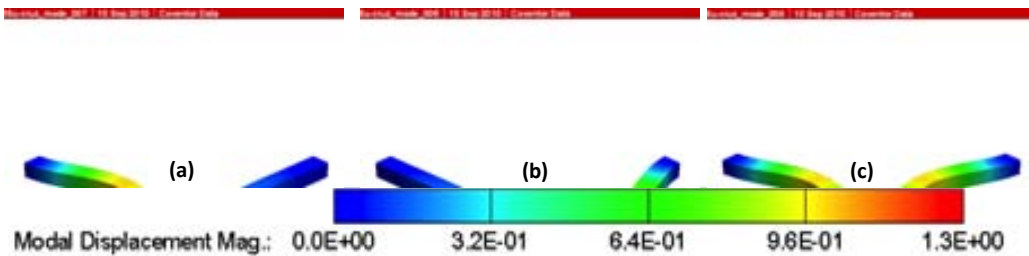


Figure 143.- Simulated lateral modes of the cross beams resonator: (a) 239MHz and (b, c) 250MHz.

Once the main dimensional parameters are established some additional layout considerations are made. The structural material chosen is the first polysilicon layer and the second polysilicon layer used for the electrodes. A vertical stack of metals and vias is placed above the electrodes in order to avoid the falling down of the electrodes due to the final etching process. Two vias with the shape of the resonator are placed to reduce the amount of silicon oxide above the MEMS and reduce the required etching time. Finally a square window of $15\mu\text{m}$ is defined as a PAD opening to leave the resonator without the passivation layer and allow the releasing of it. The whole layout is shown on the following image:

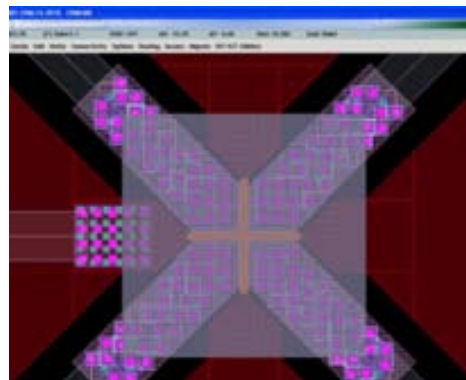


Figure 144.- Cross beams resonator whole layout with releasing adapted via and electrodes sustaining metal paths.

In the Figure 145 there are shown SEM images before and after the post CMOS releasing process. Note that the in the left image the square window on the PAD layer and the vias defined are clearly visible. After releasing it can be seen that the square PAD window is enlarged, the vias have gone and due to the tolerance of the fabrication process the dimensions designed have changed ($L=7.5\mu\text{m}$, $W=380\text{nm}$). With these

dimensions the simulated resonance frequency using Coventor is 239MHz. The (c) Figure 145 shows a zoom which reveals that the gap between the resonator and the electrodes is not homogeneous in each driver and can vary from 119nm to 214nm. The gap differences are high enough to produce different electrical couplings between electrodes and resonator depending on the arm of the cross beam.

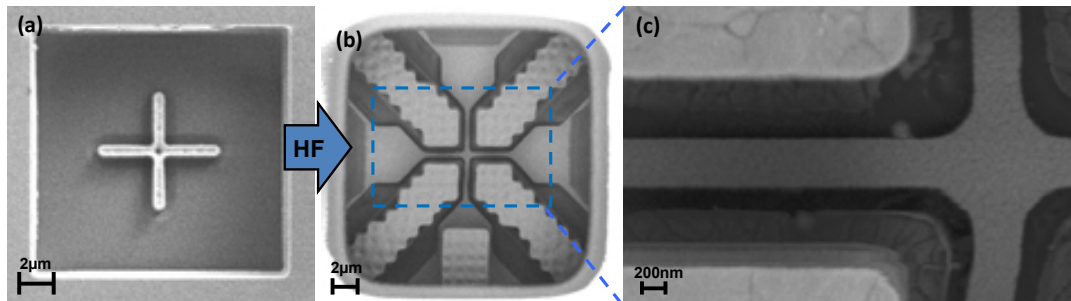


Figure 145.- SEM images of the fabricated cross beams resonator: (a) before, (b) after releasing and (c) zoom with electrodes and gap details.

To further characterize the final shape of the electrodes after the releasing process a FIB cut is done along one of the beams of the resonator, Figure 146. In the section is clearly visible the stack of metals and vias that support the polysilicon electrodes and how it seems that the structure has some remaining oxide underneath. Also it can be appreciated some defects on the second polysilicon electrodes, which can further produce differences on the electrical coupling between them and the resonator.

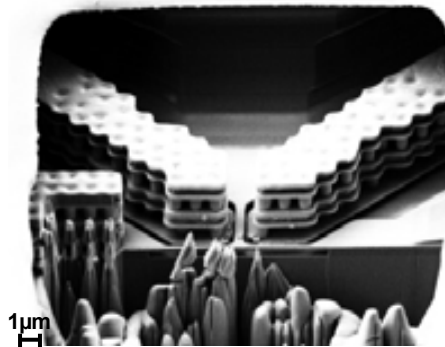


Figure 146.- Cross beams resonator section SEM image.

For the electrical characterization we designed the cross beams resonator with four electrodes connected to four pads and the structural layer connected to another pad. For this electrical characterization the set-up shown in Figure 147 is employed.

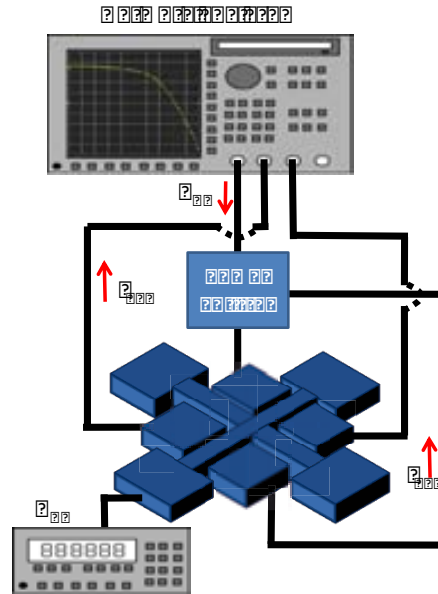


Figure 147.- Four ports electrical set-up employed for cross beam resonator.

The DC voltage is applied through a voltage source whilst the electrodes are connected to a four ports network analyzer (Agilent E5071B). Due to some oxide remaining under the resonator and several damaging of the electrodes it has not been possible to obtain a resonant frequency response. Despite no resonance is found we can use the electrical characterization out of resonance to analyze the effects of the differences of coupling between the electrodes. This electrical characterization shows that there are very significant differences in the capacitive couplings between electrodes: out of resonance (234MHz) for S21 is -84dB, for S31 is -75dB and for S41 is -96dB. In fact to allow a proper excitation of the desired mode of the cross beam and an optimal capacitive transduction (with the addition of the current from two different electrodes), the couplings between electrodes must be equal.

In order to check how the gap differences appreciated in the SEM images affect the electrical characterization along with differences on the parasitic capacitance, electrical simulations have been done. The electrical model for a linear MEMS resonator with electrostatic excitation and capacitive sensing is depicted on left Figure 148 for cross beams resonator in case that there are two different coupling. The parameters extracted from the electrical characterization of the Table 18 have been used. The R_m has a very strong dependence on the gap between the resonator and the driver ($R_m \sim g^4$). C_p will differ from each one since they depend from the out-of-resonance couplings as we have stated experimentally. In fact, this C_p in a two port system is mainly due to the parasitic capacitance between the contact pads of the excitation and read-out driver, which will be very different due to the layout of the pads. The C_p was determined from the coupling measures (R_{NA}) obtained previously.

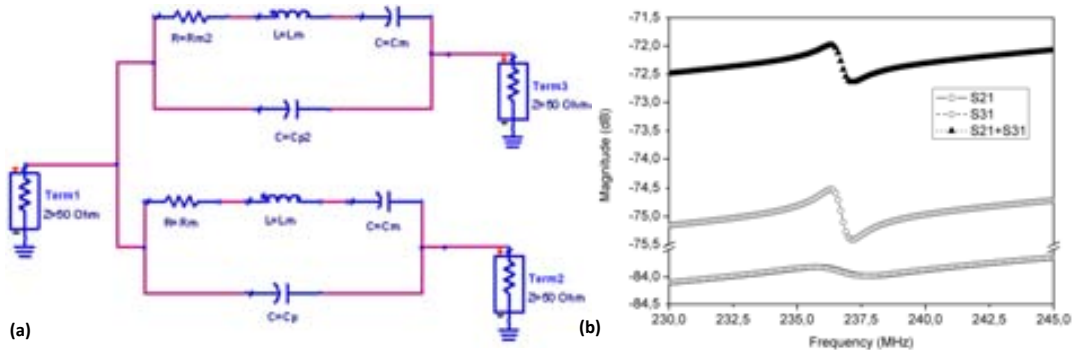


Figure 148.- (a) Electrical model for cross beams resonator with different couplings; (b) electrical simulations obtained from the cross beams model.

Considering a quality factor of 200, the resonance frequency of 239MHz, $V_{DC}=5V$ and the values of the dimensional and electrical measures from Table 18, the right graph of Figure 148 is obtained. In the Figure 148 are represented the S21 measure, the S31 measure and the combination of the two currents. It can be appreciated that the S21 magnitude shows a bigger resonance curve than the combination of S21 and S31, this is due as we have already explained due to the different electrical coupling between the electrodes. The differences in the designed dimensions and parasitic capacitances produce different couplings. The differences in gap, and thus in motional resistance (a factor of 10, see Table 18) affect the amount of signal detected due to the displacement of the MEMS. Additionally different parasitic capacitances appear due to the different place of the electrodes in the layout. It can be seen that the coupling between P1 and P3 is higher than P1 and P2 because between P1 and P2 exist a pad grounded while between P1 and P3 the distance is lower. So the theoretically improvement in coupling area using cross beams structure is negligible if the gap is not almost the same in all the electrodes and the pads were placed without symmetry.

Measure	R_{NA} (dB)	C_P (fF)	Gap (nm)	R_m (M Ω)	L_m (H)	C_m (aF)
S21	-84	0.4	214	54.9	3.14	0.14
S31	-75	1.2	119	5.25	0.97	0.46

Table 18.- Coupling measures out of resonance (234MHz) to extract parasitic capacitance and model parameters.

4.8. CONCLUSIONS

In this chapter the capacitive sensing method applied on MEMS has been explained highlighting the most relevant parameters. Different mechanical configurations of MEMS have been designed for resonator and oscillator applications. The Table 19 summarizes the devices measured sorted by increasing resonant frequency. From the quality factor point of view the highest value is obtained by the Free-free structure, the DETF oscillator has been locked on the first mode and thus the quality factor is not enhanced. In relation with electromechanical coupling factor the Free-free

offer the highest value due to their large coupling area and small transduction gap. It is remarkable that comparing the two similar CCB structures a smaller gap provides better electromechanical coupling factor despite the higher DC voltage. The cross beams resonator provides a similar electromechanical coupling factor than the CCB with a resonance frequency one order of magnitude higher. In this sense the multiple electrodes approach of cross beams allow the scaling down maintaining a large coupling area enough to be measured. The motional resistances obtained are high compared with the state of the art but the MEMS devices presented here are much smaller. An effective strategy to decrease this motional resistance consist on increasing the electromechanical coupling factor and reducing the transduction gap is the best option due to their quadratic dependence. Finally the phase noise obtained by DETF oscillator provides a state of the art solution in comparison with integrable CMOS-MEMS oscillators.

Device	f_0 (MHz)	Q	η ($\cdot 10^{-9}$)	R_m (Ω)	I_m/x (A/m)	S_{Φ} (dBc/Hz) at 1kHz
DETF	11.86	39	56 ($V_{dc}=4V$)	9.04M	4.18	-100
Free-free	25.60	197	131 ($V_{dc}=12V$)	4.80M	19.80	-
CCB	27.01	67	34 ($V_{dc}=15V$)	3.40M	5.98	-
CCB	28.07	67	70 ($V_{dc}=5V$)	754k	12.34	-
CCB	50.92	82	62 ($V_{dc}=6V$)	3.75M	19.83	-
Cross beams	250	67	44 ($V_{dc}=15V$)	4.84M	69.3	-

Table 19.- Summary over the parameters of MEMS resonators with capacitive sensing sorted by ascending resonant frequency.

5. PIEZORESISTIVE SENSING MEMS

One of the principal objectives of the NEMESYS project is to design and fabricate small resonators with more advanced CMOS technologies. In the previous chapter capacitive transduction has been extensively reported with several resonators and measures. It is well known that capacitive sensing offer reliability, integrability and low complexity set-ups. However capacitive sensing in small devices is extremely challenging due to the increase of the resonant frequencies reduces drastically the amount of motional current and furthermore the parasitics are also increased. Another problem in capacitive sensing comes from the highly motional resistances obtained which increase the complexity and the power consumption of the CMOS circuits to make oscillators. There are some methods capable to reduce the amount of parasitic current in capacitive sensing such as separating the frequencies of motional and parasitic currents [Ura07] or canceling the parasitic current by differential measures [Ura09]. But these methods imply the increase on chip area as they require specific electronic circuits which raise their complexity, power consumption and cost.

In order to provide solutions to these problems alternative sensing methods that could provide better performance at smaller scales will be studied. One alternative approach is to exploit the piezoresistive effect from semiconductor and metal materials which in theory requires virtually the smallest area possible as the detection is done by the flowing current through the resonator (there is no need of electrodes or additional structures to make the sensing which increase the whole area). The piezoresistive effect has been known since the work of Smith at Bell Laboratories in 1954 which described the effect of stress on doped silicon and germanium [Smi54]. Since then the MEMS based on piezoresistive sensors have been widely used for pressure sensors, accelerometers, cantilever force sensors, inertial sensors and strain gauges which applications comprise a substantial market share of MEMS sensors in the market from early 90's till today, [Bry96], [Knu98], [RoMp11].

In particular the main goal of improving resonators could be divided into four objectives in this chapter:

- Design and fabricate MEMS resonators based on piezoresistive sensing.
- Achieve high resonant frequencies with small RF-MEMS.
- Establish the piezoresistive characteristics of CMOS polysilicon.
- Provide a comparison between piezoresistive and capacitive sensing.

5.1. STATE OF THE ART

From the early beginnings of MEMS devices piezoresistive sensing was an important method to detect strain. The first reported piezoresistive device was a silicon cantilever [Wil68] mechanically deflected by electrically induced thermal expansion. The desired temperature gradient is produced by dissipating electrical power in a diffused resistor located near the cantilever support. The silicon cantilever with a length of 380 μm , 30 μm of width and 8 μm of thickness was loaded with a mass to decrease the resonant frequency to 1900Hz and deflections in the order of microns were observed.

Later, the application of piezoresistive sensing to cantilevers structures has allowed the development of AFM microscopy [Bin86] described on the introduction chapter. Using an AFM probe with integrated piezoresistive read-out has been used as environmental sensor [Boi00]. The cantilevers with a length of 200 μm , a width of 50 μm and 1.5 μm are fabricated in silicon and SiO₂ with integrated polysilicon resistors, Figure 1. Since the devices are bilayered structures they could be employed to detect differences in the thermal expansion coefficient of the two materials. Depositing a water-absorbing polymer layer on the cantilevers makes possible to transform the devices into a humidity sensors. Finally, after protecting the metal wires with some coating the cantilevers are immersed in water and used to detect injected alcohol.

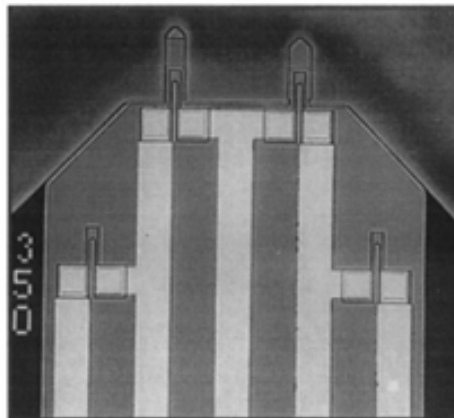


Figure 1.- Microscope image of AFM probe with integrated piezoresistive read-out, [Bo00].

Piezoresistive sensing in MEMS was also applied to sense pressure [Lam05] or inertial magnitudes like acceleration [Lyn03, Har10] or coriolis force [Gré99]. An accelerometer is shown on Figure 2 (a) where a proof mass is micromachined into a lightly implanted piezoresistive layer and the current is detected into heavily implanted conductors. The Figure 2 (b) is a MEMS gyroscope based on a mass attached to two beams with embedded piezoresistive sensors. The accelerometer of the Figure 2 (c) is

fabricated in AMI 0.5 μm CMOS technology employing anisotropic and isotropic etchings to define the proof mass and release the cantilevers. The proof mass is composed by a stack of metal layers and single crystal silicon from the substrate and the bimorph cantilevers are made by polysilicon and silicon dioxide.

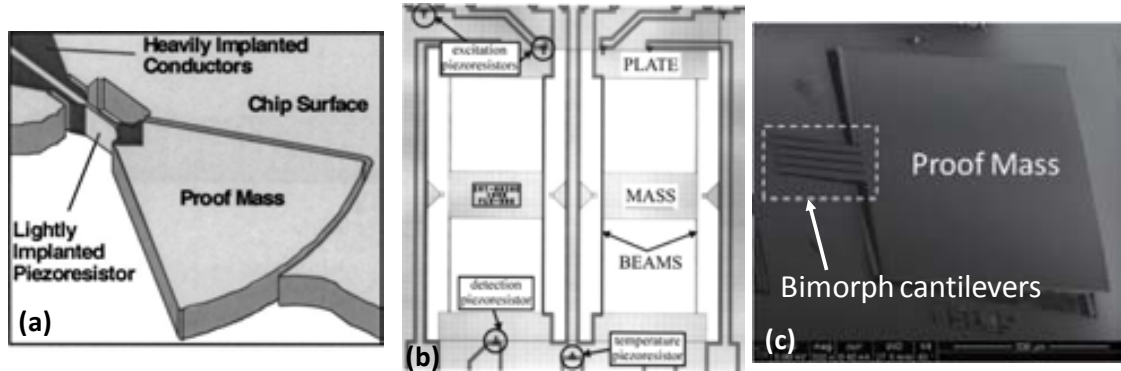


Figure 2.- Inertial MEMS sensors based on piezoresistive sensing: (a) single chip accelerometer [Lyn03], (b) gyroscope based on tuning fork structure with embedded piezoresistors [Gré99], (c) CMOS-MEMS accelerometer with embedded poly resistors on cantilevers [Har10].

In the field of RF-MEMS van Beek [VanB06] has demonstrated the capability to fabricate piezoresistive silicon resonators with bulky modes achieving quality factors from 100000 to 150000 at 10MHz, extracting the corresponding gauge factor (ratio between resistance change and strain) of 65 ± 20 and measuring a resistance of 174 Ω , Figure 3 (a). In addition, a comparison between capacitive and piezoresistive sensing is also performed giving a ratio of 130 between the two most representative magnitudes of both methods (motional impedance for capacitive and transconductance gain for piezoresistive). Later [VanB07], has also shown that such devices could be scaled down obtaining resonant frequencies from 18MHz to 1GHz with smaller resistances from 1.2 Ω to 2.1 Ω . In this case the ratio between both methods is further increased when scaling down the geometry to resonate at higher frequencies, which clearly demonstrates the advantage of piezoresistive instead of capacitive sensing for recording the resonator motion. With the aim to develop a fully functional oscillator an improvement of LBAR³³ called dogbone resonator was designed [VanB08] and measured with amplifier circuit in closed loop topology [Bon09], Figure 3 (b).

³³ Longitudinal bulk acoustic resonator

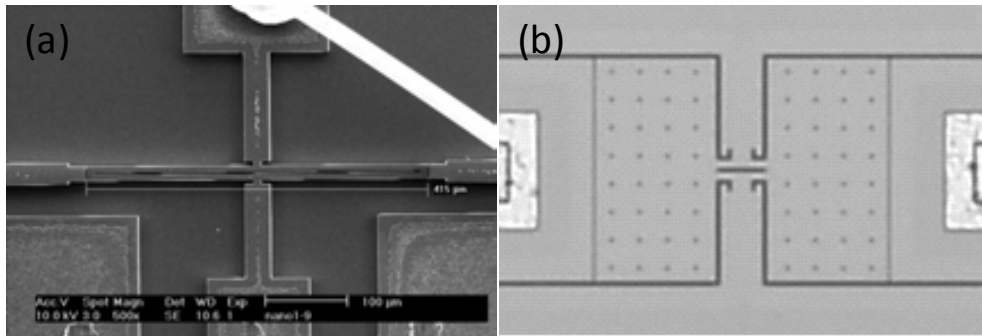


Figure 3.- Silicon MEMS resonators with embedded piezoresistive sensing: (a) LBAR resonator [VanB06], (b) dogbone resonator [VanB08].

From Taiwan there are presented some contributions based on the employment of TSMC 0.35 μ m CMOS technology. Employing a stack composed by metals, silicon dioxide and polysilicon the flexural MEMS structure and the lateral electrodes of the Figure 4 (a) are defined by means of photolithography mask and RIE etching [Chi06]. A different approach is depicted on Figure 4 where the top electrode is composed by top metal and silicon dioxide (b₁) whilst the Free-free beam (b₂) structure is made by another metal layer, silicon dioxide and polysilicon [Li12]. The metals are used to drive the device and the embedded poly resistor provides the piezoresistive current.



Figure 3. Cross-section of the movable and fixed comb.

(a)

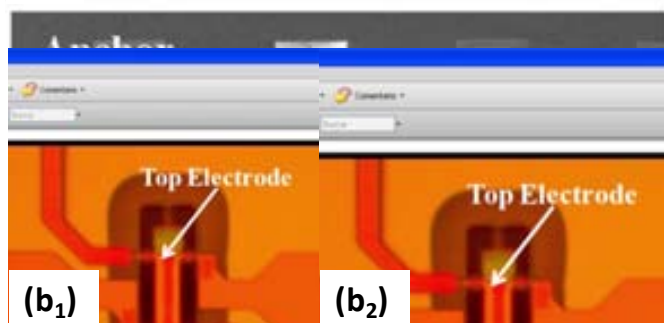


Figure 4.- CMOS-MEMS resonators with electrostatic excitation and piezoresistive sensing made by TSMC CMOS technology: (a) Side electrodes and cantilever metal/SiO₂/poly structure [Chi06]; (b₁) top metal electrode and (b₂) Free-free beam resonator with embedded piezoresistor [Li12].

The materials with higher piezoresistive effect were crystal materials like germanium or silicon. However semi crystal materials also behave piezoresistively

enough to employ this type of sensing in such materials. Piezoresistive effects in polysilicon were studied extensively from 1970s [Onu72] and a theoretical model as a function of doping, grain size and orientation is proposed in 1984 [Fre84]. Recently, the use of polysilicon in piezoresistive MEMS devices is reported [Cro09] in a vertically oriented piezoresistive transducer capable to achieve quality factors from 300 to a few thousand at 7MHz with a gauge factor of 5 and a resistance from 1.6M Ω to 74k Ω , Figure 5.

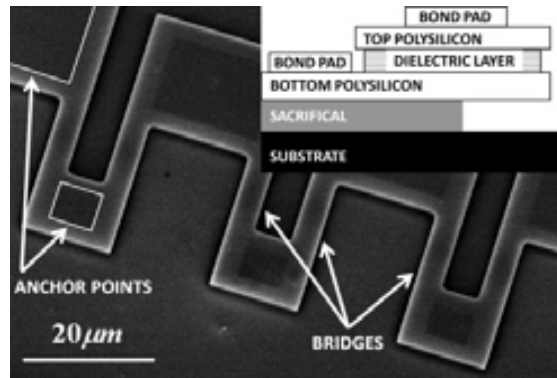


Figure 5.- Polysilicon MEMS resonator based on piezoresistive transduction, a serie of bridges is composed by doped polysilicon and SiO₂ layers (p_{bottom} -SiO₂- p_{top}) with thicknesses 277nm-53nm-303nm, [Cro09].

Related with the smallest resonators fabricated silicon nanowires have shown their good performance in piezoresistive transduction, [Yan06]. The nanowires have lengths between 5 μm and 0.5 μm with diameters from 100nm to 30nm achieving frequencies covering VHF, UHF and microwave ranges with a gauge factor of 5000. To enable piezoresistive detection in nanowires a set-up scheme based on lock-in amplifier is implemented, [He08].

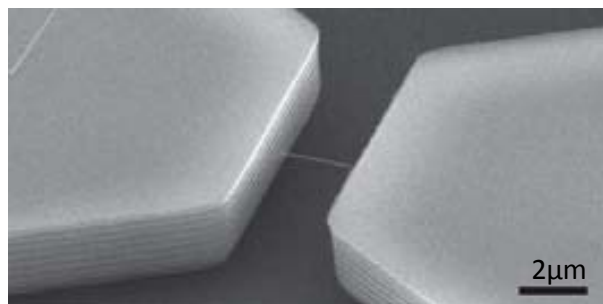


Figure 6.- Single nanowire with the $\langle 111 \rangle$ growth direction used in piezoresistive transduction set-up, [He08].

The use of piezoresistive transduction has been also demonstrated on CMOS technologies. In [Zal10] it is fabricated the arch bridge of the Figure 7 with the AMI 1.5 μm CMOS technology employing a stack of two polysilicon with the available layers

and applying few post-CMOS processes (two etchings and one photolithography steps). The arch bridge has a length of $10.5\mu\text{m}$, a width of $1.5\mu\text{m}/4.5\mu\text{m}$ and a thickness of $200\text{nm}/420\text{nm}$ for first and second polysilicon respectively. This resonator exhibits a resonance frequency of 36MHz , a quality factor of 800 and a resistance of 600Ω . Another approach to employ piezoresistive transduction in CMOS polysilicon was performed in [Chi08] where the structure of the resonator is composed by a stack of metals and the polysilicon layer to sense the motion. The composite beam device has fabricated in TSMC $0.35\mu\text{m}$ 2p4m CMOS technology and shows a resonant frequency of 14.5kHz and a quality factor of 36.

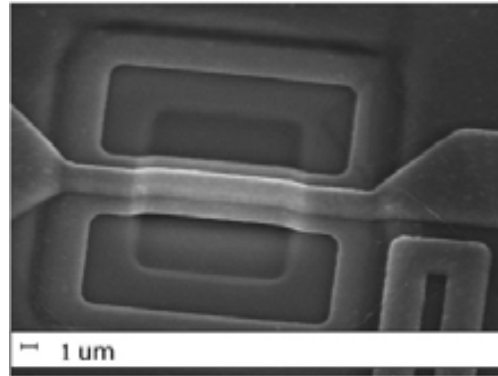


Figure 7.- arch bridge resonator composed by two polysilicon thin layers with SiO_2 between them [Zal10].

Recent contributions of MEMS resonators are focused on thermally actuation and piezoresistive readout [Rah11, Hal12], Figure 8. The dogbone structures are patterned in the top low resistivity silicon layer of SOI wafer and then released by etching the underlying silicon dioxide. The working principle of such devices is based on the input AC signal which through the resistor losses causes a temperature fluctuation that is turned into an AC mechanical force then the displacement is turned into an electrical signal by piezoresistive effect. The thermomechanical actuation and piezoresistive sensing could be smartly employed to develop an oscillator from a single resonator without amplifier [Rah11]. The key lies on the negative longitudinal piezoresistive coefficient which provides a negative resistance which is capable to surpass the electrical resistance of the actuators in every cycle leading to instability of the resonant system and self-sustained oscillation.

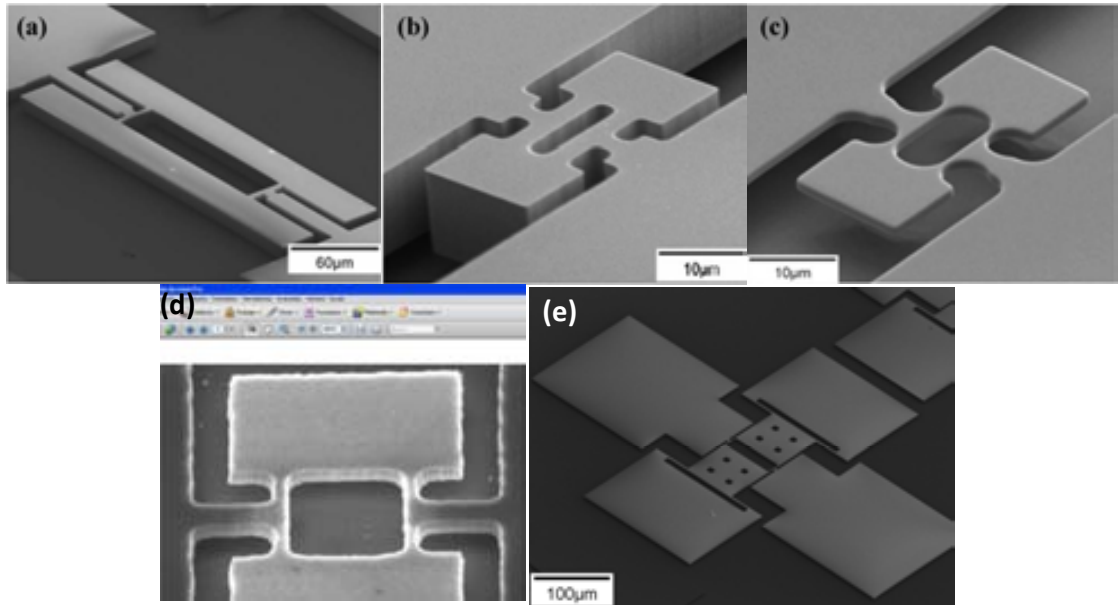
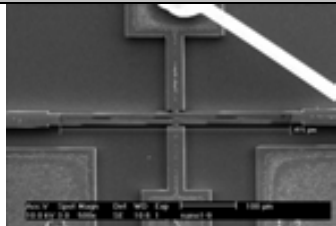
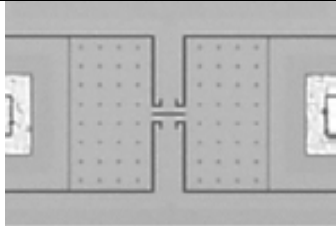



Figure 8.- Single crystal silicon MEMS with thermal actuation and piezoresistive sensing: (a,b,c) 7.9MHz, 61MHz and 41MHz dogbone resonators from [Rah11]; (d) 112MHz dogbone resonator from [Hal12]; (e) dual-plate 6.6MHz self-sustained oscillator [Rah10] .

The following Table 1 summarizes the main important parameters from the MEMS resonators reported in this section.

Ref.	Device	f_0 (Hz)	Q	R (Ω)	Current (A)	g_m (μ S)
[VanB06]		10M	150k	174	10m	92
[VanB08]		15.3M	66.6k	600	3m	904
[Chi06]		14.5k	36	51k	1.2m	-

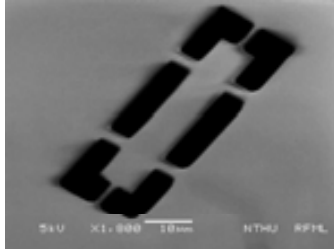
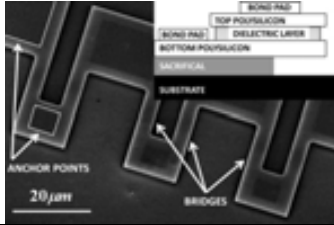

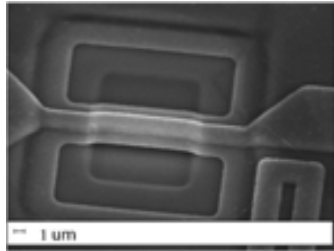
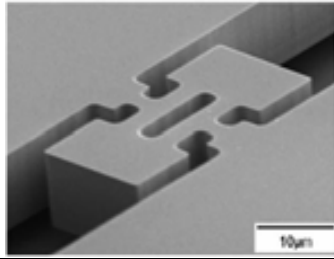
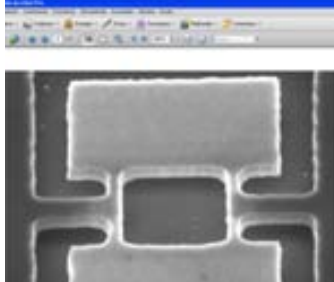
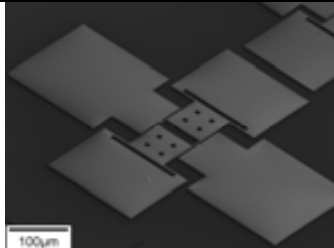
[Li12]		8.73M	4.2k	-	3m	-
[Cro09]		7M	-	74k	-	-
[He08]		75M	700	300k	-	-
[Zal10]		36.85M	800	600	-	-
[Rah11]		61M	12k	4.2	100m	21.5k
[Hal12]		112M	2.25k	3k	0.7m	1.83
[Rah10]		4.5M	48.5k	2k	3.5m	211

Table 1.- Comparison between some state of the art CMOS-MEMS resonators with piezoresistive sensing.

Figure 9 shows a rectangular beam subjected to uniaxial force F .

The definition of the electrical resistance for a homogeneous structure is function of its dimensions, shape and resistivity. The change in resistance due to applied stress is a function of geometry and resistivity changes. A longitudinal strain produces a reduction of the cross-sectional area in proportion with its Poisson's ratio ν . For metals the Poisson's ratio ranges from 0.2 to 0.35 and for anisotropic silicon ranges from 0.06 to 0.36 [Bra73, Fra04]. The fractional resistance change could be derived considering a rectangular beam with a length l and a cross sectional area A , Figure 9. The electrical resistance corresponds to the expression [5.1], where ρ_e is the electrical resistivity of the beam material. When the beam is subjected to a uniaxial force in both sides their cross section and length are changed and correspondingly this equivalent electrical resistance [5.2]. Hence, the piezoresistive effect is due to geometrical and material changes which are present in all materials but pronounced in materials that have high resistivity change $\frac{\Delta \rho_e}{\rho_e}$.

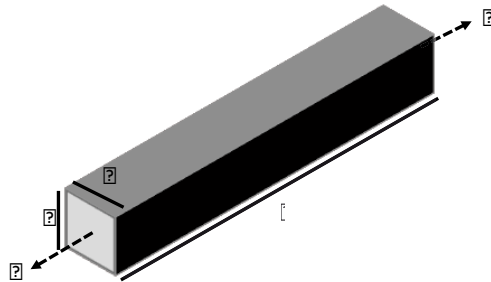


Figure 9.- Rectangular beam subjected to uniaxial force F .

$$R = \frac{\rho_e l}{A} \tag{5.1}$$

$$\frac{\Delta R}{R} = \frac{\Delta \rho_e}{\rho_e} + \frac{\Delta l}{l} - \frac{\Delta A}{A} \tag{5.2}$$

As it was explained in the second chapter the strain is defined as $\frac{\Delta l}{l}$ and considering their relation with the stress through the young modulus $\frac{\Delta l}{l} = \frac{\sigma}{E}$ and that the cross sectional area change is related with Poisson ratio as $\frac{\Delta A}{A} = -\nu \frac{\Delta l}{l}$ the change in resistance follows the equation [5.3] where the first two terms reflect the geometric effects and the third one the change in resistivity.

$$\frac{\Delta R}{R} = \left(\frac{\Delta \rho_e}{\rho_e} + \frac{\Delta l}{l} + \nu \frac{\Delta l}{l} \right) \tag{5.3}$$

For metals the change in resistivity is small, on the order of 0.3 so the geometric effect prevails. In the case of semiconductors the change in resistivity is 50-100 times larger than the geometric term but as same as the elasticity, the piezoresistivity is

direction-dependent under specified direction of loads. The geometric effect contribution to the change in resistance of [5.3] has a minimum value of 1 and a maximum of 2 obtained through the minimum and maximum Poisson ratio values. So a valid approximation in piezoresistive materials is that the fractional change in resistance corresponds almost to the fractional change in resistivity, [5.4]. For crystal type semiconductor materials the relative change in resistivity is related with the stress through a 6x6 square matrix of piezoresistive coefficients where each subscript refers to the electric field, current density and stress directions [Kanda1982], equation [5.5] and [5.6].

$$\frac{\Delta R}{R} \cong \frac{\Delta \rho_e}{\rho_e} \quad [5.4]$$

$$\frac{\Delta R_\omega}{R_\omega} = \sum_{\lambda=1}^6 \pi_{\omega\lambda} \sigma_\lambda \quad [5.5]$$

$$[\pi_{\omega\lambda}] = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{22} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \quad [5.6]$$

A simplification of the number of piezoresistivity coefficients required is obtained considering that stress is in the direction of the flowing current and/or perpendicular to it. In these cases the fractional change in resistance can be written as a function of longitudinal π_l and transverse π_t piezoresistive coefficients, [5.7].

$$\frac{\Delta R}{R} = \pi_l \sigma_l + \pi_t \sigma_t \quad [5.7]$$

The piezoresistive coefficients are direction and doping dependant so the values for longitudinal and transverse piezoresistive coefficients will differ in function of the crystal orientation and the kind of impurities implanted (considering low doping concentration of $n < 10^{17} \text{ cm}^{-3}$). The Table 2 shows selected values for piezoresistive coefficients for silicon.

	n-type			p-type		
	[500]	[510]	[511]	[500]	[510]	[511]
$\pi_l (10^{-11} \text{ Pa}^{-1})$	-102.2	-31.2	-7.5	6.6	71.8	93.5
$\pi_t (10^{-11} \text{ Pa}^{-1})$	53.4	-17.6	6.1	-1.1	-66.3	44.6

Table 2.- Longitudinal and transverse piezoresistive coefficients for silicon n and p type in different crystal orientations, [Kaa09].

Finally, dividing the fractional resistance change by the strain the gauge factor (GF) parameter as a dimensionless figure-of-merit in piezoresistive sensing is obtained, equation [5.8]. As the Poisson's ratio for almost all materials is between 0 and 0.5 the gauge factor for purely geometrical changes vary from 1 to 2. Most of metals are characterized for small change in resistivity in contrast of semiconductors in which case the geometric effect could be neglected in front of the material effect. In the Table 3 there are shown some values for the gauge factor for different materials. The huge range and the sign in case of semiconductors are due to the crystal orientation and doping dependence of piezoresistive coefficients. The nickel is an exception in the case of metals as it exhibits significant resistivity change in addition to geometrical effects.

$$GF = \frac{\Delta R/R}{\varepsilon} \quad [5.8]$$

Material	Gauge Factor
Al	1.4
Cu	2.1
Ni	-12.6
Pt	2.6
Si	-102 to 135
Si (poly)	-30 to 40

Table 3.- Gauge factors for some metals and semiconductors, [Hul99].

5.3. PIEZORESISTIVE TRANSDUCTION

To obtain the expression of the change in resistance in function of the motion an excitation method must be chosen. The electrostatic excitation is the most simplest and powerful method with our kind of devices which are integrated in CMOS technologies. An electrode is placed smartly to excite the desired mode (flexural or bulk modes) applying electrical signals at the resonant frequency over an air gap. The electrical signal exerts the force given into equation [5.9] which has been deduced on [2.97] in second chapter and rewritten here for comprehension. The excitation voltage is composed of a superposition of a DC voltage plus a much smaller AC voltage.

$$F_x = V_{DC} V_{ac} \frac{\varepsilon_0 A}{g^2} e^{j\omega t} \quad [5.9]$$

Solving the equation of motion of the spring-mass system gives the displacement $u(x,t)$ as a function of location and driving frequency as it has been explained in second chapter. Then, the integrated strain is computed using equation [5.10] and the change in resistance equals to equation [5.11].

$$\varepsilon = \frac{du(x,t)}{dx} \quad [5.10]$$

$$\frac{\Delta R}{R} = \frac{GF}{l} \int_0^l \frac{du(x,t)}{dx} dx \quad [5.11]$$

To sense the change in resistance a DC voltage is applied across the resonator structure and the current flow from equation [5.12] is sensed, where the approximation is valid when the change in resistance is much smaller than 1. The value of R represents the nominal resistance of the current path of the device. Developing the equation [5.12] by means of Taylor approximation and considering that $I = V_0/R$ the equation [5.13] is found where the fractional change in current is directly related with the fractional change in resistance allowing the piezoresistive sensing through current sensing.

$$I \mp \Delta I = \frac{V_0}{R \pm \Delta R} \cong \frac{V_0}{R} \left(1 \mp \frac{\Delta R}{R} \right) \quad [5.12]$$

$$\frac{\Delta I}{I} = \frac{\Delta R}{R} \quad [5.13]$$

5.4. ELECTRICAL MODELLING

An electrical small signal model of piezoresistive sensing is used [VanB06] assuming that the excitation signal and the sensing signal are both composed by large DC terms and small AC terms. Then the modulation current across the resonator could be written as equation [5.14], where the drainconductance is related to the electrical resistance with $g_d = 1/R$ and the transconductance is obtained through equations [5.10-5.11] for each resonator topology.

$$i_d = \left(\frac{\partial I_d}{\partial V_d} \right) \cdot v_d + \left(\frac{\partial I_d}{\partial V_g} \right) \cdot V_{AC} = g_d \cdot v_d + g_m \cdot V_{AC} \quad [5.14]$$

The equivalent small signal model of piezoresistive sensing resonator is depicted on Figure 10 where a voltage dependant current source represents the modulation of current through the induced strain and the resistance in parallel represents the current path resistance.

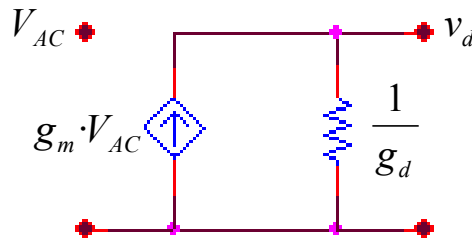


Figure 10.- Small signal model for piezoresistive sensing.

5.5. CLAMPED CLAMPED BEAM

In order to establish the piezoresistive capability of CMOS polysilicon, the simple CCB mechanical structure was adopted. The CCB has been easily released and capacitively sensed so using this structure could help in piezoresistive measures. From [He08] it has been demonstrated that flexural structures such as CCB could be piezoresistively sensed. The compensation of tensile with compressive stress avoid the standard piezoresistive sensing however there are a lengthening of the deflected beam that produces a nonvanishing longitudinal strain through it which value could be calculated from equation [5.15] and [5.16].

$$\Delta l = \int_0^{l_0} (dl - dx) dx \quad [5.15]$$

$$dl = \sqrt{\left(\frac{du}{dx}\right)^2 + \left(\frac{dx}{dx}\right)^2} = \sqrt{\left(\frac{du}{dx}\right)^2 + 1} \quad [5.16]$$

Then, from the definition of strain it becomes as equation [5.17].

$$\varepsilon = \frac{\Delta l}{l_0} = \frac{1}{l_0} \int_0^{l_0} \left(\sqrt{\left(\frac{du}{dx}\right)^2 + 1} - dx \right) dx \quad [5.17]$$

Applying the theorem of binomial expansion the strain is approximated by equation [5.18].

$$\varepsilon \cong \frac{1}{l_0} \int_0^{l_0} \left(1 + \frac{1}{2} \left(\frac{du}{dx}\right)^2 - dx \right) dx = \frac{1}{2l_0} \int_0^{l_0} \left(\frac{du}{dx}\right)^2 dx = 2.44 \left(\frac{u_{max}}{l_0}\right)^2 \quad [5.18]$$

Where u_{max} is the displacement at the beam center. Then, the change in resistance could be expressed as equation [5.19].

$$\frac{\Delta R}{R} = GF \cdot 2.44 \left(\frac{u_{max}}{l_0}\right)^2 \quad [5.19]$$

So the maximum change in resistance depends upon the square of displacement and the signal will be at twice of the resonance frequency. To sense this magnitude, a voltage signal is applied over the resonator and the output current is measured as it has been shown on, equation [5.12], which is repeated here [5.20] for completeness. There are two contributions to the total current, but they are at different frequencies.

$$I \mp \Delta I = \frac{V_0}{R \pm \Delta R} \cong \frac{V_0}{R} \left(1 \mp \frac{\Delta R}{R} \right) \quad [5.20]$$

The equation [5.19] placed on equation [5.20] gives the current detected in function of two unknown parameters, the maximum displacement and the gauge factor. In order to obtain the amount of displacement and solve for the unknown gauge factor in piezoresistive measures, capacitive measures are done. Using the standard set-up depicted in Annex A on Figure 30 composed by a network analyzer and a DC source the transmission graph of the Figure 11 is obtained with biasing of $P_{AC}=10\text{dBm}$ and $V_{DC}=15\text{V}$.

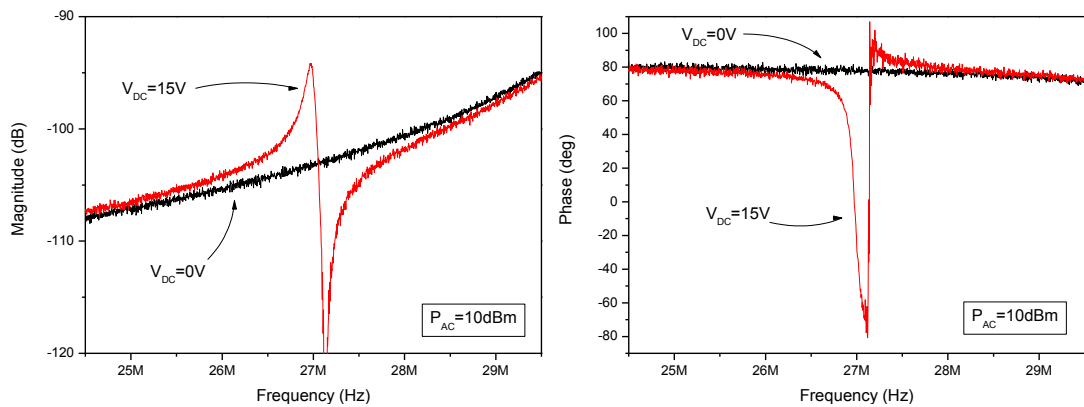


Figure 11.- Electrostatic excitation and capacitive sensing of a CCB in a probe table with $P_{AC}=10\text{dBm}$ and V_{DC} sweep from 0V to 15V .

After checking the correct behavior of the resonator the chip is attached to a PCB to allow measures in a vacuum chamber and bonded to SMA connectors. Repeating the same biasing conditions of $P_{AC}=10\text{dBm}$ and $V_{DC}=15\text{V}$ the graph of the Figure 12 is obtained. The measure shows a huge increase of the parasitic capacitance due to the PCB and bondings.

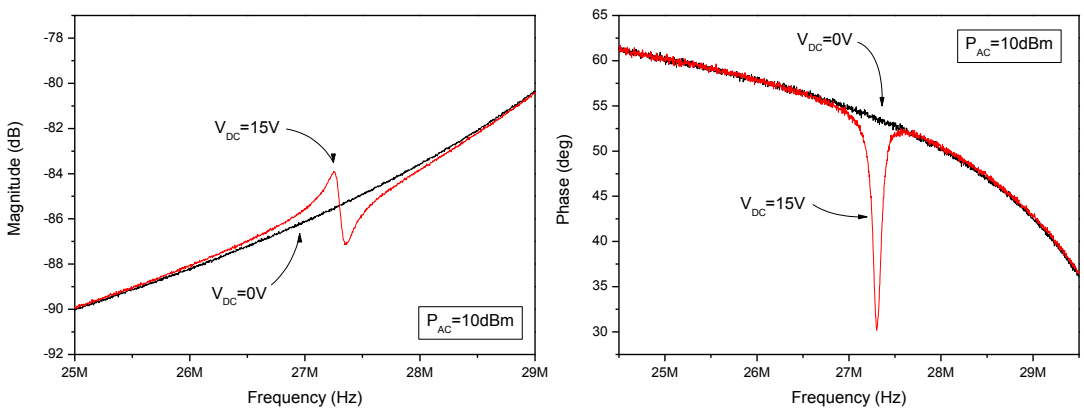


Figure 12.- Electrostatic excitation and capacitive sensing of a CCB bonded to a PCB with $P_{AC}=10\text{dBm}$ and V_{DC} sweep from 0V to 15V .

To extract the vibration amplitude peak the parasitic capacitance must be eliminated. Considering the electrical model described on chapter 4 at the resonance, the contributions of L and C cancels out each other so the real part of the current is exclusively formed by the contribution of the R whilst the imaginary part is due to the parasitic capacitance. So the magnitude of the real part of the current measured will provide the vibration amplitude. To convert the magnitude of the transmission to current the power delivered to the resonator has to be calculated. As the impedance seen by the excitation port of network analyzer is much higher than 50Ω (in the order of $M\Omega$ of motional resistance) the voltage delivered to the resonator will be two times higher than the voltage delivered by the source to 50Ω impedance for a fixed AC power. Taking the magnitude and phase of the current extracted from the Figure 12 at $V_{DC}=15V$ the real and imaginary part could be extracted as it is shown on the Figure 13.

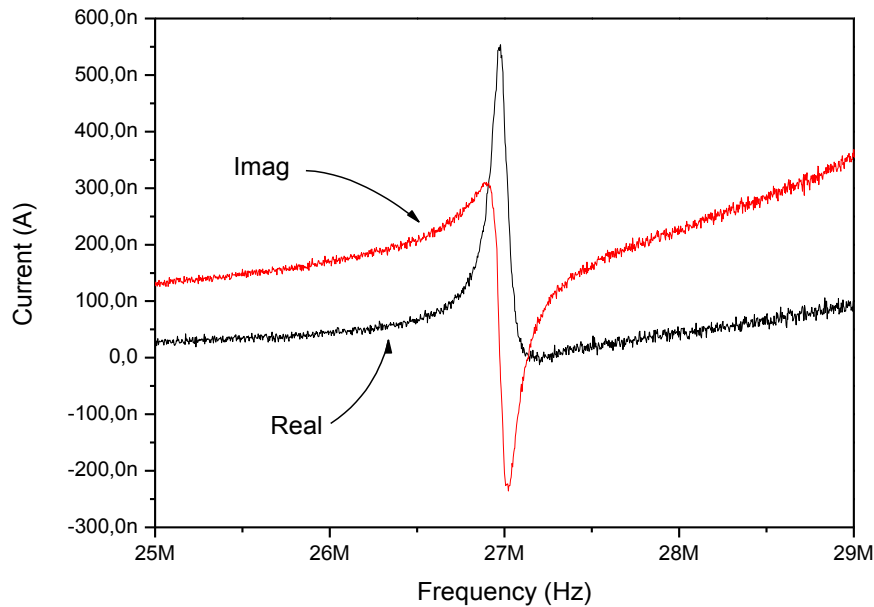


Figure 13.- Real and imaginary components of the output current from capacitive sensing of the CCB at $P_{AC}=10dBm$ and $V_{DC}=15V$.

Using the current from the real part at the resonance and the electromechanical coupling factor from equation [5.21] the vibration amplitude of 65nm is obtained.

$$x_r = \frac{|I|}{\eta \cdot \omega} = \frac{|I|g^2}{V_{DC}\epsilon \cdot l \cdot t \cdot \omega} \quad [5.21]$$

Once it is checked that the resonator works properly the down mixing sensing is used to obtain a capacitive current with low frequency. This experiment is done because a lock-in amplifier is used in the piezoresistive set-up and we want to know that the detection scheme is capable to sense signals, previously sensed by other configurations.

The lock-in amplifier is based on superheterodyne receiver where a known reference signal is multiplied by the input signal and amplified, so the scheme is capable to detect small signals even buried in noise. Employing current mixing sensing the set-up of the Annex A depicted on Figure 35 requires two signal sources and one DC source, the signals from the sources are separated in two branches by power splitters. One branch generates the reference signal through a discrete RF mixer. The other branch applies for one driver an AC signal at the resonance frequency of the MEMS whilst the other signal plus a DC added by a bias tee is applied directly to one side of the resonator. The resonator signal has a frequency composed by the resonance frequency plus an offset in the bandwidth of the lock-in amplifier. The output electrode is connected to the input of the lock-in. The remaining set-up parameters are: offset of 543.21Hz, a sweep of 1MHz, a DC of 15V and AC powers of 8dBm. The down mixing set-up provides the measure of the resonance peak current of the Figure 14 which confirms that the lock-in amplifier is capable to sense smaller currents obtained from the motion of a MEMS resonator. The down mixing current obtained is lower than the capacitive due to their square dependence with static capacitance.

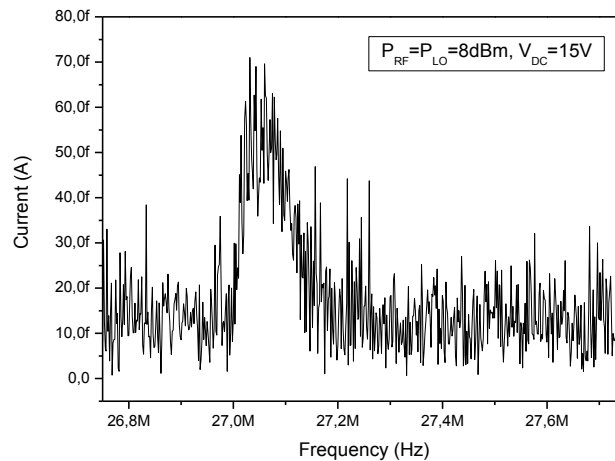


Figure 14.- Down mixing measure with lock-in amplifier for CCB resonator bonded to a PCB for $P_{RF}=8dBm$, $P_{LO}=8dBm$ and $V_{DC}=15V$.

The configuration for piezoresistive sensing of Figure 15 has some differences the one in Figure 14: a frequency doubler is added in the reference signal branch to emulate the square of the displacement, the DC is applied in the excitation electrode and the output current is sensed in the other side of the resonator. An additional consideration must be considered before taking measures. The density current flow through the resonator imposes a limitation to the maximum power applied over the resonator however the discrete mixer requires enough power to work properly, so a voltage controlled attenuator is placed between the power splitter and the resonator. With AC signal power of 10dBm the discrete mixer works properly and with attenuation of 17dB the resulting power applied to the resonator has a power of -10dBm. Maintaining a DC of 15V and frequency offset of 534.21Hz, the Figure 15 is obtained.

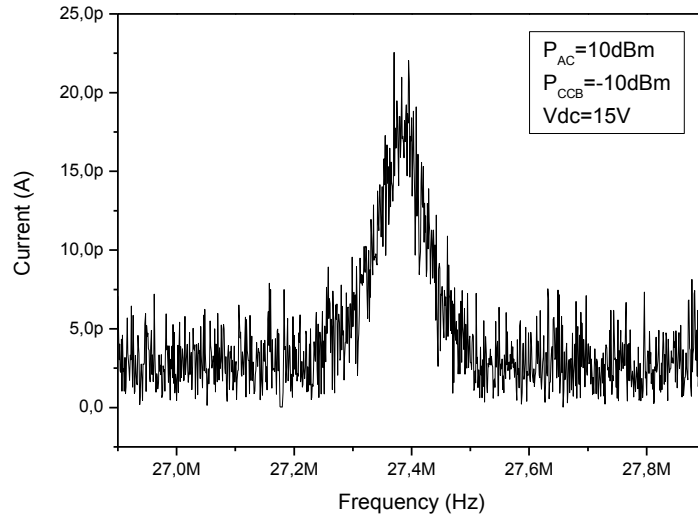


Figure 15.- Piezoresistive measure with lock-in amplifier for CCB resonator bonded to a PCB for $P_{AC}=10\text{dBm}$, $P_{CCB}=-10\text{dBm}$ and $V_{DC}=15\text{V}$.

In order to extract the gauge factor we consider that the vibration amplitude of the piezoresistive measure is the same than the capacitive measure because the same signals of $P_{AC}=10\text{dBm}$ and $V_{DC}=15\text{V}$ (neglecting the small contribution across the beam of -10dBm) are used for electrostatic excitation. The relation between motion and current is developed from the equation [5.22] assuming sinusoidal signals. The V_{CCB} corresponds to the RMS voltage applied over the resonator and R_0 is the total resistance path composed by the nominal resistance of the resonator of 396Ω and the input resistance of $2.5\text{k}\Omega$ of the lock-in amplifier in low noise mode.

$$\Delta I = \frac{V_0}{R} \frac{2.44GF}{4l^2} (u_{max})^2 \quad [5.22]$$

With peak current of 22pA , vibration amplitude of 65nm and considering that the loading impedance is large than 50Ω (the power of -10dBm corresponds to a $V_{RMS}=0.14\text{V}$) a gauge factor of $4 \cdot 10^{-3}$ is extracted. The gauge factor obtained is extremely low if we compare with the values obtained for the polysilicon however due to the large vibration amplitude it is possible to sense the piezoresistive current.

To compare the piezoresistive with the capacitive measure the relative values are obtained and the two graphs are placed together, Figure 16.

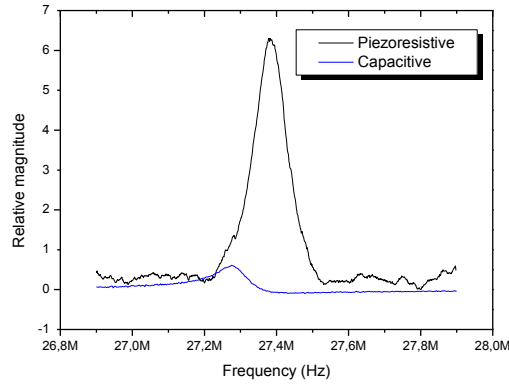


Figure 16.- Comparison between piezoresistive measure and capacitive measure without parasitics for $P=10\text{dBm}$ and $VDC=15V$.

In the above graph it is clearly shown that the piezoresistive sensing offers more peak signal with respect to the background signal than the capacitive. Also the capacitive measure is highly affected by the parasitics while the piezoresistive is unaffected by them.

???

The strain of the flexural modes on a same cross section area produce equal tensile and compressive strains on the opposite sides which represents a net zero strain and zero change in total resistance. Depositing a thin path of piezoresistive material in the device on a side parallel to the motion the compensation between compressive and tensile strains is broken and the motion could be sensed through piezoresistive current. The use of additional materials is not allowed in our CMOS-MEMS approach so the use of thin layers is not an option. In contrast of flexural, the bulk modes produce non vanishing longitudinal strains capable to be sensed through piezoresistive current flowing across the device. A simple bulk mode resonator is extracted from [Mat02] shown on the Figure 17.

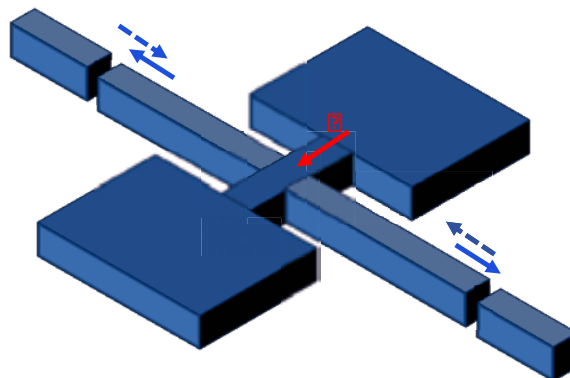


Figure 17.- Longitudinal bulk acoustic resonator structure.

However the current across the structure flows over a region where the strain is minimum and thus the change in resistance will be smaller. In order to improve the piezoresistive sensing the modification of the LBAR structure of the Figure 18 is adopted [VanB06] [VanB07]. The concept is the same as Figure 17, the bulk lateral mode is excited over the electrodes but in this LBAR the current flows over the whole structure and especially through the high strain regions where the change in resistance will be maxim.

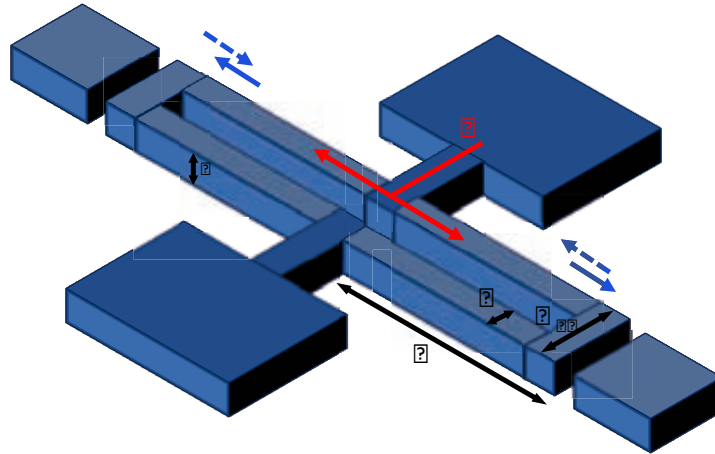


Figure 18.- Longitudinal bulk acoustic resonator for piezoresistive sensing.

The lateral length-extensional mode, where the two arms move in anti-phase is observed when the length of the resonator arm equals a quarter of the bulk acoustic wavelength (represented by the square of the Young's modulus divided by the material density), equation [5.23]. Their corresponding spring constant is obtained taking into account two parallel longitudinal single bar extensional spring constant (two springs in parallel), equation [5.24]. The effective mass for the LBAR is approximated to the effective mass of the two bars, depicted in equation [5.25].

$$L = \frac{\sqrt{E/\rho}}{4f} \quad [5.23]$$

$$k = \frac{2EA}{L} \quad [5.24]$$

$$m_{eff} = 2m \quad [5.25]$$

The design layout considerations take into account: minimum allowable width of $0.35\mu\text{m}$ for the first polysilicon layer, frequencies of operation of 250MHz and 433MHz and transduction gaps of 100nm and 150nm respectively. It is remarkable that the minimum width of $0.35\mu\text{m}$ will impose the maximum current fixed by the current density given by the CMOS technology. The LBAR devices were simulated with finite

elements software, Figure 19 and the final dimensions were adjusted to operate at the design frequencies. The Table 4 summarizes the design dimensions of the LBAR resonators.

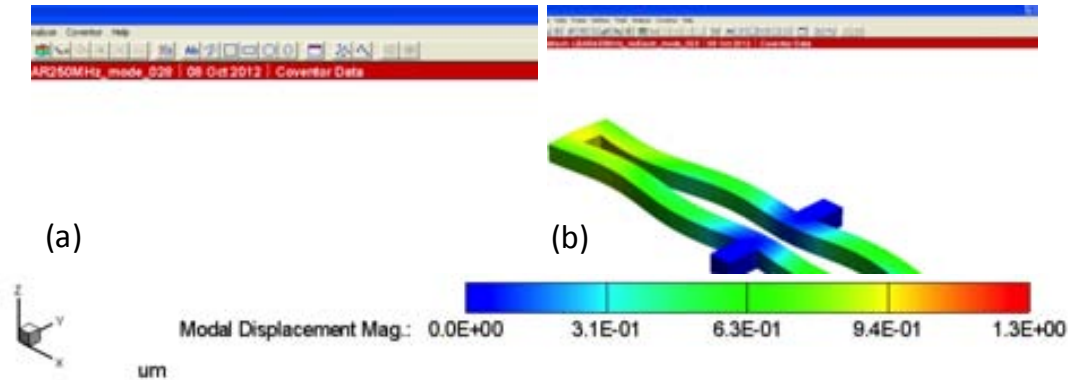


Figure 19.- Finite elements simulation of LBAR resonators: (a) 250MHz, (b) 433MHz.

l (μm)	w (μm)	w _{dr} (μm)	g (nm)	k _{eff} (kN/m)	m _{eff} (pg)	f ₀ (MHz)
4.78	0.35	1.15	100	8.15	1.09	433
8.28	0.35	1.15	150	4.71	1.91	250
4.78	0.35	1.15	150	8.15	1.09	433
8.28	0.35	1.15	100	4.71	1.91	250

Table 4.- LBAR resonators design parameters.

In order to compare the amount of piezoresistive current in front of capacitive current, the electrical models for each resonator and sensing method were used. The transconductance for LBAR resonator, [5.26], is computed solving the equation of motion of the spring-mass model, integrating the strain [5.10-1.11] and extracting it from [5.14].

$$g_m(\omega) = V_{DC} I_{d0} \frac{4\epsilon_0 GF}{\pi^2 E} \frac{w}{g^2 t} \frac{1}{1 - \left(\frac{\omega}{\omega_0}\right)^2 + j \frac{\omega}{Q\omega_0}} \quad [5.26]$$

At resonance the capacitive current is composed by the motional current and the parasitic current, equation [5.27], whilst the piezoresistive current comes from the maximum transconductance, equation [5.28], comes from the dependant current source of the Figure 10.

$$I_{cap} = \frac{V_{in}}{R_m} + V_{in} j\omega C \quad [5.27]$$

$$I_{pzt} = V_{in} g_{m_max} \quad [5.28]$$

$$\frac{I_{pzt}}{I_{cap}} = \frac{g_{m_max} R_m}{1 + j\omega C R_m} \quad [5.29]$$

Assuming a DC voltage $V_g=40V$, a current of $I_d=1mA$, a quality factor of 1000, a parasitic capacitance of 20aF and a gauge factor of 29 [Fre84], the modulus of the relation between currents gives a factor of 49, 44, 26 and 66 respectively. Despite of the current and quality factor considerations are optimistic the gain in current is still large enough in more conservative assumptions.

The physical characterization with SEM of the released LBAR after the wet etching, Figure 20, shows that the devices were correctly released but strongly residual stress of the polysilicon layer induces vertical deflection of the resonator ends. Moreover the width of the fabricated electrodes is reduced in comparison with the resonator which sizes in the layout were supposed to be equal, (c) Figure 20. This two effects produce a hugely reduction of the coupling between the electrodes and the resonator, making the excitation of the desired mode extremely challenging and the measure not suitable to be developed.

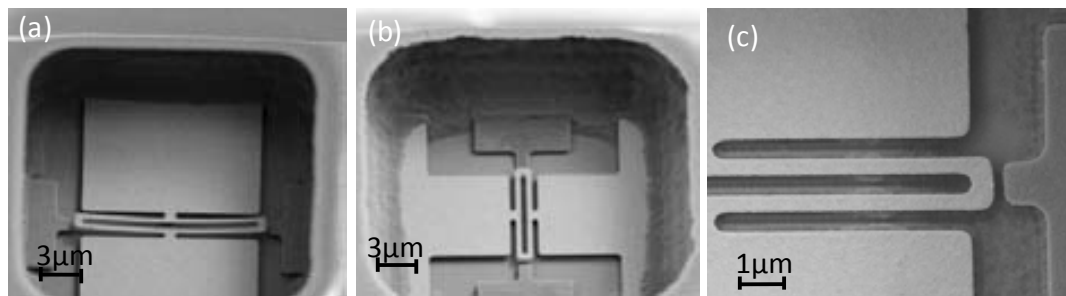


Figure 20.- SEM images of the LBAR resonators fabricated and released. The residual stress produces a vertical deflection and the final electrodes width is reduced. (a) 250MHz, (b) 433MHz and (c) detail of the width reduction of the electrodes.

5.7. DOGBONE RESONATOR

The characterization of LBAR leads to develop a more robust bulk mode structure. The so called dogbone resonator [VanB08] is an improvement of the LBAR resonator in terms of less deflection due to stress and higher electrostatic couplings maintaining the same resonance frequency than LBAR structure with smaller length. It is achieved reducing the length of the springs and concentrating a mass at the end, Figure 21.

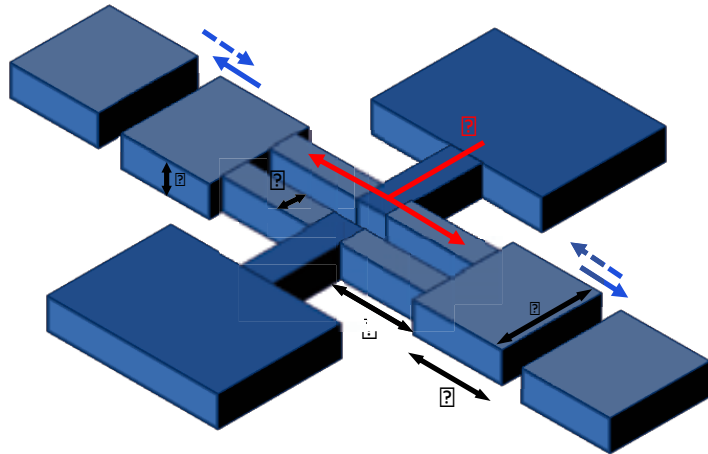


Figure 21.- Dogbone resonator for piezoresistive sensing.

The resonator can be mechanically modeled like a two parallel LBAR with a lumped mass at the end as it is shown on Figure 22. The effective elastic constant for the dogbone resonator can be approximated to effective spring constant of the LBAR, equation [5.30], because it will be considered that the lengthening will be concentrated in the springs. The effective mass takes into account the effective mass of the LBAR [5.31] and the mass of the end plate [5.32] being reflected by equation [5.33]. Note that both, the expansion of the anchors and the square plates are neglected.

$$k_{\text{eff}} = \frac{2k_{\text{LBAR}}}{2} \quad [5.30]$$

$$m_{\text{eff}} = \frac{2m_{\text{LBAR}}}{2} \quad [5.31]$$

$$m_{\text{end}} = m_{\text{plate}} \quad [5.32]$$

$$m_{\text{total}} = m_{\text{eff}} + m_{\text{end}} \quad [5.33]$$

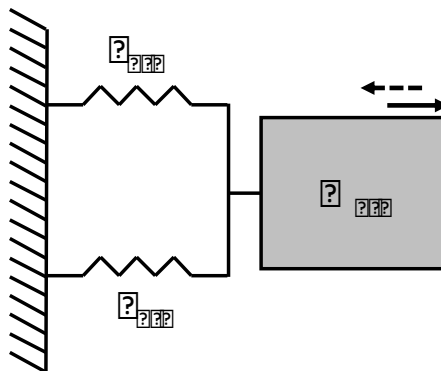


Figure 22.- Mechanical model for dogbone resonator.

5.7.1. FIRST APPROACH

The resonator is designed fixing the target frequencies of 250MHz and 433MHz, the material parameters, a spring width equal to the minimum allowed on the technology, and a mass width big enough to assure the capacitive coupling for electrostatic actuation. Holes on the edge masses were added two of the four resonators in order to facilitate the releasing of the resonator during wet etching. The dogbone resonators without holes were simulated with finite elements software and the dimensions were adjusted to the desired frequencies. The Figure 23 shows the modal displacement of the resonators where it can be seen that the displacement in anchors is negligible so the energy losses through the anchors will be minimum increasing the quality factor of the resonators. Table 5 shows the final layout parameters for the different dogbone resonators designed.

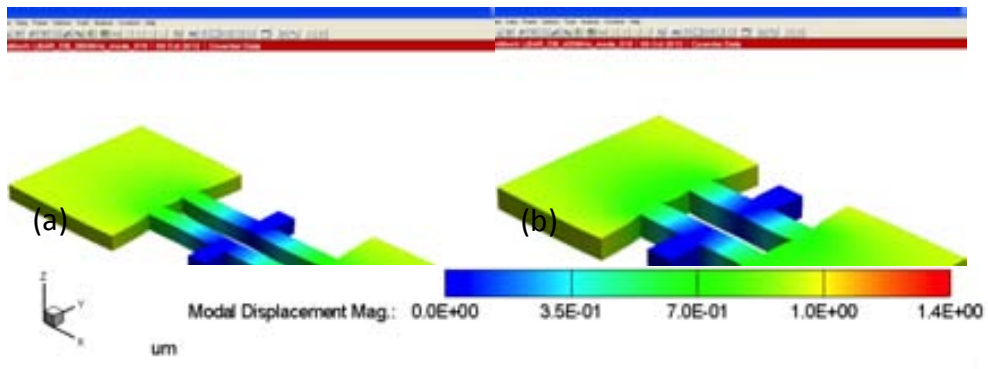


Figure 23.- Finite elements simulation of dogbone resonators without holes: (a) 250MHz, (b) 433MHz.

l (μm)	w (μm)	a (μm)	b (μm)	g (nm)	k_{eff} (kN/m)	m_{eff} (pg)	f₀ (MHz)
2	0.35	2.50	3.00	40	47.5	6.35	250
1	0.35	1.70	2.50	40	21.4	10.3	433
2	0.35	2.50	3.00	100	21.4	10.3	250
1	0.35	1.70	2.50	100	47.5	6.35	433

Table 5.- Dogbone resonators design parameters.

In the layout the top vias are designed with the same shape of the resonator in order to reduce the amount of silicon dioxide above the resonator. Metal paths and vias are placed near the end of anchors and electrodes to prevent their fall down in overetching cases, Figure 24 (a). The Figure 24 (b) shows the final layout with all the improvements made.

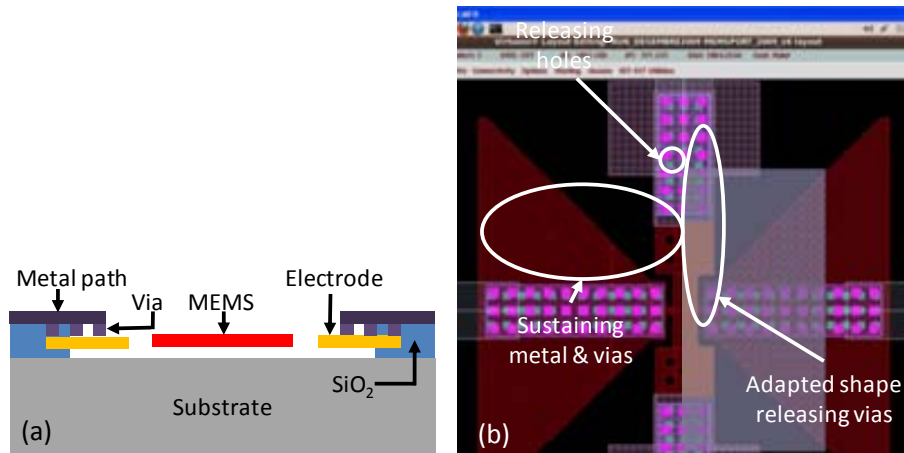


Figure 24.- (a) Cross section of the dogbone resonator with the via/metal sustaining enhancement; (b) Layout example of dogbone resonator from showing all the layers (vias and PAD layers are hidden in the left middle of the image).

The physical characterization of the devices with SEM imaging, Figure 25, shows that the addition of metal paths with vias to sustain the anchors/electrodes and the adaptation of the releasing vias to the shape of the resonator has confined the wet etching on top of the resonator and enhanced it around them. The devices has been irreversibly damaged and shorter wet etching times will not release the MEMS devices making the electrical measures unaffordable.

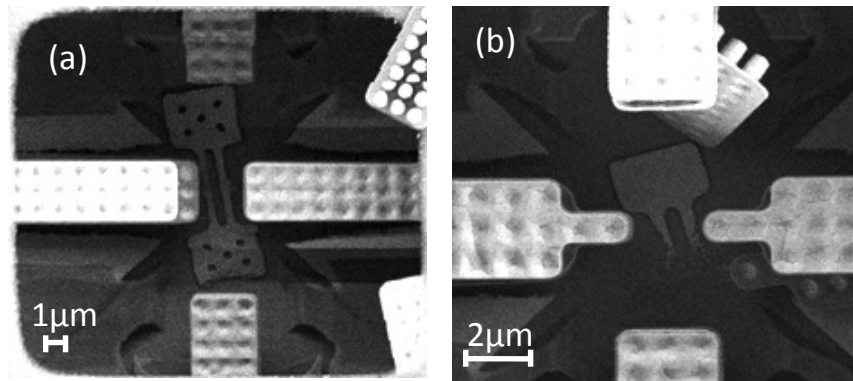


Figure 25.- SEM images of two dogbone resonators of 250MHz with holes (a) and 433MHz without holes (b) fabricated and released. The placement of vias with the shape of the resonator and metal paths to sustain the structural layer has been enhanced the etching damaging and destroying the structures.

5.7.2. SECOND APPROACH

The dogbone resonators were redesigned making the layout easier and decreasing the resonance frequencies of the dogbone structures in three different layouts in order to decrease the amount of parasitic current (through their frequency scaling) and to increase the coupling with electrodes. The design is made through the equations

[5.24] and [5.30], fixing the frequency and the width of the springs. The minimum width chosen is $0.5\mu\text{m}$ instead of $0.35\mu\text{m}$ to relax the limit of current fixed by the current density allowed in the polysilicon layer. There are three main modifications regarding the previous dogbone layout: the shape of the releasing vias is made rectangular and bigger than the opening PAD, the metal sustaining paths are avoided (the metal paths and contacts are limited to the end of anchors or electrodes which will be surrounded by silicon dioxide after wet etching) and the electrodes have been increased their width to prevent the damage of the whole driver in case of overetching of the edges of electrodes. The Figure 26 shows an example layout of one of the dogbone's designed.

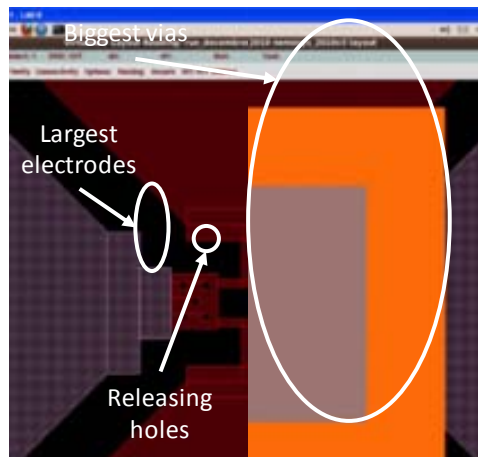


Figure 26.- Layout example of dogbone resonator from RUN Dicembre 2010 showing all the layers (vias and PAD layers are hidden in the left middle of the image).

After the first dimensioning using the mass-spring equations [5.24] and [5.30] finite elements software it is used to simulate the modal behavior and adjust the dimensions. In the Figure 27 it is shown a simulation of the symmetric bulk mode of the dogbone resonators. In the Table 6 there are detailed the final layout parameters obtained after simulation for the different dogbone resonators.

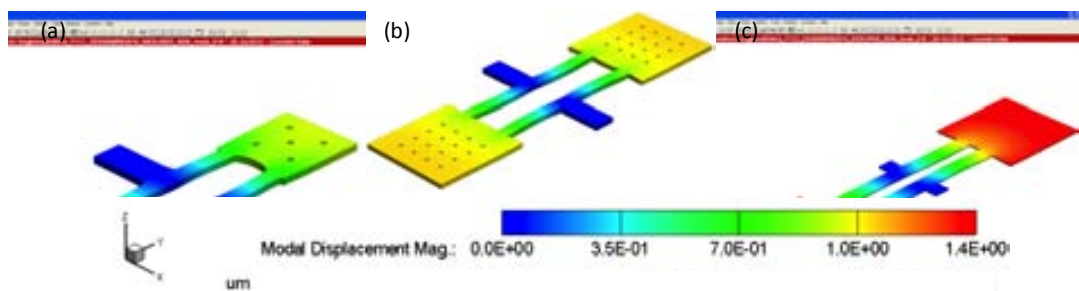


Figure 27.- Bulk mode mechanical simulation of redesigned dogbone resonators: (a) 250MHz, (b) 100MHz, (c) 50MHz.

l (μm)	w (μm)	a (μm)	b (μm)	g (nm)	k _{eff} (kN/m)	m _{eff} (pg)	f ₀ (MHz)
1.50	0.50	3.00	3.50	40	37.1	14.3	250
4.50	0.50	5.00	5.00	100	12.4	34.3	100
12.0	2.00	12.5	12.5	100	18.6	221	50

Table 6.- Dogbone resonators design parameters.

5.7.3. ELECTRICAL MODELLING

From the designed resonators is desirable to compute the electrical behavior of piezoresistive sensing using the model depicted on section 5.4. Assuming the harmonic oscillator response of the dogbone resonator allow to obtain the modal displacement $u(x,t)$ when an electrostatic force is applied, equation [5.34] and [5.35].

$$u(x, t) = u_0(\omega)e^{j\omega t} \sin\left(\frac{\pi x}{2L}\right) \quad [5.34]$$

$$u_0(\omega) = \frac{V_{ac}V_{DC}4\epsilon_0bL}{\pi^2g^2EW} \frac{1}{\left(1 - \frac{\omega^2}{\omega_0^2} + j\frac{\omega}{Q\omega_0}\right)} \quad [5.35]$$

From the displacement the strain and the change in resistance are computed through the equations of the sections 5.2 and 5.3 and the electrical model of the Figure 10 is obtained where the transconductance for the dogbone resonator follows the equation [5.36] and [5.37].

$$g_m = \frac{g_{m0}e^{j\omega t}}{\left(1 - \left(\frac{\omega}{\omega_0}\right)^2 + j\frac{\omega}{Q\omega_0}\right)} \quad [5.36]$$

$$g_{m0} = -I_dV_{DC} \frac{4\epsilon_0bGF}{\pi^2g^2EW} \quad [5.37]$$

In order to establish the biasing conditions for a certain gauge factor range a study on the piezoresistive current detected is done. There are three main limitations in the measure of piezoresistive current: the current density of the first polysilicon layer (0.5mA/μm), the dynamic range of the network analyzer and the maximum continuous voltage applicable over the gap. Taking into account that the minimum allowable width for the polysilicon layer is 350nm the maximum current through it must be of 0.175mA. The dynamic range of network analyzer Agilent E5071B is 123dB in the band of 3MHz to 1.5GHz for a IF bandwidth of 10Hz (minimum IF available) and the maximum power delivered to the output is 18dBm. The maximum DC voltage considered over a gap of 100 nm is 20V. There are three biasing parameters: the continuous current across the device, the continuous voltage and the AC power on the electrodes. Using the transconductance expression of the [5.34] and assuming a gauge factor of 20, a quality factor of 100 and sweeping the biasing conditions the Figure 28 were obtained where

the -123dB line represents the minimum detectable signal by the network analyzer. Fixing the DC voltage to the maximum of 20V and the current to 0.131mA, the AC power sweep gives 3dBm of minimum power required to measure the signal, Figure 28 (a). If the AC power is fixed to the maximum of 18dBm, the current is fixed to 0.151mA and the DC voltage is swept, the minimum DC voltage to measure a signal corresponds to 4V, Figure 28 (b).

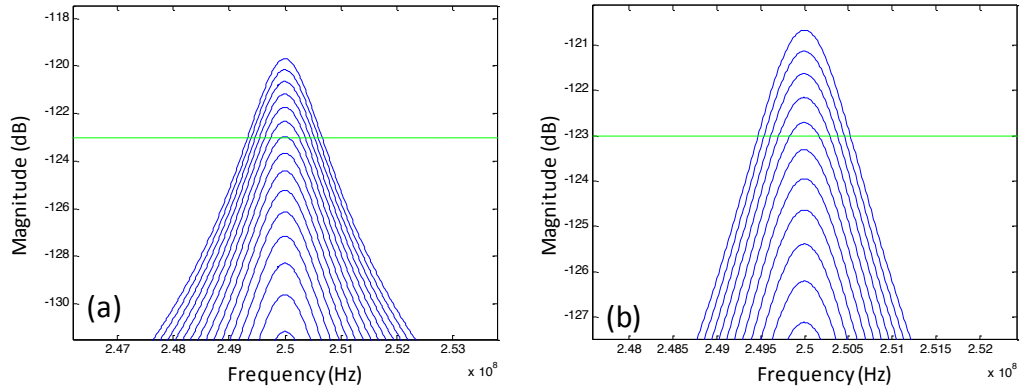


Figure 28.- Piezoresistive current simulations to determine the minimum biasing conditions: (a) $V_{dc}=20V$, $I_d=0.131mA$, (b) $V_{AC}=18dBm$, $I_d=0.151mA$.

The gauge factor is an unknown parameter for our polysilicon layer and depends on several factors such as the deposition method employed or the amount of doping impurities implanted. Despite of these parameters are foundry confidential some studies on different kind of polysilicon layers [Hul99] have shown that their gauge factor comprises a range between -30 to 40 as it is shown on Table 2. Using the expression of the transconductance for a sweep of gauge factor is made with the aim to establish their minimum value in function of biasing conditions. The gauge factor is swept from 0 to 40 in all the simulations of the Figure 29. The first case of the Figure 29 (a) represents the minimum biasing conditions found on the simulations of Figure 28 with $V_{dc}=4V$, $V_{AC}=3dBm$ and $I_d=0.131mA$ where it can be seen that the value of piezoresistive current is not enough even with the maximum gauge factor of 40 considered. In the Figure 29 (b) graph the AC power and the current are driven to its maximum of 18dBm and 0.175mA respectively, for a $V_{dc}=2V$ the minimum gauge factor capable to be sensed is of 34. In the Figure 29 (c) the DC voltage and the current are set to its maximum of 20V and 0.175mA respectively and a minimum gauge factor of 38 is detected with AC power of -3dBm. Finally, in the Figure 29 (d) the DC voltage and AC power are established to their maximum and a current of 0.015mA allows a measure of piezoresistive signal with a minimum gauge factor of 39.

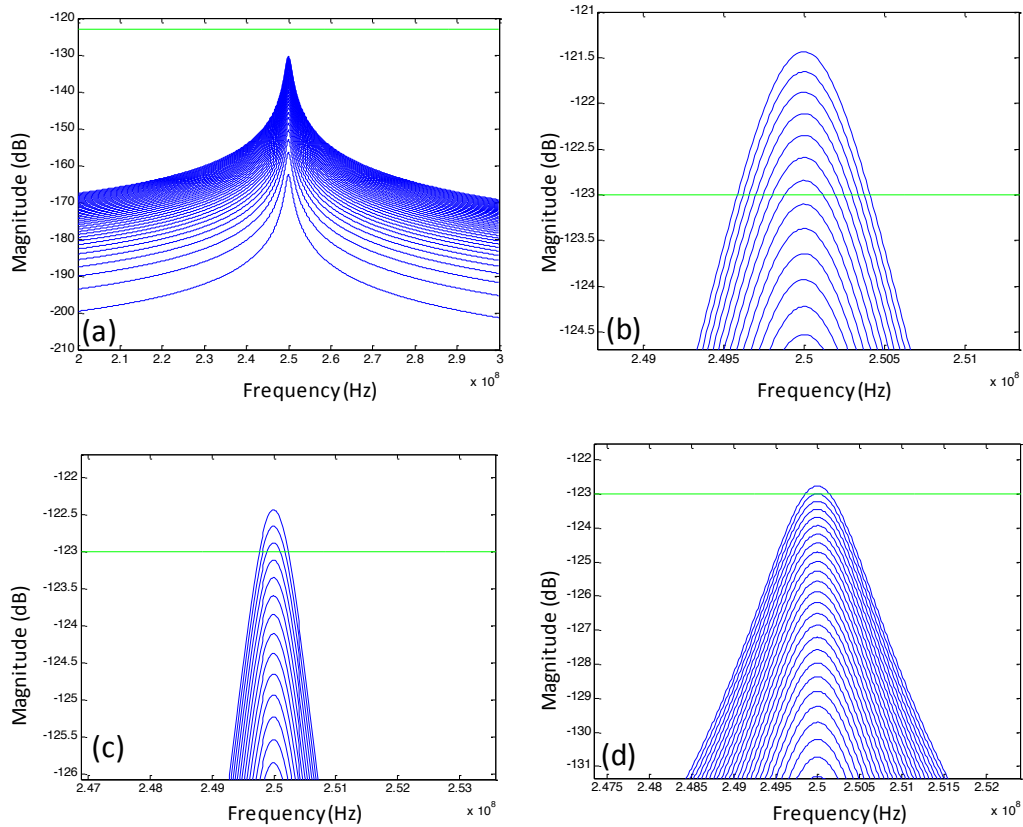


Figure 29.- Piezoresistive current simulations sweeping the gauge factor under different biasing conditions. (a) $V_{dc}=4V$, $V_{AC}=3dBm$, $I_d=0.131mA$, (b) $V_{dc}=2V$, $V_{AC}=18dBm$, $I_d=0.175mA$, (c) $V_{dc}=20V$, $V_{AC}=-3dBm$, $I_d=0.175mA$, (d) $V_{dc}=20V$, $V_{AC}=18dBm$, $I_d=0.015mA$.

The dogbone resonators are designed to be sensed piezoresistively but could be also sensed capacitively to compare both sensing methods. Assuming the capacitive model, the motional resistance gives the amount of motional current at the resonance since the motional inductance cancels the contribution of motional capacitance. Then the estimated current ratio between the theoretical piezoresistive and capacitive current at resonance will be equal to the equation [5.38].

$$\frac{I_{pZR}}{I_{cap}} = g_{m,max} \cdot R_m \quad [5.38]$$

Fixing the biasing conditions to $V_g=20V$, $I_d=0.1mA$ and assuming a quality factor of $Q=1000$ (expected value in vacuum), a gauge factor of $K=20.9$ is required to obtain 5 times more piezoresistive current than capacitive current. This gauge factor is on the range of the values obtained experimentally for the polysilicon.

5.7.4. ELECTRICAL MEASURES

The new dogbone resonators were fabricated and released by means of wet etching post CMOS process. The Figure 30 shows the three different resonators included in the RUN where the smallest device is correctly released whilst the other two still have silicon dioxide below them. A long wet etching process trying to release them, produce over etching of the electrodes destroying it.

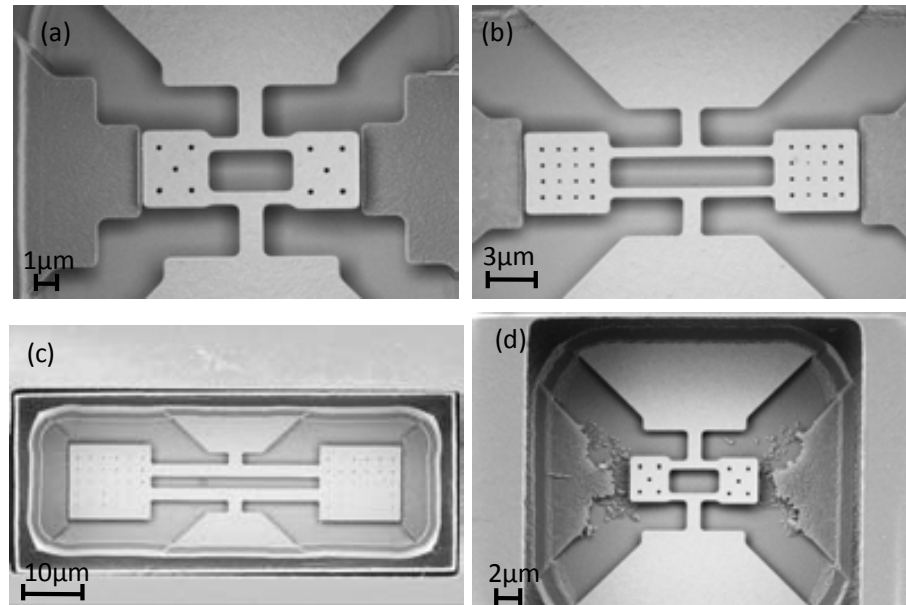


Figure 30.- SEM images of the 250MHz (a), 100MHz (b) and 50MHz (c) dogbone resonators after releasing process. The smallest device (a) is correctly released in contrast to the other two structures (b,c) which are bigger and require longer etching times. On (d) an overetched 250MHz resonator is shown where the electrodes have been irreversibly damaged.

After being correctly released the resonators are electrically tested. First of all capacitive sensing set-up is adopted, Figure 30 of Annex A, since it is a method which has been extensively tested in CMOS polysilicon resonators and will help to establish if the resonators are correctly released. The electrostatic actuation consists on applying symmetrically AC plus DC signal through the two electrodes which are combined using a Bias-Tee device. The motional current is sensed in one of the ends of the dogbone with the network analyzer E5071B previously calibrated in the measuring bandwidth. The Figure 31 shows measures of the same resonator with $P_{AC}=10\text{dBm}$ sweeping the DC voltage from 0V to 20V. The resonance peak and antiresonance valley are clearly observable despite of the extremely low level of motional current. Increasing the DC voltage the spring softening behavior produce a shift in resonance frequency as it is expected. The resonance frequency around 231MHz is lower than the design frequency of 256MHz. This effect could be explained by two reasons: the fabricated dimensions of the device are slightly different than the design dimensions because there are some design rules avoided resulting in some differences between layout and real device, the

other reason is that the anchors are not as perfect as they should be so etching below them produce a change in resonator shape shifting the frequency.

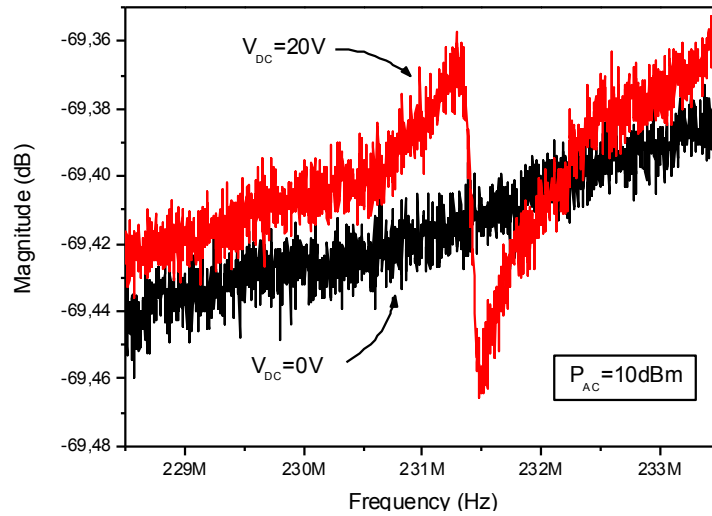


Figure 31.- Magnitude of the electrical response of 250MHz dogbone resonator obtained with network analyzer applying $P_{AC}=10dBm$ and V_{DC} sweep from 0V to 20V.

The next step consist on detect the motion through piezoresistive effect instead of capacitance variation. The excitation is also electrostatic through the electrodes with AC plus DC signals. The piezoresistive effect requires a current path and a fixed DC current where the piezoresistive variation will be added. The set-up shown on Figure 34 of Annex A has two DC sources and a network analyzer, a discrete resistor is added in the current path in order to limit the amount of current through the resonator and prevent an occasionally current peak which exceeds the current density of first polysilicon layer. The resonators are tested with this set-up with the biasing conditions established without obtaining piezoresistive measure. Then the DC voltage is increased and an abrupt change is observed. The devices were taken to SEM microscope, Figure 32, where it can be seen that the drivers have been severely damaged.

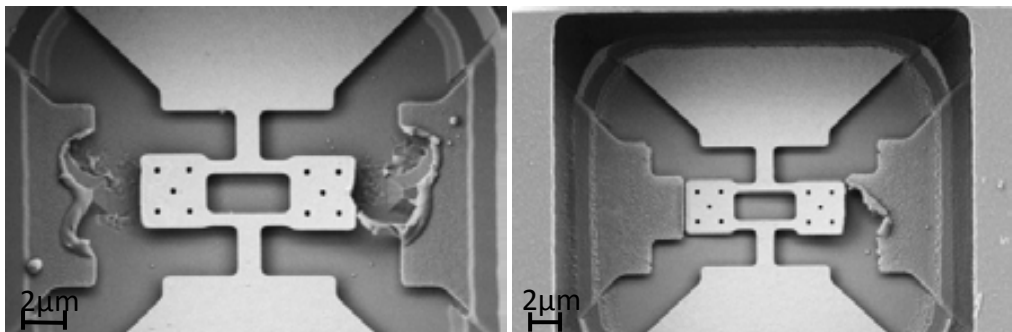


Figure 32.- Destroyed electrodes after after excessive DC voltage in piezoresistive sensing measures.

5.8. BROKEN SYMMETRY DEVICES

The main problem in piezoresistive detection on single layer flexural devices is the compensation of compressive with tensile strain making the detection extremely difficult with other piezoresistive mechanisms such as nonvanishing longitudinal strain. This compensation is intrinsic of symmetric structures so if the symmetry is broken in the current path, these contributions to the strain should be measurable.

The first broken symmetry structure is a CCB with a non symmetric slot of $1.5\mu\text{m}$ of length at one end, Figure 33. The total width of $2\mu\text{m}$ is higher enough to respect the design rules of minimum width (350nm) and minimum separation (450nm) for first polysilicon layer. Fixing the frequency to 25MHz and using the spring-mass model a length of $26\mu\text{m}$ is required. A series of holes are added along the beam to allow the wet etching to penetrate through them.

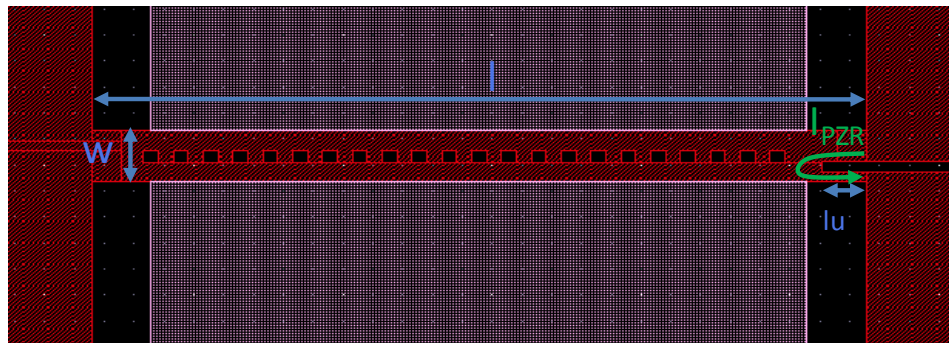


Figure 33.- Layout of asymmetric CCB included.

Finite elements simulation of the modal shape and stress is done for the first in-plane flexural mode. The resonance of the mode is around 25MHz and the stress result is shown on (a) Figure 34 where as it was expected the amount of stress at the wider edge is higher than the amount of stress at the thinner. The simulations have been made considering an electrostatic excitation of $P_{AC}=18\text{dBm}$, $V_{DC}=20\text{V}$ which gives a displacement of 28nm at the resonance frequency. The typical post CMOS wet etching process of 28 minutes is applied and the (b) image of the Figure 34 is obtained where the device is apparently correctly released.

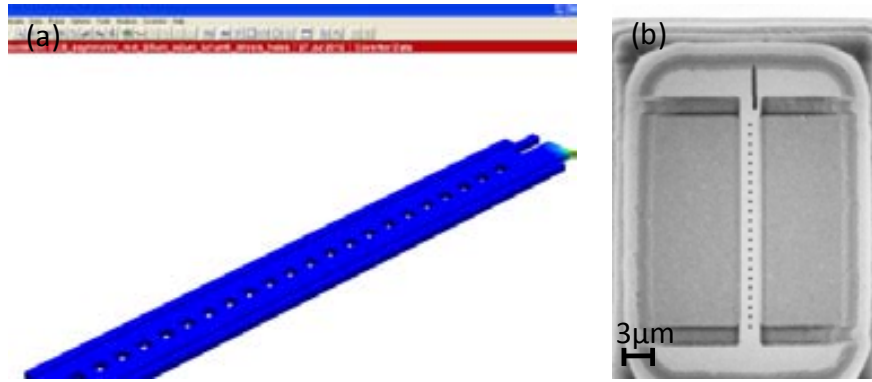


Figure 34.- (a) Stress finite elements simulation of asymmetric CCB in response to an excitation of $P_{AC}=18dBm$ and $V_{DC}=20V$; (b) SEM image of asymmetric CCB after post CMOS wet etching.

The asymmetric CCB is designed to be sensed both capacitively and piezoresistively so the next step consist on proceed with the electrical measures. The standard two electrodes capacitive sensing configuration is adopted and the measures obtained for a fixed AC power of 0dBm and a sweep of V_{DC} from 0V to 6V is shown on Figure 35. From the measures it is noteworthy that the resonance frequency is slightly higher than the one given by the simulator, probably the resonator is not completely released changing their effective length and so on their resonance frequency. The extracted quality factor is of 210 and it is also remarkable that from $V_{DC}=6V$ the resonator has a nonlinear response setting the limit of excitation.

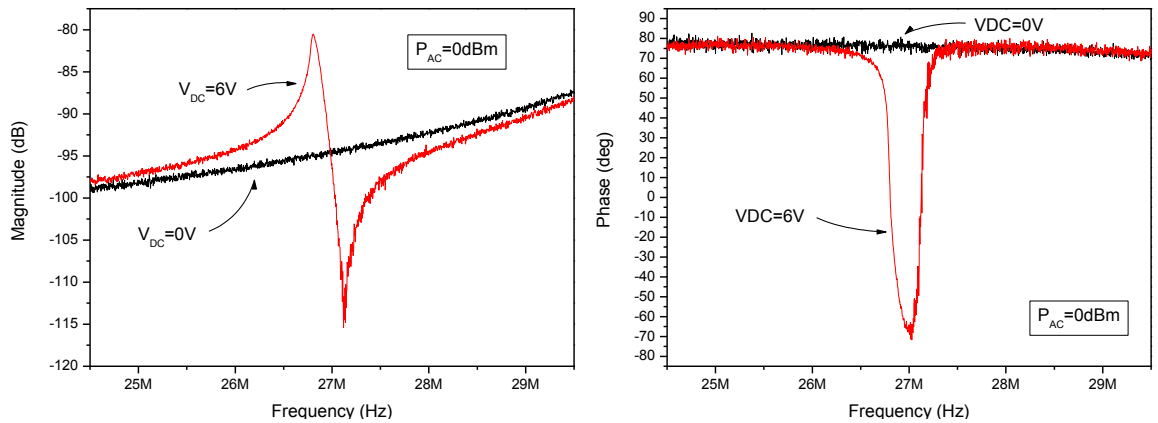


Figure 35.- Magnitude and phase of the asymmetric CCB released with $P_{AC}=0dBm$ and V_{DC} sweep from 0 to 20V.

Then the piezoresistive set-up is adopted. The resistance of the current path is 83Ω and the maximum current allowed by the limit of the polysilicon current density is $175\mu A$. So the maximum applicable VDC to enable flowing current is 23mV. There are no results obtained from piezoresistive sensing and the reason could be that there is remaining silicon dioxide under the slot which destroys the piezoresistive sensing

capability. To check that a FIB cut cross section is made on a device. Really near the two anchors there are remaining silicon dioxide which acts as anchors changing the effective length of the resonator and inhibits the stress produced by motion on the current path.

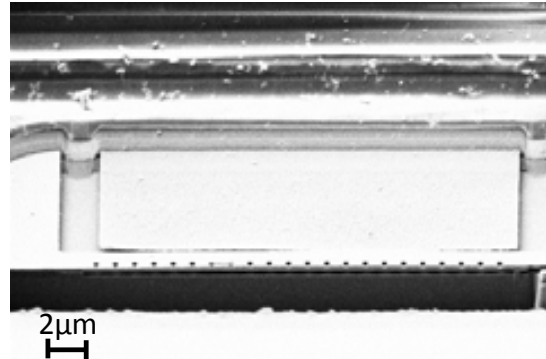


Figure 36.- SEM image from FIB cross section of asymmetric CCB after 28 minutes of wet etching.

Continuing with the broken symmetry concept a flexural/bulk cantilever has been developed, Figure 37. The total length is $12.5\mu\text{m}$, the length of the slot is $3.75\mu\text{m}$ and the total width is $3\mu\text{m}$. The two remaining widths of the beams defined by the slots are $1\mu\text{m}$ and $1.5\mu\text{m}$ respectively. As same as the layout of asymmetric CCB in the cantilever several holes are placed to decrease the difficulty of the releasing process. It is remarkable that there are three different electrodes to allow electrostatic excitation of flexural and bulk modes and capacitive reading of the flexural mode.

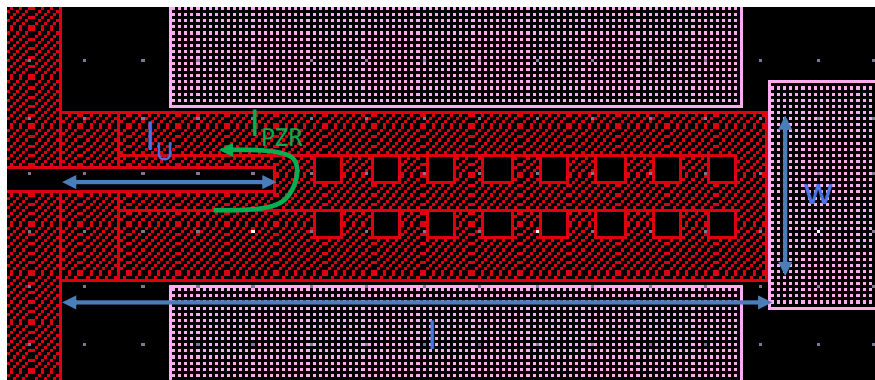


Figure 37.- Layout of thin asymmetric cantilever.

Some simulations with finite elements software were made to check the flexural/bulk modes and their corresponding stress in the current path. Equal biasing conditions than asymmetric CCB were applied (taking into account that the excitation electrode are different for flexural and bulk modes), $P_{AC}=18\text{dBm}$, $V_{DC}=20\text{V}$ which gives a displacement of 53nm at 24.85MHz for flexural mode and a displacement of

1.6nm at 163.52MHz for the bulk mode. The stress results for each mode are shown on Figure 38 where as it is expected the amount of stress in the structure is lower but much more homogenous for the bulk mode than the bulk mode where the stress is localized on the anchors but with higher value.

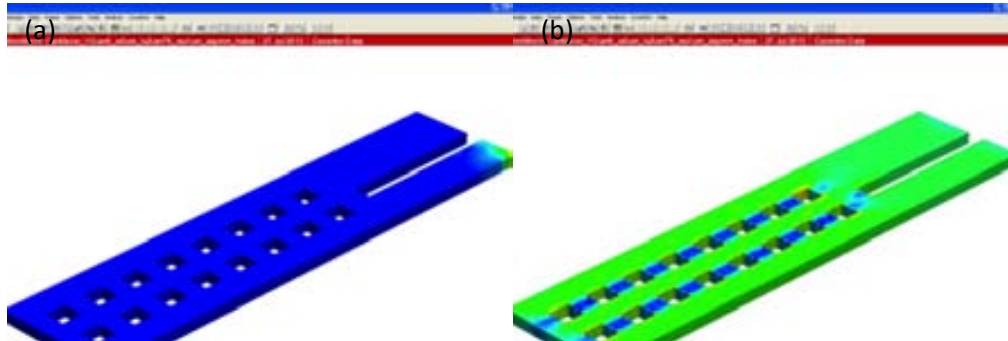


Figure 38.- Stress simulations for asymmetric cantilever structure: (a) flexural mode where a displacement over a lateral side of structure is applied; (b) bulk mode when a displacement over the top end side is applied.

The post CMOS releasing process is done and physical characterization through SEM imaging is made. The top view image of the Figure 39 shows that apparently the resonator is released but a lateral view shows that the residual stress of the polysilicon layer upward curve the resonator reducing the coupling with electrodes making the electrical measure unaffordable.

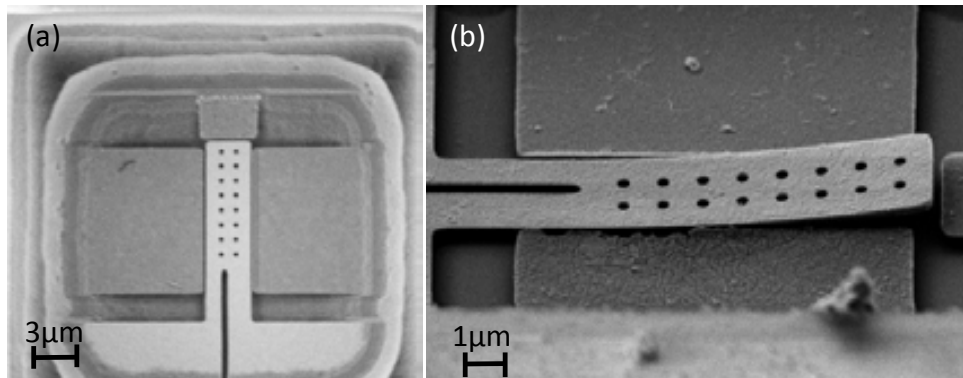


Figure 39.- SEM images of thin asymmetric cantilever: (a) top view after wet etching; (b) lateral view of same resonator of other chip after wet etching.

The previous flexural/bulk cantilever has a slot defined by two beams slightly different so another resonator with the same length of 12.5µm but a width of 6µm to allow bigger stress differences has been developed, Figure 40. The length of the slot is 4.75µm and the width of each beam is 1µm and 4.55µm respectively. This structure provides higher differences between the stresses on each beam of the slot but will be more challenging to release it.

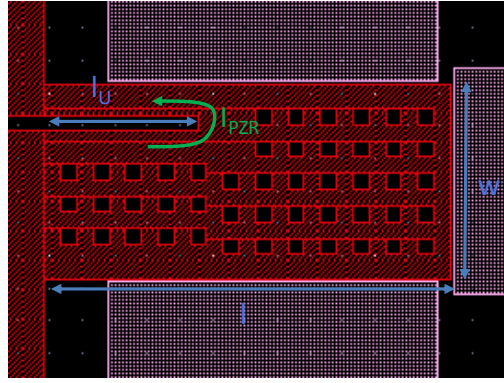


Figure 40.- Layout of wide asymmetric cantilever.

In this case simulations with finite elements software were also made. The same excitation signals of $P_{AC}=18\text{dBm}$ and $V_{DC}=20\text{V}$ are applied, giving a displacement of 10nm at 39.72MHz for flexural mode and a displacement of 0.9nm at 156.09MHz for the bulk mode. Comparing these simulations of Figure 41 with the previous thinner asymmetric cantilever Figure 38 there are a similar stress behavior in function of each mode. However the amount of stress is lower due to their higher stiffness, Table 6, due to higher width.

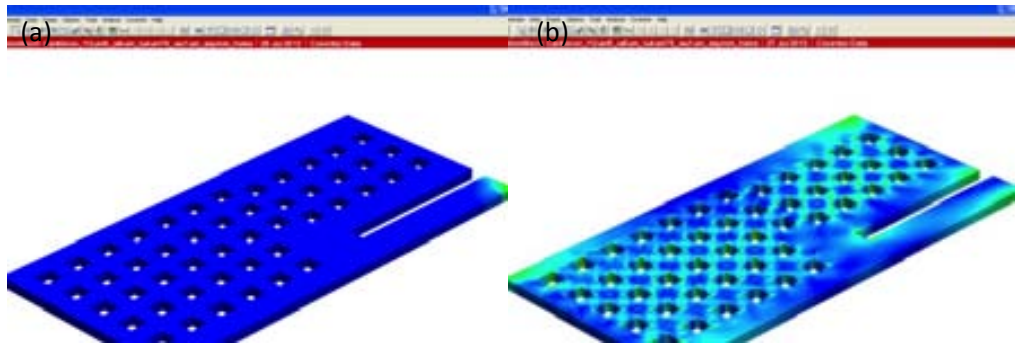


Figure 41.- Stress simulations for wide asymmetric cantilever structure: (a) flexural mode; (b) bulk mode.

After releasing the images of Figure 42 were obtained. The overetching has destroyed the electrodes and the resonator has collapsed on the substrate. In addition a FIB cut section on the right of Figure 42 was made showing that some remaining silicon dioxide is still present. The correct releasing of this resonator is extremely difficult as the mass of the device is higher enough to collapse it whilst the device is not still released and the drivers suffer from overetching.

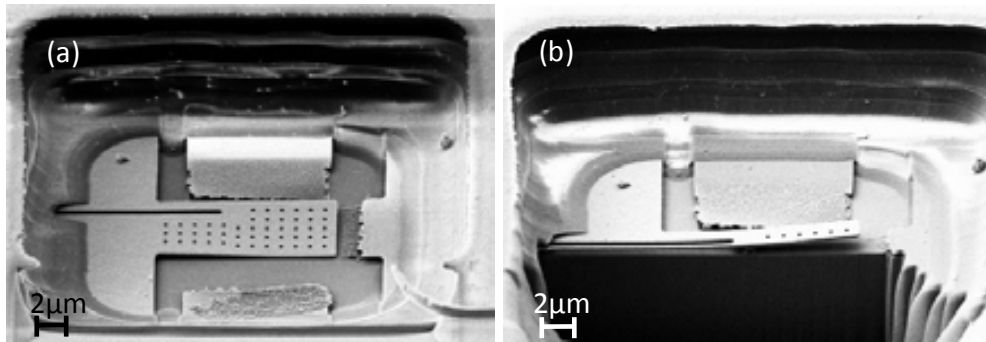


Figure 42.- SEM images of asymmetric cantilever: (a) lateral view after post CMOS wet etching where over etching has destroyed the electrodes; (b) lateral section view of the same resonator after FIB cut showing some remaining silicon dioxide beneath them.

The other topology implemented to detect piezoresistively the strain in flexural modes is the CCB-T of the left Figure 43. The length of the main beam is $11\mu\text{m}$, the length of the T beam is $2.35\mu\text{m}$ and the width of the beams is the minimum of polysilicon of 350nm . The sensing current will flow through the T beam, perpendicular to the motion in the first flexural mode and not dependant over the perpendicular tensile or compressive stress as it is shown on the simulation of the right Figure 43. The stress simulation is obtained applying a displacement of 200nm to one lateral side of the main beam. The displacement is produced for electrostatic excitation with biasing around $P_{AC}=18\text{dBm}$ and $V_{DC}=20\text{V}$.

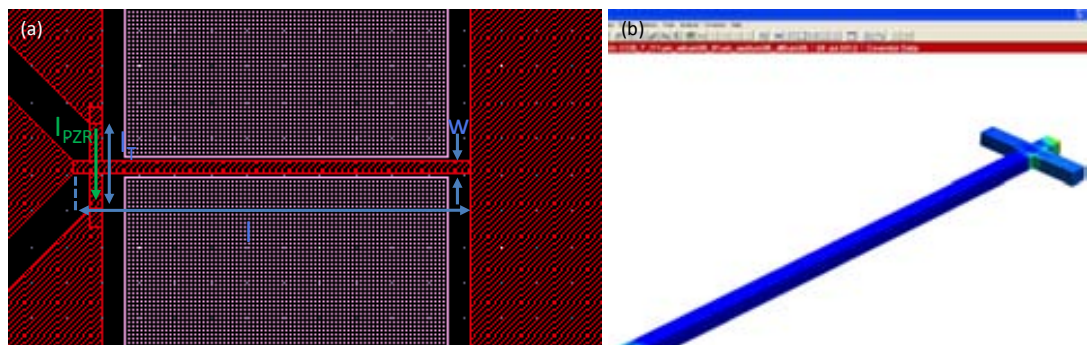


Figure 43.- (a) Layout of a T CCB resonator; (b) stress FEM simulation of CCB-T.

The devices were post processed 28 minutes with BHF wet etching and the images of Figure 44 were obtained. The two devices have the main beam correctly released however the right image shows an overetching under the electrodes which have collapsed with the substrate.

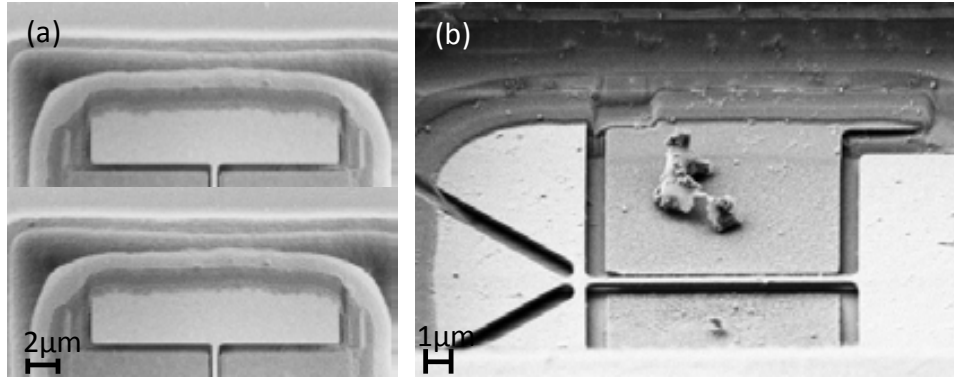


Figure 44.- SEM images of the CCB-T resonator showing top (a) and lateral (b) view images of two released devices. On the (b) image there is overetching which has produced a fall down of the electrodes.

The device is capable to be excited through electrostatic excitation and to be sensed through capacitive and piezoresistive methods. The measures shown on Figure 45 corresponds to capacitive sensing with $P_{AC}=0\text{dBm}$ and a sweep on DC voltage from 0V to 12V where the resonance with spring softening behavior is clearly observable. There are more parasitic current which masks the motional current than the asymmetric CCB due to the small width which increase the direct parasitic capacitance. The device resonates around 35MHz (the extracted quality factor from the slope of the phase is 87) a frequency higher than the 28MHz given by the simulator. This change in resonance frequency is also produced by a change in effective length due to remaining silicon dioxide near the ends of the main beam. Since the device is not still completely released the motion will not induce stress on the small T beam capable to be piezoresistively sensed.

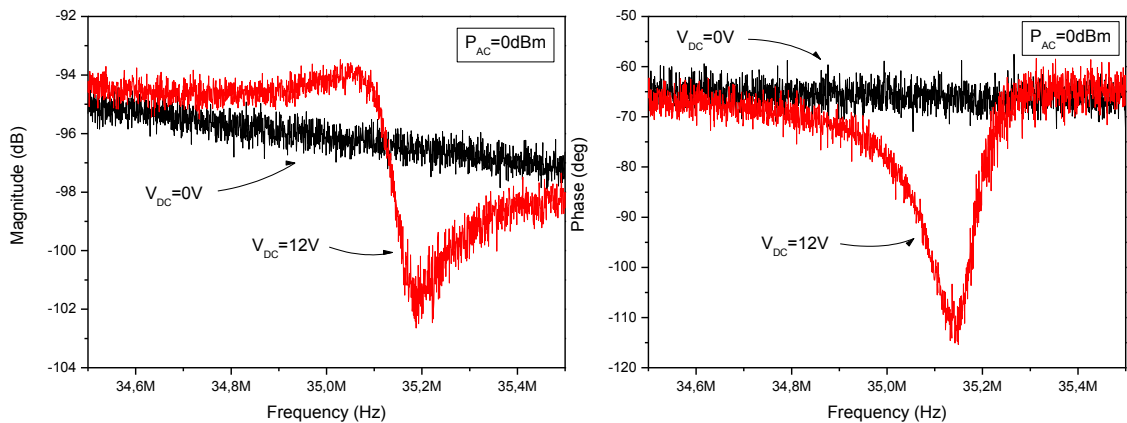


Figure 45.- Magnitude and phase response for T CCB with electrostatic excitation and capacitive sensing.

To complete the present section on the Table 7 shows a summary of the last structures fabricated, designed to be sensed both capacitively and piezoresistively. With

more accurate etching process the current paths could be eventually released enabling the piezoresistive measure of the motion. In addition, the asymmetric cantilever structures are not robust enough to remain suspended since the wider has collapsed and the thinner has curled up.

l (μm)	w (μm)	l_U / l_T (μm)	g (nm)	$k_{\text{eff flex}}/k_{\text{eff bulk}}$ (N/m)	$m_{\text{eff flex}}/m_{\text{eff bulk}}$ (pg)	$f_{\text{flex}}/f_{\text{bulk}}$ (MHz)
26.0	2.00	1.50/-	40	287.6/-	11.7/-	25/-
12.5	3.50	3.75/-	100	136.8/9830	5.61/9.31	25/160
12.5	6.00	4.75/-	100	767.1/16864	12.3/17.5	40/150
11.0	0.35	-/2.35	100	28.49/-	0.91/-	28/-

Table 7.- Summary of main parameters of broken symmetry MEMS resonators.

5.9. CONCLUSIONS

In the present chapter the piezoresistive sensing method has been described and applied to specific MEMS structures. The relevancy of the work lies on the use of the same piezoresistive structural material without adding doped layers or increasing the size of the resonator to perform the piezoresistive measurements. The measured CCB requires a specific set-up than the other stress based resonators (bulk or asymmetric flexural) because the piezoresistive mechanism is different. The dogbone resonators are promising VHF resonators which combined with CMOS circuit in closed loop configuration will provide good frequency references. The main benefit of piezoresistive sensing in frequency references field comparing with the capacitive method is that the motional resistance is substituted by the electric resonator resistance which is orders of magnitude lower. Such resistance decreasing allows easiest design of circuits with fewer stages and less gain, reducing the total oscillator size and more importantly their power consumption. The resonators could be also designed to make their resistance adapted to certain value (for example 50Ω like in RF systems) making it even easier the design complexity with the addition of standard VLSI blocks available in most of all the libraries provided by the CMOS foundries in their design kits.

The Table 8 shows the summary of all the resonators designed in this chapter highlighting their most important parameters. Comparing the obtained parameters for our designs with the state of the art given in the Table 1 some conclusions could be extracted. The resonant frequencies of our bulk and flexural resonators are higher due to the small size achieved with the CMOS technology. The low quality factor is mainly given by the polysilicon material but it is expected to be increased in vacuum ambient. The electrical resistances are in general lower than the other devices and some of them are specifically adapted to the desired value. The maximum current allowed is one order of magnitude lower than the currents employed in the measures of the papers. This restriction is given by the small thickness of the polysilicon layer and the design capability to increase the maximum current is based on the smallest device width.

Finally the estimated transconductance (for a gauge factor of 29 and assuming the biasing conditions given in each simulation) has slightly small values than the state of the art devices. Notwithstanding taking into account the small size and the high frequency the transconductance obtained is still good.

Device	f_0 (MHz)	Q	R (Ω)	Max. current (mA)	g_m (μ S)*
CCB	27	40	297	0.175	1769
LBAR	250	1000	202	0.175	3.23
LBAR	433	1000	122	0.175	3.23
Dogbone	250	100	50	0.175	0.69
Dogbone	433	100	29	0.175	0.58
Dogbone	50	100	52	1.000	0.08
Dogbone	100	100	76	0.250	0.13
Dogbone	231	100	29	0.250	0.57
CCB asymm	27	210	50	0.175	24656
Cantilever asymm	25/160	100	50	0.500	16226/0.81
Cantilever asymm	40/150	100	50	0.500	313/1.38
CCB T	35	87	45	0.175	50854

Table 8.- Summary over the parameters of MEMS resonators with piezoresistive sensing. Transconductance analytically determined using the flexural and bulk models and employing the biasing and displacements used in the FEM simulations.*

6. CONCLUSIONS AND FUTURE WORK

From the scope of the present Ph.D dissertation there are two main contributions in the field of CMOS-MEMS. By one side the fabrication of MEMS in standard CMOS technologies provides the performance and reliability of microelectronic processes for batch fabrication of MEMS devices. The smartly combination of the different layers available in the CMOS technology afford the monolithic integration of different components of a final device (e.g MEMS resonator, CMOS circuit and package). By the other side, the sensing of MEMS is challenging if the size keep scaling down. The size decreasing enhances parameters such as frequency or mass sensitivity, but also decreases the amount of useful output signal. In this sense two sensing strategies have been presented and reported: capacitive and piezoresistive sensing.

6.1. FABRICATION

The CMOS-MEMS fabrication method based on AMS 0.35 μ m CMOS technology has been presented. Only a simple mask less post-CMOS silicon dioxide wet etching process is used to release the resonators. Combining the layout design between layers it is possible to reach small transduction gaps such as 40nm.

The metal layers have been used to develop a package for polysilicon CMOS-MEMS resonators and different approaches for sealing with metal layers have been presented. The characterization of the package was performed physically and electrically. Finally the sealed package has demonstrated that allows the correct MEMS releasing and protects the resonator from subsequent processes. The challenge to maintain vacuum inside the cavity has not been accomplished. However, as a future work to reach this vacuum, different package design strategies and most reliable sealing processes could be employed. In this sense additional analysis such as outgassing from the packaging materials and long term leakage stability must be performed.

Related with fabrication it has also been presented our capability to fabricate MEMS resonators with built-in nanochannels. The preliminary MEMS designs showed are correctly released but their nanochannels are not fully emptied. As future work a better confinement of the etchant solution and reduction of the size are promising solutions to obtain a reliable MEMS with built-in nanochannels. The electrical characterization and the application on microfluidic system for sensing purposes are both future lines of work. In this sense a major challenge to face corresponds to the placement of fluidic pipes on the micron size openings of the chip.

6.2. SENSING

From the sensing point of view of CMOS-MEMS resonators, capacitive and piezoresistive approaches have been adopted.

In capacitive sensing the goal pursued with the fabricated devices has been the improvement of their performance increasing their quality factor, coupling area or enhancing the response by means of their nonlinearity. CCB resonators with state of the art performance have been successfully tested: 28MHz resonator with $754\text{k}\Omega$ of motional resistance and 51MHz with transduction gain of 19A/m . The cross beams structure presented provides an enhancement over the coupling area which could be applied in small size and high frequency MEMS resonators. This resonator could not be tested due to the strongest etching of the electrodes which can be solved in future structures adopting some modifications over the layout. MEMS with CMOS circuits have been also measured presenting a DETF oscillator with -100dBc/Hz at 1kHz and the first packaged Free-free oscillator. The fully characterization and sealing of the package are both future lines of work to provide competitive and reliable integrated CMOS-MEMS oscillators for frequency reference applications.

Considering the polysilicon material from the structural layer of CMOS-MEMS resonators the piezoresistive sensing method has been adopted with two goals. By one side, is presented as a solution for the related problems with capacitive sensing in scaling down devices. For the other side, be able to achieve a resonator without the major trouble of high motional impedance which in fact reduces the circuit complexity to develop a CMOS-MEMS monolithic oscillator. Several piezoresistive resonators have been designed considering bulk (LBAR, dogbone, asymmetric topologies) or flexural modes (CCB, CCB-T and asymmetric topologies). Their estimated transconductance has been computed obtaining values in the range of the other state of the art approaches. In order to face with the flowing current, which has destroyed several resonators; different measuring set-ups have been adopted. The piezoresistive measure of CCB in flexural mode has provided the capability to extract the gauge factor of polysilicon. A 231MHz dogbone resonator, 27MHz asymmetric CCB and 35MHz CCB-T have been capacitively measured and will be piezoresistively measured. Also as a future work it is foreseen the development of the CMOS circuits required to fabricate a fully piezoresistive CMOS-MEMS oscillator as well as the evaluation of the noise in piezoresistors.

6.3. CONTRIBUTIONS OF THE AUTHOR

In this section the contributions of this thesis work as articles published in international journals and the contributions to international conferences are listed and chronologically sorted.

6.3.1. ARTICLES IN INTERNATIONAL JOURNALS

E. Marigó, J.L. Muñoz-Gamarra, J. Giner, A. Uranga, N. Barniol, “A 230 MHz CMOS-MEMS bulk acoustic wave resonator”, *Microelectronic Engineering* vol. 98: 458-462, 2012.

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6.3.2. ABSTRACTS IN CONFERENCES

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J.L. López, **E. Marigó**, J. Giner, J.L. Muñoz-Gamarrá, F. Torres, A. Uranga, N. Barniol, CMOS-MEMS free-free beam resonators, *ESSDERC*, 13-17 September 2010, *European Solid-State Device Research Conference*, Sevilla (Spain).

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E. Marigó, J.L. Lopez, G. Murillo, F. Torres, J. Giner, A. Uranga, G. Abadal, J. Esteve and N. Barniol, “Zero level package of RF-MEMS in standard CMOS technology”, *MME*, 20-22 September 2009, *Micromechanics Europe*, Toulouse (France).

A. CMOS-MEMS CHARACTERIZATION

In this annex each specific set-up for the different measuring configurations is included. All the equipment required to perform the electrical and physical characterization of the CMOS-MEMS devices is also explained.

ELECTRICAL CHARACTERIZATION

For the electrical measures the equipment required could be divided into passive and active devices. The passive devices include the tools required to perform electrical contact between the devices and the electrical instruments. The active devices are the electrical instruments which require electrical power and provide electrical inputs or outputs.

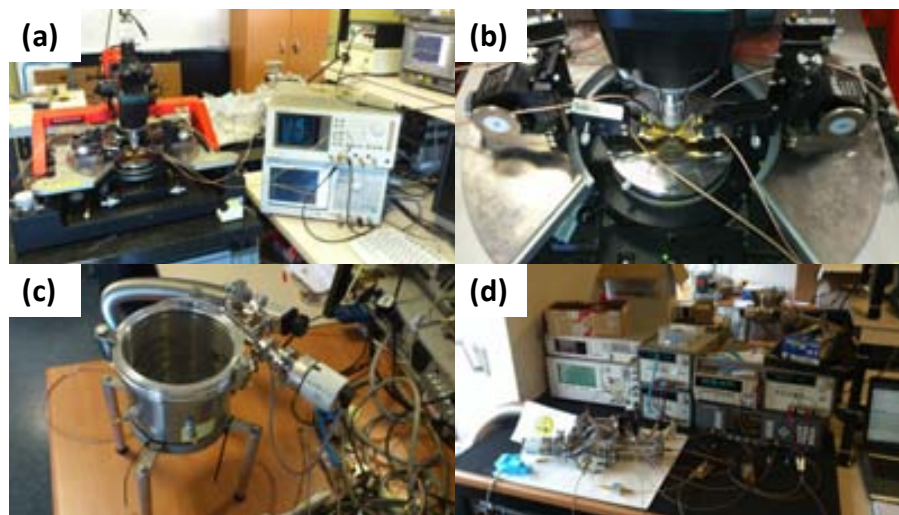


Figure 194.- Electronic equipment in the main laboratory: (a) Probe table with microscope, network and signal source analyzers; (b) detail of the probes contacting a chip; (c) vacuum chamber to perform low pressure measurements; (d) lock-in measurement set-up with signal generators, DC sources, attenuators, etc.

ELECTRICAL SET-UPS

There are several different measurement set-ups configurations in function of the type of applications and parameters searched. The set-ups from A, B, C, D and F sections correspond to electrostatic excitation and capacitive sensing whilst the ones of E and G corresponds to electrostatic excitation and piezoresistive sensing. The MEMS resonator employed for all the set-ups is a CCB with two electrodes because it could be adapted to every kind of the different measures performed.

Figure 195 shows the two ports standard configuration of MEMS with electrostatic excitation and capacitive sensing.

This is the two ports standard configuration of MEMS with electrostatic excitation and capacitive sensing. The DC source is employed to polarize the mechanical structure and enable the motional output current. The network analyzer provides the excitation AC signal and detects the output motional current. This set-up provides better performance than the one port set-up which presents higher parasitic capacitance. The set-up is employed to detect the mechanical resonance, extract the quality factor and perform DC or AC sweeps to obtain the spring softening and the dynamic range from nonlinear effects.

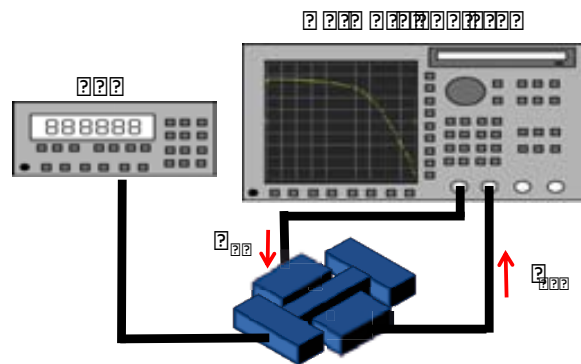


Figure 195.- Two ports electrostatic excitation and capacitive sensing of stand alone MEMS resonators.

Figure 196 shows the two ports standard configuration of MEMS with electrostatic excitation and capacitive sensing.

This set-up is similar than the previous stand alone set-up with the difference that a monolithic CMOS amplifier is added at the output electrode of the MEMS device. An additional DC source is required to polarize the CMOS circuit. This set-up provides higher power signals than the previous one and is more robust in front of the external parasitic (i.e due to the PCB or the wire bonding). The output impedance may be adapted to 50Ω by means of an output buffer. The correct polarization of the circuit is checked by means of their current consumption.

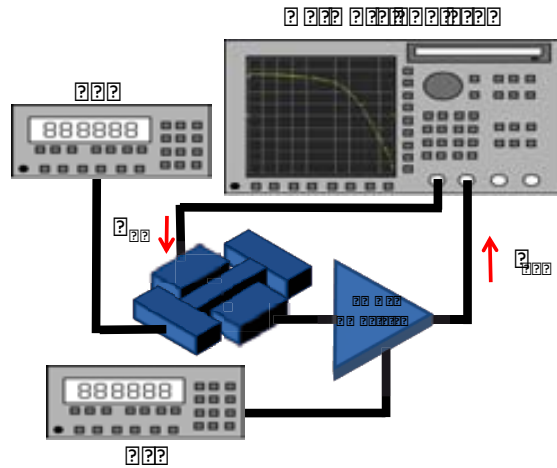


Figure 196.- Two ports electrostatic excitation and capacitive sensing of MEMS with CMOS amplifier.

When the MEMS resonator and the CMOS amplifier are connected in closed loop configuration to develop an oscillator there is no need of an external excitation signal. So the output signal can be detected with an oscilloscope or a spectrum analyzer. This set-up is capable to perform transient, frequency and phase noise measurements.

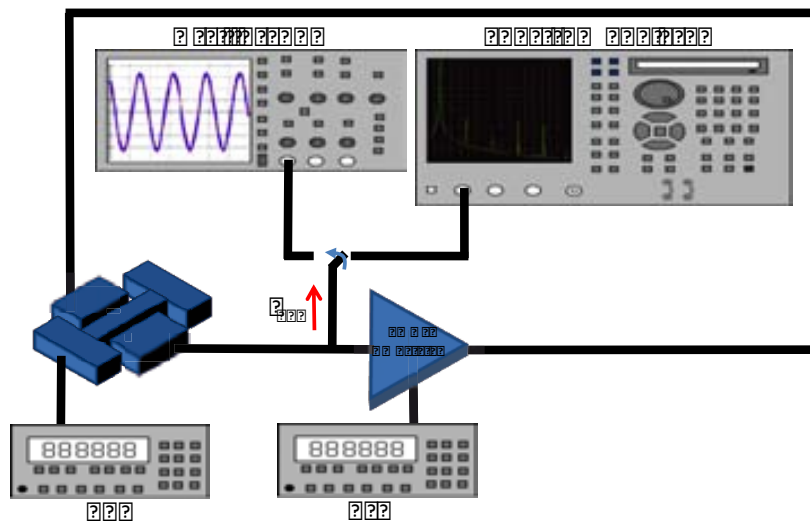


Figure 197.- Two ports electrostatic excitation and capacitive sensing of CMOS-MEMS oscillator.

In the case of four electrode resonator (i.e cross beams) the set-up requires that the excitation signal must be separated using a power splitter in order to excite symmetrically the resonator by the two actuation electrodes. The two sensing electrodes could be connected to two different ports and combine the signals by software or introduce a power combiner and perform the sensing into one single port. This configuration provides a higher coupling area and could be employed to sense small and high frequency resonators.

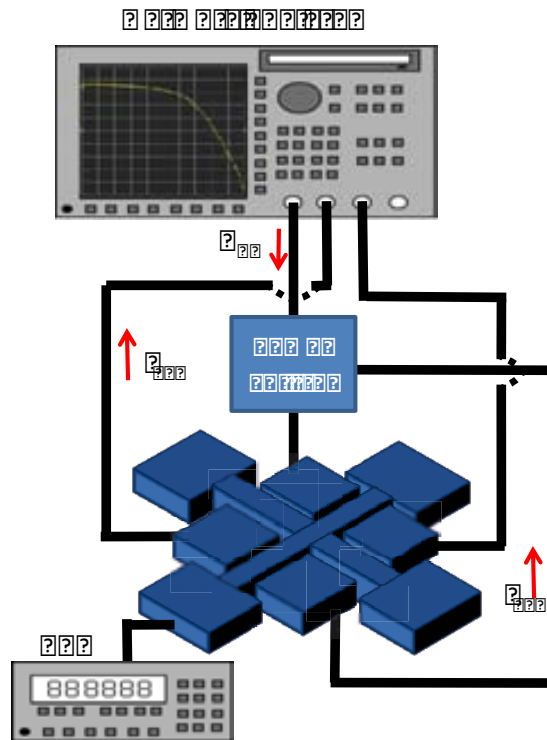


Figure 198.- Four ports electrostatic excitation and capacitive sensing of MEMS resonator.

The piezoresistive set-up with network analyzer requires two DC voltage sources. One source is connected with a bias T to the excitation port and both of them are connected to the actuation electrode. The other source is used to enable a DC current through the resonator where the resistive variations produced by the motion will be added. The obtained piezoresistive current will be detected by the network analyzer.

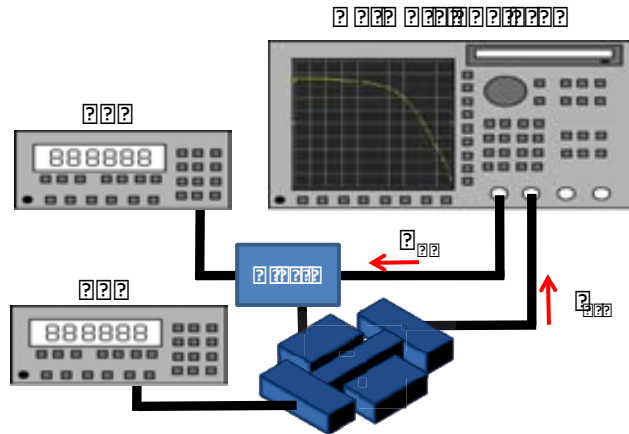


Figure 199.- Electrostatic excitation and piezoresistive sensing of MEMS resonator with network analyzer.

Figure 199 shows a network analyzer connected to a MEMS resonator. The resonator is represented by three blue rectangular blocks. The network analyzer has a screen displaying a graph. Two digital multimeters (DMMs) are connected to the resonator. Red arrows indicate the direction of signal flow: one from the network analyzer to the resonator, and another from the resonator to the network analyzer.

The following set-up based on lock-in amplifier measurement is based on electrostatic excitation and capacitive sensing with mixing configuration. Both RF signals are splitted and their frequency is combined by a mixer to obtain the reference signal of the lock-in amplifier. The MEMS resonator is excited by one electrode and the LO signal plus the DC biasing voltage is set on the structure. The attenuators are placed between each signal path to set the appropriate power level since the mixer requires a minimum level signal which can be higher for the resonator. The output down mixed current from the output electrode is detected by the lock-in amplifier.

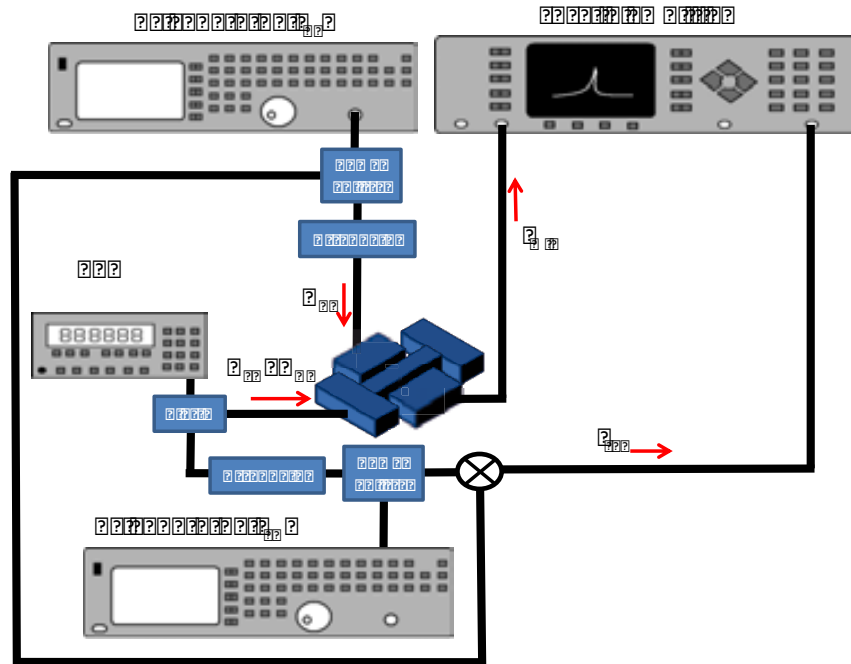


Figure 200.- Electrostatic excitation and mixing capacitive sensing of MEMS resonator with lock-in amplifier.

?

The last set-up is also based on lock-in amplifier measurement with electrostatic excitation. However the sensing in this case is piezoresistive. The piezoresistive current from the flexural CCB is obtained at the double of the resonant frequency. To sense this current with the lock-in amplifier the frequency must be down mixed by the combination of the two signals from RF generators. The frequency doubler and the mixer are used to construct the reference signal of the lock-in amplifier. The function of the attenuators is the same than the previous configuration.

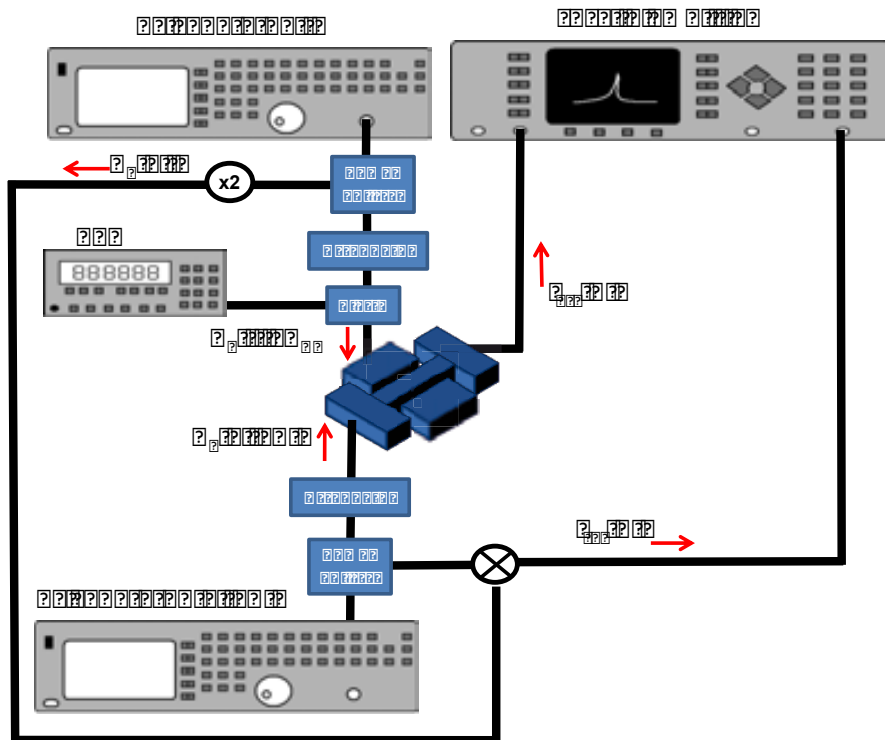


Figure 201.- Electrostatic excitation and piezoresistive sensing of MEMS resonator with lock-in amplifier.

?

In the development of the present thesis two types of characterization has been employed: electrical and physical. The electrical characterization was completely performed on the laboratories of the group whilst the physical characterization was developed also in different clean room installations (CNM, UAB and ICMAB). The electrical characterization requires tools to perform connections between the pads of the chips and the electronic instruments of the set-up. In some cases additional RF components are mandatory (power splitter, attenuator, bias-T...).

PROBE TOOLS

- Manual probe table PM-8 from Süss Microtech. It has three degrees of freedom (one for each axis), vacuum wafer suction and microscope with three lenses (10X, 20X, 100X).



Figure 202.- Probe table PM-8 from Süss Microtech.

- Probe holder Infinity from Cascade Microtech. It has three degrees of freedom (one for each axis) with $3\mu\text{m}$ of resolution and magnetic attachment.

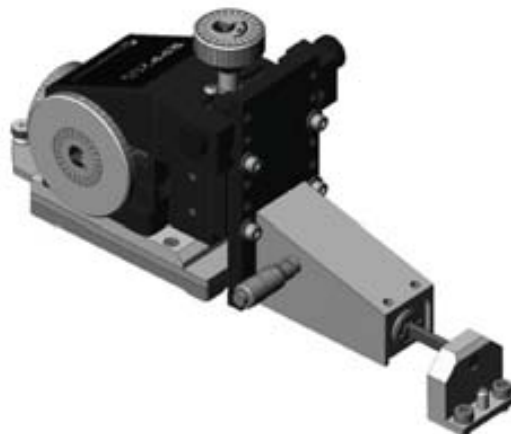


Figure 203.- Infinity probe holder from Cascade Microtech.

- RF probes from Cascade Microtech. Two RF signals shielded by three grounded probes. Pitch of 150 μ m and supported frequencies till 40GHz.

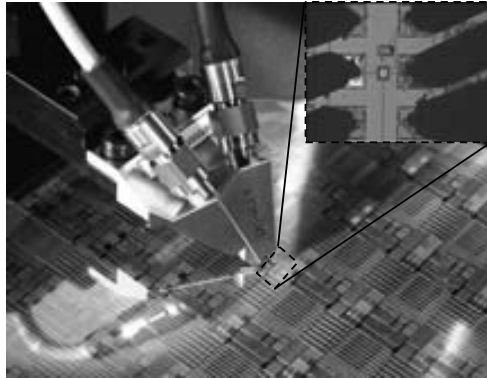


Figure 204.- Z probes from Cascade Microtech with detail zoom of the contact with metal pads.

ELECTRONIC INSTRUMENTATION

- DC voltage source Keithley 230 with range of 0-100V with maximum current of 2mA.



Figure 205.- DC voltage source Keithley 230.

- DC voltage source 6631B from H&P (Agilent Technologies) with range of 0-15V and 3A of maximum current. Current and voltage sinking display.



Figure 206.- DC voltage source 6631B from Agilent Technologies.

- DC voltage source E3631A from Agilent Technologies. Regulable triple output 6V (2A) and $\pm 25V$ (1A).



Figure 207.- DC voltage source E3631A³⁴ from Agilent Technologies.

- Source measure unit 2636 from Keithley. Current source/sink capability from 1fA to 10A and voltage from 1 μ V to 200V.



Figure 208.- Source measure unit 2636 from Keithley.

³⁴ Property of IMB-CNM (CSIC)

- RF signal generator 81150A from Agilent Technologies with two channels with signals of maximum frequency of 120MHz and 10Vpp. Capability to generate pulse, sine, square ramp and analogic or digital modulations.



Figure 209.- RF signal generator 81150A from Agilent Technologies.

- RF signal generator N5181A from Agilent Technologies. Frequency range from 100kHz to 3GHz. Maximum output power of 23dBm.



Figure 210.- RF signal generator N5181A from Agilent Technologies.³⁵

- RF signal generator E8257D from Agilent Technologies. Frequency range from 250kHz to 20GHz with maximum output power of 26dBm. Modulation and frequency/amplitude sweep capabilities.



Figure 211.- RF signal generator E8257D from Agilent Technologies.³

³⁵ Property of IMB-CNM (CSIC)

- Oscilloscope TDS220 from Tektronix. Two input channels with 100MHz of bandwidth with 1GS/s. Basic mathematic operations and FFT capabilities.



Figure 212.- Oscilloscope TDS220 from Tektronix.

- Network analyzer E5100A from Agilent Technologies. Two ports with frequency range from 10kHz to 180MHz. Maximum output signal power of 18dBm and minimum IF filter of 10Hz.



Figure 213.- Network analyzer E5100A from H&P (Agilent Technologies).

- Network analyzer E5071B from Agilent Technologies. Four ports with frequency range from 300kHz to 3GHz. Capability to perform differential measurements and introduce offset frequency between channels. Maximum output signal power of 10dBm and minimum IF filter of 10Hz.



Figure 214.- Network analyzer E5071B from Agilent Technologies.

- Spectrum analyzer E4404B from Agilent Technologies. Frequency range from 100Hz to 6.7GHz with maximum input power of 30dBm. Capability to perform phase noise measurements.



Figure 215.- Spectrum analyzer E4404B from Agilent Technologies.

- Signal source analyzer E5052A from Agilent Technologies. Frequency range from 10MHz to 7GHz with input power signals from -20dBm to 20dBm. Capability to perform phase noise measurements.



Figure 216.- Spectrum analyzer E4404B from Agilent Technologies.





- Lock-in amplifier 7280 DSP from Signal Recovery. Sensitivity from 1nV to 1V with frequency range from 0.5Hz to 2MHz.



Figure 217.- Lock-in amplifier 7280 from Signal Recovery.³⁶

RF COMPONENTS

In some set-up configurations additional RF components had been used. The following table summarizes each one of them with the main parameters and the set-up where it had been used.

	Device	Set-up used
	<p><u>Bias T</u> ZFBT-6GW+ from Mini Circuits. Frequency range from 100kHz to 6GHz, maximum RF power of 30dBm and maximum DC voltage of 30V.</p>	<p>Figure 199 Figure 200 Figure 201</p>
	<p><u>Power splitter/combiner</u> ZFSCJ-2-1 from Micro Circuits. Frequency range from 1MHz to 500MHz with maximum input power of 30dBm.</p>	<p>Figure 198 Figure 200 Figure 201</p>
	<p><u>Voltage variable attenuator</u> ZX73-2500+ from Mini Circuits. Frequency range from 10MHz to 2.5GHz with variable attenuation from 40dB to 3dB with voltage of 0V to 17V respectively.</p>	<p>Figure 200 Figure 201</p>
	<p><u>Mixer</u> ZP-5MH-S+ from Mini Circuits. Frequency range from 20MHz to 1.5GHz with maximum input level of 13dBm.</p>	<p>Figure 200 Figure 201</p>

³⁶ Property of IMB-CNM (CSIC)


	<p>Frequency multiplier (x2) FK-5-S from Mini Circuits. Output frequency range from 20 to 2GHz with typical 13dB of insertion losses.</p>	<p>Figure 201</p>
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Table 28.- RF components employed in the different measuring set-ups.

VACUUM COMPONENTS

- Group home made vacuum chamber with eight RF ports and crystal cover for devices visibility.

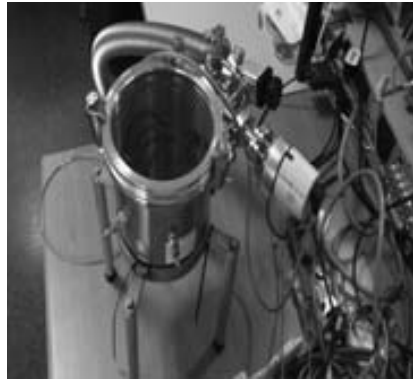


Figure 218.- Home made vacuum chamber.

- Turbomolecular vacuum pump from Pfeiffer Vacuum with ultimate pressure below $1 \cdot 10^{-7}$ mbar.



Figure 219.- Turbomolecular vacuum pump from Pfeiffer Vacuum.

PHYSICAL CHARACTERIZATION

All this equipment has been directly used by the author after being qualified self-user at the IMB-CNM and ICMA B.

- Scanning electron microscope SEM LEO 1530 Gemini from Zeiss. Acceleration voltage from 0.2kV to 30kV with maximum resolution of 1nm. Primary electron detector (inlens) and secondary electron detector (SE). Capability to perform EBL lithography.



Figure 220.- SEM LEO 1530 from Zeiss.³⁷

- Scanning electron microscope EVO MA10 from Zeiss. Acceleration voltage from 0.2kV to 30kV with maximum resolution of 3nm. Primary electron detector (inlens) and secondary electron detector (SE). Capability to perform Energy-dispersive X-ray spectroscopy.



Figure 221.- SEM EVO MA10 from Zeiss.³⁸

- Focused Ion Beam 1560XB Cross Beam with SEM from Zeiss. Acceleration voltage of SEM from 0.2kV to 30kV with maximum

³⁷ Property of IMB-CNM (CSIC)

³⁸ Property of IMB-CNM (CSIC)

resolution of 1nm. Primary electron detector (inlens) and secondary electron detector (SE). Acceleration voltage of FIB from 8kV to 30kV with maximum resolution of 7nm. Capability to perform nanomachining and EBID with real time visualization.



Figure 222.- FIB 1560XB Cross Beam from Zeiss.³⁹

OTHER EQUIPMENT

- Manual wire bonding 4526 from Kulicke&Soffa. Wire diameter of 100 μ m. Capability to perform ball or wedge bonding.



Figure 223.- Manual wire bonding 4526 from Kulicke&Soffa.

- Laser micro writer from Durham Magneto Optics. Direct-write lithography with 1 μ m of resolution and optical alignment.

³⁹ Property of ICN-CIN2

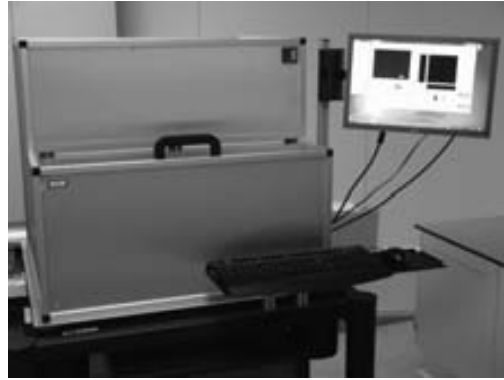


Figure 224.- Laser micro writer from Durham Magneto Optics.⁴⁰

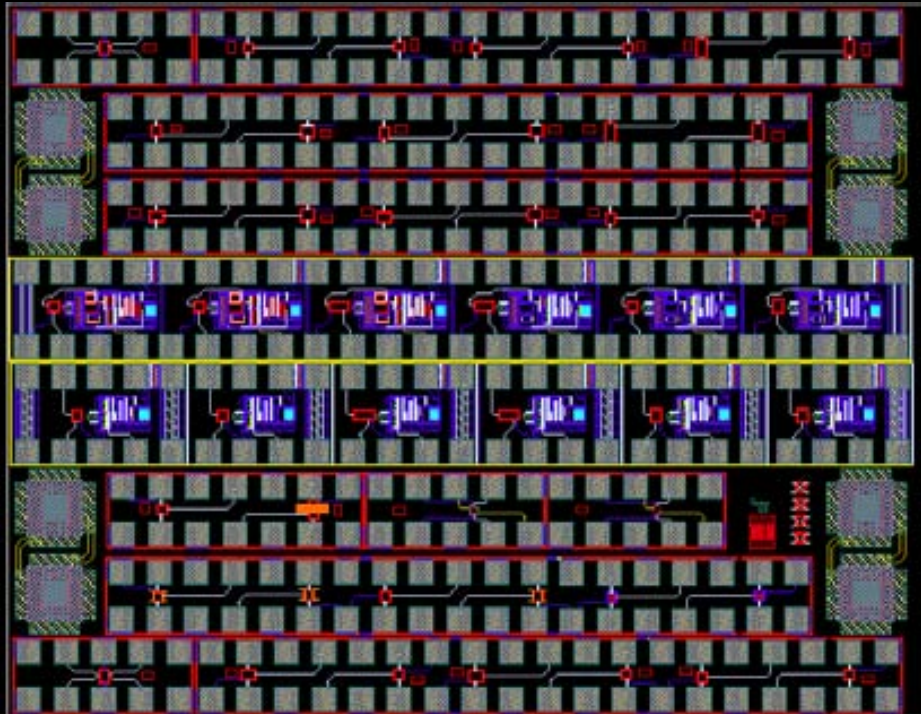
⁴⁰ Property of ICMAB

B. RUN DESCRIPTION

In this section all the chips submitted during this thesis are described. The different types of MEMS resonators included in this Ph.D thesis and contained in each RUN are also depicted and their MEMS parameters are grouped. In some RUNs the resonators are packaged and CMOS circuitry is added. The capability to be piezoresistively sensed enabling the current flow through the resonator is also established.

APRIL2008

RUN code: 12187-010	Technology: AMSC35B4C3					
Chip area: 2.8x3.6 mm ²	#chips: 30	Funding: MEMSPORT				
MEMS devices:	CCB			DETF	Free-free	
PARAMETER						
length (μm)	13.2	13.2	9.4	13	12.8	17
width (μm)	0.5	0.5	0.5	0.35	0.5	0.8
gap (nm)	100	40	40	150	40	40
support length (μm)	-	-	-	-	5.3	20
support width (μm)	-	-	-	-	0.5	0.4
coupler length (μm)	-	-	-	-	3	-
coupler width (μm)	-	-	-	-	1.5	-
stand alone	X	-	-	X	X	X
packaged	-	-	-	X	-	-
CMOS amplifier	X	X	-	-	X	X
CMOS oscillator	X	X	-	-	X	X



The micrograph displays a complex MEMS resonator chip layout. It features a central horizontal strip containing several resonator units, each with a distinct blue and purple color scheme. The chip is surrounded by a network of red and black lines representing electrical interconnects and support structures. The overall design is symmetrical and highly detailed, typical of a high-frequency MEMS device.

Author contribution: Post-processing and electrical characterization.

MARCH2009

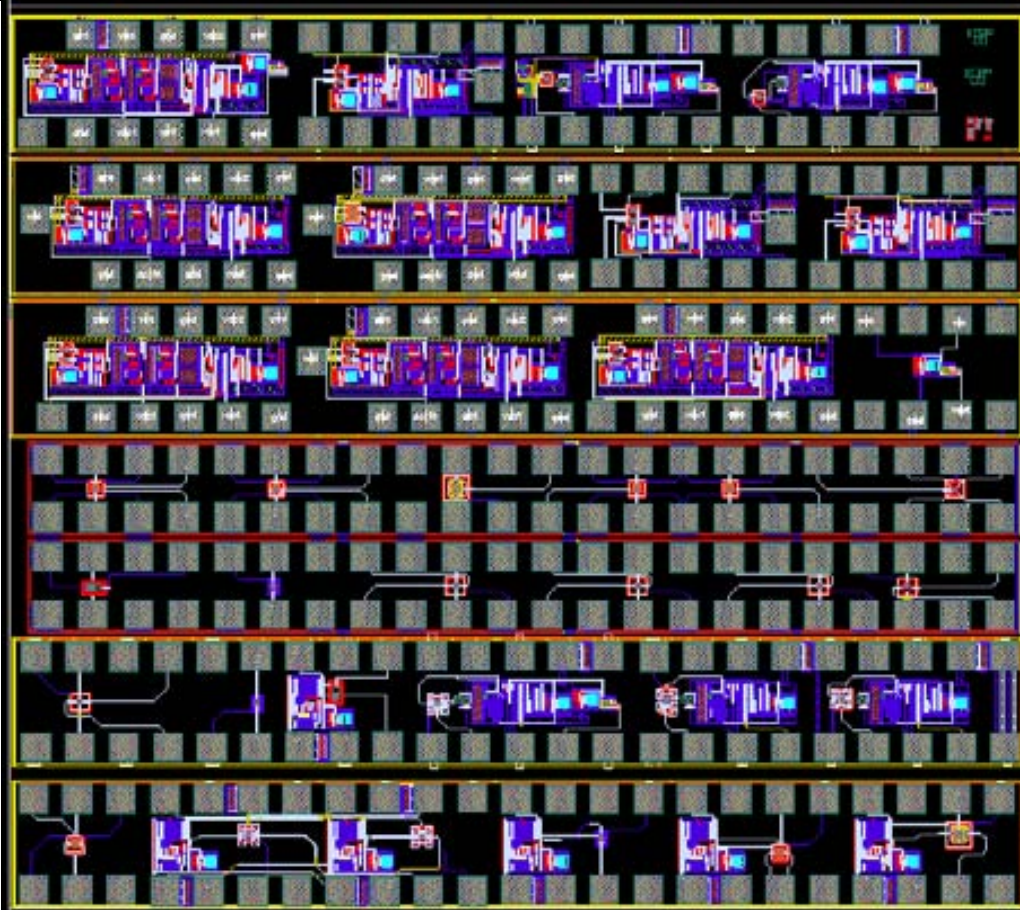
RUN code: 12281-008	Technology: AMSC35B4C3						
Chip area: 2.8x3.6 mm ²	#chips: 40	Funding: MEMSPORT					
MEMS devices:	CCB			LBAR			
PARAMETER							
length (µm)	13	13	13	13.1	13.1	7.56	7.56
width (µm)	0.35	0.35	0.35	1.15	1.15	1.15	1.15
gap (nm)	40	100	150	100	150	100	150
stand alone	-	-	-	X	X	X	X
packaged	X	X	X	-	-	-	-
CMOS oscillator	X	X	X	-	-	-	-
piezoresistive	-	-	-	X	X	X	X



Author contribution: Design, post-processing and electrical characterization.

DECEMBER2009

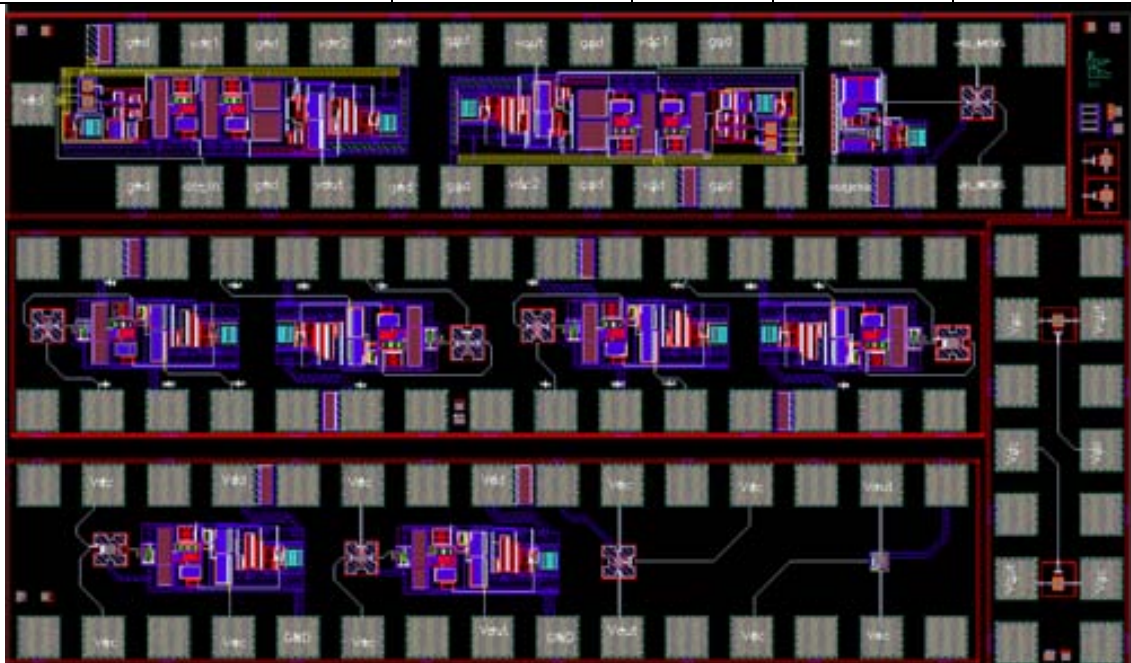
RUN code: 12350-009	Technology: AMSC35B4C3					
Chip area: 3.0x3.3 mm ²	#chips: 30	Funding: MEMSPORT				
MEMS devices:	CCB	DETF	Free-free	LBAR		
Parameter						
length (μm)	13	13	12.8	17	1	2
width (μm)	0.35	0.35	0.5	0.8	0.525	0.525
gap (nm)	150	100	40	40	40	100
support length (μm)	-	-	5.3	20	-	-
support width (μm)	-	-	0.5	0.4	-	-
coupler length (μm)	-	-	3	-	-	-
coupler width (μm)	-	-	1.5	-	-	-
mass width (μm)	-	-	-	-	2.5	3
mass length (μm)	-	-	-	-	1.7	2.5
stand alone	-	X	-	-	X	X
packaged	X	-	X	X	-	-
CMOS amplifier	X	-	-	-	-	-
CMOS oscillator	X	-	X	X	-	-
piezoresistive	-	X	-	-	X	X



Author contribution: Design, post-processing and electrical characterization.

AUGUST2010

RUN code: 12412-001*	Technology: AMSC35B4C3			
Chip area: 1.5x2.5 mm ²	#chips: 25	Funding: NEMESYS		
MEMS devices:	CCB	DETF	Free-free	
Parameter				
length (μm)	13	13	12.8	17
width (μm)	0.35	0.35	0.5	0.8
gap (nm)	40	150	40	40
support length (μm)	-	-	5.3	20
support width (μm)	-	-	0.5	0.4
coupler length (μm)	-	-	3	-
coupler width (μm)	-	-	1.5	-
stand alone	X	X	-	-
packaged	X	X	X	X
CMOS amplifier	-	X	-	X
CMOS oscillator	X	X	X	X

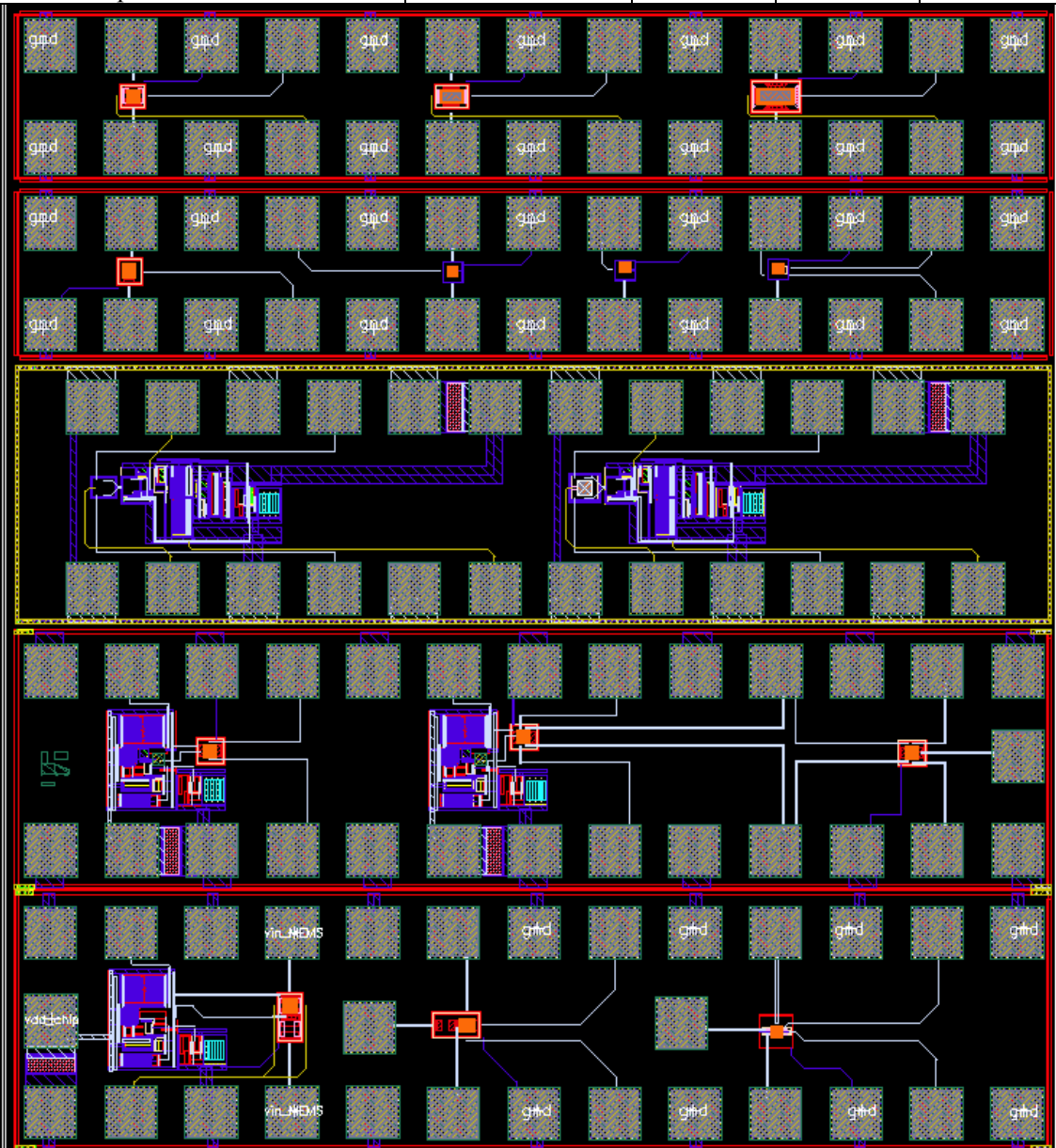


Author contribution: Design, post-processing and electrical characterization.

*In this RUN the nanochannel test structures without electrical pads have been included to check their properly fabrication.

DECEMBER2010

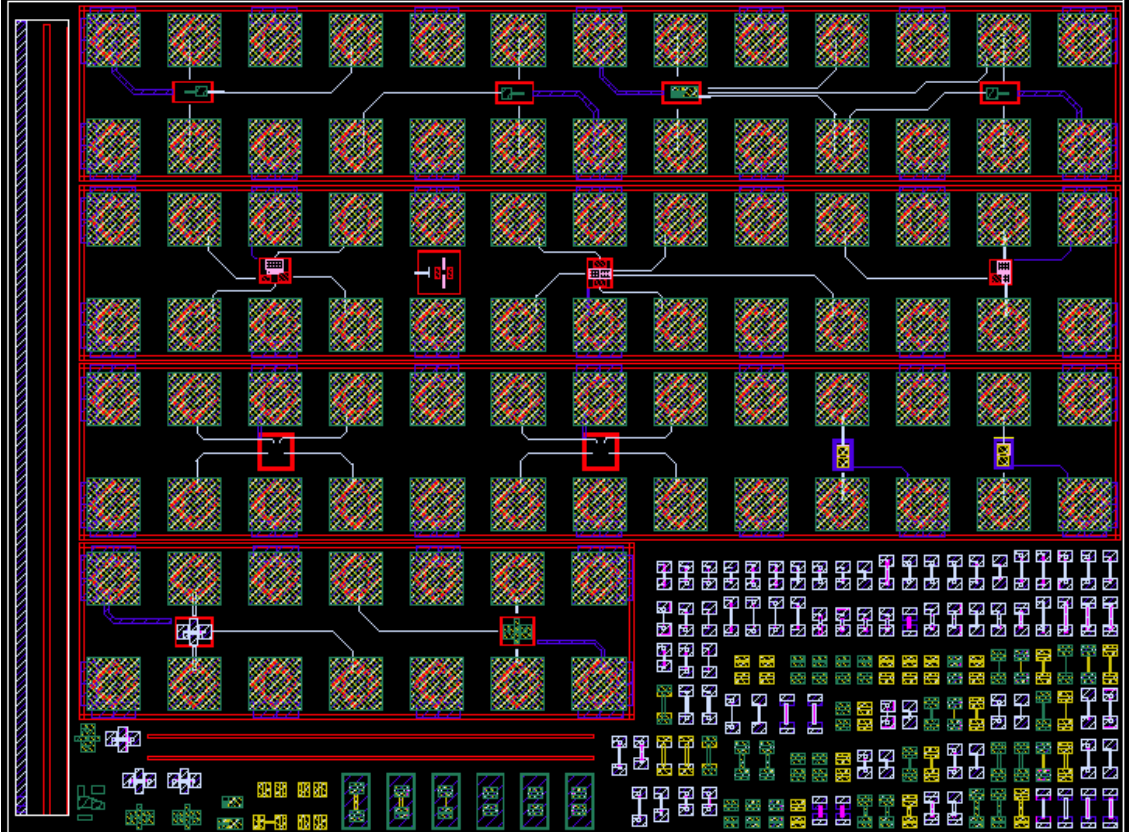
RUN code: 12434-010	Technology: AMSC35B4C3			
Chip area: 2.0x1.8 mm ²	#chips: 30	Funding: NEMESYS		
MEMS devices:	Dogbone		CCB	
Parameter				
length (μm)	1.5	4.5	12	13.2
width (μm)	0.5	0.5	2	0.5
gap (nm)	40	100	100	100
mass length (μm)	3.5	5	5	-
mass width (μm)	3	12.5	12.5	-
stand alone	X	X	X	X
CMOS amplifier	X	-	-	-
piezoresistive	X	X	-	-



Author contribution: Design, post-processing and electrical characterization.

APRIL2011

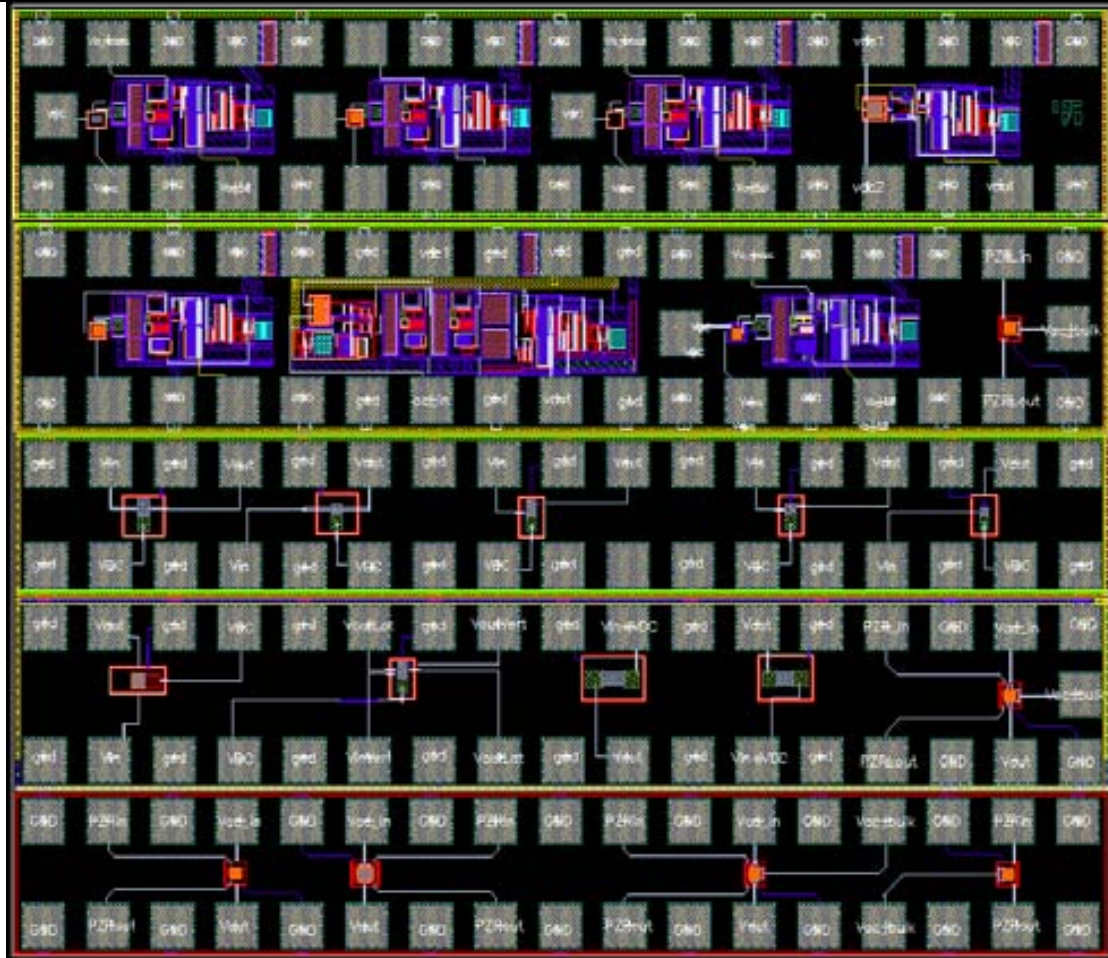
RUN code: 12462-006	Technology: AMSC35B4C3	
Chip area: 2.0x1.5 mm ²	#chips: 40	Funding: NEMESYS
MEMS devices:	CCB with built-in nanochannel	
Parameter		
length (μm)	20	10
width (μm)	4	1.45
gap (nm)	800	800
channel width (μm)	3	0.45
stand alone	X	X



Author contribution: Design, post-processing and electrical characterization.

MARCH2012

RUN code: 3335	Technology: AMSC35B4C3				
Chip area: 2.0x2.5 mm ²	#chips: 40	Funding: NEMESYS			
MEMS devices:	Asymmetric cantilever	Asymmetric CCB	CCB T	Middle DB	
Parameter					
length (μm)	12.5	12.5	26	11	6.25
width (μm)	6	3	2	0.35	2
gap (nm)	100	100	40	100	40
asymmetry length (μm)	4.75	3.8	1.5	-	-
asymmetry width (μm)	0.45	0.45	0.45	-	-
T length (μm)	-	-	-	2.35	-
T width (μm)	-	-	-	0.35	-
mass length (μm)	-	-	-	-	6.5
mass width (μm)	-	-	-	-	6.5
stand alone	X	X	X	X	X
piezoresistive	X	X	X	X	X



Author contribution: Design, post-processing and electrical characterization.

ABBREVIATIONS AND ACRONYMS

AC	Alternating current
AFM	Atomic force microscope
AMS	Autriamicrosystems
BEOL	Back-end-of-line processes
BPSG	Borophosphosilicate
CCB	Clamped clamped beam
CMOS	Complementary metal oxide semiconductor
CMP	Chemical mechanical planarization
CSIC	Consejo superior de investigaciones científicas
DC	Direct current
DECT	<i>Digital enhanced cordless telecommunications</i>
DETF	Double-ended tuning fork
DMD	Digital micromirror device
DRIE	Deep reactive ion etching
EBID	Electron beam induced deposition
EBL	Electron-beam lithography
ECAS	Electronic circuits and systems
FEOL	Front-end-of-line processes
FIB	Focused ion beam
GDSII	Graphic database system v2
HTO	High thermal oxide
IC	Integrated circuit
ICMAB	Institut de ciència de materials de Barcelona
ICTS	Instal·lació científica i tecnològica singular (Singular scientific and technological installation)

IMB-CNM	Institut de microelectrònica de Barcelona - Centro nacional de microelectrónica (Barcelona microelectronics institute – National center of microelectronics)
KOH	Potassium hydroxide
LBAR	Longitudinal bulk acoustic resonator
LCD	Liquid crystal display
LPCVD	Low pressure chemical vapor deposition
MEMS	Microelectromechanical systems
MIBK	Methyl isobutyl ketone
MMA	Methyl methacrylate
MPW	Multi project wafer
M ³ EMS	Modular, monolithic MEMS
NEMS	Nanoelectromechanical systems
PCB	Printed circuit board
PECVD	Plasma enhanced chemical vapor deposition
PMMA	Polymethyl methacrylate
PVD	Physical vapor deposition
RIE	Reactive ion etching
RF	Radiofrequency
SCM	Single chip module
SEM	Scanning electron microscope
SOI	Silicon on insulator
TMAH	Tetramethyl ammoniumhydroxide

