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Common-mode Voltage Cancellation in Single-and Three-Phase Transformer-less PV Power Converters

Gerardo Vázquez Guzmán

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Common-mode Voltage Cancellation in Single-and Three-Phase Transformer-less PV Power Converters

Gerardo Vázquez Guzmán

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Para mis padres y hermanos

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Resumen

La generación de energía eléctrica es una causa de gran preocupación alrededor del mundo. Se han hecho una gran cantidad de esfuerzos en este sentido para intentar cubrir la creciente demanda de energía eléctrica. Además del aumento en la demanda de energía eléctrica se requiere que sea renovable. Debido a esto, muchos países están haciendo grandes inversiones en sistemas de generación de energía eléctrica a partir de fuentes renovables como la energía del viento y la energía solar.

Los sistemas que generan energía eléctrica a partir de energía solar actualmente proporcionan un alto porcentaje del total de energía producida. De acuerdo con el último reporte de la agencia internacional de energía (IEA por sus siglas en inglés) en referencia al programa de sistemas de potencia fotovoltaica (PVPS por sus siglas en inglés), el total de potencia fotovoltaica instalada en el mundo hasta finales de 2009 fue de alrededor de 20.3 GW de los cuales 6.188 GW fueron instalados en 2009. Del total de potencia fotovoltaica instalada en 2009, 6.113 GW corresponden a sistemas conectados a la red eléctrica. El crecimiento de este tipo de sistemas se debe a la introducción de nuevas tecnologías y desarrollos que han permitido reducir los costes de diseño, manufactura e instalación de una planta solar.

Dado que el mayor porcentaje del total de la energía fotovoltaica instalada proviene de sistemas conectados a la red eléctrica, este trabajo de tesis está enfocado al análisis y a la presentación de soluciones en sistemas fotovoltaicos conectados a la red eléctrica sin transformador, los cuales pueden proporcionar eficiencias más altas que aquellos que usan transformador. Cuando no existe transformador entre el convertidor de potencia y la red eléctrica, corrientes parásitas pueden circular a través de los condensadores parásitos y causar serios problemas para los usuarios.

La principal tarea de este trabajo de tesis ha sido analizar y evaluar la operación de diferentes topologías sin transformador que han sido encontradas en la bibliografía y de esta forma proponer algunas soluciones para minimizar o eliminar las corrientes parásitas que pueden presentarse debido a las características del panel fotovoltaico y de las condiciones de operación generales del sistema.

Este trabajo de tesis está dividido en 6 capítulos. En el primer capítulo se expone el estado del arte en el cual se analizan las principales topologías usadas en aplicaciones de sistemas fotovoltaicos. En este análisis general se incluyen topologías tanto de sistemas monofásicos como de sistemas trifásicos. Se exponen las ventajas y desventajas principales para cada caso.

El segundo capítulo proporciona un análisis detallado de las principales topologías sin transformador en sistemas monofásicos. Las topologías con mayor eficiencia han sido estudiadas y se propone una nueva estructura de convertidor que presenta la característica de reducir a valores cercanos a cero la corriente parásita. Se presentan resultados tanto de simulación como experimentales para justificar las características de la topología propuesta.

En el tercer capítulo se introduce el problema de las corrientes parásitas en los sistemas trifásicos empleando un modelo de tensión de modo común del sistema. Una vez hecho este análisis, se presenta una nueva topología que ha sido llamada FB10 y que resuelve el problema de las corrientes parásitas. La topología consiste básicamente de dos buses de corriente continua y de un inversor trifásico en puente completo. Se presenta también para el FB10 un modelo de modo común basado en el modelo convencional. Se proporcionan detalles de la estrategia de modulación empleada para controlar el convertidor y un análisis de pérdidas para cada semiconductor usando PSIM® (Power Simulator) como herramienta de simulación. En este caso también se han realizado las correspondientes simulaciones, asimismo se proporcionan resultados experimentales para justificar la topología.

En el capítulo cuatro se presentan cuatro diferentes estrategias de modulación diseñadas para controlar el convertidor FB10. Cada estrategia de modulación presenta un comportamiento distinto tanto en pérdidas de potencia como en distorsión harmónica y generación de corrientes parásitas. Por esta razón se ha desarrollado un análisis completo de estos parámetros. Se presentan resultados de simulación y experimentales que proporcionan los detalles de operación de las cuatro estrategias de modulación.

Dado que los paneles fotovoltaicos no son fuentes constantes de tensión, en el capítulo cinco se proponen dos estrategias que permiten compensar el sistema tanto en tensión como en potencia. Un breve análisis muestra cómo funciona cada una de ellas. Se presentan resultados de simulación y experimentales de las estrategias propuestas.

Abstract

Covering the energy demand is an issue that is continuously cause of concern around the world. In the case of electrical energy many efforts have been lately addressed to cover the continuously growing electrical energy demand by means of using energy sources, different from those based on fossil fuels. In this sense, many countries have made a very strong bet on energy generation systems based on renewable sources, mainly wind and solar energy, something that has contributed to develop a solid and promising industry around these technologies.

At the present time, solar energy systems provide a significant percentage of the total energy production. According to the latest report of the International Energy Agency (IEA) regarding Photovoltaic Power System Program (PVPS), the cumulative installed PV power at the end of 2009 was around 20.3 GW out of which 6.188 MW were installed in 2009. From the total PV power installed in 2009, 6.113 MW were grid connected systems. The growth in the installed PV power is mainly due to the new technologies and developments that have permitted to reduce costs in the design and installation of PV systems.

As the major percentage of the total PV energy installed belongs to grid connected systems, this PhD deals with the analysis and proposals of transformerless grid-connected PV systems which, can provide higher efficiencies than PV systems with transformers. However, the lack of transformer between the electrical grid and the power converter generates serious problems regarding the appearance of leakage ground currents. This issue associated to these transformerless topologies, as well as the proposal of solutions oriented to overcome this drawback, is one of the main goals of this thesis work.

The main research task in this thesis work is to analyze and evaluate the operation of the different transformerless topologies presented in the bibliography and to provide some

solutions to minimize the leakage ground current phenomenon in order to comply with the standard requirements.

This dissertation is divided in 6 chapters. The first chapter deals with the state of the art, in which the main topologies used in PV applications are analyzed. This analysis considers not only single-phase structures but also three-phase topologies.

The second chapter provides an analysis of single-phase transformerless topologies. The most efficient topologies are studied and a new topology is proposed. Simulations and experimental results are provided in order to endorse the proposed topology.

The third chapter introduces the three-phase systems and the leakage ground current problem. A general common mode model for the conventional three-phase system is showed. Then a three-phase transformerless topology namely FB10 (Full-Bridge 10) is presented. As it will be further discussed this topology consists basically on two DC independent sources and a conventional three-phase inverter. A common mode model for the proposed topology, as well as a modulation strategy are explained in this chapter. In the framework of this study an analysis of the distribution losses, based on simulation, was also performed and presented in this work.

The fourth chapter deals with four different modulation strategies designed to control the FB10 topology. The modulation strategies have different performance in both power quality and efficiency. Therefore a complete analysis regarding losses, power quality and leakage ground current was performed introducing the IGBT model to measure the losses in each semiconductor. In this chapter experimental results are also shown for each case.

As the PV panels are not constant DC sources, the fifth chapter gives two proposals; one to control the power converter under voltage unbalances in the DC sources and the second one is a proposal to control the power injected from the PV panels. Also in this case, simulations and experimental results are provided.

In the last chapter the general conclusions and the future works of this PhD thesis are given.

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CHAPTER 1.

Introduction

In the last decades, renewable energies have emerged as a reliable solution to classical generation power plants based on fossil fuels, which are finite, nonrenewable and pollutants. Even new developments oriented to enhance the operation, control and performance of renewable energy based generation systems have contributed positively to improve its penetration into the electrical network; however there is still a lot to do in different fields in order to reach a massive integration of such systems. The usage of fossil fuels has contributed to maintain an alarming increase over the last 100 years in the atmospheric pollution level and global warming (which can reach a global average temperature as much as 6 ºC during XXIth century) this effect in the climate conditions, as well as the increasing environmental concern, has paved the way for the fast development and installation of renewable energy technologies like wind power (WT) and photovoltaic (PV) systems, whose development has been supported by the local governments, especially in European countries. As an example, WT in the range of several MW as well as PV farms in this power range are currently installed all around the world with great success.

Due to its high potential for producing clean energy among all of the renewable energy sources, solar energy continues to be one of the most attractive choices for investors and manufactures, mainly in grid connected residential applications. According with the European Photovoltaic Industry Association (EPIA) the total PV power installed at 2010 is around 37 GW compare to 20.3 GW in 2009. During 2010 Europe alone added between 11.6 and 13.3 GW of new PV installed capacities. Germany has been the leader in new PV installations in the last two years with around 7 GW (in 2010) followed by Italy, Czech Republic, France and Spain. Out of Europe the PV market is also growing, in 2010 the major markets progressed to reach in total between 2.6 and 3.2 GW of PV power installed, where Japan is the leader with 1 GW followed by USA (~800 MW) and China (~600 MW). In Figure 1.1, it is shown the historical PV global market development, for instance Europe is

the leader in 2010 with at least 13.3 GW representing around 80% of the global cumulative PV installed capacity [1.1].

The expectative for the future in PV energy industry is hopeful. Experts believe that in 2011 the market could reach up to 16 GW in a moderate scenario. The PV industry is hopping markets such as the French, Italian, Spanish, American and Chinese will pull the demand.

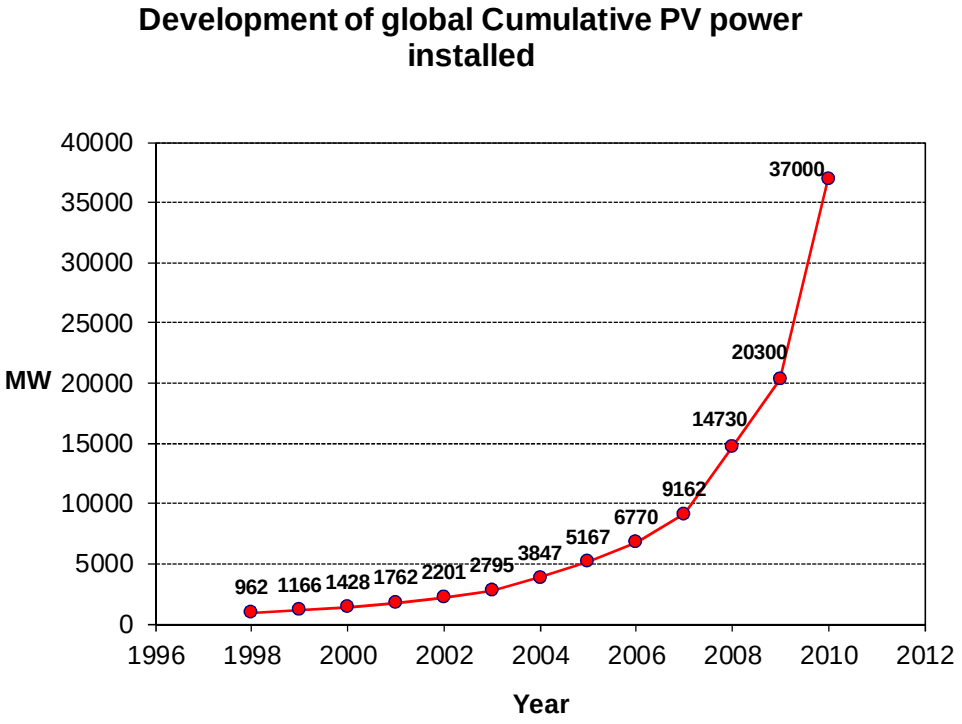


Figure 1.1. Evolution of the PV market during the last ten years.

1.1. Background and Motivation

The increase in the installation of power plants based on renewable energy sources has been almost exponential during the last years. These technologies are continuously under evolution and relevant efforts are being addressed in different research field in the aim of making these technologies more efficient, reliable and competitive. In this sense based on the research and evaluation performed some solutions and improvements can be provided in order to make a better use of the renewable energy resources.

Among renewable energy sources PV systems are gaining more and more importance in the renewable energy market. The power electronic systems used to convert the solar energy

from the PV panel (DC nonlinear power supply) into electrical energy have a special importance in the design of a PV power system, due to the fact that the PV panels itself have not a very high efficiency, commonly between 15% and 20% in average in commercial products. This means that the electronic power conversion stage must have a very good efficiency in order to make the overall system competitive from a power production point of view. Additionally the system must be reliable in terms of security and life time.

At the beginning, and still today in many applications, PV systems are designed for being connected to the grid through an isolation transformer that can be found in the system as a Low-Frequency Transformer (LFT) on the AC side, or as a High-Frequency Transformer (HFT) on the DC side. The main problem in this concept is that the transformer introduces additional losses in the system and its integration can be somehow difficult, as it is a heavy and bulky component, meanwhile it increases the overall costs. Another alternative to implement the PV system is to take out the isolation transformer and connect the system directly to the electrical grid by means of a filter (i.e. a LCL filter). The new *Transformerless* system can get a better efficiency than the first ones, but the main drawback is that now there is no galvanic isolation. Therefore, and due to the high frequency operation (typically in the range of 2 to 20 kHz) some leakage currents may appear trough the stray capacitance formed between the PV panel frame and the earth. The main motivation to develop this research work is to propose efficient power electronic solutions to solve the leakage current problem in transformerless PV applications.

1.2. Objectives

The main objectives of this PhD are focused in the study, analysis, test and proposal of new solutions within the field of PV transformerless inverters in both: single-phase and three-phase systems. In a nutshell, the main goals of this work are listed in the following:

- To review and evaluate the electrical effects of the leakage ground currents in PV systems.
- To model and proposed solutions to the leakage ground current problem in the case of PV transformerless topologies in single and three-phase systems.
- To make the proposed solutions compatible with the requirements established by the current standards applicable to PV systems connected to the electrical grid.
- To develop solutions that can be competitive with the commercial PV inverters not only in single-phase topologies but also in three-phase systems in terms of efficiency.
- To propose specific pulsed width modulation strategies to control the energy transfer in the proposed topologies.

According to the points listed above, the main objective of this thesis is to propose solutions based on hardware and control techniques that give rise to PV power systems able to reduce or eliminate the leakage ground currents, keeping or improving the total efficiency of the PV power conversion system.

1.3. Thesis Scope and limitations

This PhD work is focused in the PV power converter, which is the conversion stage responsible of managing the power flow between a DC input, coming from the PV panels, to an AC output, which is the distribution network. The power conversion stage can be implemented in different ways, for instance: three stages systems (Boost converter+Inverter+Low-frequency transformer), two stages (Inverter+Low-frequency transformer), etc. This thesis is focused just in single stage DC to AC configurations, where an inverter is connected directly to the grid through a grid connection filter. In this regard both, single-phase and three-phase systems were analyzed and the most interesting topologies were experimentally implemented. The PV array has been implemented using a constant DC source in both simulation and experimental tests.

1.4. Contributions

The contributions of this thesis work are the study about the problem associated to common mode voltage (CMV) and efficiency in the PV transformerless power converters and the proposal of solutions oriented to eliminate or reduce the leakage ground current magnitude.

In the case of single-phase systems a new topology called HB-ZVR topology with high efficiency and constant CMV has been proposed. The analysis and operation of this topology is widely explained in this document. A comparative analysis with the most extended topologies used in single-phase systems regarding the efficiency and leakage ground current was carried out in order to validate the feasibility of the proposed system.

In the case of three-phase systems, a new topology was proposed. The topology is three-phase extension of the H5 topology concept, in this case the CMV is constant and the leakage ground current is close to zero. This new topology is called FB10 topology.

1.5. State of the art

The PV panel technology has undergone a fast evolution in the last decades, improving noticeably their efficiency. Nowadays the commercial PV Silicon (Si) cells convert between 14% and around 22% of the solar radiation into usable electrical energy. Moreover, there are new PV technologies under development which are able to reach efficiencies close to 40.1%, as introduced in [1.2] and [1.3].

In the beginning, the PV modules were connected in series in order to get a higher voltage (each panel producing 40V) without using amplification system. Those arrays were later connected in parallel, so a higher power levels could be reached. These kinds of systems were experiencing some limitations, such as the need of high voltage DC cables, the high power losses, etc. However the main drawback of this configuration was its inadequate design for the massive production [1.4]. To overcome these limitations new structures and control methods have been developed.

Not only the PV technology and the connection configuration have been improved, but also the power electronics devices. The first PV generation plants were controlled using thyristors. As a consequence there were important problems regarding harmonics because they can produce a poor power quality. The modern MOSFET´s and IGBT´s which today are broadly used have contributed to reduce that problem thanks to their high switching frequency operation, i.e. in the case of MOSFET's. It should be remarked that certain PV systems may require devices that support 1000 V, for instance when series array of PV modules are directly connected to the inverter [1.4]. In order to overcome this limitation multi-string topologies can be implemented. These systems normally consist of a single PV strings connected to a DC-DC converter that is linked finally to a common inverter, responsible of injecting the power to the electrical grid.

At the beginning PV systems were designed for stand-alone operation, in which the grid connection was not required. This kind of applications are used in small camp houses, farms, public lighting systems, etc. (generally low power applications), in these applications single-phase systems are commonly used. At the present time, most PV systems are connected to the electrical grid by means of three-phase PV inverters. In this sense, lot of research has been done in order to overcome all the problems related to the grid connection, performance and security.

1.5.1. General PV system layout

A PV system consists in a few well defined stages. First stage is the PV panel or PV panel arrays; the PV panels receive and harvest the solar energy in order to transform it into electrical energy. This PV source is a DC nonlinear power supply that delivers its electrical energy to a second stage called DC-DC converter. The second stage can be omitted depending on the application and the PV array. This stage has at least two main functions which are to step-up the DC voltage and to performance the MPPT (Maximum Power Point Tracking) task. Third stage consists of an inverter which is responsible to change the DC voltage into an AC voltage. The AC voltage is then used as an input in a LCL filter which is directly connected to the grid (fourth stage). Finally a very important stage is the control system which has a lot of tasks to do; some of them are listed below:

- MPPT control
- DC bus control
- Inverter control
- Grid Synchronization
- Anti-islanding protection
- Grid support control

As can be seen, the complete system becomes complex when all parts are added. Figure 1.2 shows the different parts of a PV system connected to the electrical grid. The PV system is a single-phase system with a DC-DC boost converter which increases the input voltage to a suitable level. A LCL filter takes out the high frequency component from the output current and finally a low-frequency transformer connects the system to the electrical grid. This

transformer provides galvanic isolation for the PV system. The variables that in general are used to control the system are also shown. Input DC current (I_{pv}) and voltage (V_{pv}) are necessary to implement the MPPT algorithm of the PV panels. On the AC side, the output current (I_g) and voltage (V_g) are required to perform functions as: Current control, grid synchronization, etc.

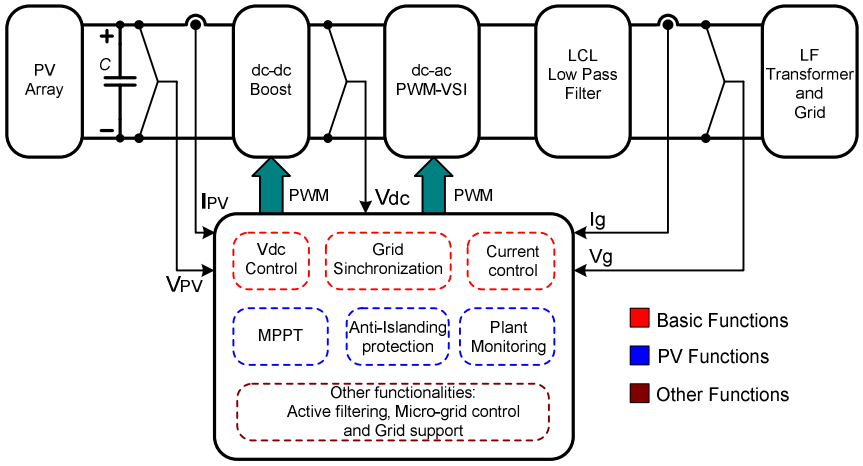


Figure 1.2. General layout of a PV system connected to the electrical grid.

1.5.2. PV inverters classification

There are different power converters topologies for PV systems, as it is reported in [1.4]-[1.5], but within all this variety, it is possible to classify them in two main groups. In one side there are topologies which use a galvanic isolation (transformer) either in the AC side (Low-Frequency) or in the DC side (High-Frequency) and, on the other side, those that do not use transformer (transformerless). In general power converters for PV systems can be classified as show in Figure 1.3.

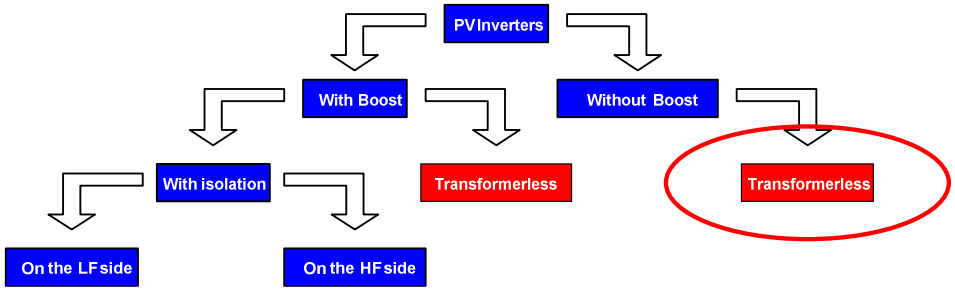


Figure 1.3. General classification of the PV inverters.

Another way to classify PV inverters can be performed considering the PV power plant configuration and the power rate. According to these criteria power plants can be classified as indicated in the following:

- *Centralized PV inverters:* This kind of inverters links a large number of PV modules to the grid. The PV modules are connected in series, called *strings* and then connected in parallel through string diodes in order to generate enough DC voltage to inject current to the electrical grid. The drawbacks of this configuration are the long DC cables between the inverter and PV panels, the mismatch losses in the panels and the losses generated by the string diodes [1.4].

- *Modularized inverters*: The modularized inverters can be connected with one or several PV modules with a total power below 500W. In this case the PV array voltage is around 30-150 V [1.6]. According with this, it is require to step-up the DC input voltage, as a consequence, a system with several stages can be implemented, including topologies with transformer.

- *String PV inverters*: In order to obtain a better performance in a PV system, a new kind of PV plant was proposed. String PV inverters get the best of modularized inverters and centralized inverters. Several PV panels can be set in series reaching DC voltage around 150 to 450 V with power level around 2 kW, a better power range regarding to the above concepts [1.6]. With this power rating it is easy to reduce the cost and increase the efficiency.

- *Multi-string PV inverters:* With the need of reducing costs, came up a new approach to configure a PV plant. In this case the idea is to connect in parallel some PV strings with its own MPPT control (boost converter) and then, with a DC bus, link them to the electrical grid with a PWM inverter, which includes all supervisory and protections functions.

1.5.3. PV Inverters with transformer on the AC side (LF)

The simplest scheme used in the energy conversion in a PV system is shown in Figure 1.4. This topology use only one conversion stage and a LF transformer. The PV panels deliver a DC voltage to the inverter, with an adequate modulation scheme for S1, S2, S3 and S4 it is possible to obtain a square waveform (with sinusoidal component) at the output of the inverter. The high inductance of the transformer can reduce harmonic distortion meanwhile the transformer provides galvanic isolation. In spite of these good characteristics, the operation frequency of this transformer is around 50-60 Hz, therefore this transformer will be big, bulky and expensive. In addition, another drawback of this topology is that the DC input voltage should be high enough to reach the voltage level of the electrical grid without using a very high turn ratio in the transformer, which would result in very high currents and losses [1.7].

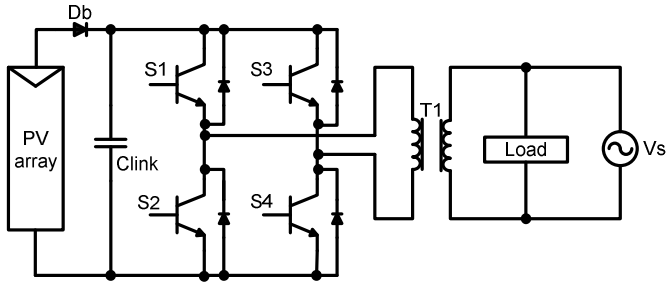


Figure 1.4. Full-bridge PV inverter with low frequency transformer.

In order to solve the problem of the low DC voltage at the input, some topologies with DC-DC boost converter have been proposed. This DC-DC converter boost the DC input voltage and follows the maximum power point of the PV panel or array. The Figure 1.5 shows the scheme of this converter.

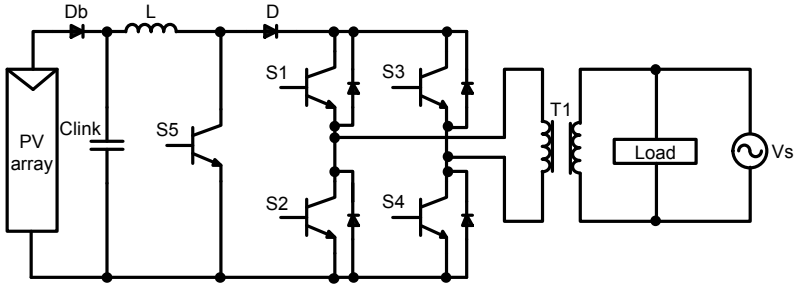


Figure 1.5. Full-bridge PV inverter with low-frequency transformer and DC-DC boost converter.

In the converter structure of Figure 1.5, there are more components than in the first topology, as a consequence this topology become more expensive and the control could be more complex. In spite of these drawbacks this inverter is on the market with efficiencies between 93% and 95% [1.7].

The low-frequency transformer isolates the circuitry from the grid and minimizes the EMC (Electromagnetic Compatibility) problems even when an asymmetric Pulse Width Modulation (PWM) pattern is used. Moreover, the LF transformer has losses in the core reducing the total efficiency of the system. In general, the LF transformer is a big drawback in PV systems connected to the electrical grid.

1.5.4. PV Inverters with transformer on the DC side (HF)

In order to overcome the associated problem with the LF transformer a new configuration was proposed [1.8]. Figure 1.6 shows a full-bridge inverter with a high-frequency

transformer. This converter has some stages which consist of a high frequency inverter, high-frequency transformer, rectifier, filter and finally a low frequency inverter.

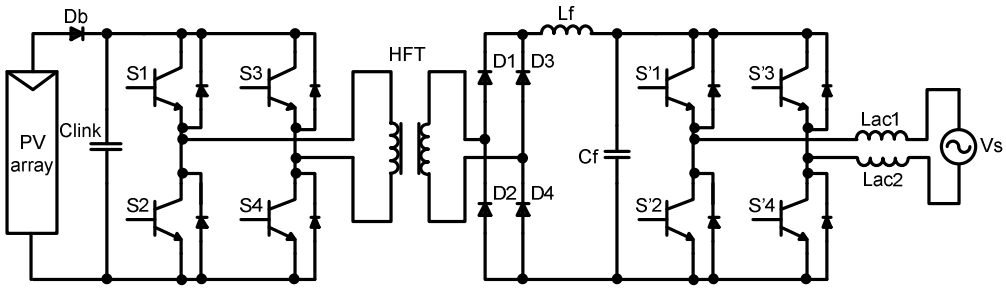


Figure 1.6. Full-bridge PV inverter with high-frequency transformer.

The PV panels are still isolated from the grid and the first inverter delivers a high frequency square waveform to the high-frequency transformer. Therefore, the transformer size is reduced. Maximum efficiency of 95% is achievable [1.7]. As can be seen in Figure 1.6, there are eight switches which should be controlled, therefore the control becomes more complex compared to other topologies. An alternative to generate the high frequency square waveform to feed the high-frequency transformer is shown in Figure 1.7.

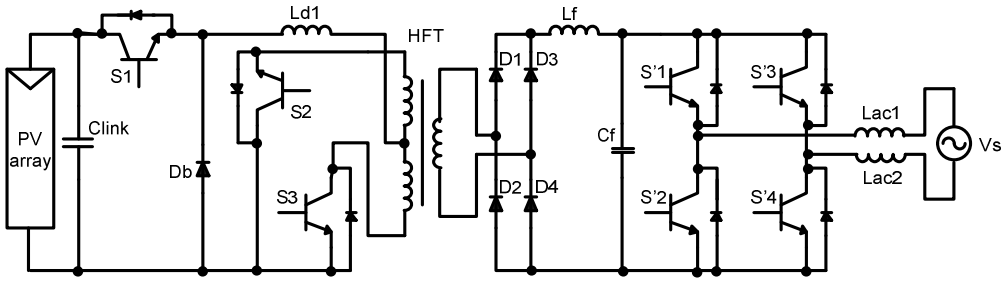


Figure 1.7. Full-bridge PV inverter with push-pull converter and high-frequency transformer.

As can be seen in the figure above, the total amount of switches is reduced to seven but the losses produced by the transformer still affect the total efficiency. The push-pull converter is used to boost the input voltage in order to reduce the switching losses on the high voltage side. As in the previous case, both converters in series reduce the total efficiency and the control is still complex.

1.5.5. PV Inverters without transformer (transformerless)

According with the previous section, the transformer in the PV systems has some critical drawbacks; size, weight, high losses, expensive, etc. In order to avoid the use of transformers, in the last years, some topologies which do not use transformer have been

developed. When a transformer is not used, the inverter is connected directly to the electrical grid through a LCL filter; therefore there is not galvanic isolation between them.

PV panels are typically manufactured in layers involving glass, silicon semiconductor and a backplane. The junction of these layers is covered by a grounded metallic frame. A PV inverter typically operates with a switching frequency in the range of kHz (2-15 kHz depending on the power level), this high frequency can generate leakage currents which flow through the frame and the stray capacitances. These stray capacitances are established between the ground and the metallic frame, in Figure 1.8 the stray capacitances connected to the positive and negative terminals are modeled in the diagram. The stray capacitances are finally an element of a closed circuit which consists on the PV panels, the AC filter elements and the grid impedance. These capacitances provide a full path for the current to flow through ground. The value of these capacitances depends on the weather conditions, PV topology, PWM pattern, the material used in the metallic frame and the values in the passive elements of the converters. Some experiments have been done in order to determine approximately the value of these parasitic elements (under certain conditions) which has been concluded to be around 100nF/kW according with [1.9].

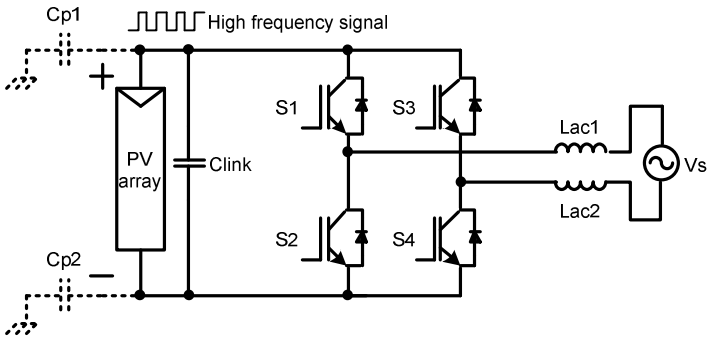


Figure 1.8. Leakage capacitances in a PV system.

The flow of leakage currents through the stray capacitances is not a problem just from the electrical point of view, but it is also a serious problem related to the safeness of the workers. In this sense some standards have been established in Germany by DIN (Deutsches Institut für Normung e.V.). In this standard it is established that the maximum leakage current should be 300 mA [1.10]. Considering this standard, some topologies have been developed to fulfill its requirements. In this section some of the most important transformerless PV inverters able to avoid the appearance of these currents will be explained.

Transformerless single-phase PV inverters

In the case of the single-phase PV systems, one of the most popular topologies is based on the basic full-bridge Inverter and is named H5 [1.11]. In Figure 1.9 the H5 structure is shown.

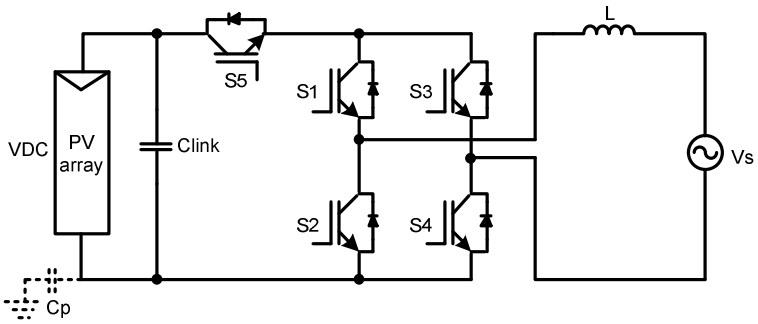


Figure 1.9. Single-phase H5 PV topology (SMA technologies).

The PWM pattern for this topology can be design in order to get constant CMV. The PWM pattern in this case introduces the null state through S5. During the positive half cycle, when switches S5, S1 and S4 are ON and S2 and S3 are OFF, an active state is applied to the output. In this state, the current in the link inductor increases, Figure 1.10 a). In order to apply a null state at the output, S5 and S4 goes OFF and S2 and S3 remain OFF. In this case, the current decreases and flows through S1 and the diode of S4. This means that the S5 and S4 are switching at high frequency, Figure 1.10 b).

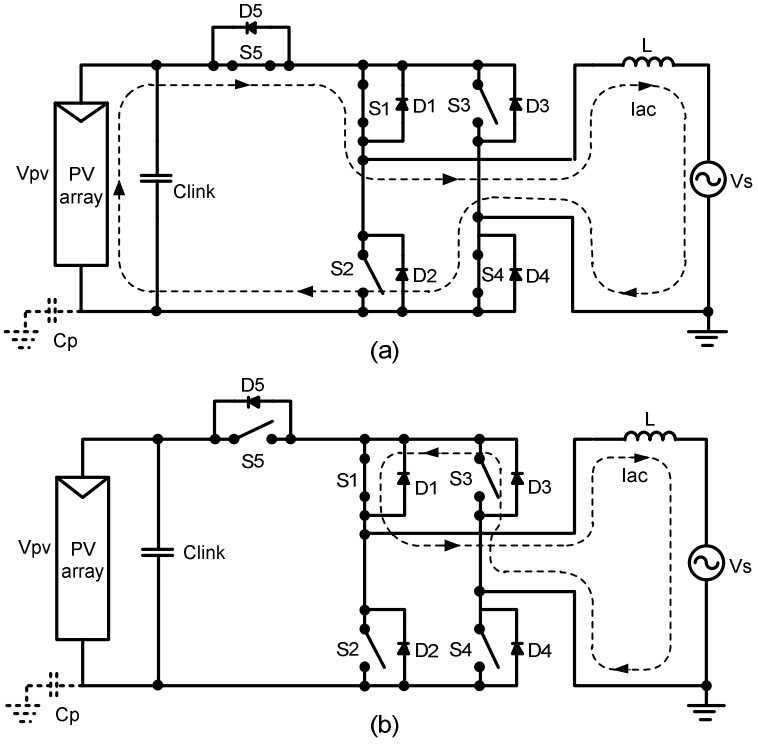


Figure 1.10. Modulation states during positive half cycle; (a) Active state, (b) Null state.

On the other hand, during negative half cycle when switches S5, S3 and S2 are ON an active state is applied to the load. This means that the current in the link inductor increases, Figure 1.11 a). The zero voltage state can be applied if S5 and S2 go OFF. In this case, the current decreases and flows through S3 and free-wheeling diode of S1. In this half cycle S5 and S2 are switching at high frequency, this state is shown in Figure 1.11 b).

The pulse width modulation explained above, shows that the 5th switch allows to isolate the PV panels from the electrical grid during zero voltages states and as a consequence constant CMV on the PV converter is obtained and the leakage ground current does not flow through the stray capacitances. As an additional characteristic, the 5th switch avoids reactive power exchange between the C_{link} and the L filter, reducing the losses in the semiconductors and reactive components.

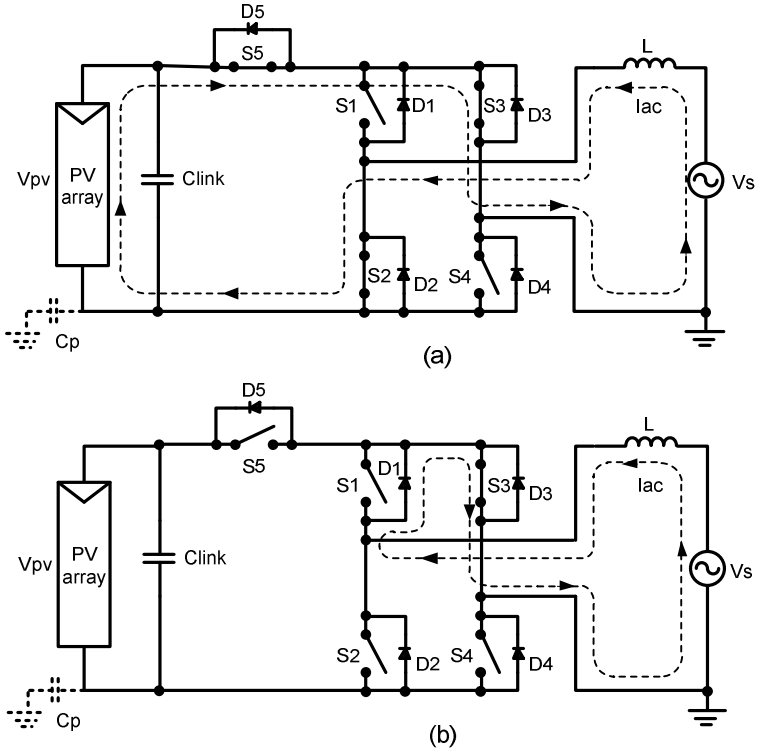


Figure 1.11. Modulation states during negative half cycle; (a) Active state, (b) Null state.

H5 is very suitable for transformerless PV applications due to its good characteristics regarding to EMI (Electromagnetic Interference) components at PV terminals and high efficiency. Actually, H5 is currently commercialized by SMA in the series SunnyBoy 4000/5000 TL with European efficiency higher than 97.7% and maximum efficiency of 98%.

Another transformerless PV topology which is widely used in the PV market is the HERIC (High Efficiency Reliable Inverter Concept) topology. This topology is also based in the conventional single-phase full-bridge inverter and was patented by Sunways in 2006. In this case, this topology generates the null state at the AC side by using extra switches, which allows set all the switches of the full-bridge in OFF during the null state. In this way the PV panels are isolated from the AC side. The scheme of this structure is depicted in Figure 1.12.

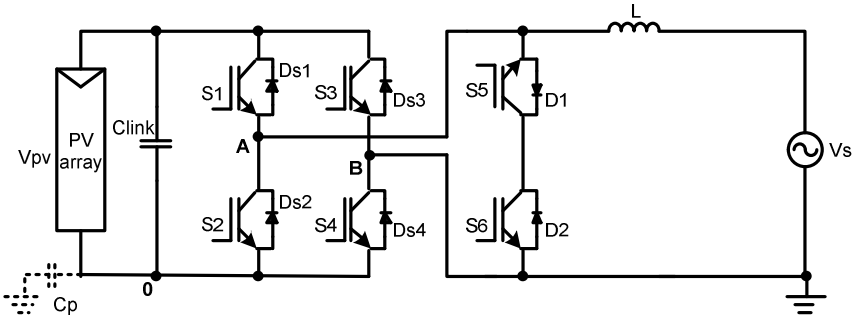


Figure 1.12. Single-phase transformerless HERIC topology [1.12].

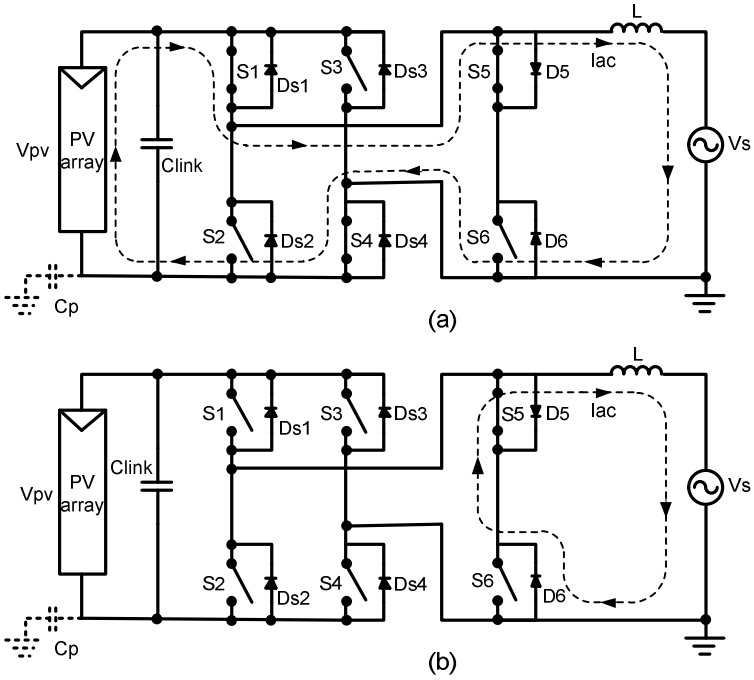


Figure 1.13. Modulation states during positive half cycle; (a) Active state, (b) Null state.

As it can be appreciated in Figure 1.12, there are two additional switches with the collector connected at the same point, forming a bidirectional switch. In Figure 1.13 a), during the positive half cycle, when S1, S4 and S5 are ON (S2, S3 and S6 are OFF), an active state is applied to the output. In this case, the output current increases. In order to apply a null state, S1 and S4 go OFF while S5 remains ON (S2, S3 and S6 are kept OFF). In this case, the output current decreases and flows through the S5 and D2 (free-wheeling situation). This state is shown in Figure 1.13 b). During all positive half cycle S1 and S4 are switched at switching frequency while S5 is switched at the line frequency. On the other hand, during the negative half cycle, when S2, S3 and S6 are ON (S1, S4 and S5 are turned OFF), an active state is applied and then the output current increases, see Figure 1.14 a). The null state is applied by means of turning OFF S2 and S3 while S1, S4 and S5 are kept OFF and then the output current flows through the S6 and D1. In this case, the current decreases. This state is shown in Figure 1.14 b). As in the case of the positive half cycle, S2 and S3 are switched at the switching frequency and S6 is switched at the line frequency.

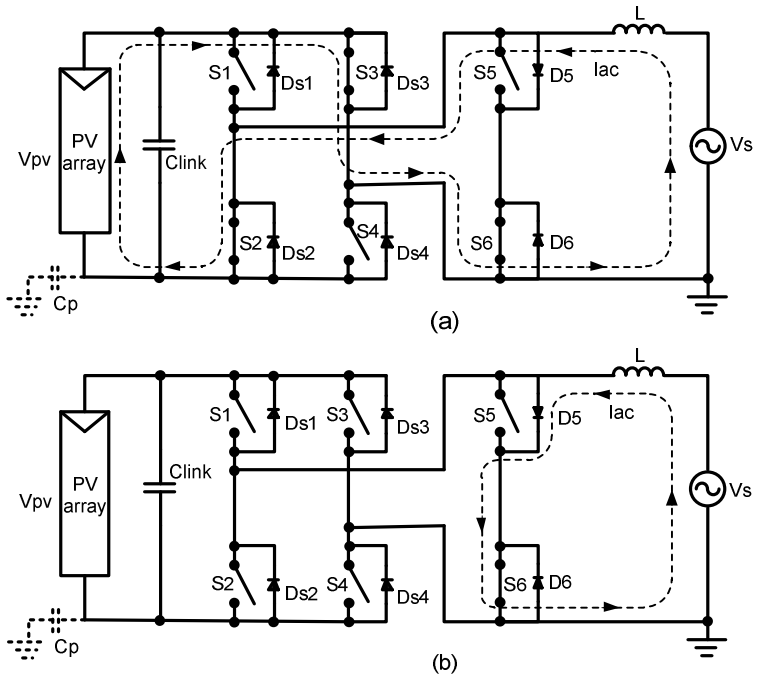


Figure 1.14. Modulation states during negative half cycle; (a) Active state, (b) Null state.

From the modulation explained above, it is possible to see that the two additional switches can avoid the reactive power exchange between the L filter and the C_{link} capacitance. Moreover these two switches operate as a bidirectional switch and provide a path during zero voltage states. With this solution the voltage across the filter is unipolar, yielding in lower core losses. As a result, considering these two important characteristics, the efficiency in this

topology can be high, around 97%. Moreover, no common mode switching frequency components can appear over the PV panel terminals, therefore there are not leakage ground currents flowing through the stray capacitances.

Another promising topology in single-phase PV systems for transformerless applications is the NPC (Neutral Point Clamped) topology. This topology consists in a leg with four transistors in series as shown in Figure 1.15 [1.13].

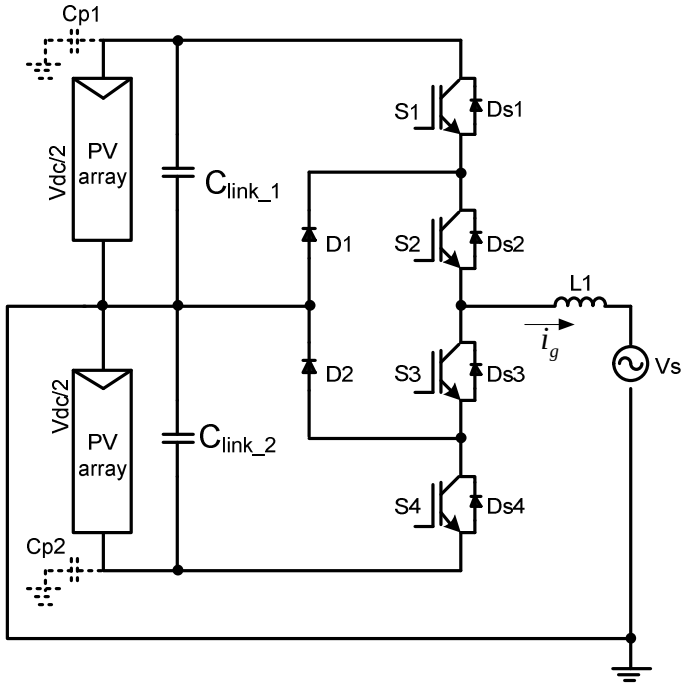


Figure 1.15. The NPC topology for transformerless single-phase PV applications.

The NPC topology is a structure that consists in four switches connected in series which are modulated in order to obtain an AC waveform at the output. This topology is suitable for PV transformerless systems because there are not voltage fluctuations on the DC side since the PV panels are ground clamped. The null state is achieved by connecting (clamping) the output to the grounded middle point of the DC bus using D1 and D2, depending on the sign of the output current.

During the positive half cycle, S2 remains ON while S1 and S3 are switched at switching frequency in a complementary way in order to generate the active and null states. When S1 is ON and S3 is OFF, an active state is applied to the output and the current in the link inductance increases and flows through S1 and S2 toward the output, as is shown in Figure 1.16 a). On the other hand, when S1 goes OFF and S3 comes ON a null state is applied to the output and the output current decreases while flows through S2 and D1, see Figure 1.16 b).

In negative half cycle, shown in Figure 1.17, S3 remains ON along the whole negative half cycle, while S2 and S4 are switched at the switching frequency in a complementary way to provide the active and null states to the output. The active state is applied when S4 comes ON and S2 goes OFF. In this case, the current in the link inductance increases and flows though the switches S3 and S4 see Figure 1.17 a). The null state is applied when S4 goes OFF and S2 comes ON, dealing in a decrease of the output current, which flows through D2 and S3. This state is depicted in Figure 1.17 b).

The NPC topology has the advantage that the voltage across the output filter is unipolar, thus it is possible to obtain low core losses. Moreover, with this configuration there is not power exchange between the C_{link} and L filter at the output during null states, so the efficiency can be high, around 98%. Another important thing that contributes to improve the efficiency is that S2 and S3 are switched at the grid frequency. Finally, in order to increase the efficiency even more, the voltage rating of the switches S1 and S4 can be reduce to $V_{dc}/4$, leading in a switching losses reduction. The most remarkable problems with this topology lays in the fact that there are two additional diodes, requires double voltage input in comparison with the conventional full-bridge inverter and unbalance switching losses may appear because of the different switching frequency in S1 and S4 (high frequency) and S2 and S3 (grid frequency). It is important to mention that due to the way in which the null states are generated there are no voltage fluctuations on the PV terminals and, as a consequence, no leakage current appears [1.14].

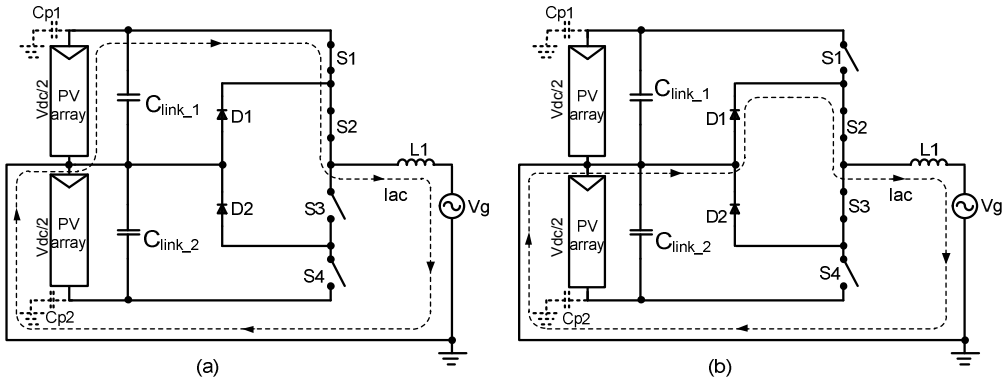


Figure 1.16. Modulation states in the NPC topology during positive half cycle; (a) Active state, (b) Null state.

This inverter is currently used by *Danfoss Solar inverters* in the *TripleLynx* series (three-phase 10/12.5/15 kW), and it is commercialized with an European Efficiency around 97% and maximum efficiency around 98% [1.15].

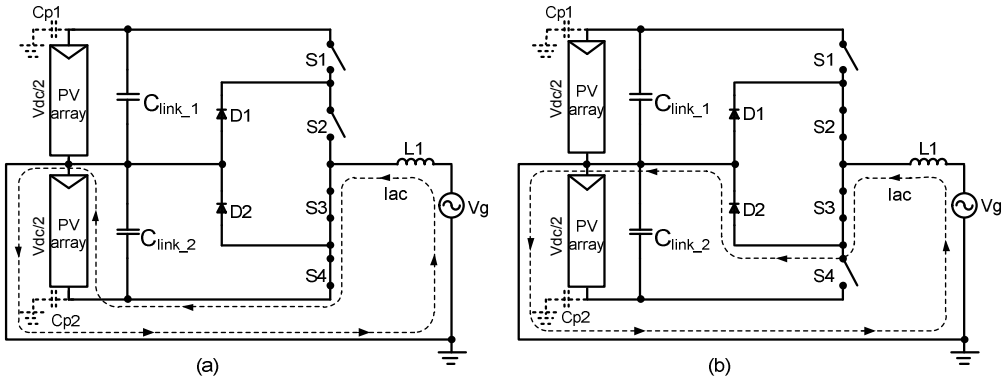


Figure 1.17. Modulation states in the NPC topology during negative half cycle; (a) Active state, (b) Null state.

Finally, the last topology included in this summary related to the single-phase transformerless topologies for PV applications is also based on the full-bridge inverter. This topology is a modified H5 topology, the main difference is that in this topology the AC side is not floating, but it is clamped at the middle point of the dc-link capacitors. The scheme of this structure is shown in Figure 1.18 [1.16].

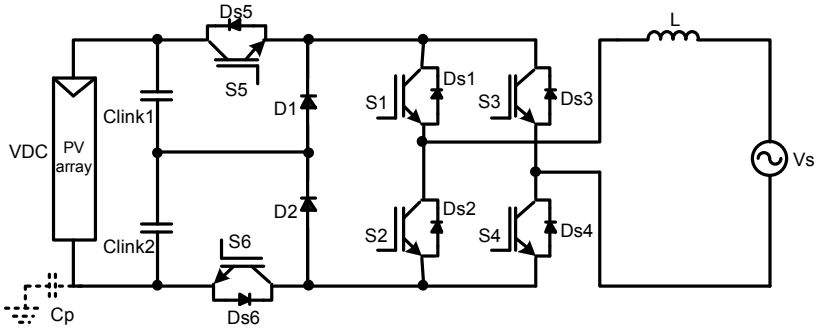


Figure 1.18. Full-bridge inverter with DC by-pass.

In this case, the main idea is to disconnect the DC bus from the grid during null states of the converter, as in H5. The way in which this topology is modulated is as follow: during the whole positive half cycle S1 and S4 are ON while S5 and S6 are switched at the switching frequency and S2 and S3 are switched at the same time that S5 and S6 but in a complementary way. Thus, when an active state is applied S1, S4, S5 and S6 are ON and S2 and S3 are OFF, given rise to an increase in the output current, which flows through S1, S4, S5 and S6, Figure 1.19 a). On the other hand, when a null state is applied, S5 and S6 comes OFF while S2 and S3 go ON (S1 and S4 remain ON). The result is that the output current decreases and gets divided in two paths: one through S1 and Ds3 and another one through S4 and Ds2, as a consequence, S2 and S3 are switched with zero current, therefore there are not switching losses in these two switches, see Figure 1.19 b).

In the case of the negative half cycle, S2 and S3 are ON during whole half cycle and S5 and S6 are operating at the switching frequency, as S1 and S4, but in complementary way. When S2, S3, S5 and S6 are ON and S1 and S4 are OFF, an active state is applied to the output, Figure 1.20 a), on the contrary, a null state is applied when S5 and S6 comes OFF and S1 and S4 comes ON. In this case, the current is divided into two paths: one through the S3 and Ds1 and another one through the S2 and Ds4. Thus, as in the previous case S1 and S4 are switched without current, see Figure 1.20 b).

As can be seen in the modulation sequence, the zero output voltage is achieved by clamping the inverter in the middle point of the DC link. This zero voltage situation permits to get unipolar voltage across the output filter, and therefore there is not reactive power exchange between the DC link and the AC filter. Another interesting characteristic is that the rating voltage for the switches S5 and S6 is the half of the DC input voltage because the diodes D1 and D2 fix the voltage to $V_{pv}/2$. It should also mentioned that the voltage across the C_p, has only the grid frequency component thus the leakage ground current should be very low.

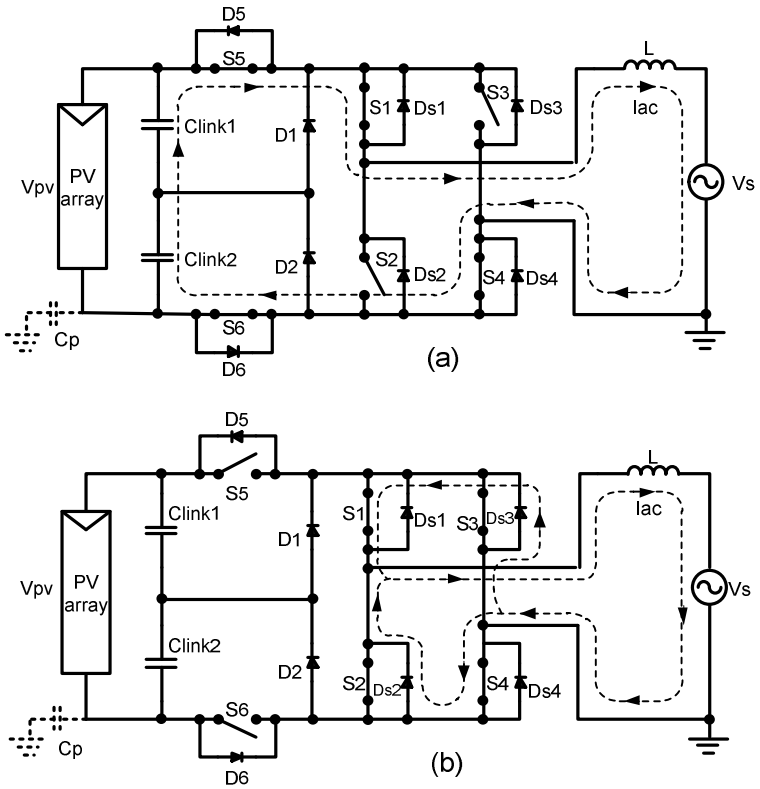


Figure 1.19. Modulation states in the full-bridge inverter with DC bypass during the positive half cycle; (a) Active state and (b) Null state.

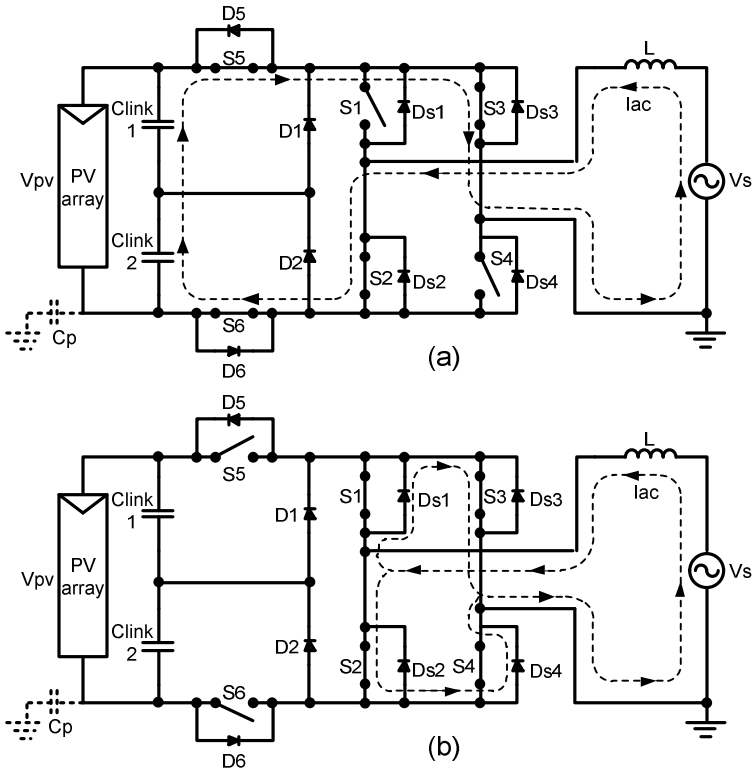


Figure 1.20. Modulation states in the full-bridge inverter with DC by-pass during the negative half cycle; (a) Active state, (b) Null state.

The topology described above is commercially available (Ingeteam) and it is used in transformerless PV applications getting an european efficiency around 95.1% and a maximum efficiency around 96.5% [1.17].

Three-Phase Transformerless Inverters

The conventional three-phase full-bridge inverter is the most widely used inverter in the general PV applications with galvanic isolation. The Figure 1.21 shows this topology with no low-frequency transformer. This converter can be considered as a first approach in order to look for a solution in which the heavy, bulky and expensive transformer can be avoided.

In the inverter shown in Figure 1.21, there are more switching states than in any of the previously commented single-phase system. In general eight states vectors are applied to the output along the grid period, six active vectors and two null vectors. The performance of this inverter has been evaluated in different applications [1.18]-[1.20]. As aforementioned, PV system can be designed using galvanic isolation or connecting the system directly to the electrical grid. This three-phase full-bridge inverter was evaluated in [1.5] for both cases.

The results clearly show that this system is no suitable for transformerless applications. In the case of [1.5], a specific modulation scheme was used. In order to understand how the modulation scheme can affect the CMV behaviour, some PWM (Pulse Width Modulation) techniques based on space vector modulation (SVM) have been proposed and analyzed in [1.21]-[1.22].

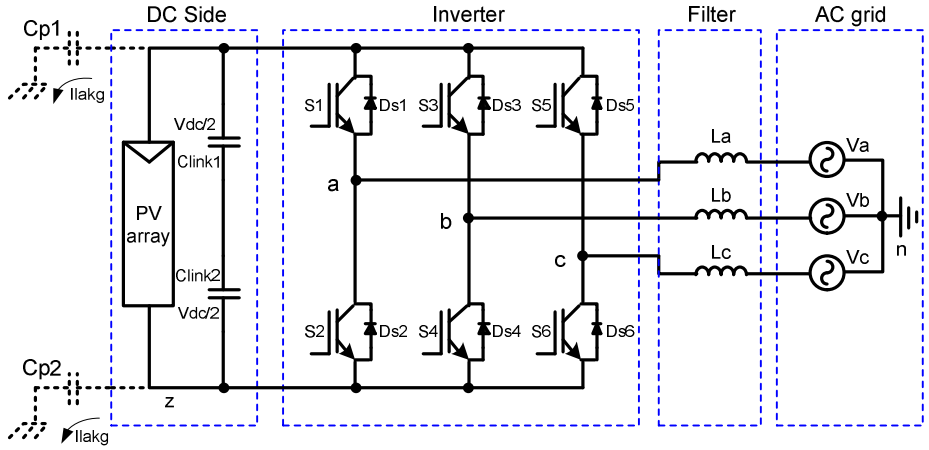


Figure 1.21. Three-phase two-level transformerless inverter.

In the case of the topology shown in Figure 1.21, which is a conventional two-level three-phase inverter, it is possible to obtain eight vectors by combining the state of the six switches, begin six of them the active vectors and two null vectors, as mentioned before. As shown in [1.23], the three-phase system can be represented in the alpha-beta plane. Therefore, the eight vectors generated by this inverter can be represented in the same way, as show in Figure 1.22.

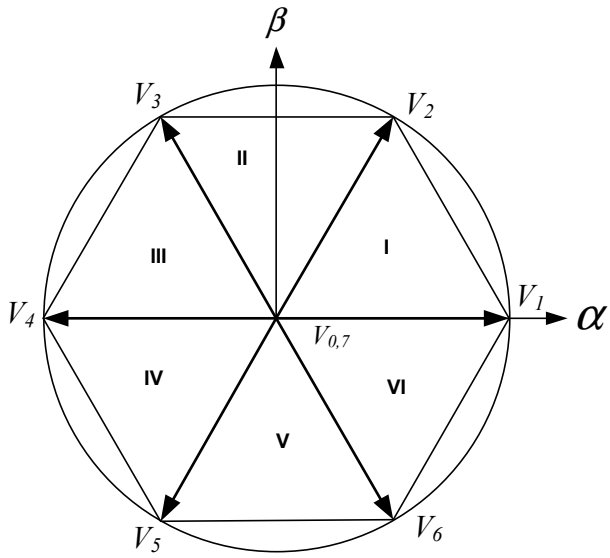
In the standard three-phase two-level inverter shown in Figure 1.21, the output CMV is defined as the average of the sum of the output voltages. In this case, the CMV, which is actually the potential voltage between the star neutral point in the load "n" and the "z" common reference for the three outputs, can be expressed by the equation (1.1)[1.24].

$$V_{nz} = \frac{V_{az} + V_{bz} + V_{cz}}{3}. \tag{1.1}$$

In this way taking into account the equation (1.1), it is possible to obtain the CMV generated by each space vector of Figure 1.22. Table 1.1 shows the CMV generated by the eight space vectors.

As Table 1.1 shows, the CMV is always jumping between 0, 1/3 Vdc, 2/3 Vdc and Vdc, this means that ground leakage currents can appear at the PV terminals, since this is the

"floting voltage" of the point "z" respect to the neutral point "n", which is usually connected to the earth potential. In order to attempt to overcome this problem, some SVPWM (Spacer Vector Pulse Width Modulation) strategies have been investigated and analyzed in [1.22].



Active Vectors	*Null Vectors*
(0,0,0)V1	*(0,0,0)V0*
(1,1,0)V2	*(1,1,1)V7*
(0,1,0)V3	
(0,1,1)V4	
(0,0,1)V5	
(1,0,1)V6	

Figure 1.22. General SVM for three-phase inverters.

Vector	*CMV*
V_0 (0,0,0)	0
V_1 (1,0,0)	1/3 Vdc
V_2 (1,1,0)	2/3 Vdc
V_3 (0,1,0)	1/3 Vdc
V_4 (0,1,1)	2/3 Vdc
V_5 (0,0,1)	1/3 Vdc
V_6 (1,0,1)	2/3 Vdc
V_7 (1,1,1)	+Vdc

Table 1.1 CMV generated by two-level FB inverter.

The main idea in [1.22] is to evaluate the performance of this three-phase two-level converter under different modulation strategies based on SVPWM. Some of these strategies have good performance regarding the CMV but on the other side, some problems regarding voltage linearity, harmonic distortion factor and simultaneous switching may appear. Some of these PWM techniques are shown in Figure 1.23.

As a result of the evaluation in [1.22], it is possible to mention some well-defined characteristics of these strategies. For instance, in the case of the Active Zero State Pulse Width Modulation 1 (AZSPWM1) and AZPWM2 the CMV magnitude is reduced but the CMV frequency is high and also presents a high harmonic distortion factor in the output voltages. The Remote State Pulse Width Modulation (RSPWM) has low CMV magnitude and the frequency is also low (around three times the grid frequency), but the modulation index is very low and output harmonic distortion is very high. In order to attempt to solve the CMV problem in the three-phase power converters, another idea was proposed in [1.25]. The proposed converter is shown in Figure 1.24.

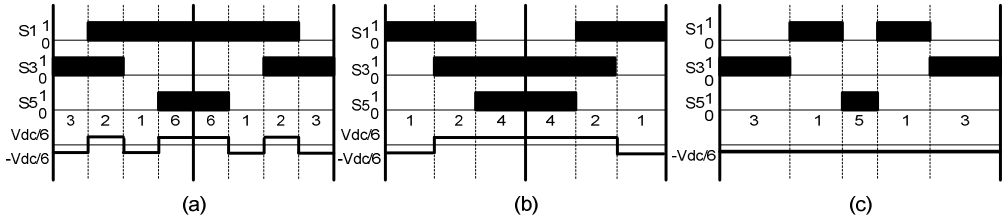


Figure 1.23. Reduced CMV space vector modulations, (a) AZSPWM1, (b) AZSPWM2, (c) RSPWM3 [1.22].

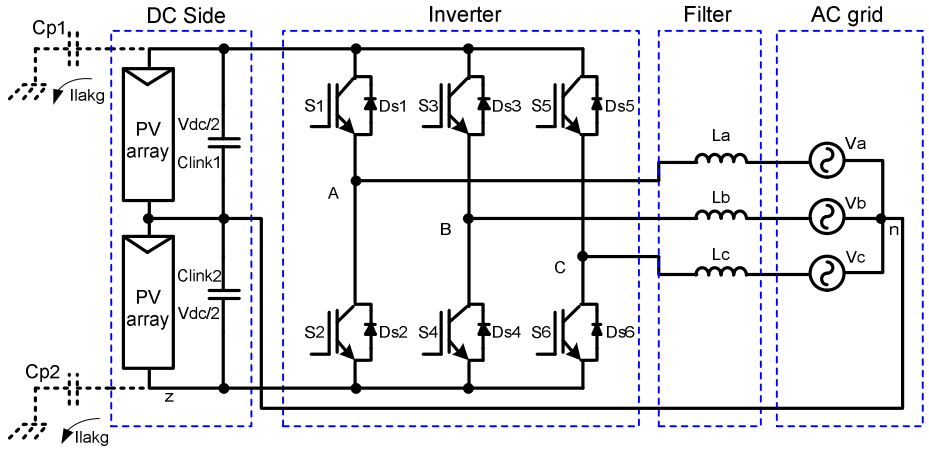


Figure 1.24. Three-phase two-level converter with the neutral point clamped to the middle point of the DC bus.

The difference regarding to the conventional inverter is that the neutral point of the load is connected to the middle neutral point in the DC bus. Thus this topology is equivalent to three independent single-phase half-bridge inverters. With this new characteristic, it is possible to reduce the CMV by using a specific modulation technique. When interleaved triangular signals are used for the PWM, the switching harmonics in the grid current cancels out the neutral current [1.25]. Using this modulation strategy, the CMV for the three individual phases can be almost constant. As a consequence the fluctuations on the DC bus terminals

are very low regarding to the conventional full-bridge three-phase inverter because the neutral point is connected to the middle point of the DC bus holding this voltage at zero volts [1.5]. In this way, the leakage current is significantly reduced by this inverter configuration. In addition, this inverter has an advantage since no additional semiconductors are needed and, as a consequence, the CMV can be reduced without any additional cost. The main drawback of this topology is that the SVM algorithm can not be used. Therefore, the use of the DC voltage is lower than in the SVM strategy.

Another structure which is widely used in three-phase PV systems is the three-phase three-level Neutral Point Clamped converter. This inverter is dated back to early 1980s when first three-level diode clamped inverter was developed by Nabae, Takahashi and Akagi [1.26]. After that breakthrough, there appeared new topologies with a higher number of levels and also at the beginning of 1980s first modulation techniques were well clarified. Although, up to the present, a lot of different topologies with a different number of levels are in use, three-level inverter in NPC configuration is the most often applied on the market [1.27], the topology is shown in Figure 1.25.

One of the most important advantages of this converter regarding to the conventional two-level inverter is that the efficiency is much better due to the reduction of the blocking voltage in each IGBT. This voltage reduction is due to the series connection of the switches in each leg. Additionally, each phase has more than two voltage levels, thereby having a lower harmonic distortion. Another important characteristic is that due to the three voltage level at the output, the filter size is smaller than in the conventional two-level inverter case because of the lower dv/dt.

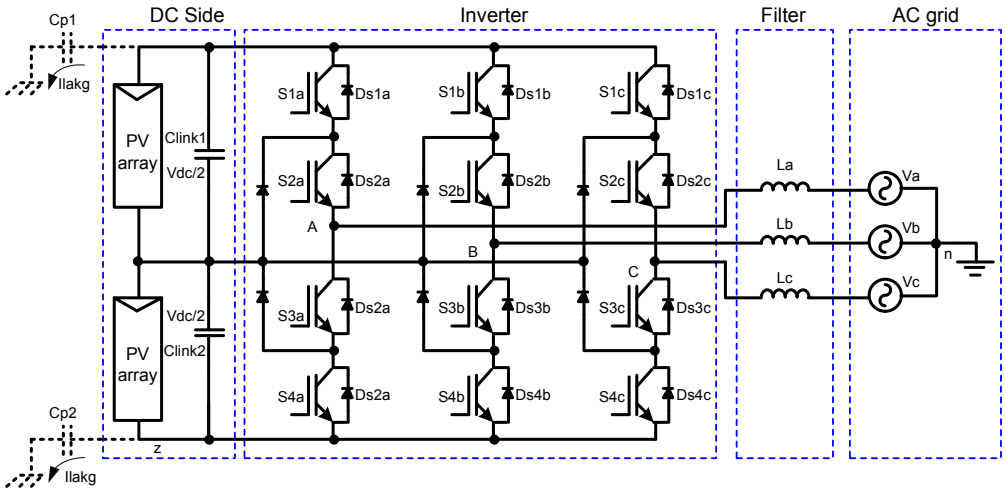


Figure 1.25. Three-phase three-level NPC converter.

The use of this topology in three-phase transformerless PV systems is feasible thanks to the small voltage ripple which appears at the PV terminals, thus the leakage ground current

through the parasitic capacitance at PV terminals (*Cp1* and *Cp2* in the case of Figure 1.25) is very low [1.5].

One of the most remarkable drawbacks of this topology is that unbalance voltage can appear in the DC bus capacitors. If any current is injected to the neutral point (middle point between *Clink1* and *Clink2*) a capacitor will be charged and the other will be discharged. Thus, the voltage in the middle point will be different of zero and its value will depend on the current value and direction. This means that the voltage over the terminals in *Clink1* and *Clink2* will be different. As a consequence the voltage applied to the output would become asymmetric [1.28].

The unbalance problem is not only caused by the current in the neutral point but also by the unequal parameters of the DC link capacitors, minor failures of the DC link capacitors, unequal parameters on the switching devices and the unbalance on the non-linear loads [1.29]. The unbalance problem should be mitigated, otherwise the switching devices can suffer premature failures, the Total Harmonic Distortion (THD) at the output would increase and the maximum modulation ratio will be limited by the terminal with the lower voltage. In order to solve the unbalance problem some considerations must be taken into account during the design of the modulation scheme and control system [1.29]. Another disadvantage that should be taken into account in this topology is that there is a major number of switches and diodes (six switches and four additional diodes), this increase the cost of the whole converter.

In order to mitigate the effects of the CMV on the whole system, some PWM techniques have been proposed in the literature [1.30]. In this sense, there are more possible vector combinations to reduce the magnitude and frequency of the CMV. It is well know that all the vectors that can be generated by the NPC converter can be represented in a g-h plane as shown in Figure 1.26 [1.30]. Figure 1.26 shows that there are 27 switching states and some of them are redundant for a specific vector reference position. It should be noted that this redundancies appear at the inner hexagon and they can provide power either from one of the two DC buses. This redundancy provides some degrees of freedom in the pulse width modulation process design. Using equation (1.1) and taking into account Figure 1.26 it is possible to calculate the CMV generated by each state. Table 1.2 shows the CMV generated by each vector in Figure 1.26.

According to [1.30] and Table 1.2, there are seven states in which the CMV is zero. If only these states were used and all the remaining states were excluded from the modulation strategy, no CMV would be generated. Clearly, the peak attainable voltage magnitude would be limited to the circle inscribed in the hexagon created by these six zero CMV vectors.

The bus utilization achieved by this modulation strategy can be geometrically shown to be 86.6% of the utilization of the nearest three vectors modulator (reference vector is synthesize using the nearest three vectors, NTV). Additionally it can be noted that the state selection is no longer carried out on an adjacent state basis, which leads to higher ripple and harmonic distortion in the output voltage and current. As the CMV is directly proportional to the

neutral point voltage, any current harmonics injected into the neutral point will be observed in the output CMV.

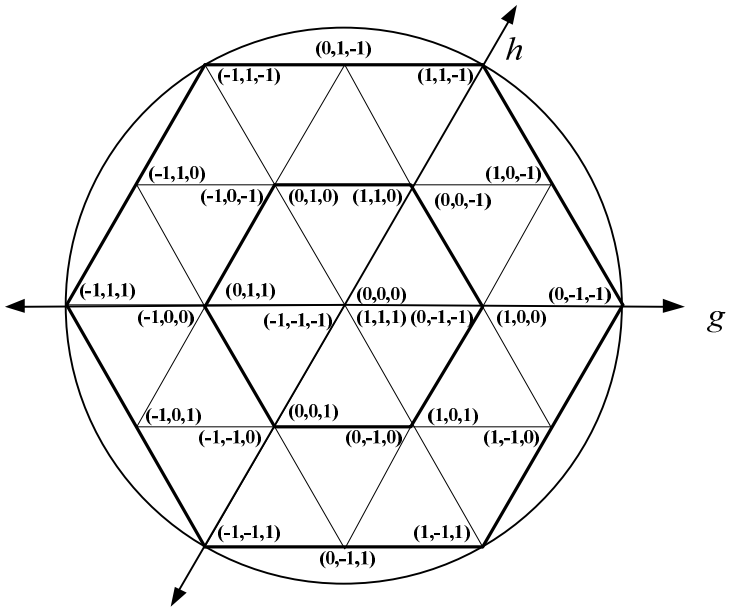


Figure 1.26. Switching states for the three-level NPC converter.

Finally, in order to complete the review of the three-phase transformerless converters, another topology based on the NPC converter will be briefly explained. This topology is a multilevel converter which use an active clamped instead a diode clamped circuit. This topology was developed by Brückner and Bernet in 2001 [1.31]. The topology is depicted in Figure 1.27 [1.32].

The additional switches of this topology regarding to the conventional NPC converter, permit to improve the performance in the overall losses distribution and also it is possible to have better semiconductor utilization.

As in the NPC three-level inverter, there are 27 vectors available in order to set the output voltage level at +Vdc/2, -Vdc/2 or 0. The main difference in respect to the conventional NPC inverter is that the path to set the zero voltage level has more than one way. This means that there are more switching states which can provide zero voltage at the output. In the case of the converter of Figure 1.25 the utilization of the upper and lower paths is determined by the direction of the phase current. In the case of the Active Neutral Point Clamped (ANPC) converter, switches S2 and S3 are always in ON position during zero voltage state. If active NPC switches are applied by turning ON S5 and S2, the phase current can be conducted through the upper path of the neutral tap in both directions. In the same manner, by turning ON S6 and S3, the phase current can be draw through the lower path of the neutral tap in both directions. Of course, all four switches S5, S3, S6 and S2 can be turned ON at the same

time. In such case the current distribution between the upper and the lower NPC path is determined by the variation of the ON-state characteristics of the devices used.

State	CM Voltage	CM Voltage Vdc~1pu V_0 ~0
(-1,-1,-1)	$-V_{DC}/2$	-1/2
(-1,-1,0)	$-V_{DC}/3 + V_0/3$	-1/3
(-1,-1,1)	$-V_{DC}/6$	-1/6
(-1,0,-1)	$-V_{DC}/3 + V_0/3$	-1/3
(-1,0,0)	$-V_{DC}/6 + 2V_0/3$	-1/6
(-1,0,1)	$V_0/3$	**0**
(-1,1,-1)	$-V_{DC}/6$	-1/6
(-1,1,0)	$V_0/3$	**0**
(-1,1,1)	$-V_{DC}/6$	+1/6
(0,-1,-1)	$-V_{DC}/3 + V_0/3$	-1/3
(0,-1,0)	$-V_{DC}/6 + 2V_0/3$	-1/6
(0,-1,1)	$V_0/3$	**0**
(0,0,-1)	$-V_{DC}/6 + 2V_0/3$	-1/6
(0,0,0)	V_0	**0**
(0,0,1)	$V_{DC}/6 + 2V_0/3$	+1/6
(0,1,-1)	$V_0/3$	**0**
(0,1,0)	$V_{DC}/6 + 2V_0/3$	+1/6
(0,1,1)	$V_{DC}/3 + V_0/3$	+1/3
(1,-1,-1)	$-V_{DC}/6$	-1/6
(1,-1,0)	$V_0/3$	**0**
(1,-1,1)	$V_{DC}/6$	+1/6
(1,0,-1)	$V_0/3$	**0**
(1,0,0)	$V_{DC}/6 + 2V_0/3$	+1/6
(1,0,1)	$V_{DC}/3 + V_0/3$	+1/3
(1,1,-1)	$-V_{DC}/6$	+1/6
(1,1,0)	$V_{DC}/3 + V_0/3$	+1/3
(1,1,1)	$V_{DC}/2$	+1/2

Table 1.2. Three-level states and CMV.

When +Vdc/2 is applied to the output (S1 and S2 in ON state), S6 should be turned ON to guarantee an equal voltage sharing between S3 and S4. On the other hand, when –Vdc/2 is applied to the output S5 should be turned ON in order to balance the voltage between S1 and S2. This means that the additional balancing resistors are no needed. The distribution of conduction losses during the null state can be controlled by the selection of the upper and

lower NPC path. The conduction losses in the +Vdc/2 and –Vdc/2 can not be influenced by the selection of the upper and lower NPC path [1.31].

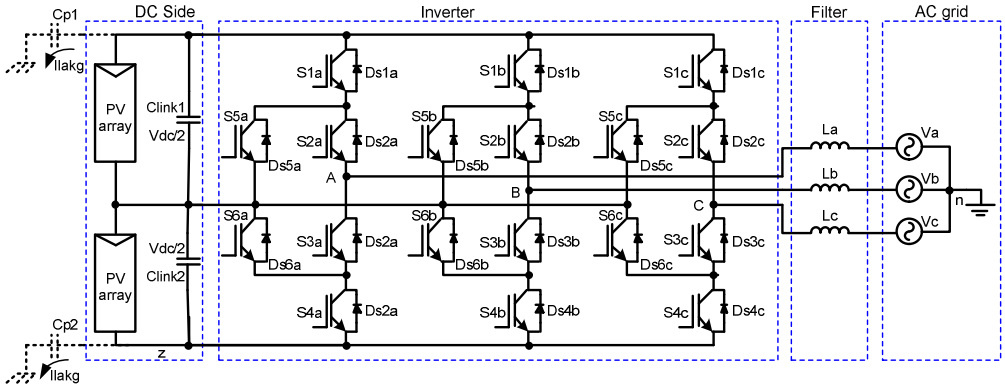


Figure 1.27. Three-phase ANPC multi-level converter.

As a short conclusion of this section, it can be said that there are some main aspects which should be overcome in any transformerless application either in single-phase or in three-phase systems connected to the electrical grid. One of these main problems is related to power losses. In this sense, the number of semiconductors has a great influence and also the way and conditions in which they are switched. So, this is an aspect that will be faced in this research work. On the other hand the problem related to the leakage ground current, which has a big influence in the personal security is strictly regulated by DIN (Deutsches Institut für Normung e.V.) standard and as a consequence this requirement should be fulfilled. In order to fulfill this standard, new structures and modulation techniques will be studied and exposed in next chapters in this thesis.

1.5.6. Current controllers for PV systems

The design of control scheme is a critical issue in any power electronic system. One of the most important tasks of a controller is to track a current reference with minimum error. To do that, it is necessary to modulate the output voltage generated by the power converter according to a given duty cycle, namely, it is necessary to generate the signals to properly command the switches to synthesize the voltage reference set by the current controller.

The control system in a PV converter connected to the electrical grid should be satisfying some special requirements in order to get a good performance when it operates in a global electrical system. Some of these functionalities to be implemented in a PV system are listed below (from Figure 1.2).

- Maximum Power Point Tracking (MPPT) control.
- Grid synchronization.
- DC voltage control.
- Current control.

- Other complementary functionalities (Grid support, micro-grid control, etc)

This section is focused on the current controllers for PV systems connected to the grid, thus some of the most popular structures and functionalities in PV systems will be shortly presented as a complementary part of this introductory section.

1.5.6.1. Proportional-Integral (PI) controllers

PI controllers are the most popular linear controllers used in PV systems. In contrast with nonlinear controllers, linear controllers have clearly separated current error compensation and voltage modulation parts; this characteristic permits to exploit the advantage of the open-loop modulators and an independent design of the overall control structure can be done. Current control is also the responsible for the dynamics of the system so its design is a critical issue. In Figure 1.28, a general scheme of the current control in the case of single-phase system is depicted.

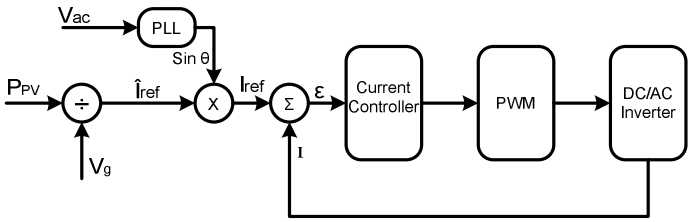


Figure 1.28. General scheme of the current controller in a single-phase PV system.

A PI controller can be used as the **current controller** block. The transfer function of the PI controller is given in equation (1.2).

$$G_{PI} = K_P + \frac{K_i}{s}. \tag{1.2}$$

The main disadvantage of the PI controller is its inability to track a sinusoidal reference without steady-state error and the poor disturbance rejection capability. In order to improve the performance regarding to the dynamic response of the PI controller a grid voltage feed-forward is used [1.33].

In the case of three-phase system a grid current control using PI controllers has been proposed in [1.34]. The scheme of this current controller is shown in Figure 1.29.

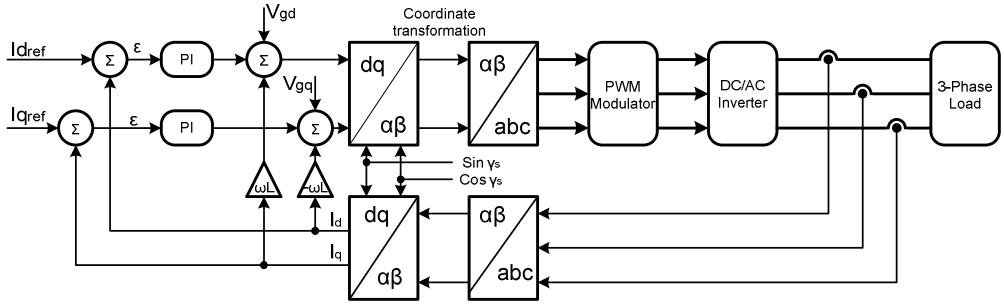


Figure 1.29. Current controller for a three-phase PV system using PI controllers in the current loop.

In three-phase systems there are a lot of applications in which ideally sinusoidal current waveform is required, because even small phase or amplitude errors cause incorrect system operation. The control system shown in Figure 1.29 has a good performance to fulfill this requirement. This current control scheme is also called "Synchronous Controller" and is based in two PI controllers for the current vector components defined in rotating synchronous coordinates d-q [1.35][1.36][1.37]. As can be seen in Figure 1.29, the inputs (i_d and i_q) of the PI controller are DC constants because of the synchronous coordinate transformations. Therefore, the PI controller is able to cancel out errors for the fundamental frequency component which is the frequency of the synchronous d-q transformations [1.38].

Even when the d-q controller works properly at the fundamental synchronous frequency with not steady state error and good dynamics response a simpler controller with not angle estimation dependency was proposed in [1.39][1.40]. This control is shortly explained in the next section.

1.5.6.2. Proportional-Resonant (PR) controllers

PR controllers are suitable to fulfill the requirements of AC current regulators (zero phase and magnitude error) and at the same time reduce the complexity of the control algorithm. The transfer function is shown in (1.3) where K_r is the DC gain and ω_1 is the resonant angular frequency of the resonant element.

$$G_r(s) = \frac{K_r}{1+\left(\frac{s}{\omega_1}\right)^2}. \tag{1.3}$$

It should be noted that the value of $G_r(s)$ goes to infinite when $s=j\omega_1$. In this case, the resonant angular frequency ω_1 is set to the angular frequency ω_s of the supply voltage. The AC error signal can be applied to the resonant element without any coordinates transformation. The output signal in the resonant element will be used as a reference signal

to modulate the converter. A reduced block diagram of a proportional-resonant current controller is shown in Figure 1.30.

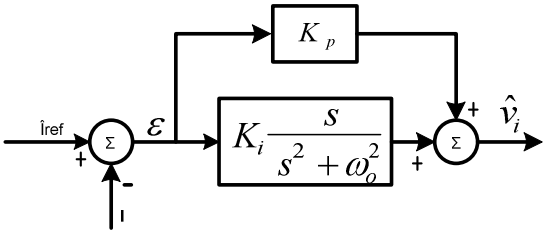


Figure 1.30. Proportional resonant current controller for a three-phase and single-phase systems.

In Figure 1.30, the output signal of the resonant element is adjusted automatically to a value which makes the fundamental frequency component of the AC input current coincide exactly with its AC reference, eliminating completely the steady-state error in the fundamental component of the supply current. In general, the transfer function of the PR current controller is given by (1.4).

$$G_{PR}(s) = K_P + K_i \frac{s}{s^2 + \omega_o^2}. \tag{1.4}$$

Since no transformations are necessary, this controller can be easily used in single-phase PV systems. This current controller can be also used to regulate not only the fundamental frequency component, but also other harmonic frequencies. This can be done by means of cascading several resonant blocks as is shown in Figure 1.31 [1.41].

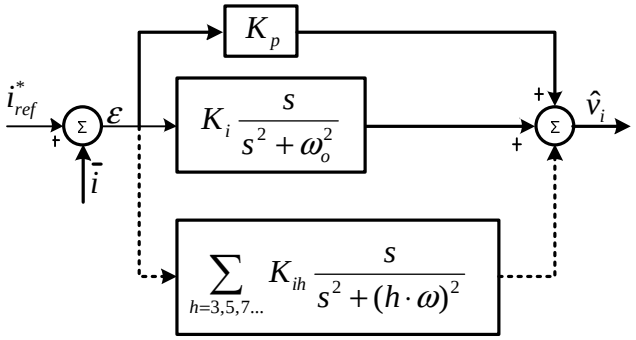


Figure 1.31. Proportional resonant current controller and low-order harmonic compensator.

Finally it should be said that the proportional gain K_i in the PR controller determines the bandwidth and acts to eliminate the steady state phase error [1.42].

1.5.6.3. Hysteresis controllers

As an alternative to PWM control techniques, hysteresis current controllers have been broadly used also in grid connected converters, as they can be easily implemented with no complex hardware. Another important advantage of this kind of controllers is their fast dynamic response and their inherent capability to limit the peak current injected by the converter. In addition, hysteresis controllers do not require any information about the system parameters, something that enhances its robustness.

The basic hysteresis current control is based on an on-line PWM control that sets the output voltage of the inverter instantaneously [1.43]. The main task of the PWM current controller is to adjust the output current, *i*, in order to track the current reference provided by i^*. By comparing the instantaneous current at the output with the reference signal, the controller should determine the active times for each switch in the power converter. As a consequence, the error signal (δ) should be kept in a tolerance band [1.44]. A basic scheme of a general inverter with a hysteresis current controller is shown in Figure 1.32.

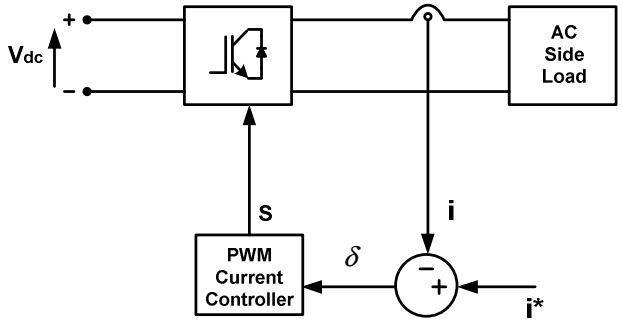


Figure 1.32. Basic hysteresis current controller.

In this kind of controllers, the converter switching state depends on the error between the current set-point and the real currents injected by the converter. In this way when in a conventional hysteresis current control the load current is lower than the current reference, the inverter connects the positive of the DC bus to the load, reducing thus the currents. On the contrary when the load current reference, is higher than the current reference, the inverter connects the negative side of the DC bus to the load. As it is shown in [1.45], there are some other hysteresis control structures that provide three output voltage levels. Taking into account the previous description, the error signal can be maintained within a certain fixed band. Figure 1.33 shows the evolution of the load current when a basic hysteresis current control is used.

However and in spite of its good dynamic response, this fixed error band makes the switching frequency to vary according to the grid voltage level and the slope of the reference signal. This variable switching frequency may cause several problems in the system such as: overheating of the converter, difficulty in the filter design, resonances and appearance of no optimum current ripple in the load [1.45].

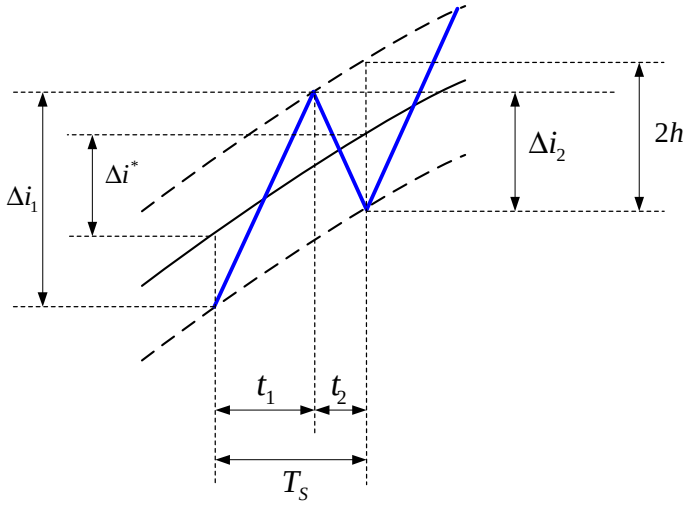


Figure 1.33. Output current in an inverter using a conventional hysteresis current controller.

In order to overcome the aforementioned problems the basic hysteresis current control can be modified in order to get an almost constant switching frequency by using an adaptive hysteresis band.

1.5.7. Grid integration of PV systems

Nowadays the PV power systems represent an important percentage of the total power injected to the electrical grid. This means that this kind of systems should be connected to the electrical grid in a way in which they can fulfill the requirements set by the electrical grid. The waveform of the current injected should be as sinusoidal as possible, in order to present a good performance regarding the harmonic content requirements established in the IEC61727/IEEE929 standard.

In order to get a good power factor, it is necessary to synchronize the current with the grid voltage. In this sense some techniques have been proposed and evaluated. One of the most extended techniques is the Phase-Locked Loop (PLL) [1.46]-[1.48]. This system consists in basically three blocks: phase detector, loop filter and Voltage Controlled Oscillator (VCO). The first block generates an output signal proportional to the phase difference between its two input signals. Depending on the type of the phase detector, high frequency AC components appear together the DC phase difference signal. The second block, exhibits low pass filter characteristic and filters out the high frequency AC components from the phase detector output, typically this is a 1-st order LPF (Low Pass Filter) or a PI (Proportional Integral) controller. Finally the VCO generates at its output an AC signal whose frequency varies respect a central frequency as a function of the input voltage. Figure 1.34, shows a block diagram with the basic structure of the PLL.

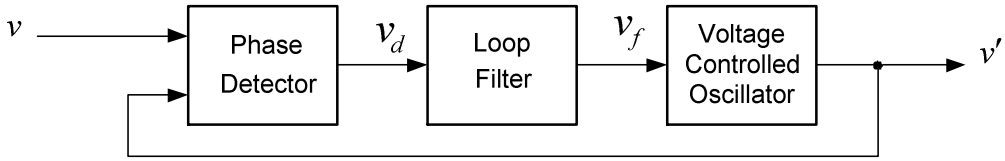


Figure 1.34. Block diagram of the basic Phase Locked Loop (PLL) system.

1.5.8. Codes for grid connection of PV systems

The grid connection codes are a very important issue in the design of grid connected converters. Some of the most representative codes are explained in this section.

The waveforms of the current and the voltage are ideally sinusoidal, but in some particular cases, they are different from its ideal appearance. These particular cases deal with perturbations or grid faults. In order to have a clear idea about how grid faults can occur, it is necessary to explain the most common cases.

Steady state voltage unbalances can occur in the three-phase electrical grids as a consequence of the connection of unbalanced single-phase loads or when one of the phases of the three-phase grid is disconnected. However, the most common transient unbalances can occur as a consequence of unbalanced grid faults. This unbalance situation generates negative sequence and zero sequence components in the grid voltages, which seriously affect to the power converter controllers. Voltage amplitude variations (>±10%) are another kind of perturbations due to failures in the transmission lines, bad connections, high excitation currents, etc. Moreover, some fluctuations in the frequency grid signal can be generated in the generation power plants due to the high variations in the load. Other common problems in electrical grids are harmonics. Harmonic currents are generated by nonlinear loads as, computers, electronic equipment, etc. These harmonic currents, which are multiples of the fundamental frequency, generate problems as resonances, overheating and malfunctions, which can be damage other equipment connected to the grid.

As an example, it is possible to take into consideration, the standard EN 50160, which regulates the voltage characteristics of the distribution system. This standard it was established in Brussels, Belgium in November of 1999 [1.49]. In this standard, the following requirements affecting to PV systems can be highlighted:

- The maximum voltage unbalance for three-phase inverters should not exceed 3%.
- The maximum variation allowed in the voltage amplitude is ±10%
- In case of the frequency variations the maximum level allowed is ±1%
- The voltage dips duration should be less than 1 sec in duration and less than 60% in deep.
- The THD can not exceed 8%.

When a PV system is connected to an electrical grid it must fulfill some specific requirement regarding:

- THD and individual harmonic current levels
- Power Factor (PF)
- Level of injected DC current
- Voltage and frequency range for normal operation
- Detection of islanding operation
- Synchronization and automatic reconnection
- Grounding connection

Some of the international standards that regulate the grid connection of PV systems are listed in the following:

- IEC 60364-7-712:2005. Electrical Installations of Buildings. Part 7: requirements for special installations or locations. Section 712: Photovoltaic power supply systems [1.50].

- IEEE 1547.1-2005 IEEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems [1.51].

- UL 1741. Standard for Safety Inverters, Converters, Controllers and Interconnection System Equipment for Use with Distributed Energy Resources. 7th May 1999, updated in 2005.

- IEEE 929-2000. Recommended Practice for Utility Interface of Photovoltaic (PV) Systems [1.52].

- IEC 61727 (1995-06) Photovoltaic Systems – Characteristics of the Utility Interface [1.53].

- DS/EN 61000-3-2 (2001) EMC, Limits for harmonic emissions (equipment input current up to and including *16 A* per phase) [1.54].

- VDE0126-1-1 (2006) Selbsstättige Schaltschtelle zwischen einer netzparalellen Eigenerzeugungsanlage und dem öffentlichen Niederspannungsnetz [1.55].

Most of these standards pay a special attention to the THD and to individual harmonics levels of the injected current, as well as the normal voltage and frequency operating range, anti-islanding detection and the level of the DC current injected into the grid. Particularly, the German standard VDE 0126-1-1 states that disconnection is mandatory in 0.2 s in case of DC current injection higher than 1 A. The VDE-0126-1-1 also regulates the leakage ground currents and faults levels in the case of transformerless inverters. According to the VDE-0126-1-1, there are three different currents to be monitored:

- ✓ Ground fault current, which happens in case of isolation failure when the current flows through the ground wire.

- ✓ Fault current, which represents the sum of the instantaneous values of the line currents, which under normal operation conditions should be zero.
- ✓ Leakage ground currents, which are the result of potential variations across the capacitive coupled parasitic elements.

Monitoring is typically done using a Residual Current Monitoring Unit (RCMU), which measures the fault and leakage current of the whole system. The standard states that the power converter should be disconnected from the main grid within 0.3 s in case the leakage current is higher than 300 mA. Furthermore, the Root Mean Square (RMS) value of the fault/leakage current jumps, and their respective disconnection times, are regulated according to the Table 1.3.

As can be seen in Table 1.3 in cases of increasing the RMS value of fault/leakage current by 30 mA, the disconnection is mandatory in 0.3 s. It can be also appreciated that as the leakage ground current increases the disconnection time is reduced in a significant ratio. This means that in case of a fault characterized by high leakage ground currents the systems should go automatically into a complete stop in a very short time.

Leakage current Jump value (mA)	Disconnection time (s)
30	0.3
60	0.15
100	0.04

Table 1.3. Leakage current jumps and their corresponding disconnection time from VDE 0126-1-1.

1.6. Outline of the thesis

This thesis is focus on the study and analysis of transformerless PV power inverters, and proposes new solutions to overcome the main problems of this kind of systems, namely, cancellation of leakage currents flowing through the stray capacitances of the PV panels and converters. The contents of this thesis are divided in six chapters according to the following schedule:

The first chapter reviews the state of the art in transformerless PV systems. A general overview and presentation of the main PV topologies is performed. In the case of single-phase systems, the review is focus in those most common topologies currently installed in PV systems. In the case of three-phase systems, some high performance topologies in terms of CMV and efficiency are presented. The introduction, objectives, background, motivation and scope of the thesis project are also presented in this chapter.

The second chapter describes in detail the operation and characteristics of single-phase transformerless PV inverters. A new topology base on HERIC topology is proposed. The effectiveness of the proposed system is demonstrated by experimental and simulation results. Some conclusions regarding leakage current and efficiency of the proposed topology are presented at the end of this chapter.

The third chapter is devoted to study and analyze the performance of three-phase systems regarding the CMV resulting from their modulation. The model to analyze the leakage ground current is described. A new topology able to solve the problem of the leakage ground current is proposed and its modulation strategy is presented. The CMV model for this new topology is describe and analyzed as well. The chapter ends with some conclusions regarding the performance of this new three-phase power conversion topology.

The fourth chapter analyses different modulation strategies for the power conversion topology proposed in Chapter three. All of the proposed modulation strategies are evaluated by simulation and experimentally under given operation conditions in order to compare their performance. A comparative analysis about total harmonic distortion was performed as well. Finally an analysis regarding power losses is also conducted.

The fifth chapter is basically focused on the control of the DC bus of the topology proposed in Chapter three. On one side, a technique to compensate the differences between both DC sources is proposed, analyzed and evaluated, both in simulation as experimentally. On the other side, a technique for DC power sharing control is proposed. Simulation and experimental results are presented to demonstrate the effectiveness of the proposed technique.

The last chapter contains the conclusions obtained as a result of the analysis and evaluation performed during this thesis and also contains the future works in this researching line.

1.7. List of publications

The following articles were published during the course of this PhD project.

1. Vazquez G., Kerekes T., Rolan A., Aguilar D., Luna A., Azevedo G., "*Losses and CMV evaluation in transformerless grid-connected PV topologies*", IEEE International Symposium on Industrial Electronics, 2009, ISIE 2009, Page(s): 544-548, DOI: 10.1109/ISIE.2009.5213296.

2. Azevedo G.M.S., Rodriguez P., Calvancanti M.C., Vazquez G., Neves F.A.S., "*New control strategy to allow the photovoltaic Systems operation under grid faults*", Brazilian Power Electronics Conference, 2009, COBEP'09, Page(s): 196-201, DOI: 10.1109/COBEP.2009.5347705.

3. Azevedo G.M.S., Vazquez G., Luna A., Aguilar D., Rolan A., "*Photovoltaic inverters with fault ride-through capability*", IEEE International Symposium on

Industrial Electronics, 2009, ISIE 2009, Page(s): 549-553, DOI: 10.1109/ISIE.2009.5213298.

4. Vazquez Gerardo, Rodriguez Pedro, Ordoñez Rafael, Kerekes Tamas, Teodorecu Remus, "*Adaptive hysteresis band current control for transformerless single-phase PV inverters*", 35th Annual Conference of IEEE Industrial Electronics, 2009, IECON'09, Page(s): 173-177, DOI: 10.1109/IECON.2009.5414770.

5. Kerekes. T., Teodorescu R., Rodriguez P., Vazquez G., Aldabas E., "*A new high-efficiency single-phase transformerless PV inverter topology*", IEEE Transactions on Industrial Electronics, 2009, Issue: 99, Page(s) 1-1. DOI: 10.1109/TIE.2009.2024092.

6. V. Gerardo, L. Alvaro, G. Eduard, "*Advanced Features in Power Electronics Converters for a Best Integration of Photovoltaic (PV) Systems to the Electric Grid*", IEEE International Symposium on Industrial Electronics, ISIE 2007.

7. Gerardo Vázquez, Tamás Kerekes, Joan Rocabert, Pedro Rodríguez, Remus Teodorescu, Daniel Aguilar, *"A Photovoltaic Three-Phase Topology to Reduce Common Mode Voltage"*, IEEE, International Symposium on Industrial Electronics, ISIE2010.

8. Hector Beltran, Maciej Swierczynski, Alvaro Luna, Gerardo Vazquez, Enrique Belenger, *"Photovoltaic Plants Generation Improvement Using Li-Ion Batteries as Energy Buffer"*, IEEE International Symposium on Industrial Electronics, ISIE2011.

9. Pedro Rodríguez, Raúl S. Muñoz Aguilar, Gerardo Vázquez, Ignacio Candela, Remus Teodorescu, *"Constant Common Mode Voltage Modulation Strategy for the FB10 Power Converter"*, IEEE Energy Conversion Congress and Exposition ECCE2011, Phoenix, Arizona, EEUU, September 17-22 2011.

10. Pedro Rodríguez, Raul S. Muñoz Aguilar, Gerardo Vazquez, Ignacio Candela, Emiliano Aldabas, Ion Etxeberria Otadui, "*Symetrical Ripple Constant Common Mode Voltage Modulation Strategy for FB10 Three-Phase Topology"*, 37th Annual Conference of the IEEE Industrial Electronics Society, IECON 2011, Melbourne, Australia; Noviembre 2011.

11. Pedro Rodríguez, Raul S. Muñoz Aguilar, Gerardo Vazquez, Ignacio Candela, Emiliano Aldabas, Ion Etxeberria Otadui, "*FB10 Converter: A PV transformerless Three-Phase Inverter"*, 37th Annual Conference of the IEEE Industrial Electronics Society, IECON 2011, Melbourne, Australia; Noviembre 2011.

12. Raúl Santiago Muñoz Aguilar, Pedro Rodríguez, Gerardo Vázquez, Ignacio Candela, Emiliano Aldabas, *" Efficiency Analisys of DCM-232 Three-Phase PV*

Topology", 38th Annual Conference of the IEEE Industrial Electronics Society, IECON 2012, Montreal Canada; October 2012.

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CHAPTER 2.

Single-phase transformerless PV power converters

Transformerless PV converters can improve the efficiency of the energy conversion process in PV systems. However, the use of transformerless converters in a PV power plant entails new challenges to be overcome in the design process. For instance, as it was explained in Chapter 1, when no isolation transformer is used in the connection of the PV converter to the electrical grid, leakage ground current can appear through the stray capacitance formed between the frame of the PV panels and the earth plane. The magnitude of these leakage ground currents depends on the different parameters and conditions of the PV facility, for example, the PV panel size, whether conditions, humidity, PWM strategy used to control the inverter, etc. In order to study the causes and effects of the parasitic currents, a common mode model will be presented in the next section.

2.1. Common mode model

This common mode model is aimed to be a useful tool to explain how the CMV contributes to the generation of currents through the stray capacitances of a PV facility. In a first step, it is necessary to consider the complete system and its stray elements. The system shown in Figure 2.1 corresponds to a single-phase PV system with a low- frequency transformer connected to the electrical grid [2.1], [2.2], [2.3], [2.4], [2.5]. The power system depicted in this figure includes the low-frequency transformer, with the stray capacitances that exist between the primary and secondary windings. The value of these capacitances can be estimated in the range of hundreds of picofarads. These very small stray capacitances allow a very big attenuation of the common mode currents. The EMI filter at the primary of the low-frequency transformer should filter the high frequency current components generated by the CMV. Therefore, the filter size becomes very small and easy to design.

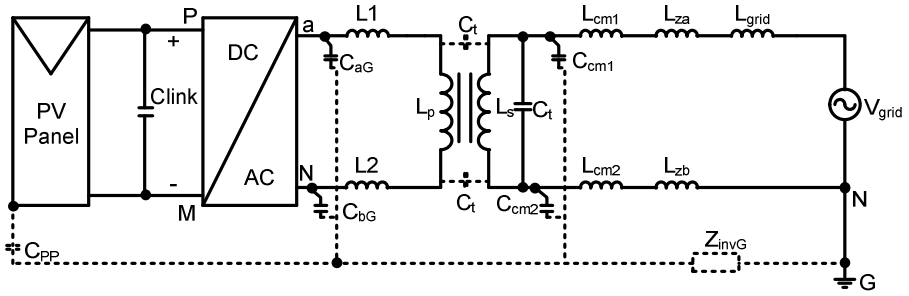

Figure 2.1. General single-phase PV system with low-frequency transformer.

From Figure 2.1 a simplified common mode model of a single-phase transformerless PV system can be deduced, as it is shown in reference [2.6]. In this model the power converter is simplified using two voltage controlled sources, meanwhile the low-frequency transformer is removed and just the output filter is considered. The model includes the CMV source and also the contribution of the asymmetries in the filter inductance which can be located in the positive line, in the neutral line or in both of them. The way in which the *L* filter is considered can vary the common mode currents in the PV stray capacitances. The final model obtained from this simple analysis is shown in Figure 2.2.

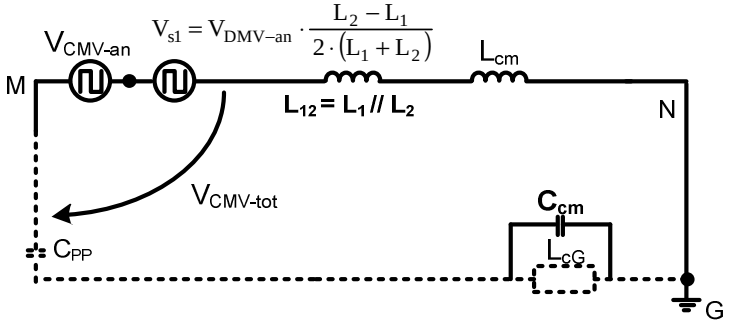

Figure 2.2. Final common mode model of the single-phase PV power converter.

This model can be very useful when the objective is to evaluate the leakage current level in the stray capacitances of the PV panel. In Figure 2.2, V_{s1} corresponds to the CMV that can be introduced by the asymmetries in the output filter inductances, V_{CMV-an} is the CMV, C_{pp} is the stray capacitance, $V_{CMV-tot}$ is the total CMV resulting from the addition of the V_{CMV-an} and V_{s1}, and finally C_{cm} and L_{cG} represent the impedance along the neutral path. Considering this simplified model, the leakage current behaviour for different PV topologies can be evaluated.

2.2. Analysis of the H5 and HERIC topologies

Two of the most used topologies in single-phase transformerless PV systems are the H5 and the HERIC (High Efficient and Reliable Inverter Concept) topologies [2.7], [2.8]. Figure 2.3 shows these two topologies, which are based in the conventional full-bridge converter.

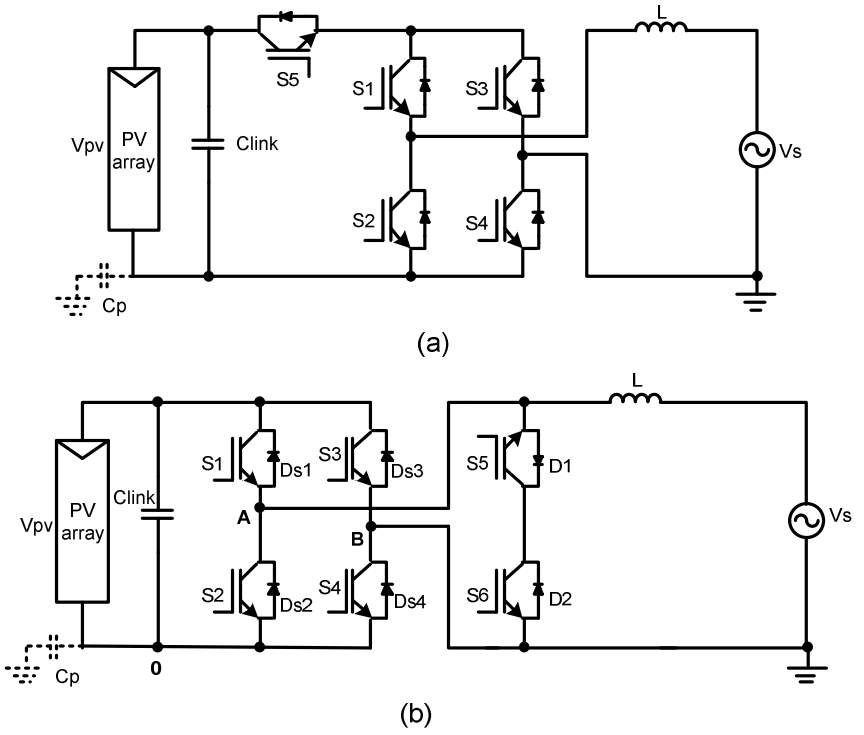

Figure 2.3. Popular single-phase transformerless PV systems; (a) H5 and (b) HERIC.

In Figure 2.3 (a), the H5 topology is depicted. As explained in Chapter 1 this topology disconnects the DC bus during the null states of the modulation strategy. As a result, the CMV can be kept constant and the leakage ground current can be drastically reduced. This characteristic gives a very good performance in transformerless PV applications. In addition, due to the way in which the modulation strategy is designed, the efficiency can arrive to very high values.

Figure 2.3 (b) shows the HERIC topology. This topology was also presented in Chapter 1. As the H5 structure, this topology is also based in the full-bridge inverter. The main difference is that there is a bidirectional switch on the AC side that is responsible to generate the null states at the output of the converter. All the switches of the full-bridge are set to OFF during null states. Therefore, as in the previous topology, this characteristic permits to keep

constant the CMV at the terminals of the PV panels and reduce significantly the leakage ground currents. The efficiency that this topology can achieve is also very high.

2.3. The HB-ZVR topology

The proposed topology is inspired on the HERIC topology. The main idea is to design the bidirectional power switch at the output of the power converter with a different power configuration. In the proposed topology, the bidirectional switch is implemented using one switch and a diode bridge. The proposed topology is depicted in Figure 2.4. The bidirectional switch is implemented on the AC side as in the HERIC topology. This topology was named "HB Zero-Voltage State Rectifier" because the null states are formed using a rectifier. The way in which this topology is modulated can be explained as follow: first, in the positive grid semi-period, the active state applied to the load is set by means of S1 and S4. The positive terminal of the DC bus is connected to the load under these operating conditions; see Figure 2.5 (a).

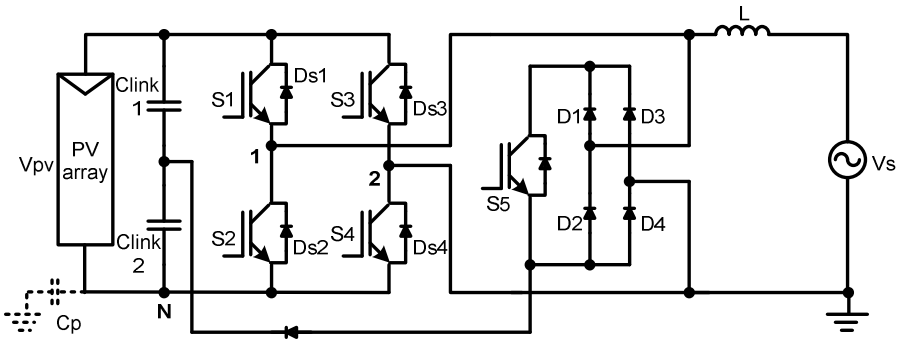

Figure 2.4. Proposed HB-ZVR transformerless topology.

After the application of an active state, switches S1 and S4 should be turn-OFF and S5 should be turn-ON in order to apply a null state to the output. Before applying the null state, the dead-time should be introduced between these two states to avoid short-circuiting the DC bus. This switching state is shown in Figure 2.5 (b). During the dead-time between the active state and the null state, there is a short time period in which all the switches are open and the current flows through the free-wheeling diodes and the DC bus capacitor. This switching state results in higher losses than in the case of the HERIC topology, where the free-wheeling current always flow through the bidirectional switch formed by S5 and S6.

Once the dead-time is elapsed, the null state is applied by means of S5, which should be turn-ON. The gate signal to drive S5 should be the complementary of the signal used to drive S1 and S4, adding the corresponding dead-time. When the null state is applied to the output, the free-wheeling path for the load current is through the single-phase rectifier and S5, as is shown in Figure 2.6.

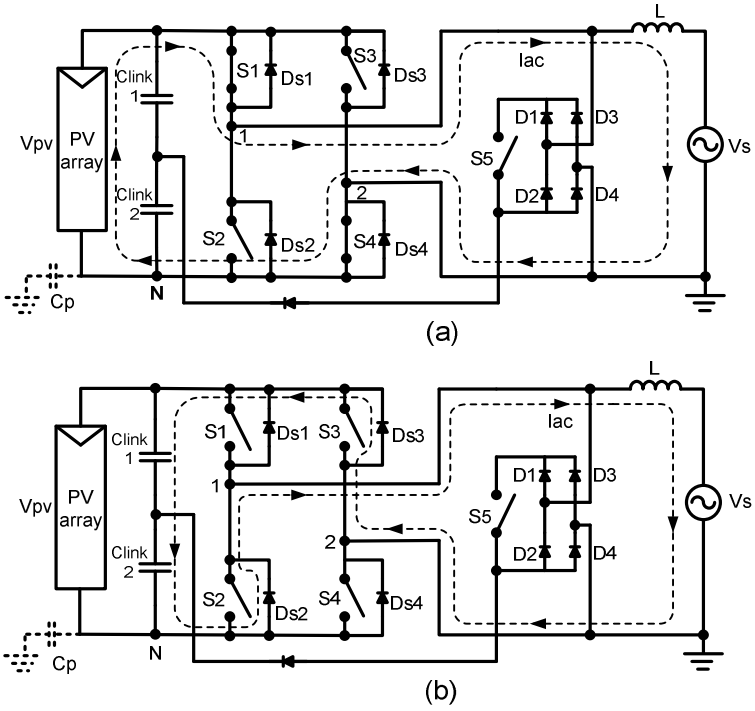

Figure 2.5. a) Positive active state condition and b) Dead-time state after turn-OFF S1-S4 in the HB-ZVR topology.

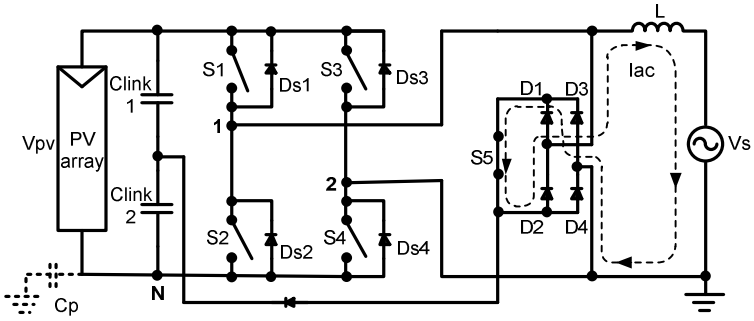

Figure 2.6. Null state during the positive half cycle in the HB-ZVR topology.

During the negative semi-period, the active state is applied by turning ON S2 and S3. In this case, the signal for S5 should be the complementary signal to the ones for S2 and S3, including and additional dead-time between these two signals as previously explained.

In this new topology, the bidirectional switch is clamped to the midpoint of the DC bus in order to fix the potential of the PV array also during the zero voltage periods, when S1-S4 and S2-S3 are opened. An extra diode is used to protect the lower DC-link capacitor from a short-circuiting condition.

Simulation results for this new topology are shown in Figure 2.7, where the sinusoidal load current, DC voltage (positive terminal) to ground and the leakage ground current are depicted. As can be appreciated in Figure 2.7 (b), the voltage is almost constant, which leads to very low leakage ground currents as it is shown in Figure 2.7 (c).

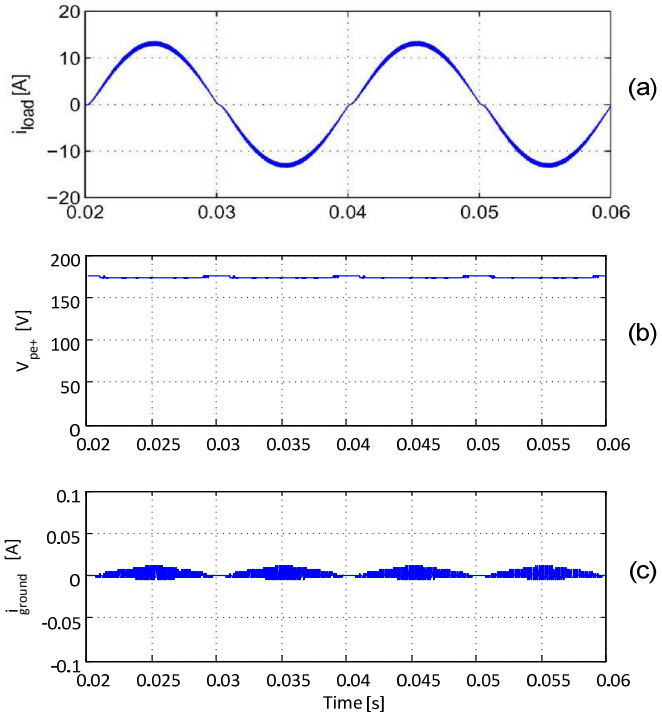

Figure 2.7. Simulation results of: (a) Load current, (b) DC+ terminal voltage respect to ground and (c) Leakage ground current.

The CMV for each switching state of the HB-ZVR topology can be calculated according to equation (2.1).

$$V_{cm} = \frac{V_{1N} + V_{2N}}{2}. \tag{2.1}$$

Therefore, the values for the CMV in the HB-ZVR topology are:

$$Positive\,Vector: V_{1N} = V_{dc}; V_{2N} = 0 \Rightarrow V_{cm} = \frac{V_{dc}}{2}, \tag{2.2}$$

$$Zero\,Vector: V_{1N} = \frac{V_{dc}}{2}; V_{2N} = \frac{V_{dc}}{2} \Rightarrow V_{cm} = \frac{V_{dc}}{2} \tag{2.3}$$

and

$$Negative\,Vector: V_{1N} = 0; V_{2N} = V_{dc} \Rightarrow V_{cm} = \frac{V_{dc}}{2}. \tag{2.4}$$

As shown in previous equations, the CMV in the HB-ZVR topology remains constant for all the switching states. The CMV only presents some short transient glitches during the dead-time separating active and null states. This low variability in the CMV justifies the low level of leakage ground current in the HB-ZVR topology, as was shown in Figure 2.7 (c).

2.4. Experimental results

To compare the performance of the HB-ZVR topology with the one from the conventional H-bridge inverter (HB with unipolar modulation strategy) and the HERIC topology some experiments were conducted in the lab. Some of the plots resulting from these experiments are shown in Figure 2.9 and Figure 2.10.

The parameters used in the experiments matched the ones used in simulation. These parameters were set as follow: V_{dc} = 350 V, C_{dc} = 250 μF, f_{sw}= 8 kHz (in case of the unipolar PWM f_{sw}= 4 kHz), dead-time = 2.5 μs and C_P = 100nF. In order to perform a fair comparison, all the experiments were done using the same switches, i.e., the PM75DSA120 Intelligent Power Modules from Mitsubishi, which are IGBT modules with maximum ratings of 1200 V and 75 A and the DSEP 30-06BR from IXYS, which is a module of fast diodes with maximum ratings of 600 V and 30 A. This diodes module was used in the diode bridge of the HB-ZVR topology.

The setup constructed in the lab is shown in Figure 2.8. The experimental results showed that the main difference between these three topologies is that in the case of the HB topology, the CMV is jumping along the time as it is shown in Figure 2.9 (a). Channel "M" in this figure, which is the FFT of the CMV measured between the DC+ terminal of the PV panel and ground, evidences that there is a high component at the switching frequency. In the case of the HERIC and the HB-ZVR topologies, the CMV is constant along the time. This means that the leakage ground current will be very low as it is shown in Figure 2.9 (b) and

Figure 2.10, where the Ch1 represents the voltage between the positive terminal of the DC bus and ground, Ch2 is the leakage ground current and Channel "M" represents the FFT of Ch1, where just the DC component appears.

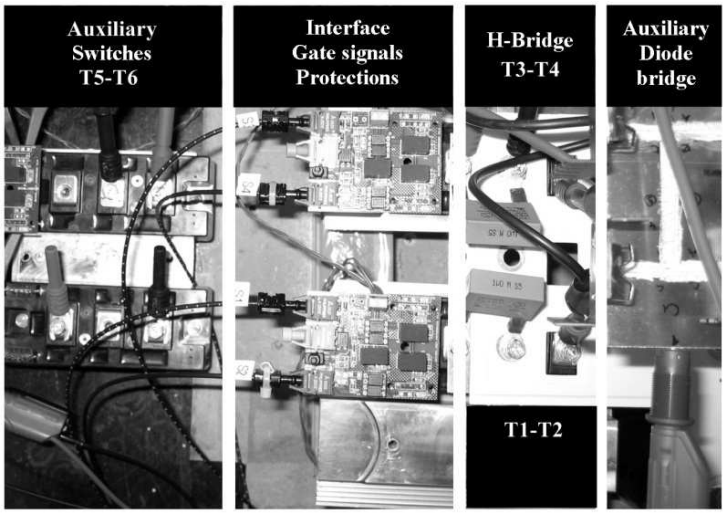

Figure 2.8. Modular experimental setup to test the single-phase transformerless PV inverters.

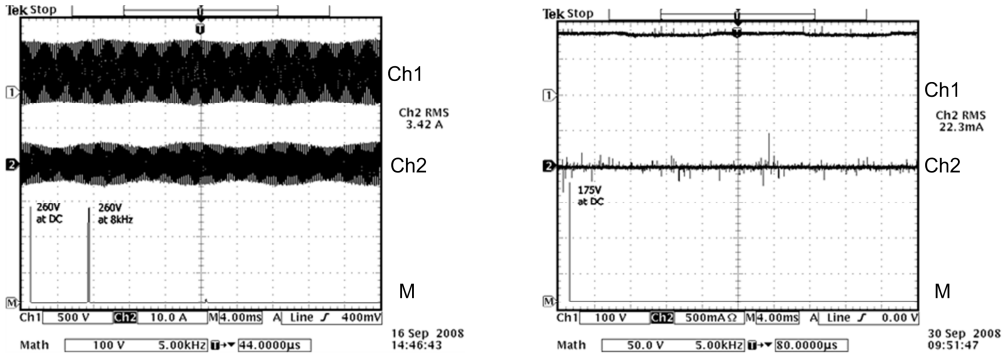

Figure 2.9. Experimental results for: (a) Full-bridge inverter (with unipolar modulation strategy), Ch1 shows the voltage to ground of the DC+ terminal, Ch2 is the leakage ground current and M is the FFT of Ch1 and (b) HERIC topology (same channel distribution than "(a)").

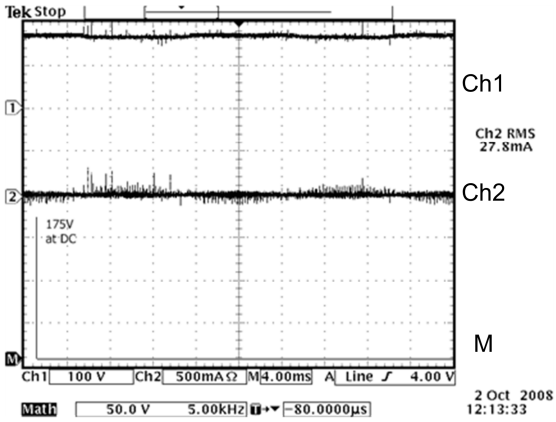

Figure 2.10. Experimental results for the proposed HB-ZVR topology, Ch1 shows the voltage to ground of the DC+ terminal, Ch2 is the leakage ground current and M is the FFT of Ch1.

As mentioned in section 2.3, the HB-ZVR generates the zero-voltage state in a similar way as the HERIC topology, but using another solution for the bidirectional switch configuration. Therefore, the common-mode performance of the proposed topology is similar as was the case of the HERIC topology. In Figure 2.10 the experimental results for the HB-ZVR topology are depicted. As can be seen, there are no high frequency components in the plot represented by Ch1 and the leakage ground current is close to zero (Ch2) with an *rms* value of around 27 mA. The FFT represented by plot "M" confirms that only a DC component appears in the CMV represented by Ch1.

2.5. Comparative analysis

During the experimental test, some other data regarding the operation of these three topologies were collected. The efficiency is one of the most important parameters and it was evaluated under different power levels. The efficiency was measured considering that the minimum DC input voltage in the European zone has to be at least 350 V, otherwise a boost stage is required.

The HERIC topology has very high efficiency along the whole operation range and has the best efficiency among all the three compared topologies, as detailed in Table 2.1 and in Figure 2.11.

The HB-ZVR topology has a slightly lower efficiency than HERIC, due to the fact that the bidirectional switch is controlled at the switching frequency and also because of the additional four diodes in the diode bridge, while in the case of the HERIC topology the bidirectional switch is controlled at the grid frequency. The maximum efficiency obtained with the HB-ZVR topology is 94.9%, which is a very attractive figure of merit for transformerless PV applications.

Finally, in the case of the HB converter with the bipolar PWM strategy has the lowest efficiency because of its two-level output voltage. By using unipolar PWM modulation, the voltage at the output of the converter will have three levels, but in this case, the generated CMV will have high frequency components that generate very high leakage ground currents.

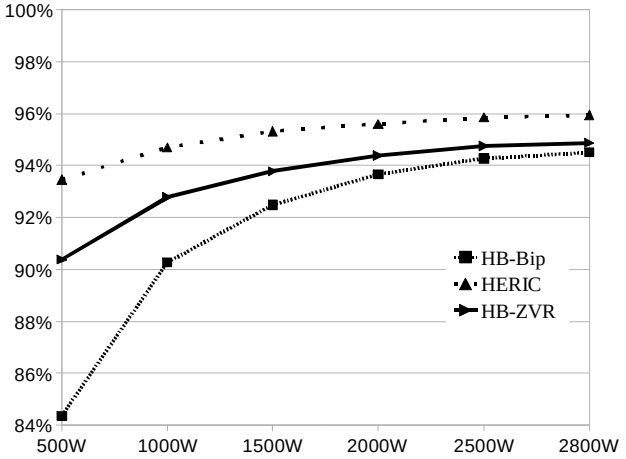

Figure 2.11. Efficiency comparison between the three topologies under test.

Topology	500W	1000W	1500W	2000W	2500W	2800W
HB-Bip	84,3%	90,2%	92,5%	93,6%	94,3%	94,5%
HERIC	93,4%	94,7%	95,3%	95,6%	95,8%	95,9%
HB-ZVR	90,4%	92,8%	93,8%	94,4%	94,8%	94,9%

Table 2.1. Efficiency obtained at the different power levels in the three topologies.

One advantage of the HB-ZVR topology compared with the HERIC topology is that the HB-ZVR topology can inject reactive power into the grid along the whole grid period. This is due to the fact that the HERIC topology is though for PV systems feeding the grid with unitary power factor. This is because the bidirectional switch composed by S5 and S6 in Figure 2.3 can not be turned-ON at the same time. This means that the current can only flow in a predefine direction defined by the switch currently turned-ON. On the other hand, in HB-ZVR topology it does not matter what the sign the current has, the current will always find a path to flow into the bidirectional switch composed by the diode bridge and a switch. This can provides the possibility to inject reactive power to support the electrical grid with additional services any time during the operation of the inverter.

2.6. Conclusions

Transformerless PV power converters offers a better efficiency that those that use a transformer to provide galvanic isolation between the power converter and the electrical grid.

The main drawback is that the CMV in transformerless converters greatly influences the ground leakage current flowing through the parasitic capacitances of the PV panels.

Modern full-bridge based PV converters, like H5, HERIC and the proposed HB-ZVR topologies, match the two most interesting requirements in transformerless PV converters, namely, high efficiency and constant CMV. The HB-ZVR topology presented in this chapter provides a new solution to implement the bidirectional switch on the AC converter side used to generate the zero voltage state. Based on the good performance of the HB-ZVR topology, demonstrated by analysis, simulation and experimental results, it can be concluded that this topology may an attractive alternative solution in single-phase transformerless PV applications.

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CHAPTER 3.

Three-Phase transformerless PV power converters

Single-phase PV facilities are small-scale PV systems with a rated power around 5-6 kWp. Single-phase PV systems use low DC voltage (350-400V) and generate pulsating instantaneous power at the output, with oscillating component at twice the fundamental grid frequency. Therefore, large DC capacitors are required to smooth the DC voltage oscillations, which decrease lifetime and reliability of the overall system [3.1]. Three-phase systems generate constant instantaneous power, which means that large capacitors are not necessary in this case, leading to lowest cost and a higher reliability of the whole system. Another important characteristic that should be pointed out is that power level in three-phase PV systems is higher than in the single-phase case, starting from 10-15 kWp, in the case of the rooftop applications, and arriving up to the MWp level in centralized inverters for large PV power plants. As in single-phase systems, if there is not a transformer insolating the power converter from the grid, leakage currents can flow through the PV panels stray capacitances. The value of these leakage ground currents depends on the different conditions in the PV facilities [3.3], [3.4], for instance, the PV panel size, whether conditions, humidity, PWM strategy [3.5], etc.

The leakage ground current can be a personal safety problem. This is the reason why research efforts have been focused on finding solutions to the leakage current problem. These solutions can be oriented to design of new PWM techniques and converter structures, which can improve the performance of the transformerless applications. In this research work, a new three-phase PV topology is proposed, analyzed and validated by simulation and experiments. This new topology has the capability of reducing significantly the leakage ground currents, keeping an overall good performance. In order to understand the leakage ground current problem, a detailed analysis based on the common mode model of the power converter is performed in the next sections. The proposed topology will be presented and

discussed in detail in this chapter, as well as the modulation technique used to drive the resulting power converter.

In this section, the common mode model for the classical two-level three-phase inverter is presented as an introductory study case. In this common mode model, the contribution from all the voltage components in the system will be analyzed. After that, a new three-phase topology is presented and its common mode model is derived from the previous one. The modulation strategy for this new topology will be presented in detail.

3.1. Leakage ground current model

One of the most significant problems in the transformerless PV systems is the leakage ground currents caused by the absence of galvanic isolation between the PV source and the electrical grid as it was explained in chapter 2. In order to understand the causes and effects of these undesirable currents the three-phase PV system depicted in Figure 3.1 will be analyzed. The low-frequency transformer has been included in the analysis in order to explain how the parasitic elements are involved in the path of the leakage current.

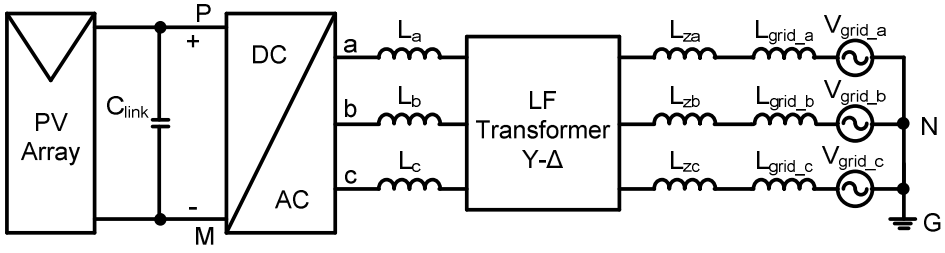


Figure 3.1. General three-phase PV system.

The general system consists in several stages, which are listed below:

- Power DC source (PV panel)
- DC link
- DC-AC converter
- Low pass filter
- Low-frequency transformer
- Electrical grid

The scheme in Figure 3.1 does not include the parasitic elements that can become very important when the operation frequency is high [3.6]. For instance, in the case of the PV panels, a stray capacitance is formed between the PV panel and the earth. In the output of each phase can also appear some small stray capacitances which are formed by the output wires and the earth plane [3.7]. The low-frequency transformer has also some parasitic elements in its structure, e.g., the stray capacitance between the primary and the secondary windings of the transformer [3.8]. On the grid side, the parasitic inductance of the wires has

been also considered. Figure 3.2 shows a model of the three-phase system of Figure 3.1 in which all the stray and parasitic elements have been included [3.9], [3.10].

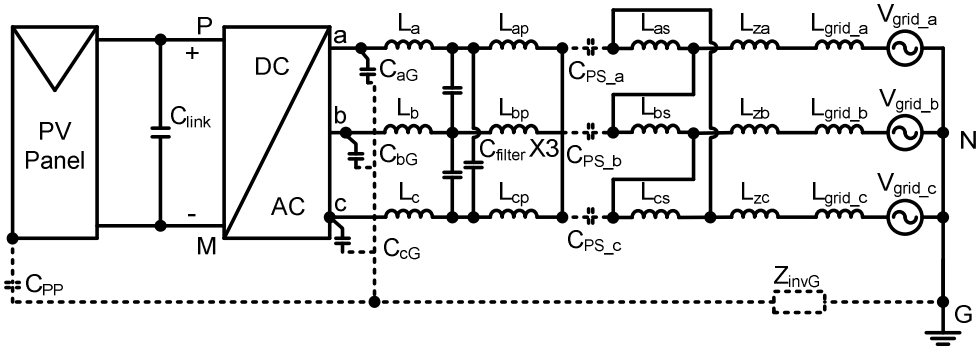


Figure 3.2. Three-phase PV system model with transformer considering the parasitic elements in the system.

The following stray and parasite elements have been considered in the circuit of Figure 3.2:

- C_{PP} is the parasitic capacitance that exists between the PV panel and ground.
- C_{aG}, C_{bG}, and C_{cG} are the stray elements that can appear at the three outputs of the converter (its value depends on the way in which the switches are connected with the grounded heatsink).
- C_{PS_a}, C_{PS_b} and C_{PS_c} are the stray capacitance between the primary and secondary windings of the low-frequency transformer.
- L_{za}, L_{zb} and L_{zc} are the series impedance (mainly inductive) of each phase at the grid side.
- Z_{invG} is the series impedance between the ground connection points of the inverter and the neutral grid connection.

As it is shown in Figure 3.2, the common mode current can only flow through the stray capacitance of the low-frequency transformer (C_{PS_a}, C_{PS_b} and C_{PS_c}). These stray capacitances can be model with a value in the range of 100 pF [3.11]. As a result, the common mode currents level at frequencies lower than 50 kHz are very low due to the low value of such capacitances. For frequencies higher than 50 kHz, the common mode currents can be filtered by an EMI filter. Thus, the low frequency leakage ground current behaviour is not influenced by the converter topology or its modulation technique when a low-frequency transformer is used to connect the PV converter to the grid [3.12].

On the contrary, in the case of the transformerless PV systems, the leakage ground current behaviour is strongly influenced by the converter topology and the PWM strategy because, in this case, the PV system is directly connected to the grid and the CMV in the system can generate large leakage ground currents flowing through the parasitic capacitance C_{PP} [3.13].

Considering the circuit of Figure 3.2, the voltages seen at the outputs of the inverter are set by the position of the switches in each step of the modulation sequence. Therefore, the output voltages can be studied as controlled voltage sources connected to the negative terminal of the DC bus. In this way, the circuit of Figure 3.2 may be redrawn as Figure 3.3 shows [3.14].

The voltage provided by V_{aM}, V_{bM} and V_{cM} is a function of the switching pattern of the switches composing the modulation strategy. As is explained in [3.15], the analysis of the common-mode and differential-mode voltages in the circuit of Figure 3.3 can be done by using just two phases. Actually, the analysis of three-phase systems with not neutral point connection can be done by using different combination between phases. For example, phase "a" and phase "b", phase "b" and phase "c" or phase "b" and phase "c" can be used. Therefore, just one of these three cases will be considered in further analysis, since results from the other two cases are equivalent.

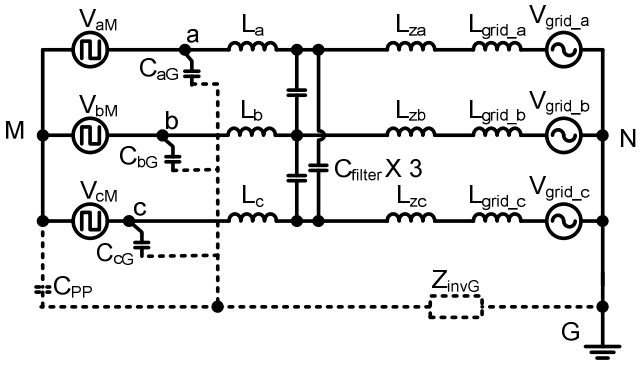


Figure 3.3. Three-phase transformerless inverter with the controlled voltage sources.

As the CMV may be defined as the average of the sum of voltages between the output voltages and a common reference [3.16], [3.17], [3.18], the equation (3.1) can be written from Figure 3.3.

$$V_{CMV-ab} = \frac{V_{aM} + V_{bM}}{2}. \tag{3.1}$$

On the other hand, the differential voltage between both outputs is defined as the difference between its two voltages as follow:

$$V_{DMV-ab} = V_{aM} - V_{bM} = V_{ab}. \tag{3.2}$$

Considering equations 3.1 and 3.2, the total output voltage of the two outputs "a" and "b" referenced to the common point "M", may be expressed as follow:

$$V_{aM} = \frac{V_{DMV-ab}}{2} + V_{CMV-ab};$$
$$V_{bM} = -\frac{V_{DMV-ab}}{2} + V_{CMV-ab}. \tag{3.3}$$

The equations in (3.3) can be draw as is show in Figure 3.4, where now just the two phases “a” and “b” are considered.

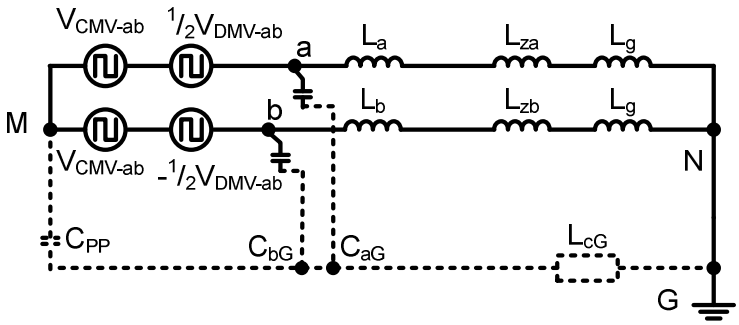


Figure 3.4. Common mode and differential mode voltages in a transformerless three-phase inverter.

A more simplified model can be obtained considering that the CMV appears in both legs as it is shown in Figure 3.4, the model now may be draw as is depicted in Figure 3.5. Furthermore the influence of the output inductors and the heatsink to ground capacitances can be separated as is also shown in Figure 3.5.

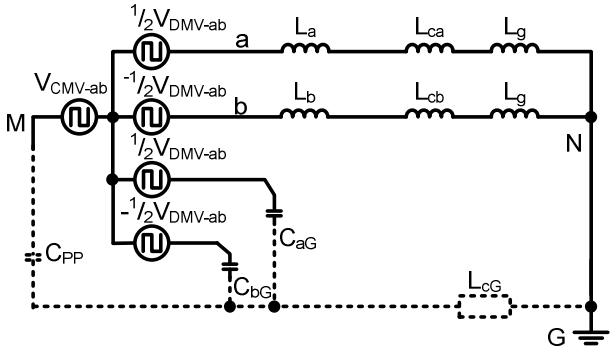


Figure 3.5. Simplified model of the three-phase inverter using two legs.

By introducing the equivalent circuits of the model implemented in Figure 3.5, the equivalent circuit in Figure 3.6 a) is derived. The equations V_{ab1} and V_{ab2} in (3.4) are two

voltage sources due to the asymmetries in the differential mode impedances that correspond to the line inductances and the leakage capacitances between the converter switches and the heatsink. Even if the converter does not generate any CMV, it is possible to have common mode currents when there are asymmetries in the mentioned impedances. In most of the cases, the two converter outputs are physically symmetric, therefore it can be assume that the C_{aG} and C_{bG} are very similar, as a result, V_{ab2} will be close to zero. The final simplification is depicted in Figure 3.6 b).

$$V_{ab1} = V_{DMV-ab} \frac{L_b - L_a}{2 \cdot (L_b + L_a)};\ V_{ab2} = V_{DMV-ab} \frac{C_{ag} - C_{bg}}{2 \cdot (C_{ag} + C_{bg})}. \tag{3.4}$$

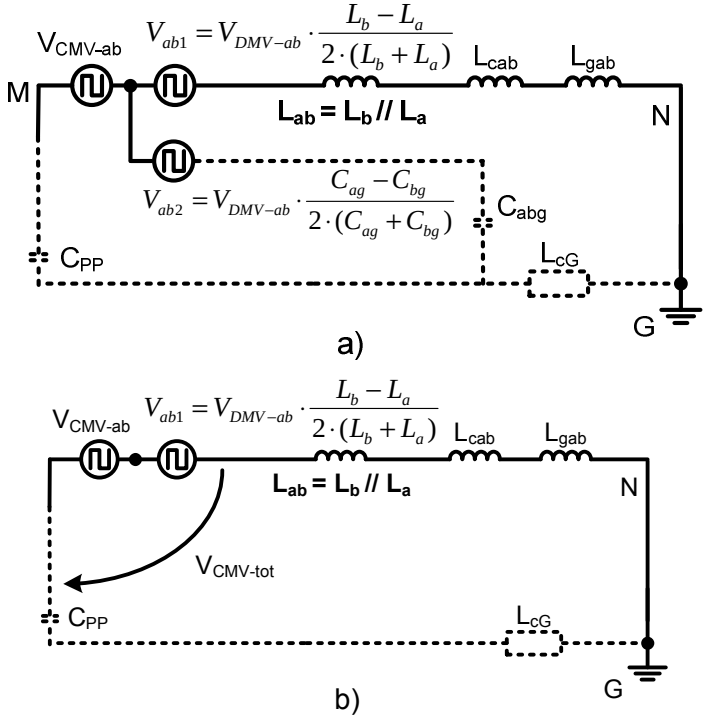


Figure 3.6. Simplified model for the two legs of the inverter; a) Considering the unbalance impedances and b) Final simplified common mode model.

Based on the above analysis and considering the three phases in the power converter, the total CMV can be defined as follow (including the effect of the unbalances in the load inductors).

$$V_{CMV-T} = V_{CMV-3\approx} + \frac{V_{ab1} + V_{bc1} + V_{ca1}}{3}, \tag{3.5}$$

where:

$$V_{CMV-3\approx} = \frac{V_{CMV-ab} + V_{CMV-bc} + V_{CMV-ca}}{3} = \frac{V_{aM} + V_{bM} + V_{cM}}{3}. \tag{3.6}$$

Equation (3.5) represents the total CMV in a three-phase system which is produce by the modulation strategy and the unbalances of the load. The voltage calculated from equation (3.6) charges and discharges the stray capacitance C_{PP}. This means that the variations in this voltage will produce dv/dt over the stray capacitance, resulting in current flows through the C_{PP}. The magnitude of this leakage ground current depends on the amplitude and frequency of the voltage across the stray capacitances C_{PP} and its value [3.19].

The complete model considering the three phases in the three-phase system is shown in Figure 3.7.

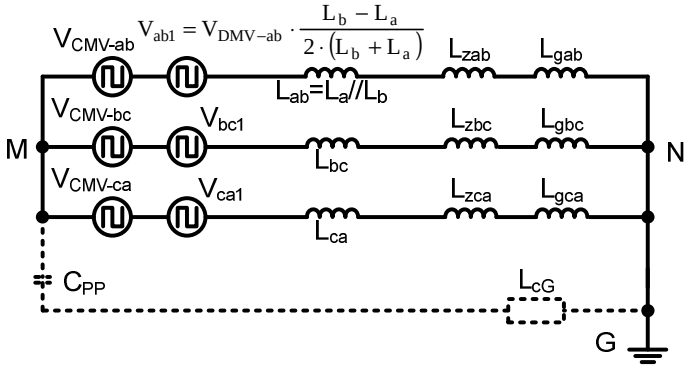


Figure 3.7. Final simplified model for the three-phase system including the CMV voltage sources.

3.2. The FB10 topology

The new three-phase transformerless topology proposed in this PhD work is named FB10 (Three-phase Full-Bridge with 10 switches) and it has been design with the objective of reduce as much as possible the CMV variations and consequently to reduce the magnitude of the leakage ground current in the stray capacitances of the PV system. The FB10 PV converter topology is shown in Figure 3.8. This topology consists basically of two stages; one of them is the DC decoupling stage and the other one is a three-phase full-bridge two level inverter. The DC decoupling stage is formed by four switches controlling two DC

buses. These two DC buses can be formed by two separated strings of PV panels. In addition, in the case of the two-level full-bridge inverter, the vectors that should be applied to the output are arranged according a specific pattern that allows an optimized use of the DC resource.

As explained in Section 1.5.5 of Chapter 1, the conventional three-phase two-level inverter has four different CMV levels, i.e., 1/3 Vdc, 2/3 Vdc, Vdc and -Vdc [3.20], [3.21]. The CMV level equal to 1/3 Vdc is produce when an odd vector is generated at the inverter output, i.e., V1, V3 and V5. On the other hand, the CMV level is equal to 2/3 Vdc when an even vector is generated at the inverter output, i.e., V2, V4 and V6. The CMV levels equal to Vdc and –Vdc correspond to the zero vectors V7 and V0. In conventional three-phase inverters, the modulation process originates voltage jumps over these CMV levels, which results in very high currents though the stray capacitance formed by the PV panel and the ground.

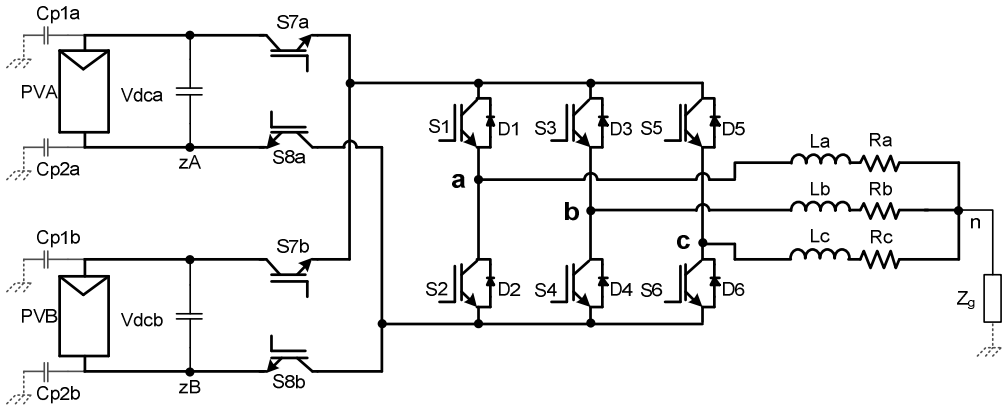


Figure 3.8. Proposed FB10 transformerless three-phase PV topology.

The operating principle of the FB10 topology stems from the approach used in the design of the H5 topology, namely, the DC bus is disconnected from the AC grid during the null states. In the FB10 topology, there are two DC buses (DC bus A and DC bus B) and their disconnection is performed by the switches S7a, S8a, S7b and S8b. The two-level full-bridge formed by the switches S1, S2, S3, S4, S5 and S6 is in charge of setting the vectors that will be generated at the converter output, either when one of the DC buses is connected (active vectors) or both of them are disconnected (zero vectors). The main idea supporting the FB10 topology is that those vectors generating 1/3 Vdc of CMV (V1, V3 and V5) will be generated by connecting the DC bus A, while the vectors generating 2/3 Vdc of CMV will do by connecting the DC bus B. The zero vectors are applied isolating both DC sources from the AC side. In this way, the CMV charging the stray capacitances of the PV panels connected to both DC buses will remain constant and not leakage current will flow through them.

An analysis of the common mode behaviour in the FB10 topology is presented in the next section. After that, the modulation technique used to drive the three-phase PV inverter is explained.

3.3. Common mode model of the proposed topology

The common mode model analysis of the FB10 topology can start by analyzing the DC buses in a separated way. The system can be evaluated without considering any neutral point connection. Therefore, the circuit of the FB10 transformerless inverter, including stray capacitances, can be depicted as Figure 3.9 shows. In this case the AC voltage sources which are forming the electrical grid are included, but as it will see in the next, they do not influence the common mode behaviour of the total system considered in the analysis.

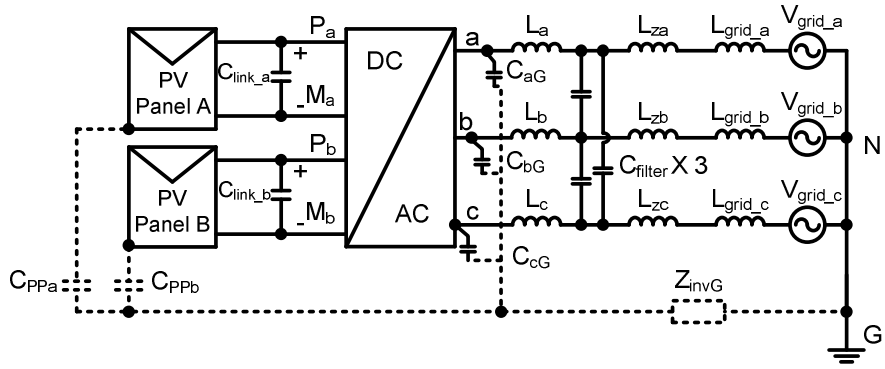


Figure 3.9. Proposed FB10 transformerless topology scheme considering its stray elements.

C_{PPa} and C_{PPb} in Figure 3.9 are the stray capacitances formed by the PV modules and the earth plane in each DC source (PV Panel A and PV panel B). On the converter side, three parasitic capacitances are considered, i.e., C_{aG}, C_{bG} and C_{cG}. These capacitances are formed between the converter outputs and the heatsink. The common mode and differential voltages of the FB10 topology can be obtained by considering the three phases of the system. However, as this is a three-phase system without neutral point connection, the analysis of the system can be simplified by just analysing the voltage between two phases, since the performance of the third one will be set by the currents Kirchhoff law, i.e., $i_a+i_b+i_c = 0$.

Therefore, the system depicted by Figure 3.9 can be also modelled as Figure 3.10 shows. In this case, the phase voltages are modelled as a controlled voltage sources. The voltage generated by these sources depends on the voltage vector applied to the output.

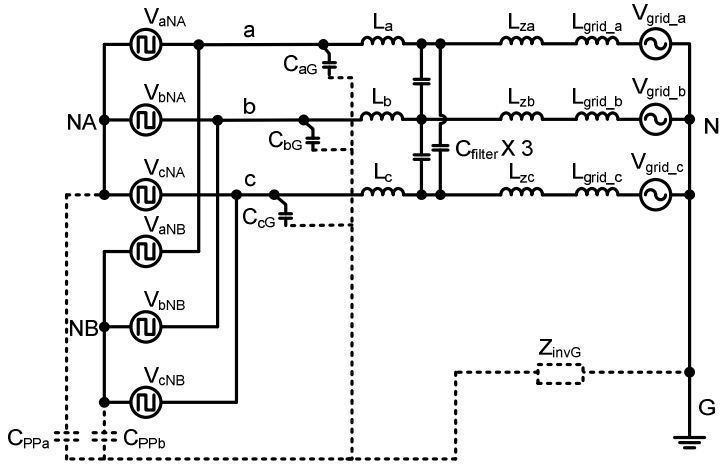


Figure 3.10. Initial common mode model proposed for the FB10 transformerless topology.

In Figure 3.10, NA represents the negative terminal of the PV panel A and NB is the negative terminal of the PV panel B. In both cases, the negative terminals are connected to the parasitic capacitances C_{PPa} and C_{PPb}, respectively. Therefore, the controlled sources are connected between the converter outputs and the negative terminals of the DC sources, being necessary to point out that the DC sources are isolated each other, i.e. the terminals of the DC buses are independent.

As abovementioned, the analysis of the FB10 topology can be conducted by just using two phases. Thus, the model can be simplified as it is show in Figure 3.11.

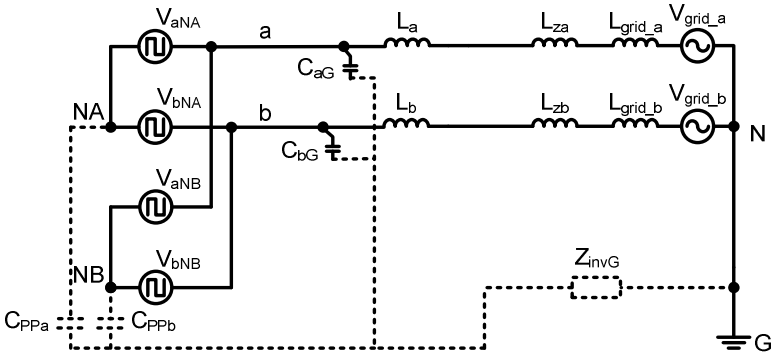


Figure 3.11. Common mode model proposed for the FB10 transformerless topology (using just two phases).

From Figure 3.11, the CMV can be calculated as the average of the sum of the voltages between the outputs of the converter and a common reference point. In this case, two CMV

are calculated by considering a reference points the negative terminal of each of the DC buses. So, following equations can be written, one for each DC bus:

$$V_{CMVA-ab} = \frac{V_{aNA} + V_{bNA}}{2}. \tag{3.7}$$

$$V_{CMVB-ab} = \frac{V_{aNB} + V_{bNB}}{2}. \tag{3.8}$$

Likewise, the equations for the differential voltages can be written as follow:

$$V_{DMVA-ab} = V_{aNA} - V_{bNA} = V_{abA}. \tag{3.9}$$

$$V_{DMVB-ab} = V_{aNB} - V_{bNB} = V_{abB}. \tag{3.10}$$

Using (3.9) and (3.10), the voltages between the converter outputs and the negative terminals of both DC buses can be calculated. Therefore in the case of DC bus A the equations are:

$$V_{aNA} = V_{DMVA\_ab} + V_{bNA} \tag{3.11}$$

and

$$V_{bNA} = -V_{DMVA\_ab} + V_{aNA}. \tag{3.12}$$

In the case of the DC bus B, the equations are:

$$V_{aNB} = V_{DMVB\_ab} + V_{bNB} \tag{3.13}$$

and

$$V_{bNB} = -V_{DMVB\_ab} + V_{aNB}. \tag{3.14}$$

Using equations (3.11) to (3.14) and combining them with equations (3.7) and (3.8), the voltages for each DC source can be defined as a function of the differential and common model voltages. In the case of the DC bus A, the output voltages can be written as:

$$V_{aNA} = \frac{V_{DMVA\_ab}}{2} + V_{CMVA\_ab} \tag{3.15}$$

and

$$V_{bNA} = -\frac{V_{DMVA\_ab}}{2} + V_{CMVA\_ab}. \tag{3.16}$$

In the case of the DC bus B, the equations can be written as follow:

$$V_{aNB} = \frac{V_{DMVB\_ab}}{2} + V_{CMVB\_ab} \tag{3.17}$$

and

$$V_{bNB} = -\frac{V_{DMVB\_ab}}{2} + V_{CMVB\_ab}. \tag{3.18}$$

With these equations, a new circuit model for the FB10 topology can be derived, as shown in Figure 3.12.

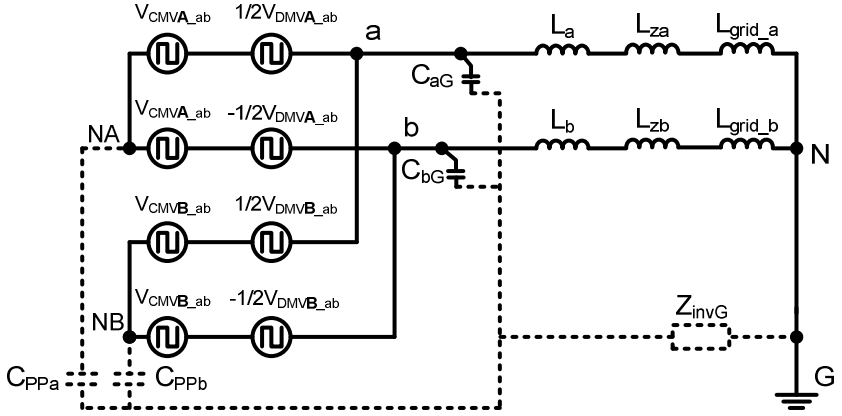


Figure 3.12. Common mode model for the FB10 transformerless topology using the equations (3.15) to (3.18).

Since the CMV is the same for both legs of the model, the model can be modified as shown in Figure 3.13. Furthermore the influence of the output inductors and the heatsink to ground capacitances can be separated as is also shown Figure 3.13.

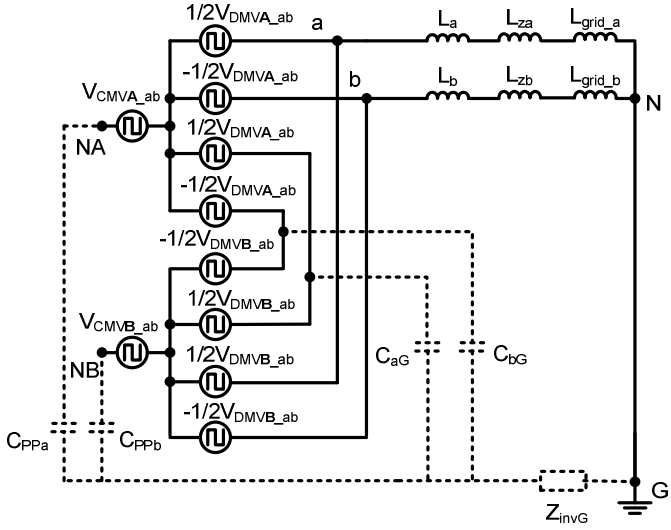


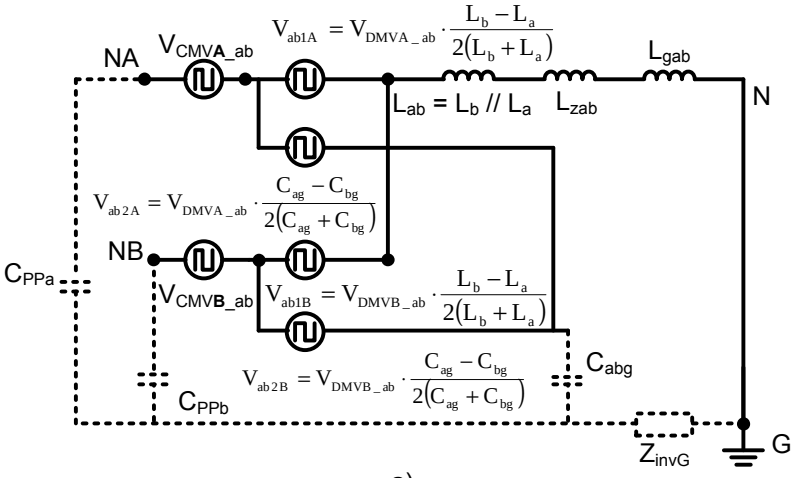
Figure 3.13. Simplified common mode model for the FB10 transformerless topology following the equations (3.15) to (3.18).

By introducing the equivalent circuits of the model depicted in Figure 3.13, the simplified model shown in Figure 3.14 a) is derived. The equations V_{ab1A}, V_{ab2A}, V_{ab1B} and V_{ab2B} shown in Figure 3.14 a), are the voltage sources due to the asymmetries in the differential mode impedances that correspond to the line inductances and the leakage capacitances between the converter switches and the heatsink as in the case of the conventional three-phase full-bridge inverter. Even if the converter does not generate any CMV, it is possible to have common mode currents when there are asymmetries in the mentioned impedances. In most of the cases the two converter outputs are physically symmetric, therefore it can be assume that the C_{aG} and C_{bG} are very similar, then V_{ab2A} and V_{ab2B} will be close to zero. The final simplification is depicted in Figure 3.14 b).

Considering Figure 3.14 b), the equation for the total CMV for each DC bus using the conventional definition and considering the three phases may be written as in equations (3.19) for DC bus A and (3.20) for DC bus B:

$$V_{CMV3A\approx} = \frac{V_{CMVA\_ab} + V_{CMVA\_bc} + V_{CMVA\_ca}}{3} = \frac{V_{aNA} + V_{bNA} + V_{cNA}}{3}. \qquad (3.19)$$

$$V_{CMV3B\approx} = \frac{V_{CMVB\_ab} + V_{CMVB\_bc} + V_{CMVB\_ca}}{3} = \frac{V_{aNB} + V_{bNB} + V_{cNB}}{3}. \qquad (3.20)$$



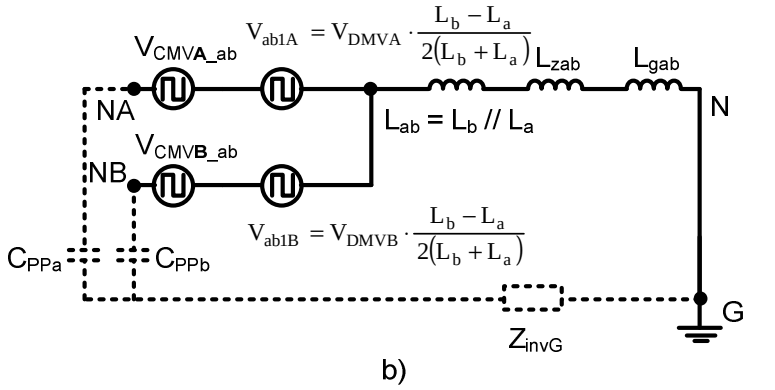


Figure 3.14. Simplified common mode model; a) Considering the unbalanced impedances and b) Final simplified common mode model.

In the case of unbalances in the output inductors, the effect of the differential voltage can also generate CMV in the system. In such a case, the total CMV for the DC bus A and DC bus B can be written as:

$$V_{CMV\_TOTA} = V_{CMV3A\approx} + \frac{V_{ab1A} + V_{bc1A} + V_{ca1A}}{3},$$
$$V_{CMV\_TOTB} = V_{CMV3B\approx} + \frac{V_{ab1B} + V_{bc1B} + V_{ca1B}}{3}. \quad (3.21)$$

Therefore, the complete model for the three-phase FB10 topology, considering all the effects affecting to the CMV, can be drawn as Figure 3.15 shows.

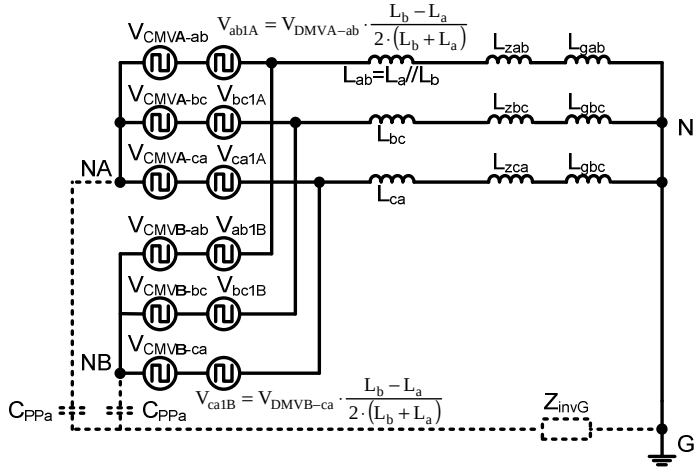


Figure 3.15. Final simplified common mode model for the FB10 transformerless topology.

In the next section, a modulation strategy for the FB10 topology is presented. The operation of this modulation strategy is illustrated by using simulation and experimental results.

3.4. Modulation strategy

The main objective in the modulation strategy proposed for the FB10 topology is to keep constant the CMV and to solve the problem of leakage currents in three-phase transformerless PV converters [3.22], [3.23]. With this objective in mind, the proposed modulation strategy allows using the two DC buses, A and B, to feed the grid while keeping constant the voltage across their stray capacitances. To do that, one of the DC buses, let say the DC bus A, is used to feed the grid when an **odd** active vector (V1, V3 and V5) is applied. Likewise, the other DC bus, namely, the DC bus B, is used to feed the grid when an **even** active vector (V2, V4 and V6) is applied. Moreover, both DC buses are disconnected from the grid when a zero vector is applied at the converter output. It is worth to point out that the

active vectors in the full-bridge inverter are pre-set during the time in which the zero vectors are applied to the output. For example, if the vector V1 should be applied to the output (S1-On, S2-Off, S3-Off, S4-On, S5-Off and S6-On), it will be pre-set in the full-bridge switches during the time in which a zero vector is applied (S7-Off and S8-Off). Once the V1 vector is pre-set in the full-bridge, the switches S7a and S8a are turned-ON (the V1 vector is an odd vector to be generated with the DC bus A) and the vector is generated at the output of the converter to feed the grid (see Figure 3.16). Therefore, the FB will present multiple switching states during the zero vectors since it is in charge of pre-setting the active vector to be generated at the output in the next switching state. This switching pattern allows keeping constant the CMV in the PV panels connected to the buses A and B, although the value of the CMV for each group of PV panels is different.

With the configuration of the switches shown in Figure 3.16, the current flows from the DC bus A toward the load, as in a conventional two-level full-bridge inverter. In the switching step, when a zero vector should be generated according to the modulation pattern, the switches S7a and S8a should be turned-OFF. Therefore, the DC bus A is isolated from the grid and the three-phase current flows through the switches and the free-wheeling diodes of the full-bridge to generate the zero vector. Just after the DC bus A is isolated from the grid, the switches of the full-bridge remain with the same switching state as when V1 was generated at the output of the converter, as shown in Figure 3.17.

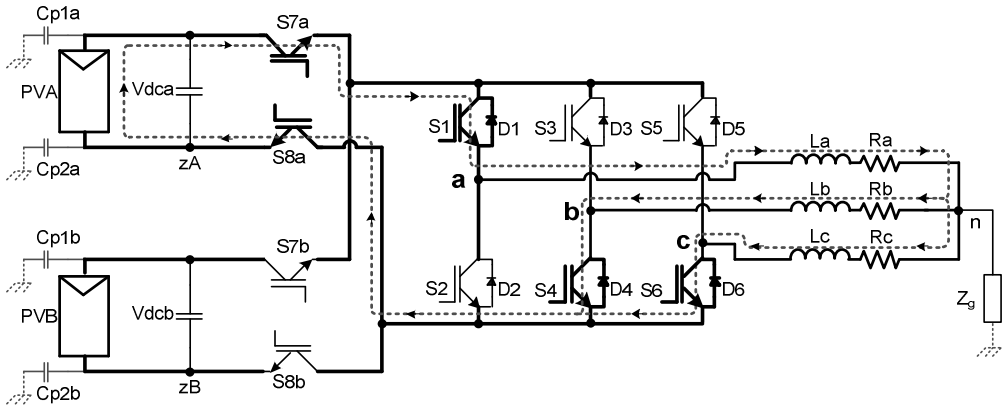


Figure 3.16. FB10 topology configured with an odd active vector (V1).

Lets call V10 to the switching state shown in Figure 3.17, i.e., a switching state in which a zero vector with V1 configuration in the full-bridge is present at the output of the power converter. During such switching state the current flows though S1, D2, D3, S4, D5 and S6. This means that the output current is share in multiple paths, as shown in Figure 3.17. This zero vector configuration allows reducing the current in the switches during the zero vectors respect to the case of the conventional full-bridge with a single DC bus permanently connected, which results in a better distribution of the conduction power losses during the zero vectors. Due to the fact that the DC voltage is isolated from the full-bridge, the change between switching states during the zero vector generation can be performed without

introducing any dead-time in the switching pattern. Figure 3.18, shows the switching state for the V20 vector, i.e., the case in which the vector V2 is pre-set in the full-bridge during the zero vector state.

To generate the vector V2 at the output of the converter, the switches S7b and S8b are turned-ON to connect the DC bus B to the full-bridge, as shown in Figure 3.19.

The modulation pattern presented in this section allows reducing the impact of power losses because the switching between the active vectors is made during the zero vector states, i.e., with zero voltage switching.

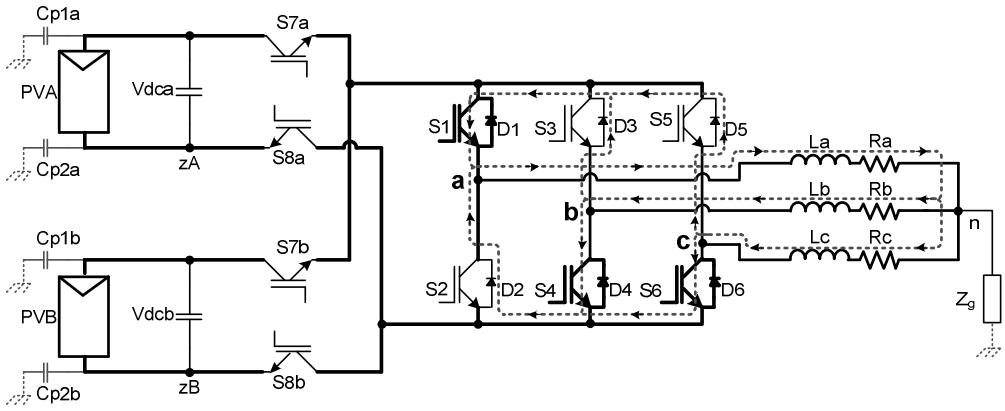


Figure 3.17. FB10 topology configured with a null vector (V1 is configured in the full-bridge circuit).

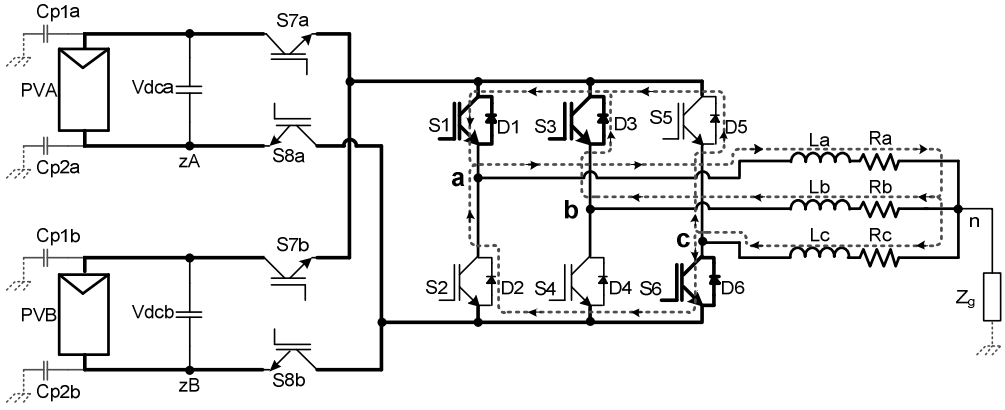


Figure 3.18. FB10 topology configured with a null vector (V2 is configured in the full-bridge circuit).

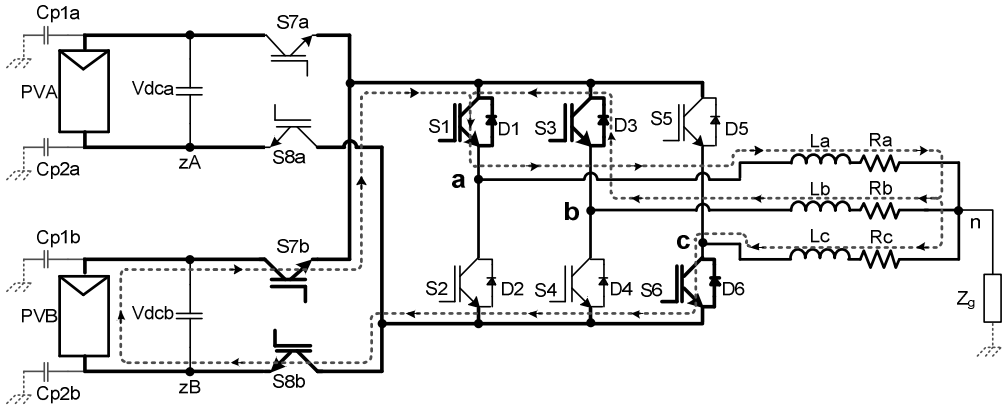


Figure 3.19. FB10 topology configured with an even active vector (V2).

Figure 3.20 shows the modulation strategy for a one switching period. In this figure, S1, S3 and S5 are the full-bridge upper switches signals, while S2, S4 and S6 are the complementary signals for the lower ones which are not depicted in Figure 3.20. The signals S7a and S7b control the connection of the DC bus A and B. The name of the different switches states are also shown in the Figure 3.20.

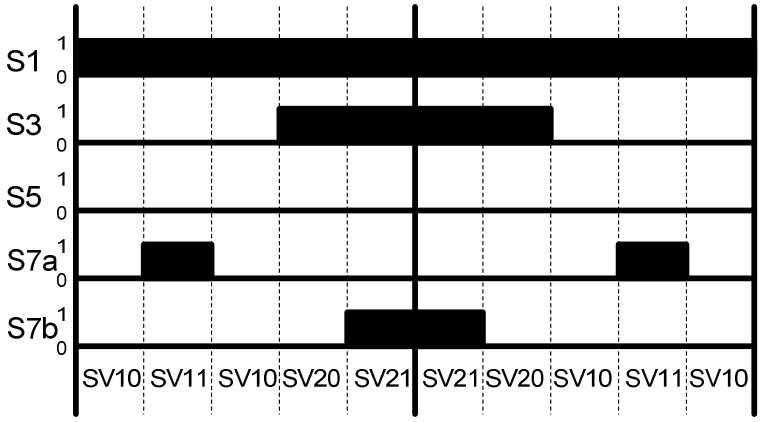


Figure 3.20. Initial modulation strategy proposed to control the FB10 PV inverter topology.

The names for different switching states in Figure 3.20 represent:

- **SV10** → Zero vector state with a V1 pre-set.
- **SV11** → Active vector V1 state.
- **SV20** → Zero vector state with a V2 pre-set.
- **SV21** → Active vector V2 state

As previously mentioned, no dead-time should be added to change among the different switches states of the full-bridge. In the same way, no dead-time is included between the zero vector and the active vector states. Additionally, the signals for connecting both DC buses to full-bridge should be mutually excluding, i.e., S7a and S8a cannot be turned-ON at the same time as switches S7b and S8b do.

The proposed modulation strategy for the FB10 topology is based on the general SVM algorithm; therefore it is a well-known algorithm easy to be implemented, for example, in C code language. The SVM algorithm calculates the ON and OFF times for each switch along the switching period. In this work, these times were calculated by using the α-β coordinates system, obtained from the a-b-c coordinates system by using the *Clarke* transformation (3.7).

$$\begin{bmatrix} v_{\alpha}^{*} \\ v_{\beta}^{*} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{2}/3 & -\sqrt{2}/3 \end{bmatrix} \cdot \begin{bmatrix} v_{an}^{*} \\ v_{bn}^{*} \\ v_{cn}^{*} \end{bmatrix}. \tag{3.7}$$

Therefore, the different vectors that can be generated by the three-phase full-bridge can be represented in a two-dimension α-β plane, as shown in Figure 3.21. A generic reference vector can be synthesized by calculating its projection of the full-bridge generating vectors as indicated in Figure 3.21.

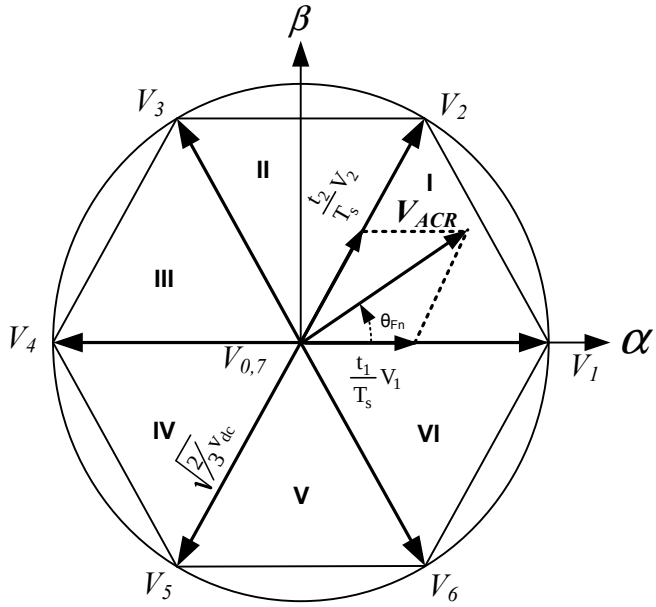


Figure 3.21. SVM represented in the α-β plane.

The magnitude of the reference vector can be calculated as:

$$\left|\vec{V}_{ref}\right| = \sqrt{v_{\alpha}^{*2} + v_{\beta}^{*2}}, \tag{3.8}$$

and the phase-angle will be:

$$\theta^{*} = \tan^{-1} \cdot \frac{v_{\beta}^{*}}{v_{\alpha}^{*}}. \tag{3.9}$$

As explained in Chapter 1, the SVM consist in six active vectors and two null vectors. The six active vectors are distributed along the grid period, giving rise to six different regions or sectors. The reference vector is synthesized in each region by using the two nearest active vectors and the two zero vectors. In the conventional SVM, the two active vectors are set consecutives, i.e, a reference vector in the sector 1 is synthesized by using the following switching pattern: V0-V1-V2-V7-V2-V1-V0 [3.24]. In general, the switching time for each vector is determined by using the first sector, independently the region in which the reference vector is located. To do that the following equation is used:

$$\theta_r = \theta_{Fn}^{*} - (r-1) \cdot \frac{\pi}{3}; \quad r \subset \{1,2,...,6\}. \tag{3.10}$$

Where θ_{Fn}^{*} is the phase-angle of the reference vector, r is the region where this vector is located and θ_r is the relative phase-angle of the reference vector in the first sector. The times for each vector are calculated according to (3.11).

$$\vec{V}_{ref} = \frac{t_1}{T_S} \cdot \vec{V}_1 + \frac{t_2}{T_S} \cdot \vec{V}_2. \tag{3.11}$$

Considering (3.11), the time period for the active and zero vectors are:

$$t_1 = \frac{\sqrt{2} \cdot \left|\vec{V}_{ref}\right|}{v_{dc}} \cdot T_S \cdot \sin\left(\frac{\pi}{3} - \theta_r\right). \tag{3.12}$$

$$t_2 = \frac{\sqrt{2} \cdot \left|\vec{V}_{ref}\right|}{v_{dc}} \cdot T_S \cdot \sin(\theta_r). \tag{3.13}$$

$$t_0 = Ts - t_1 - t_2 . \tag{3.14}$$

Therefore, as shown in Figure 3.20, the modulation sequence of the FB10 topology is V10-V11-**V10-V20**-V21-V21-**V20-V10**-V11-V10. The vector V11 is applied during the time t_1 according to (3.12), the vector V21 is applied during the time t_2 according to (3.13), and the vectors V10 and V20 share the t_0 time calculated by using (3.14).

Figure 3.22 shows some signals resulting from simulating the modulation algorithm of the FB10 power converter.

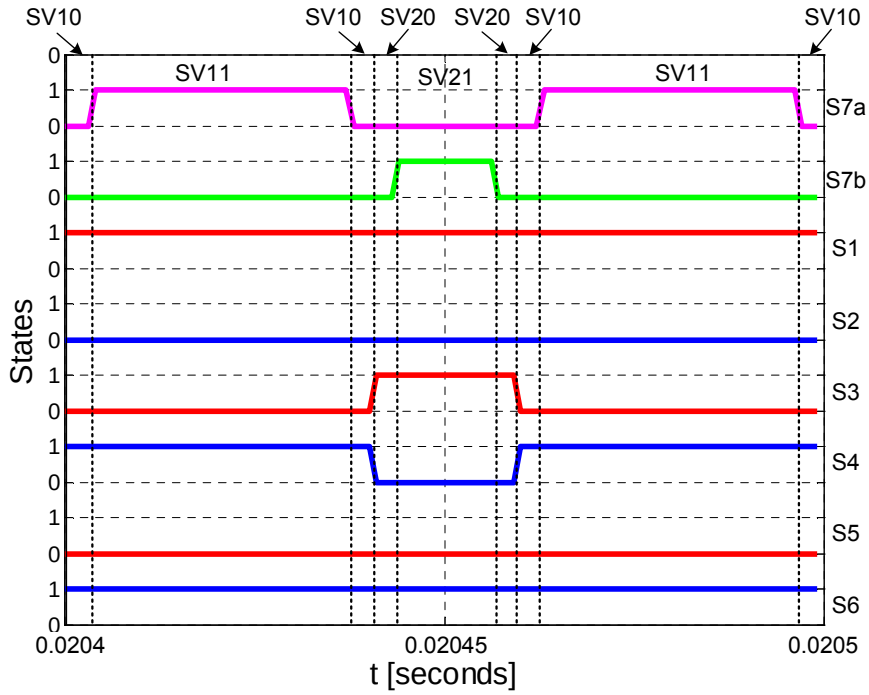


Figure 3.22. Simulation results with the initial modulation strategy to control the FB10 PV inverter topology.

As can be seen in the Figure 3.22, V1 is applied to the load when the switch S7a waveform is set to "1" during t_1, and vector V2 is applied to the load when the signal of S7b is set to "1" during t_2. The zero vectors are symmetrically distributed during the rest of switching period, i.e., during t_0. As it can be appreciated in the Figure 3.22, the switching state in the full-bridge is changing during zero vector states. These changes in the switching state are made with no dead-time, i.e., S3 and S4 signals change at the same time from state SV10 to SV20 and from state SV20 to SV10.

Thanks to the simultaneous switching at zero voltage during the configuration of the active vectors, the power losses in the full-bridge circuit will be only due to the current flowing through the semiconductors (conduction losses). Actually, according with Figure 3.22, the major power losses will be concentrated in the switches controlling the connection of both DC buses, because they are the ones performing a hard switching during the turn-OFF. A complete analysis of the power losses of the FB10 power converter is presented later in Chapter 4.

In Figure 3.23, some waveforms resulting from the simulation of the FB10 three-phase PV inverter are shown. In this simulation, a balance LR load with L= 2.8 μH and R= 13 Ω was connected at the output of the FB10 power converter. The voltage for both DC buses was set to 600 Vdc. The switching frequency was set to 10 kHz. The stray capacitances in the simulation circuit were also considered, being connected to the DC sources terminals, i.e., one stray capacitance in each DC bus terminal with a value of 150nF. These capacitances were connected in a common point, which was connected to the neutral point of the load through a small impedance. This connection allowed measuring the current flowing through the stray path. Figure 3.23 a) shows the symmetrical sinusoidal waveforms at the output for the FB10 power converter with a peak value around 15 A.

The Figure 3.23 a) shows the output currents of the FB10 power converter. As can be seen here the magnitude of the ripple in the load currents is a bit lower in the positive peak than in the negative peak along the grid period. A detailed explanation of this effect will be given in next chapter.

The Figure 3.23 b) shows the measured voltage over the stray capacitances. As it can be appreciated in this figure, the voltage across these capacitances is constant. This means that there is not any dv/dt over the parasitic capacitances and therefore the leakage ground current magnitude in the path to the neutral point of the load will be almost equal to zero.

Finally, the leakage ground current is shown in Figure 3.23 c). As can be observed, this current is very small, far away from the requirement set by of the standard VDE 0126-1-1, where is stated that the maximum level for the leakage ground current should be 300 mA as maximum. The spectrum of the leakage ground current is show in Figure 3.24. In this figure, the bigger component is located at 10 kHz, which is the switching frequency set in the simulations of the FB10 converter.

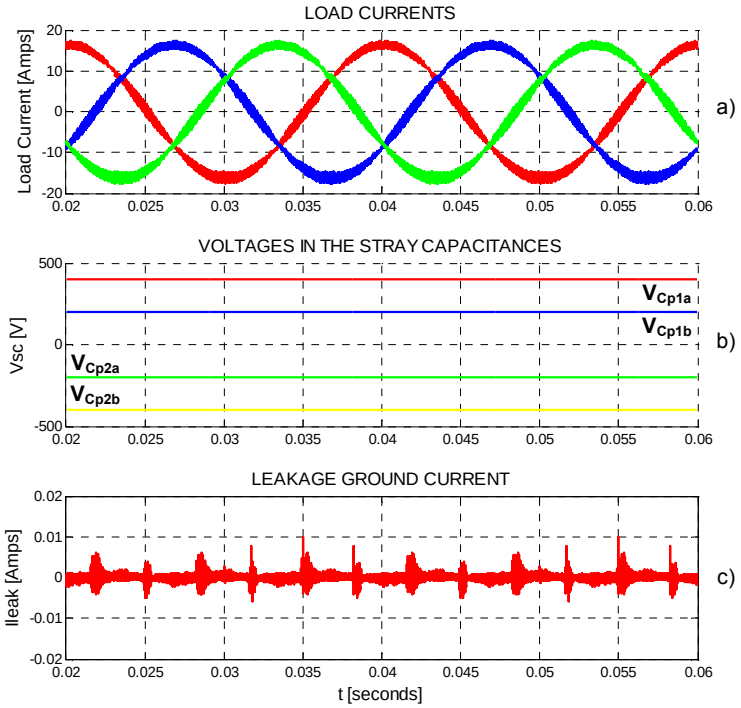


Figure 3.23. Simulation results for the FB10 topology, a) Load currents, b) Voltages across the stray capacitances (C_{p1a}, C_{p2a}, C_{p1b} and C_{p2b}), c) Leakage ground current.

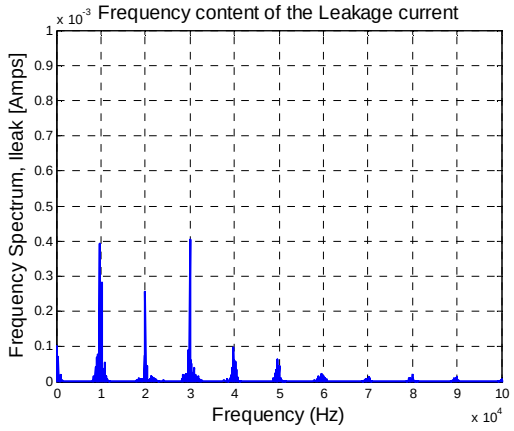


Figure 3.24. Frequency spectrum of the leakage ground current.

In Figure 3.25 a) "case 1" the phase output voltages referred to a common point "zA" are shown. From this phase voltages, the CMV is shown in Figure 3.25 b) "case 1", where it is possible to appreciate how it has a constant value equal to 200V, which is calculated using equation (3.19) and corresponds with the CMV generated by the odd vectors. The CMV in the case of the DC bus B can be calculated using equation (3.20) resulting in 2/3Vdc generated by the odd vectors, "case 2" in Figure 3.25.

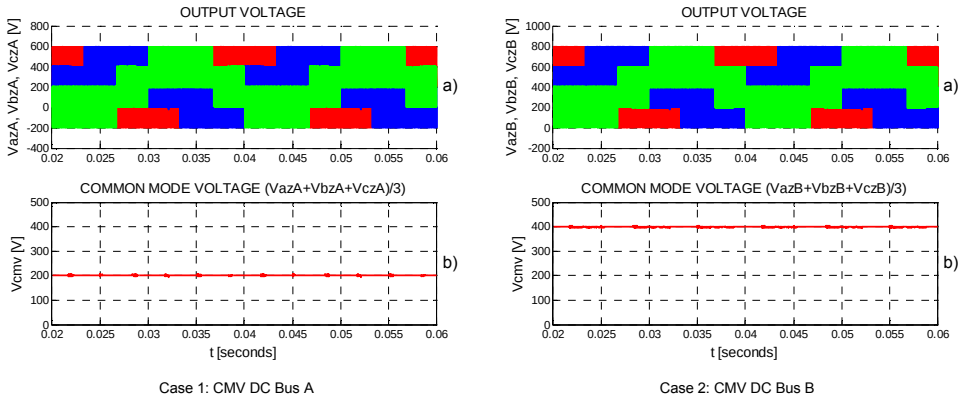


Figure 3.25. CMV in the FB10 topology; Case 1: a) Output voltage respect to a common point "zA" (zA is the negative terminal of the V_{dcA}), b) CMV measured using equation (3.19). Case 2: a) Output voltage respect to a common point "zB" (zB is the negative terminal of the V_{dcB}), b) CMV measured using equation (3.20).

In Chapter 4 some other modulation strategies will be explained and a comparative analysis regarding losses, total harmonic distortion and efficiency will be performed.

The performance of the FB10 topology was also tested experimentally in the lab. An experimental setup was built using IPMs (Intelligent Power Modules) from Mitsubishi. The selected module was the PM75DSA120 (Ic = 75 Amp and Vce = 1200V), as in the single-phase experiments conducted in Chapter 2. Figure 3.26 depicts the general scheme of the experimental setup used to test the performance of the FB10 topology.

In Figure 3.26 an autotransformer was used to set a variable voltage from the grid voltage. This autotransformer presents the capability of boosting the AC voltage further than 400 Vac. The output of the booster is connected to the primary of two 1:1 transformers to achieve isolation from the AC grid. The output of these transformers is connected to a pair of three-phase rectifiers with a LC filter in order to create the two independent DC bus voltage sources, i.e., de DC bus A (V_{dcA}) and the DC bus B (V_{dcB}). The switches S7a, S8a, S7b and S8b of the FB10 topology of Figure 3.26 were implemented by using an ultrafast diode in series with an IGBT (switch with anti-parallel diode). This series connection is necessary because the IPM IGBT has an anti-parallel diode that can give rise to some current paths to discharge the parasitic capacitances in some stages of the modulation strategy. In order to

ensure a proper operation of the FB10 topology, it is recommended to use unidirectional switches to control the connection of the DC bus. Figure 3.27 shows a picture of the different elements used in the experimental setup.

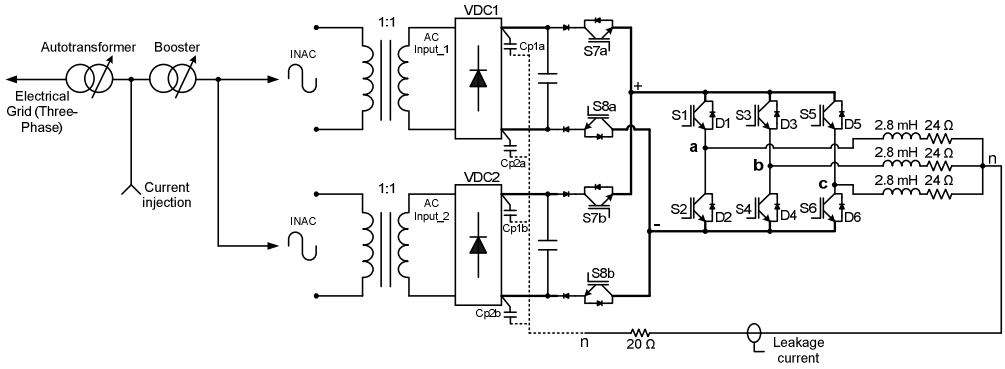


Figure 3.26. Scheme of the experimental setup of the FB10 topology.

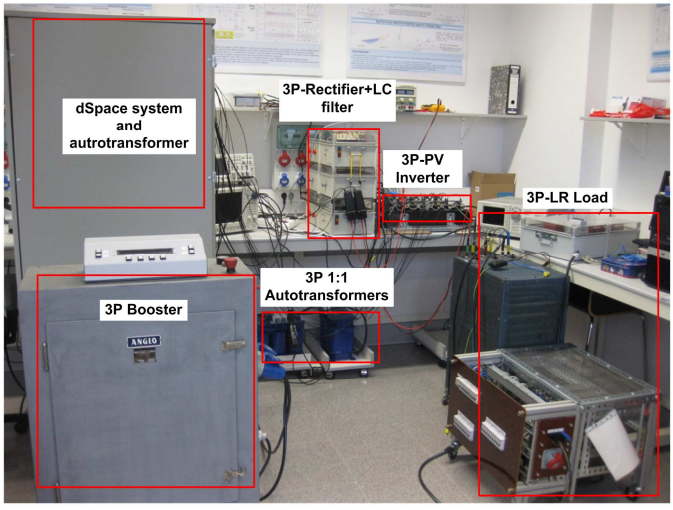
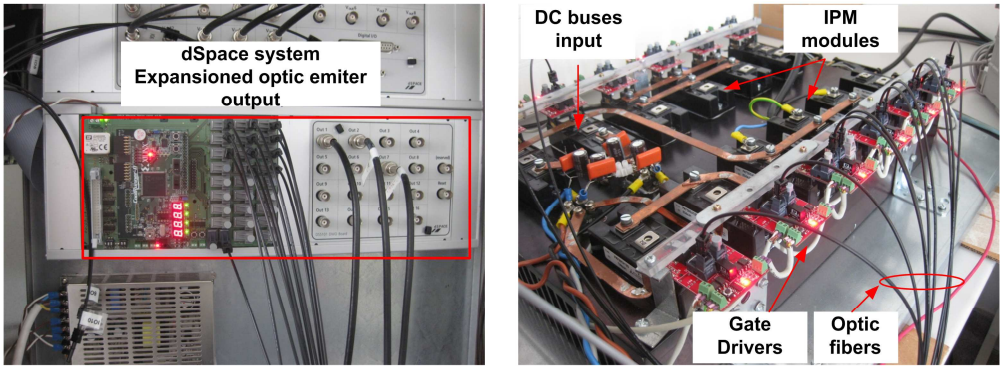


Figure 3.27. Experimental setup of the FB10 topology.

The signals to control the power modules were programmed by using C code in a 1006 dSpace system. These signals were connected to the IGBT modules by using optic fibers to ensure a proper isolation, see Figure 3.28 a). Over-current, over-voltage and over-temperature protections where also implemented in the experimental prototype. A detail of the prototype constructed to evaluate the performance of the FB10 topology can be seen in the Figure 3.28 b).



a) b)

Figure 3.28. Detail of the three-phase transformerless FB10 inverter.

To test the performance of the FB10 topology in terms of common mode currents, a small capacitance (150nF) was connected in each terminal of both DC buses (C_{p1a}, C_{p2a}, C_{p1b} and C_{p2b}), as it is shown in Figure 3.26. The common point connection between the "stray" capacitances was connected to the neutral point of the load by using a small impedance. In this case, a resistor with a value of 20 ohms was used. In general, the experimental setup presents the same parameters as the circuit considered in the simulations.

Figure 3.29 shows some experimental results obtained by using the modulation strategy previously explained. As can be observed in this figure, the waveform of the load currents is quiet similar to that ones that were obtained in the simulation results, with the characteristic unbalance ripple, see Figure 3.29 a). The voltages across the stray capacitances are almost constant, like in the simulation, but in this case some small oscillations appear. These oscillations are due to the resonances between the passive elements in the circuit, but it does not affect in a significant way the behaviour of the leakage ground current, see Figure 3.29 b). The waveform of the leakage ground current, Figure 3.29 c), shows that the maximum peak is around 50 mA, this signal includes the noise add it by the current sensor. Moreover, the maximum value in the frequency spectrum of this current is lower than 50 mA, as shown in Figure 3.30. This means that the leakage current characteristic fulfils the requirements set by the standard VDE 0126-1-1.

Some other modulation strategies for the FB10 topology will be presented in Chapter 4. A detailed analysis regarding power losses distribution, harmonic distortion and efficiency will be provided. Simulation and experimental results will be performed in order to evaluate the performance of the proposed modulation strategies.

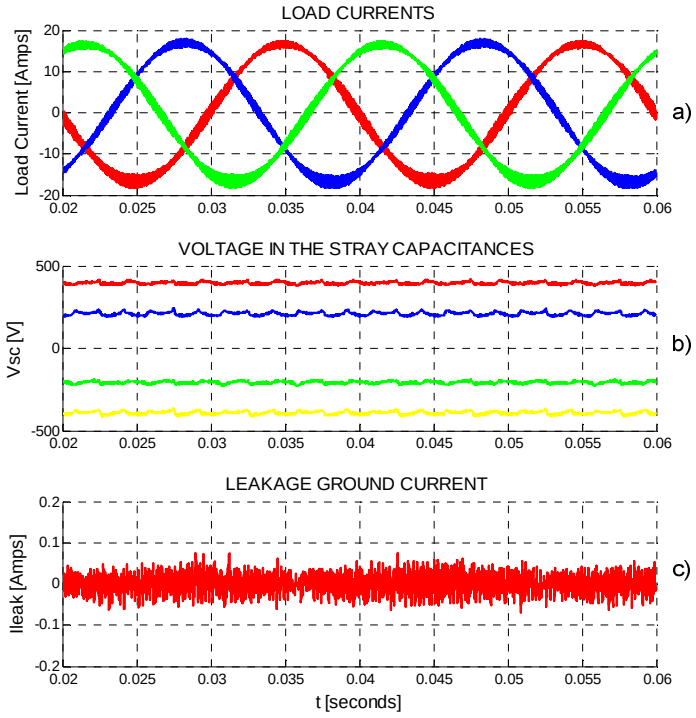


Figure 3.29. Experimental results of the FB10 topology.

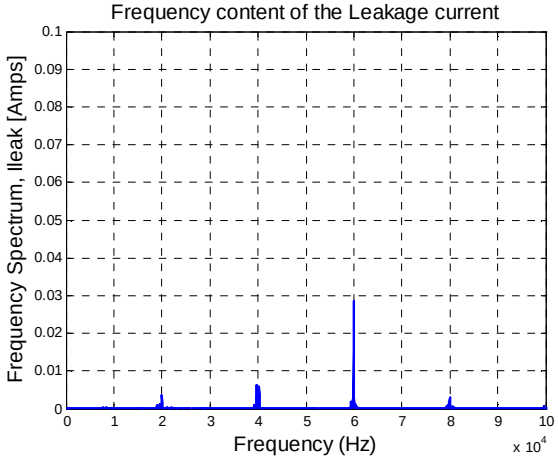


Figure 3.30. Experimental frequency spectrum of the leakage current.

3.5. Conclusions

From the analysis conducted in this chapter, it can be concluded that the new FB10 topology can be a very suitable solution in the case of the three-phase transformerless PV inverters. As it explained in this chapter, the main idea supporting the FB10 topology consists in isolating the vectors that generates 1/3 Vdc of CMV from the ones that generate 2/3 Vdc. This idea allows obtaining a system with no common mode currents, since the CMV is constant. This is the main advantage of the FB10 topology. On the other hand, the utilization of the DC buses is the same as in the case of the conventional two-level three-phase inverter with SVM.

Regarding power losses, it is logic to expect that they will be low, thanks to the way in which the modulation strategy has been designed. It can be expected that the main power losses will come from the switches that are controlling the connection of the DC buses because they experience a hard switching during the turn-OFF. The full-bridge switching state changes during the zero vector states, with all the switches changing simultaneously at zero blocking voltage, which leads to low power losses.

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CHAPTER 4.

Modulation strategies for FB10 topology

Space vector modulation [4.1], [4.2], [4.3], [4.4], [4.5], [4.6] was the background technique for designing the modulation strategies for the FB10 three-phase PV inverter. As the SVM technique allows several combinations in setting the vectors sequence during the switching period, some different modulation strategies can be proposed to control the FB10 topology. In this chapter, four different modulation patterns based on SVM are presented. The modulation strategies are mainly derived from the modulation strategy presented in Chapter 3. In order to compare the performance of each modulation pattern, an analysis considering the power losses in the semiconductors and the waveform quality of the output current was performed. The power losses were analyzed by simulation, using the Thermal Module toolbox of PSIM® and experimentally measured by using a precision power meter. The results obtained from these evaluations were quantified in terms of Efficiency, and THD.

4.1. Unsymmetrical Zero Placement SVM (UZP-SVM)

The Unsymmetrical Zero Placement SVM (UZP-SVM) was already presented in Chapter 3, it is called in this way because the DC bus A has more switching transitions than DC bus B during a switching period. Figure 4.1 presents the line current and phase voltage for a switching period. Note that in the phase voltage (Figure 4.1 at the bottom) a 400 V value which represents the connection of the DC bus A source appears twice in the switching cycle, while the 200V value, which represents the connection of the DC bus B appears just once. For this reason, the current (Figure 4.1 top) presents a long rising time and two short

falling times during the switching period. This behaviour results in an unsymmetrical ripple at the output waveform. This behaviour will be discussed later.

Other three modulation strategies based on the same concept introduced by the UZP-SVM are proposed in the following. These schemes were proposed to solve the unsymmetrical ripple caused by the unsymmetrical zero placement, which sets a different number of switching transitions for each DC bus in each switching period.

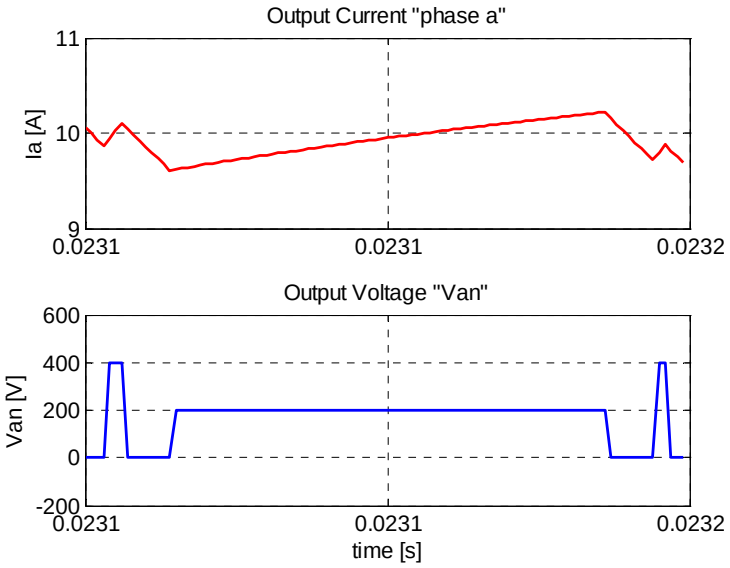

Figure 4.1. Ripple details for the UZP-SVM technique.

4.1.1. Description of the UZP-SVM strategy

As aforementioned, the UZP-SVM strategy was introduced in Chapter 3. Additional results will be presented here by using the same experimental setup. Figure 4.2 shows the experimental results of the modulation signals.

In Figure 4.2, the modulation signals for the DC side and the leg A switches are shown. The plots represents, from top to bottom the modulation signals of the DC bus A (S7a), DC bus B (S7b), leg A upper switch (S1) and leg A lower switch (S2), respectively. The lower four plots are a zoom of the previous ones. Note how the switches S1 and S2 are switched at the same time during the null vectors (Zero Voltage Switching, nor S7a neither S7b are switched ON). The switches S7a and S7b provide the active vectors when each of them is ON. Also note, how the switch S7a has four switching transitions during a switching period while switch S7b has only two; therefore the switching losses will be greater in S7a.

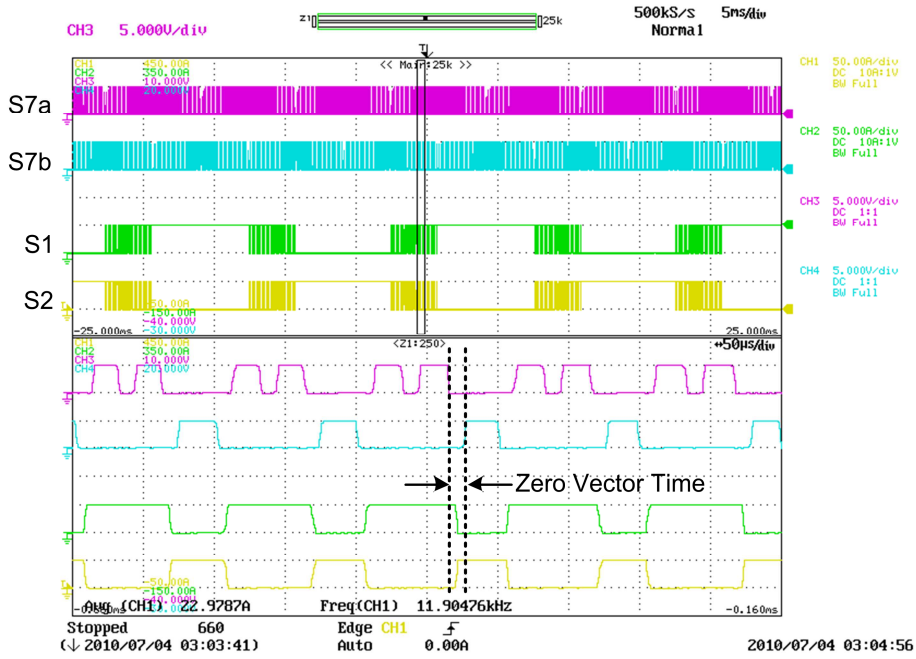

Figure 4.2. Experimental results of the UZP-SVM strategy.

4.1.2. Losses analysis

The power losses are concentrated in those switches that control the DC sources (namely, S7a, S7b, S8a and S8b) because of their hard switching transitions. In this section, the voltage that is blocked by the abovementioned switches during each modulation state is analyzed. Figure 4.3, shows the equivalent circuit for the DC side, during a zero vector (with the DC sources, both isolated from the load).

The CMV referred to the negative terminal of the DC bus A (Vdc) is 1/3 of the Vdc when an active vector is applied to the load, as a consequence the voltage over the C_{p2a} will be -1/3 Vdc. Analyzing the circuit formed by C_{p2a}, V_{dc} and C_{p1a} (Figure 4.3 a), using the Kirchhoff's voltage law it is possible to know that:

$$V_{Cp1a} = 2/3V_{dc}. \tag{4.1}$$

According to the analysis described above, and doing the same for the DC bus B, the blocked voltage by the switches S7a and S7b is 1/3 Vdc, and the voltage that is blocked by the switches S8a and S8b is 2/3 Vdc (the same voltage appears over the stray capacitances during the zero vector because the DC bus is isolated), this means that the losses will be different for each pair of switches of each DC bus. Moreover, some additional differences in

the power losses distribution will be introduce by the modulation strategy, due to the different switching frequency of each DC bus.

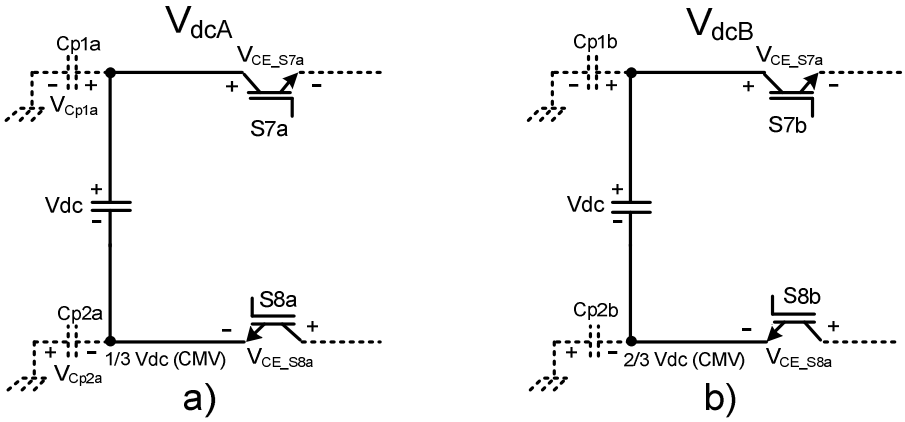

Figure 4.3. Equivalent circuits on the DC side when a null vector is applied to the load.

The losses were calculated using the "Thermal Module" from PSIM®. This software permits to calculate the switching and conduction losses for the IGBT´s and diodes. The software uses equation (4.2) to calculate the conduction losses across the diode [4.7]:

$$P_{cond\_cal} = V_d \cdot I_F \,, \tag{4.2}$$

where V_d is the diode voltage drop and I_F is the diode forward current.

In the case of the switching losses, the diode turn-ON losses are neglected. The diode turn-OFF losses due to the reverse recovery effect may be calculated in two different ways (depends on the available dates),

$$P_{sw\_off} = E_{rr} \cdot f \tag{4.3}$$

or

$$P_{sw\_off} = \frac{1}{4} \cdot Q_{rr} \cdot V_R \cdot f \,, \tag{4.4}$$

where E_{rr} are the reverse recovery energy losses, Q_{rr} is the reverse recovery charge, V_R is the reverse blocking voltage, and f is the frequency. The frequency can be defined basically in two ways: being this, the grid frequency or the switching frequency, in the first case the

losses will be calculated along a grid period and in the second case the losses will be calculated for a switching period. Parameter Q_{rr} can be defined as

$$Q_{rr} = \frac{1}{2} \cdot t_{rr} \cdot I_{rr} . \tag{4.5}$$

The conduction losses of the IGBT can be calculated from equation (4.6) [4.8],

$$P_{cond\_cal\_Q} = V_{ce(sat)} \cdot I_C , \tag{4.6}$$

where $V_{ce(sat)}$ is the collector-emitter saturation voltage on the transistor, and I_C is the collector current.

The switching losses computation is based on the dissipated energy during the turn-ON and turn-OFF transitions, the equations may be written as follow:

$$P_{turn\_on} = E_{on} \cdot f \tag{4.7}$$

and

$$P_{turn\_off} = E_{off} \cdot f , \tag{4.8}$$

where E_{on} are the transistor turn-ON energy losses, E_{off} are the transistor turn-OFF energy losses and f is the frequency. The losses in the antiparalell diode of the IGBT are calculated as explained above for the discrete diode [4.9].

In Figure 4.4 is shown a bar graph of the losses across all the switches and diodes of the converter. The losses are ordered by device, for instance at the upper left corner, the losses for the switch S1 appear. The first bar represents the switching losses of S1 (which are close to zero in this case), in the second bar are the conduction losses of S1, moreover the switching losses of the antiparalell diode appears and also the conduction losses, finally there are three bars that represent (in this order), the total losses of the switch S1, the total losses of the antiparalell diode D1 and the total losses of the IGBT (S1 plus antiparalell diode D1). The same order representation has been done for all the devices in the two first rows. The first six groups (two first rows), are the losses in the full-bridge circuit. And the next two rows are the losses for the switches and auxiliary diodes in the DC buses.

In general the losses in the devices that are forming the full-bridge inverter (S1, S2, S3, S4, S5 and S6) are very low; because of the zero voltage switching of the switches.

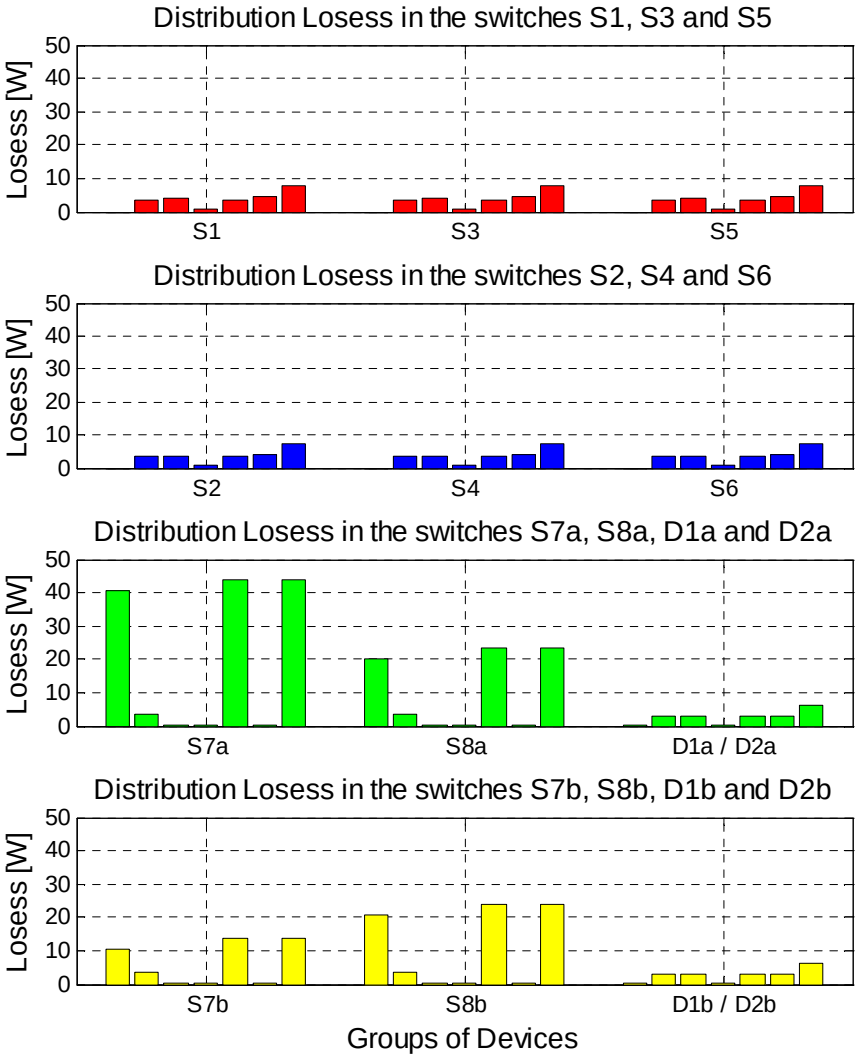

Figure 4.4. Distribution losses in the FB10 topology using UZP-SVM strategy.

On the contrary if the two second rows are observed, the losses are higher than in the previous case because of the hard switching in the DC switches. It should be note that the losses are no equal over the four switches, this is because of two main reasons: one of them is the blocking voltage in each switch, as it was explained earlier in this chapter, the blocked voltage by the switch S7a is 2/3 Vdc and the blocked voltage by the switch S8a is 1/3 Vdc.

The second reason is that there are more switching cycles for the switches S7a and S8a than for the switches S7b and S8b. Finally, the losses distribution for the auxiliary diodes has been also included. In this last case the bars are distributed in a different way than in the rest of the devices. The switching losses of one diode, for instance for D1a, are in the first column, the conduction losses are in the second column, the total losses for this device are in the third column and in the last column (at the right) are shown the losses of D1a plus D2a. The same order has been implemented for the other three diodes. As can be seen for these diodes, the power losses are mainly conduction losses and they are low, although they may affect the total efficiency.

It should be remarked that the model of the switch was adjusted experimentally. The IPM was tested under the same conditions than for the simulation. In this experiment the losses were measured using a precision power meter and the circuit used for the test was a half-bridge converter.

4.1.3. Efficiency and power quality

The efficiency is perhaps the most important parameter of the proposed PV topology. In PV applications the power inverter should take the most of the energy generated by the PV panel, because if the power conversion efficiency is small, the power generated by the PV panel cannot be injected into the AC utility system effectively. Thus, it is necessary to increase the power conversion efficiency as high as possible. In order to evaluate accurately the efficiency of the proposed converter, the effect of the shadows over the total output power must be taking into account; the reason to do this is because the output power is changed by the magnitude of the solar irradiation. In this regard the time at which the power rating is less than the nominal power is longer. This means that the inverter efficiency should be high over an extensive output range. In the case of the proposed topology, the efficiency was evaluated using simulations and also experimentally using the equation (4.9) [4.10], [4.11].

$$\eta = \frac{P_{out}}{P_{inA} + P_{inB}}. \tag{4.9}$$

The power measurements in equation (4.9) were considered just taking into account the semiconductor power losses (in the case of the simulation). The efficiency measured for the first modulation strategy by means of simulation was 98.55% with a power range around 6 kW. The same measuring was done (with a precision power meter) for the experimental test; the result indicates 95.9 % for the same power range.

The quality of the output current was evaluated using a power analyzer and also for the simulation test. The total harmonic distortion obtained by simulation was 0.07%. On the other hand in the case of the experimental measurement was 1.9%. Both measurements indicate that the output current waveform is almost sinusoidal and full fill the grid standard requirements.

4.2. Symmetrical Zero Placement SVM (SZP-SVM)

The Symmetrical Zero Placement Space Vector Modulation (SZP-SVM) introduces two additional switching transitions in the DC bus B bringing as a result a symmetrical ripple in the output current as it will be show below. Knowing that the switching in the IGBT´s controlling the DC buses is hard, it should be expected that the switching losses will be increased. On the other side the quality of the output current could be improved because of the symmetrical ripple. In the next subsections, it will be explained in detail the advantages and disadvantages of this modulation strategy.

4.2.1. Description of SZP-SVM strategy

The modulation signals of the SZP-SVM strategy are depicted in the Figure 4.5. As can be seen, the sequence used is: V10-V11-V10-V20-V21-V20-V20-V21-V20-V10-V11-V10, basically the idea is to introduce a zero vector in the middle of the switching period, in this way both DC buses have the same number of switching transitions and the current ripple can be symmetric. This modulation strategy keeps the same soft switching characteristic for full-bridge legs.

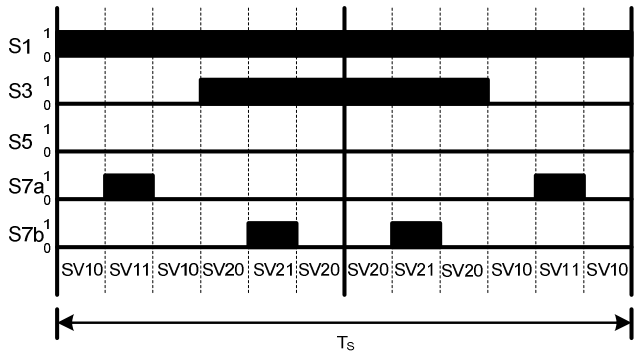

Figure 4.5. Modulation signals for SZP-SVM strategy.

In Figure 4.5 note how the signals for the switches S7a and S7b have the same number of ON-OFF and OFF-ON transitions, also it can be noted that another zero vector appears at the middle of the switching period (SV20). In order to show the current ripple of this modulation strategy the load currents obtained by simulation are depicted in Figure 4.6.

In this modulation, the phase voltage (Figure 4.6 at bottom) has during two short periods the 400 V value, which represents the connection of the DC bus A and appears twice in the switching cycle, and also the 200V value which represents the connection of the DC bus B appears twice. For this reason, the line current (Figure 4.6 top) presents two periods where is increasing and two short periods where is decreasing. This behaviour results in a symmetrical ripple and solves the unsymmetrical ripple caused by UZP-SVM strategy.

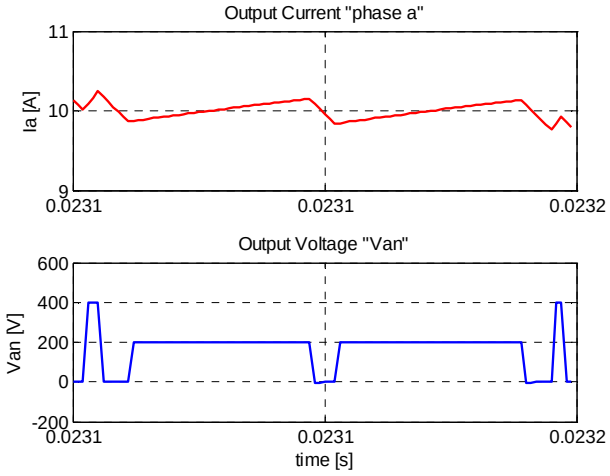

Figure 4.6. Current ripple for the SZP-SVM strategy.

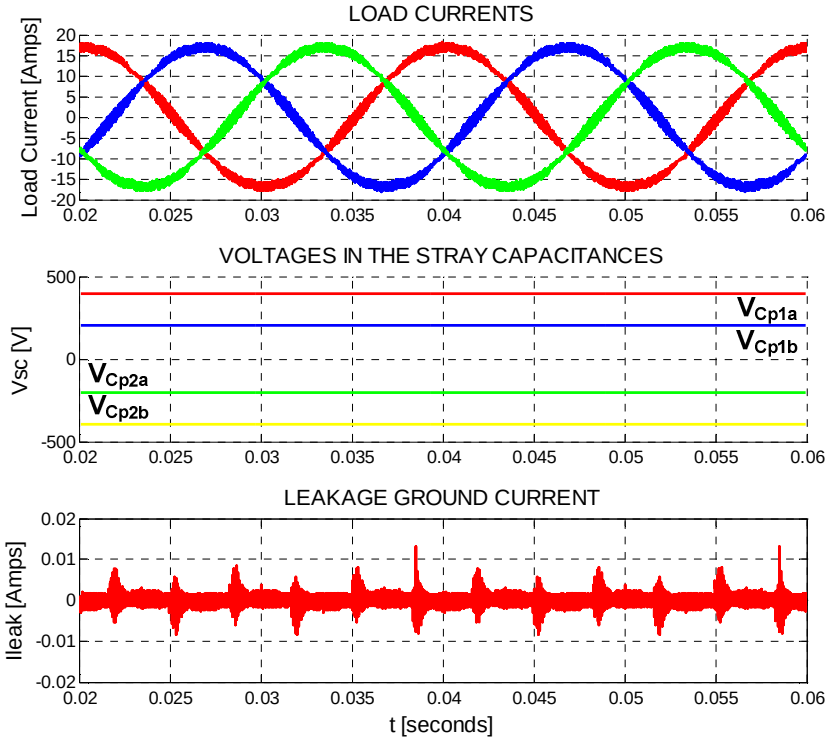

Figure 4.7. Simulation results for the FB10 topology, a) Load currents, b) Voltages across the stray capacitances (C_{p1a}, C_{p2a}, C_{p1b} and C_{p2b}), c) Leakage ground current.

Simulations results for the SZP-SVM are shown in Figure 4.7. The load current is presented in Figure 4.7 a), each phase has a sinusoidal performance and its peak value is around 15 A. The voltage across the stray capacitances, which is constant, is shown in Figure 4.7 b). As these voltages are constant, the leakage ground current is close to zero as it is shown in Figure 4.7 c).

This modulation strategy was also implemented in the experimental setup.The modulation signals for DC side and switches of the leg A are shown in Figure 4.8. Similarly to the previous modulation strategy, from top to bottom the plots are representing the modulation signals of DC bus A (S7a), DC bus B (S7b), leg A upper switch (S1) and leg A lower switch (S2), respectively. Note in this figure, how the modulation signals of both DC buses, S7a and S7b, have two pulses in each switching period and the switches S1 and S2 are switched at the same time during the null vectors.

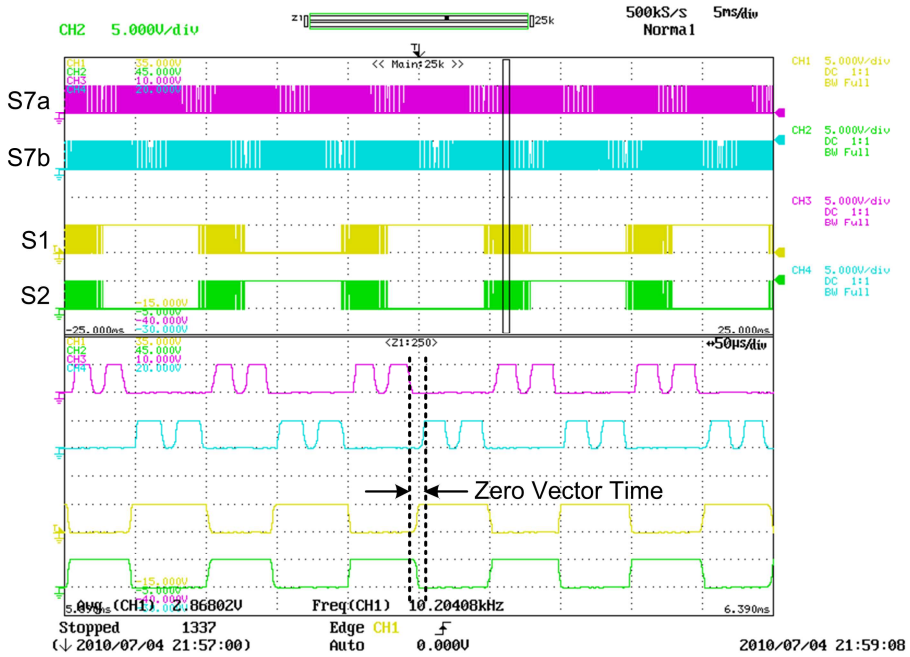

Figure 4.8. Experimental results of the SZP-SVM strategy: Modulation signals.

The experimental results for the load currents, voltages across the stray capacitances and leakage ground current are shown in Figure 4.9 a), b) and c) respectively, all of them are in good agreement with the simulated ones.

The frequency spectrum of the leakage ground current is presented in Figure 4.10. Note the low magnitude of the different harmonic components. As a result the leakage current characteristic fulfils with the standard requirements.

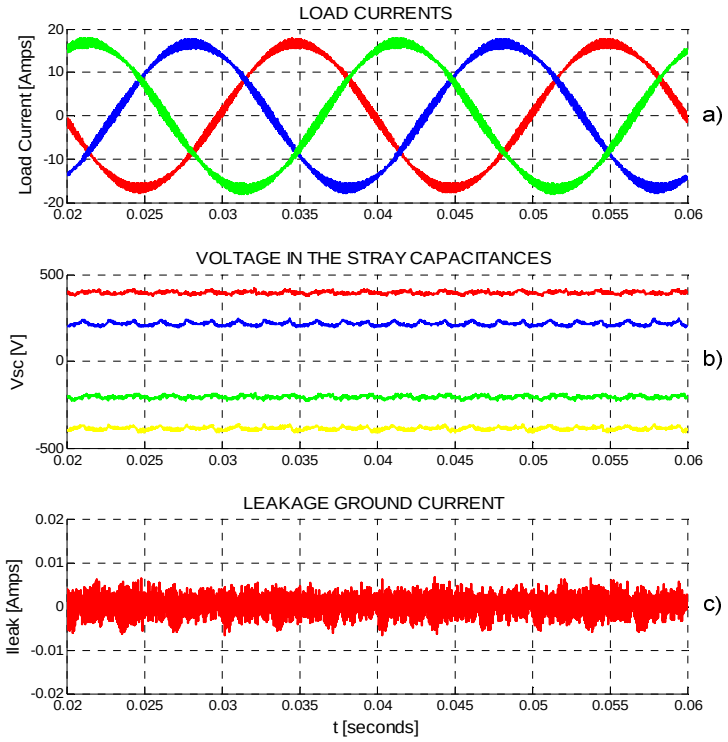

Figure 4.9. Experimental results of the SZP-SVM strategy: a) Load currents, b) Voltage in the stray capacitances and c) Leakage ground current.

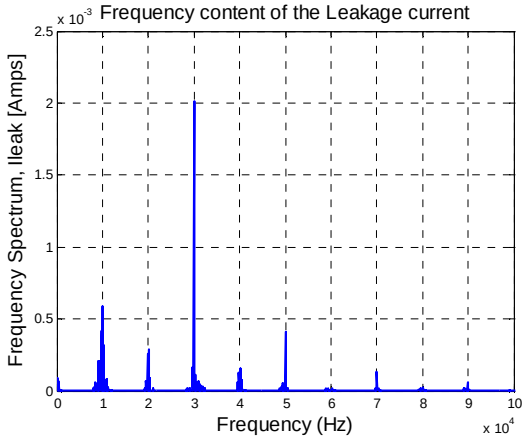

Figure 4.10. Experimental frequency spectrum of the leakage ground current for SZP-SVM strategy.

4.2.2. Losses analysis

As in the previous case, the losses were evaluated using the *Thermal Module* toolbox from PSIM®. In this case the simulation results are depicted in Figure 4.11

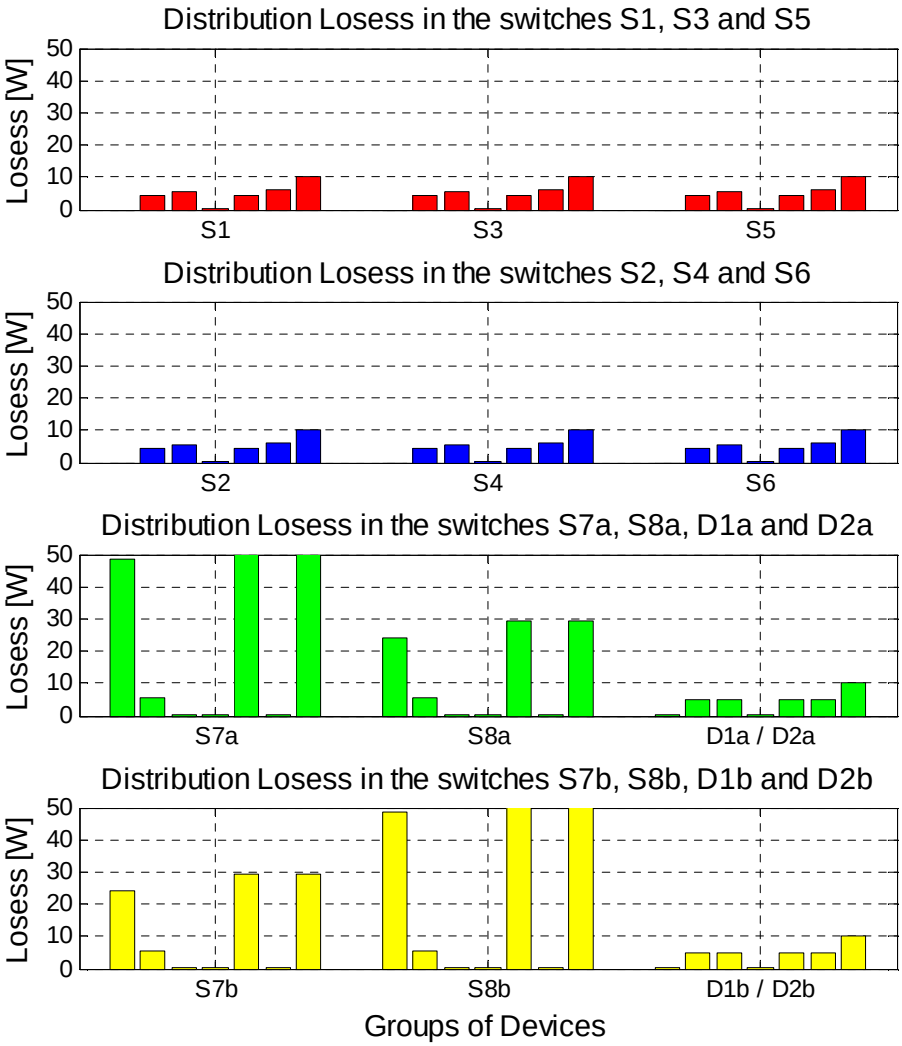

Figure 4.11. Distribution losses in the case of the SZP-SVM strategy.

Figure 4.11 shows the power losses distribution for each IGBT and diode in the FB10 topology modulated using the SZP-SVM strategy. As it can be seen, the losses along the first six switches that correspond to the full-bridge circuit have a similar losses distribution profile. The power losses across these devices is also very similar to that ones in the UZP-SVM strategy, again the turn-ON and turn-OFF transitions of these devices is done with zero voltage, therefore just the conduction losses are appreciable. The losses are concentrated in the switches that are controlling the DC buses (S7a, S8a, S7b and S8b) mainly due to the switching losses. The total losses in the case of switch S7a are higher than the losses in the switch S8a, this is due to the difference in the blocked voltage in each switch (S7a blocks 2/3 Vdc and S8a blocks 1/3 Vdc). On the other hand, the opposite situation happens with the other DC bus, while S7b blocks 1/3 Vdc, switch S8b blocks 2/3 Vdc. This means that switch S7b will have higher losses than switch S8b, as it is show in the previous figure. One detail that should be commented is that there are not power losses in the anti-parallel diodes of the switches S7a, S8a, S7b and S8b, this is due to the fact that the current flows just in one direction, from the power supply to the load. Another thing that should be observed is that the power losses in the switches S7a and S8b are almost equal; this is due to the addition of the null vector in the middle of the switching period. Finally, the power losses in the auxiliary diodes are depicted in the groups labeled as D1a/D2a and D1b/D2b. These diodes are not very significant because in the optimization process they will be eliminated.

4.2.3. Efficiency and power quality

The efficiency was evaluated in the same way than in the previous case. The same equations and power level (6kW) was used to quantify the power losses. In this case the results indicate that the efficiency was 98.65% due to the additional hard switching introduced by the additional zero vector. In the case of the efficiency measure in the experimental setup the results indicates a value of 94.97%.

The quality of the output current was evaluated for the simulation test and also for the experiments using the power analyzer equipment. The THD obtained by simulation was 0.06%. On the other hand in the case of the experimental measurement, the THD was 1.8%. These two measures obtained provide a good idea about the quality of the output current waveforms. The main cause of distortion in the current waveforms is the ripple whose magnitude depends of different factors such as; switching frequency, load, modulation strategy, filtering, etc. The ripple effect may be reduced introducing an LCL filter in the grid connection.

4.3. Combine Zero Placement SVM (CZP-SVM)

The CZP-SVM is called in this way because the odd or even starting vector is swapped at each switching period, as a consequence the zero vector position and the double switching transitions of the DC bus switches are swapped each time step. Thus not additional switching losses will be introduced in the total quantification of the power losses. In addition the power losses in the DC bus switches can be shared better than in the first modulation strategy. In contrast the signal quality will be affected because of the swapping. In the next sections the modulation strategy will be described in detail.

4.3.1. Description of the CZP-SVM strategy

In the CZP-SVM strategy the vectors sequence is swapped each switching period, this means that the sequence of the vectors will be: V10-V11-V10-V20-V21-V21-V20-V10-V11-V10 during a switching period and V20-V21-V20-V10-V11-V11-V10-V20-V21-V20 in the next one. Thus the vectors sequence will be swapped from the first sequence to the second sequence and vice-versa each switching period. The modulation signals are depicted in Figure 4.12.

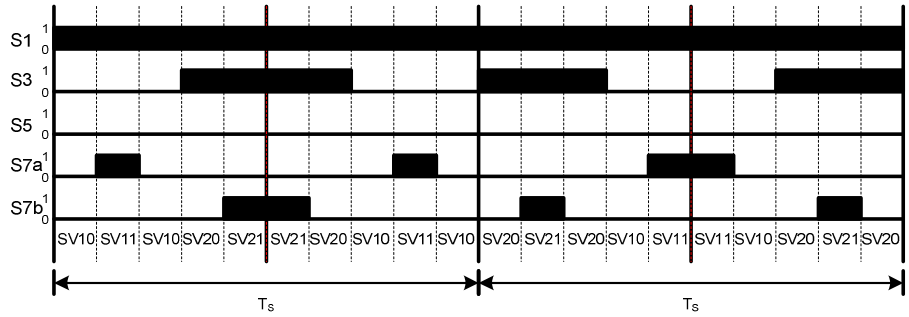

Figure 4.12. Modulation signals of the CZP-SVM strategy.

The vector sequence shown in Figure 4.12 permits to obtain a quasi-symmetrical average ripple for the load currents, i.e., the ripple is changing from a big one to two small ones in each switching period for each DC bus. The resulting ripple of the swapping between the two modulation sequences will be a mix with a higher magnitude in a switching period than in the other one.

Figure 4.13 depicts the simulation results for the CZP-SVM. The load current presented in Figure 4.13 a) has a sinusoidal behaviour and same amplitude as in the previous modulation strategy. The voltage across the stray capacitances which is also constant is shown in Figure 4.13 b). As it was concluded before, the leakage ground current is close to zero as it is shown in Figure 4.13 c).

As in the previous cases, the modulation strategy was also implemented in the experimental setup and the results are shown in Figure 4.14.

In Figure 4.14 the modulation signals for the switches S7a, S7b, S1 and S2, are shown respectively. Note that in the switches S7a and S7b (plots at the top) the vector sequence is changed each period, in this case the S1 and S2 switches are also following the swapping in the vector sequence.

The sinusoidal load currents, constant voltages in the stray capacitances and close to zero leakage ground current are shown in Figure 4.15 a), b) and c) respectively.

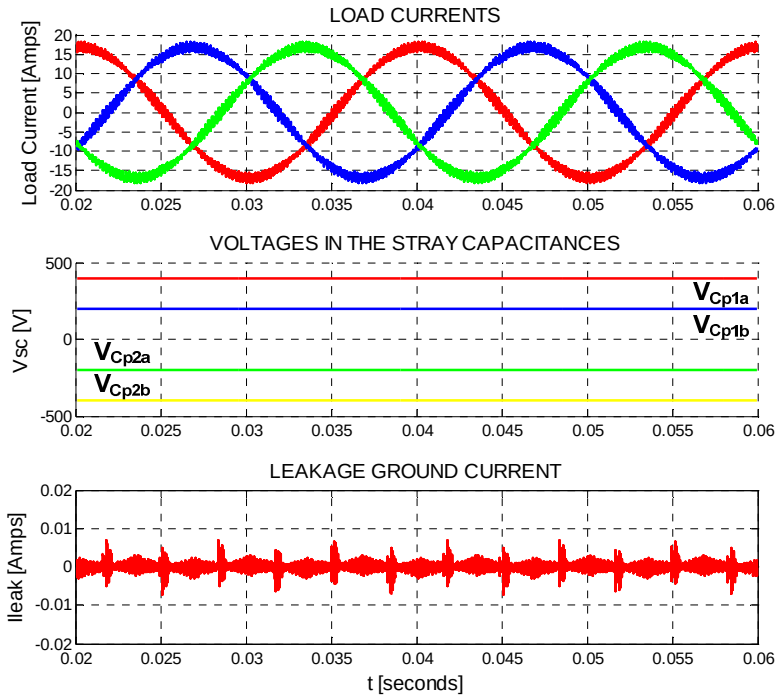

Figure 4.13. Simulation results for the FB10 topology, a) Load currents, b) Voltages across the stray capacitances (C_{p1a}, C_{p2a}, C_{p1b} and C_{p2b}), c) Leakage ground current.

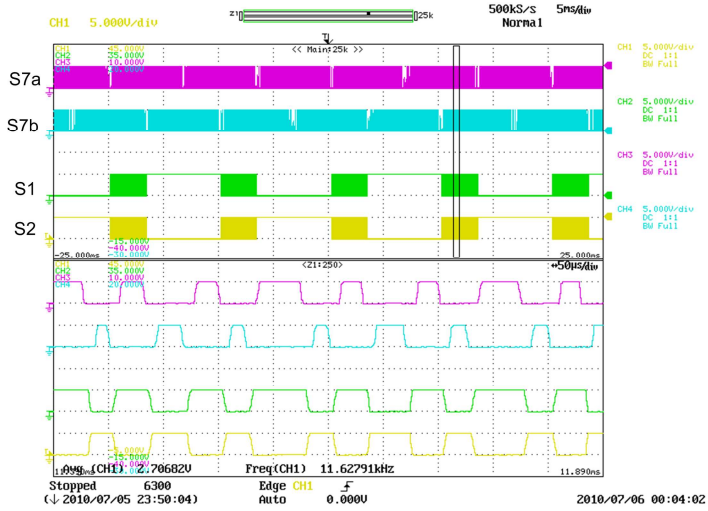

Figure 4.14. Experimental results of the CZP-SVM strategy: Modulation signals.

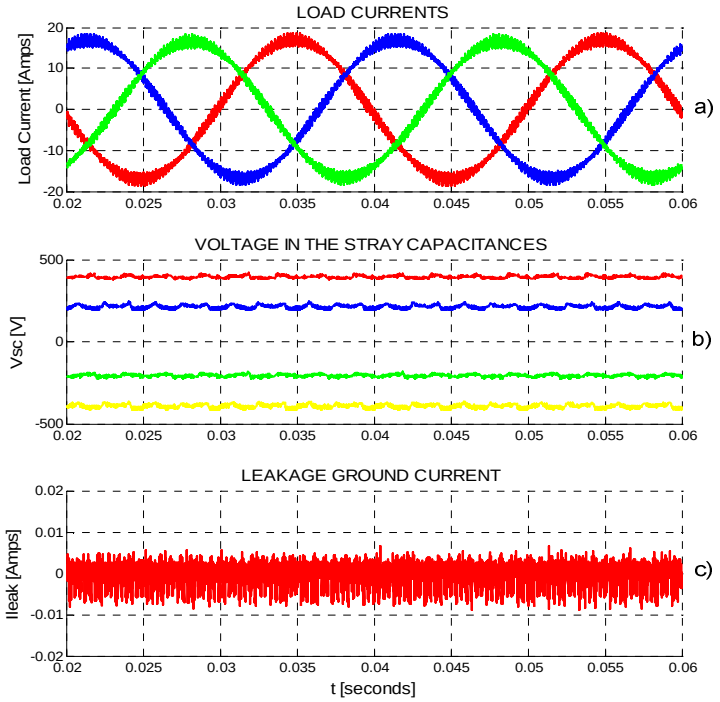

Figure 4.15. Experimental results of the CZP-SVM strategy: a) Load currents, b) Voltage in the stray capacitances and c) leakage ground current.

For the CZP-SVM, the spectrum characteristics of the leakage ground current are shown in Figure 4.16.

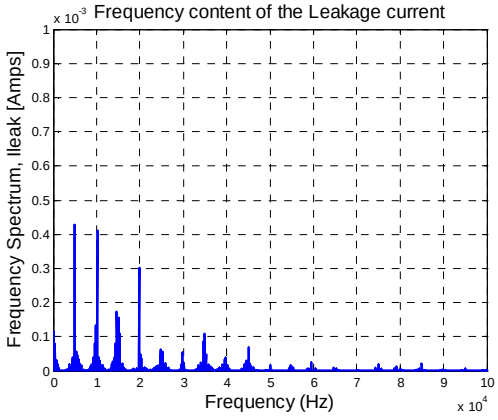

Figure 4.16. Experimental frequency spectrum of the leakage ground current for CZP-SVM strategy.

4.3.2. Losses analysis

In order to know how the distribution power losses are, the power losses evaluation was also performed using the *thermal module* from PSIM®. The simulation results of the power losses distribution are shown in Figure 4.17. These simulations were done using the same parameters than those used for the first two cases in order to perform a fair comparative analysis.

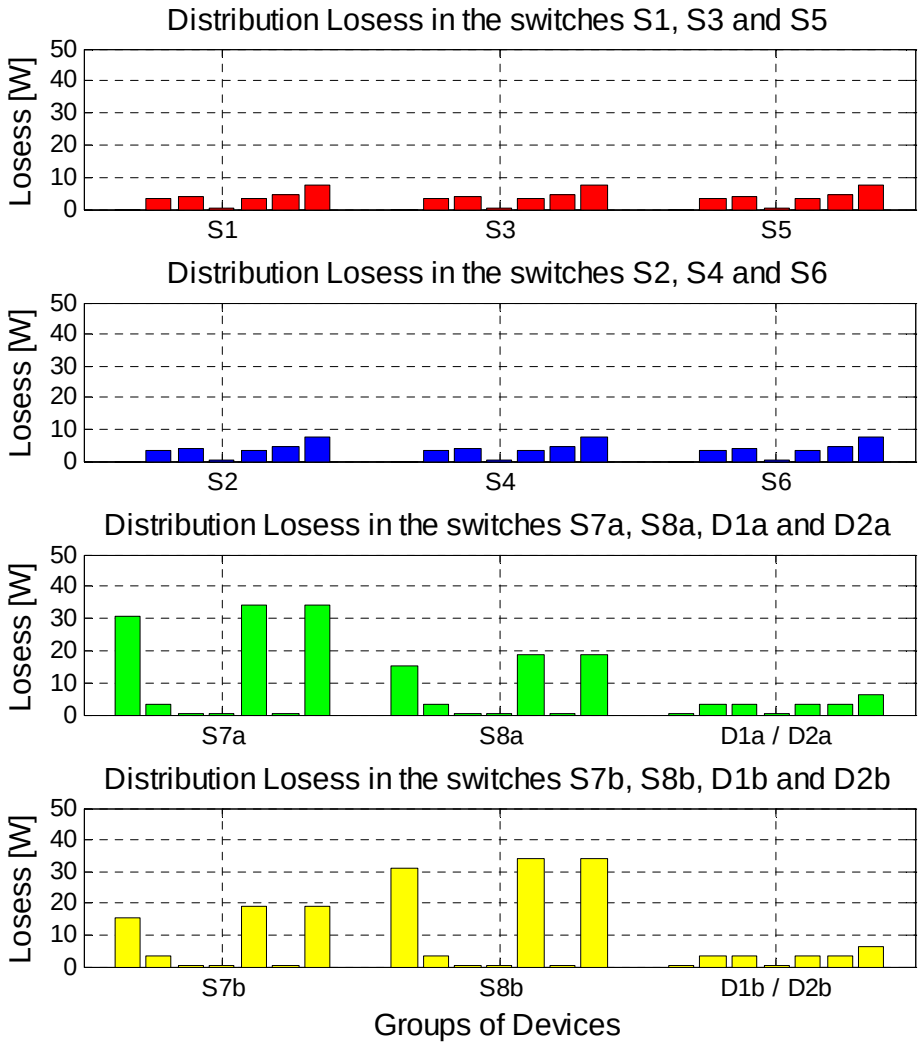

Figure 4.17. Distribution losses in the case of CZP-SVM strategy.

Figure 4.17 permits to observe how the losses are distributed. As in the previous modulation strategies, the power losses in the case of the semiconductors that are forming the full-bridge circuit are very low and there are not switching losses across the IGBT, only some switching losses appear in the case of the anti-parallel diodes. Moreover as expected, the major power losses were again for the switches S7a, S8a, S7b and S8b. In this case, the distribution of the power losses were according with the blocking voltage for each switch, switches that are blocking 2/3 Vdc will have higher losses that those which are blocking 1/3 Vdc. In addition, due to the way in which the modulation strategy is designed, the losses are lower than in the previous case. This means that the efficiency can be increased, but on the other side the load current quality will be affected.

4.3.3. Efficiency and power quality

The efficiency was evaluated using the results obtained from the IGBT model introduced in PSIM®. The same equations used previously were also used here to calculate the efficiency of the converter just considering the power losses in the semiconductors. The output power of the inverter was 6kW as in the previous cases. The efficiency obtained was 98.56%, as it can be seen this efficiency value is higher than that in the previous case because not additional switching losses are introduced in the circuit. On the other hand, the experimental test indicates that the efficiency was around 95.7% under the same power conditions as for the simulations.

The total harmonic distortion was evaluated for simulation and also in the experimental setup. The results obtained by simulation indicate a THD equal to 0.07% and 1.35% for the experimental case. The experimental and simulations results are below the limits required by the electrical normative.

4.4. Combined Double Zero Placement SVM (CDZP-SVM)

The CDZ-SVM combines the two techniques proposed before, i.e., it uses the vectors sequence swapping and the addition of the null vector in the middle of the switching period. This means that the ripple that can be obtained in this case will be symmetric and the harmonic content will be lower. Moreover, it should be expected that the power losses will be increased because of the additional hard switching in the DC buses.

4.4.1. Description of CDZ-SVM strategy

As aforementioned, the CDZ-SVM strategy consist in the swapping of the vectors sequence and the insertion of the zero vector in the middle of the switching period in order to keep a uniform current ripple with a constant frequency. Then, the sequence of the vectors will be: V10-V11-V10-V20-V21-V20-V20-V21-V20-V10-V11-V10 during a switching period, and V20-V21-V20-V10-V11-V10-V10-V11-V10-V20-V21-V20 for the next one. Thus the vectors sequence will be swapped from the first sequence to the second one and

vice-versa for each switching period. The vectors sequence of this modulation strategy is shown in Figure 4.18.

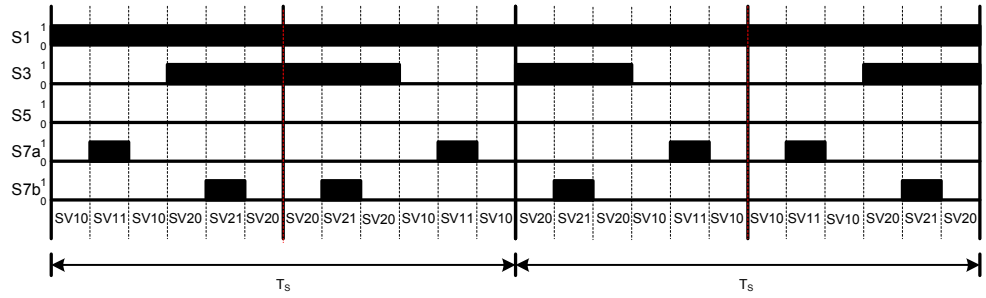

Figure 4.18. Vectors sequence of the CDZP-SVM strategy.

The modulation strategy shown above permits to get good results regarding to the current waveform, but in contrast the additional switching transitions will reduce the total efficiency of the converter.

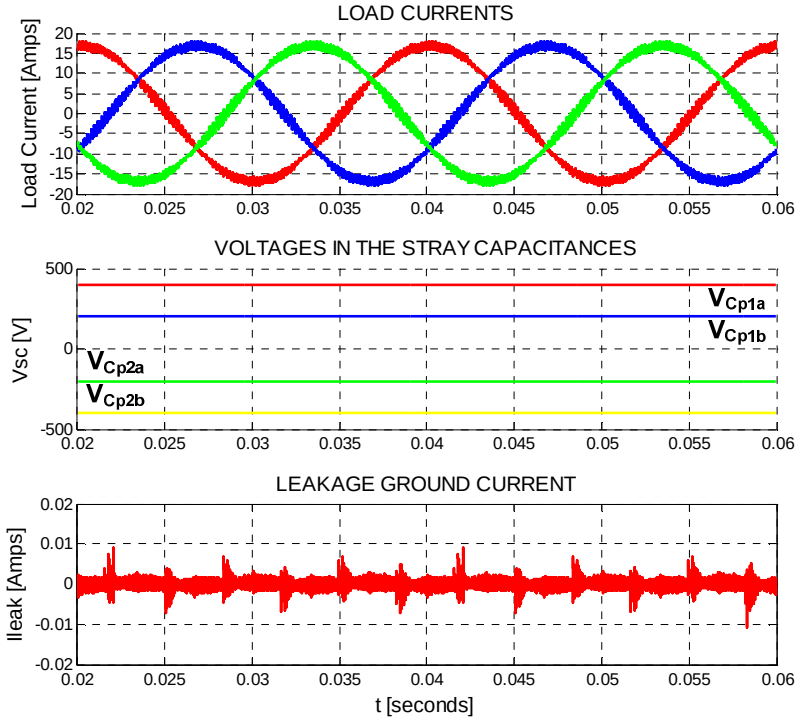

Figure 4.19. Simulation results for the FB10 topology, a) Load currents, b) Voltages across the stray capacitances (C_{p1a}, C_{p2a}, C_{p1b} and C_{p2b}), c) Leakage ground current.

As for the previous modulation techniques, the Figure 4.19 a), b) and c) show the simulations results for the CDZP-SVM for the load current, voltage across the stray capacitances and the leakage ground, respectively. The behaviour is quite similar to that obtained in the above modulation techniques.

This modulation strategy was also implemented in the experimental setup; the results are shown in Figure 4.20

The experimental results depicted in the Figure 4.20 show the modulation signals for the switches S7a, S7b, S1 and S2, respectively. Note that the switches S7a and S7b have the swapping in each switching period and also the zero in the middle of this switching period. The modulation for the switches S1 and S2 follows the vector sequence that is imposed by the switches in the DC bus.

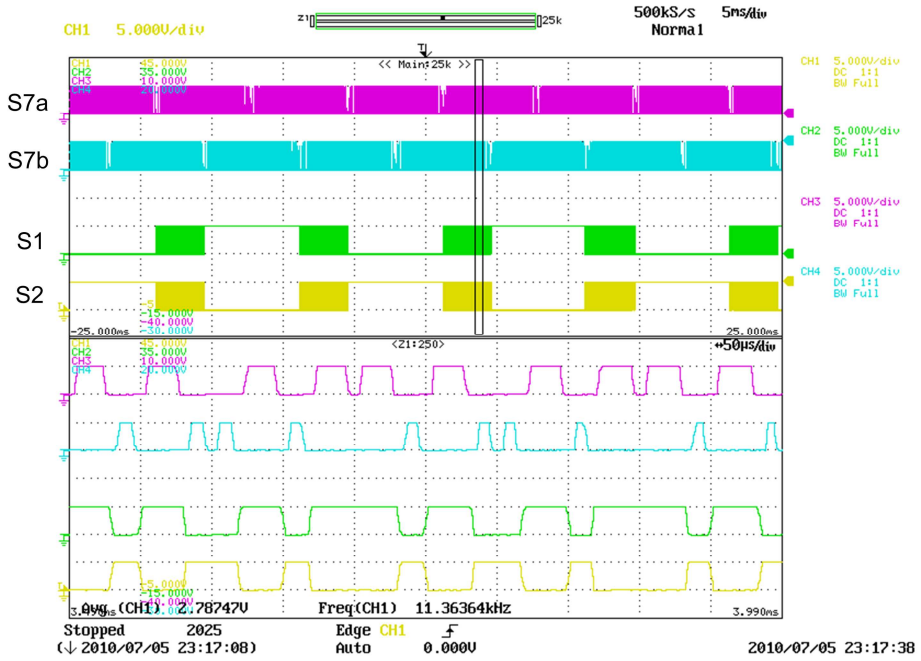

Figure 4.20. Experimental results of the CDZP-SVM strategy: Modulation signals.

Finally additional experimental results for the CDZP-SVM are presented in Figure 4.21, the load currents, voltages in the stray capacitances and leakage ground current are depicted in a), b) and c), respectively. The results are in good agreement with the simulated ones.

Figure 4.22 depicts the frequency spectrum characteristic of the leakage current, which behaves similar to that obtained with the previous modulation techniques.

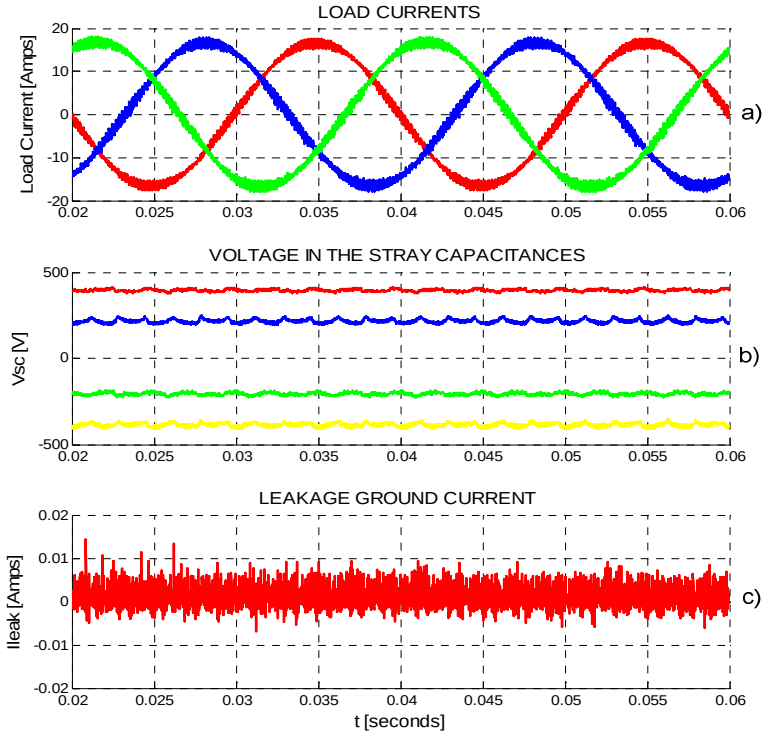

Figure 4.21. Experimental results of the CDZP-SVM strategy: a) Load currents, b) Voltage in the stray capacitances and c) Leakage ground current.

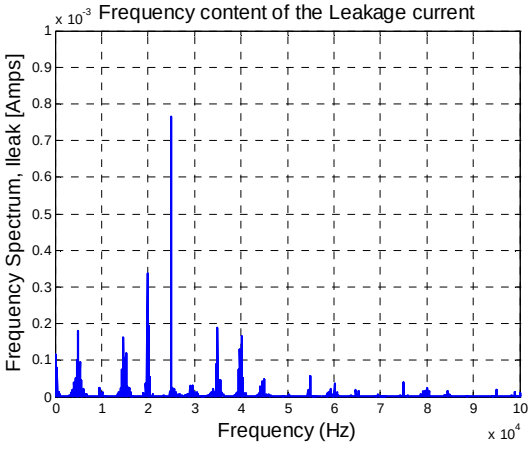

Figure 4.22. Experimental frequency spectrum of the leakage ground current for CDZP-SVM strategy.

4.4.2. Losses analysis

In order to know how the distribution losses is for this case, some simulations results were obtained using the thermal module of PSIM® in the same way as it was done in the previous three modulation strategies, the results of these simulations are shown in Figure 4.23.

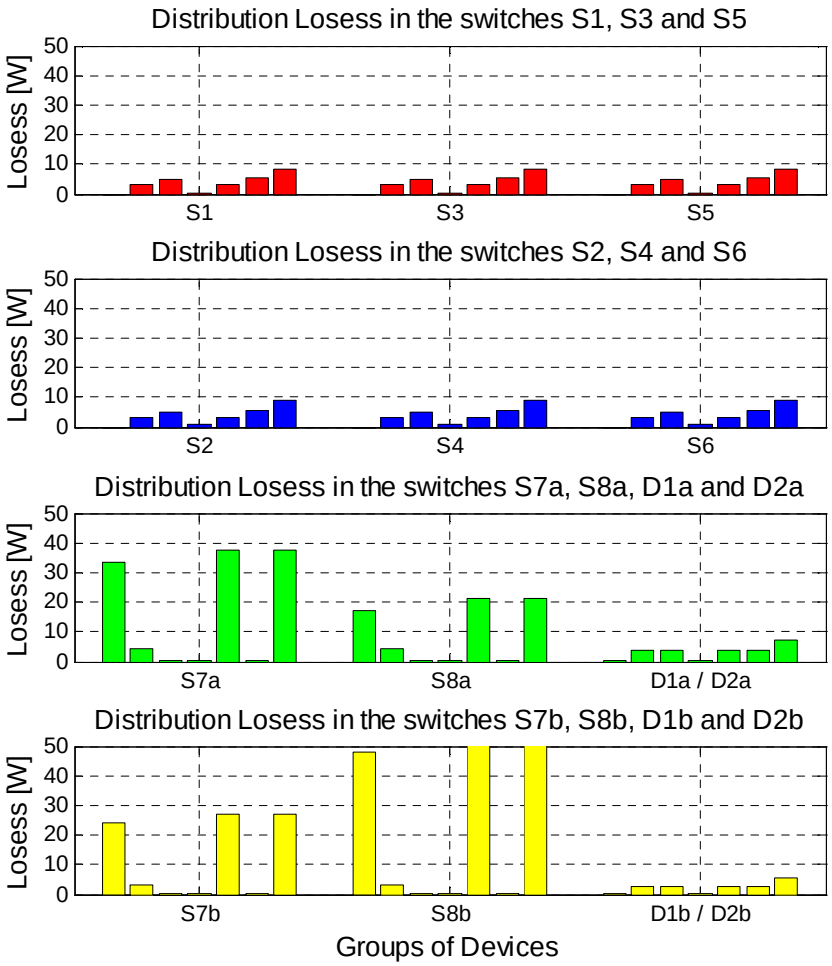

Figure 4.23. Distribution power losses in the case of CDZP-SVM.

As in the previous cases, the power losses across the switches forming the full-bridge circuit are low because of the zero voltage switching. In each case, all the switches contribute only with conduction losses. On the other hand in the case of the switches S7a, S8a, S7b and S8b the losses clearly increased due to the addition of the null vectors in the middle of the

switching period. The same situation occurs for all the cases regarding to the blocking voltage, the losses depends significantly on this parameter. For instance, the switches blocking voltages like 1/3 Vdc, will have less losses that those that are blocking voltages of 2/3 Vdc. This means that switch S7a will have more losses than S8a because the first one is blocking 2/3 Vdc. The same situation is for the case of the DC bus B; switch S7b will have less power losses than S8b, because of its blocking voltage.

Finally in the case on the auxiliary diodes, the losses are low and they have only conduction losses as it can be observed in Figure 4.23. As it was explained earlier, these diodes can be removed if an IGBT without anti-parallel diode is used, in this case, the total losses of the power converter will be significantly reduced because this diodes are used in both DC sources. Avoiding the power losses in these diodes the efficiency can be significantly increased.

4.4.3. Efficiency

The efficiency was evaluated using the model of the IGBT that was used also in the experimental setup. The efficiency obtained for the simulation test was around 98.53%. For the experimental results regarding to this parameter the efficiency was around 95.01%. This result confirms that the power losses are certainly higher in this case than in the previous one, due to the fact of the addition of hard switching transitions. As for all four cases, the power level in the test was set around 6kW.

In the case of the current quality, the same measurements were done as for the other three cases. The results in this case show that the quality of the output current is quite good. In the case of the simulations, the THD obtained was around 0.06%, in the case of the results obtained experimentally, the THD measured was around 1.11%. This means that the load current quality is quite good and can easily fulfill the standard requirements.

4.5. Summary of the analysis of the modulation strategies

In order to extract the most important characteristics of the modulation strategies, the main data are synthesized in Table 4.1. In this table, the total efficiency for each modulation strategy (calculated by simulation and experimentally) is given.

Modulation strategy	Total Efficiency %(Simulation)	Total Efficiency %(Experimental)
UZP-SVM	98.55	95.90
SZP-SVM	98.65	94.74
CZP-SVM	98.56	95.70
CDZP-SVM	98.53	95.01

Table 4.1. Comparative analysis regarding efficiency in all four modulation strategies.

As can it be seen in Table 4.1, the best result regarding the power losses belongs to CZP-SVM strategy. It can be observed also that the worst efficiency is for the CDZP-SVM strategy; this is due to the additional hard switching introduced by the zero vectors added. A comparative summary of the THD obtained not only by simulations but also experimentally is shown in Table 4.2. As can it be seen, the worst waveform is for the UZP-SVM strategy, of course, the best case is for that one that has a lot of switching transitions which is the CDZP-SVM strategy.

Modulation strategy	THD %(Simulation)	THD %(Experimental)
UZP-SVM	0.07	1.9
SZP-SVM	0.06	1.8
CZP-SVM	0.07	1.35
CDZP-SVM	0.06	1.11

Table 4.2. Comparative table regarding waveform quality for the proposed modulation strategies.

4.6. Losses optimization

The losses optimization process consists mainly in to determine if it is possible to improve the performance of the proposed converter. It is important to say that the power converter was built with not optimized semiconductors (Maximum collector-emitter voltage and collector current), this means that the devices used in this experimental test were not the best. In this regard, some changes were done for the simulation test in order to be sure that the performance of this converter can be improved.

One change that it has done, is the elimination of the losses in the case of the auxiliary diodes, they were changed by ideal diodes. As it was explained before, they are not going to be useful in the case in which the converter is implemented just with IGBT´s without anti-parallel diodes. Another change that it was performed is the addition of new models of the IGBT devices in the *Thermal module* toolbox of PSIM®. The main idea was to improve the most important characteristics that affect the performance of the converter, such as: the drop voltage of the anti-parallel diode (in the case of the full-bridge circuit); the duration times for the ON/OFF transitions (rise and fall time) and also the collector-emitter voltage. With these changes, the total efficiency can be improved until **99.0%**. There are some other changes that can be done, for instance, the selection of the IGBT considering the ratings of the blocking voltage and load current.

4.7. Conclusions

After evaluating four different modulation strategies designed for the FB10 three-phase transformerless topology it can be conclude that for each case the CMV is kept constant,

therefore the leakage ground current in every case is close to zero. Another conclusion is that the FB10 power converter can be modulated using different modulation strategies that can provide different performance not only in efficiency but also in the power quality, leakage current and power distribution losses.

In solar PV applications the efficiency is the most important parameter, because of the low efficiency of the PV panels. The proposed FB10 topology has a very good efficiency; this characteristic is very attractive in transformerless applications. On the other hand, no leakage current is generated and the international standard can be widely fulfilled.

References

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CHAPTER 5.

FB10 topology DC bus management

The FB10 topology may be useful for several applications processing power from the DC bus. Therefore, the study of the strategies for properly manage the energy sources connected to the DC bus is an issue that should be studied in detail. As it was explained in Chapter 3, the FB10 power converter has two isolated DC sources, e.g, two PV panels, therefore two DC sources can be processed at the same time. The I-V characteristic curve of a PV panel is nonlinear [5.1], [5.2], [5.3] and its output current mainly depends on the irradiation, the temperature and the voltage. In order to operate at the maximum power point of each of the two panels, the converter should be able to operate under unbalance DC conditions. This chapter presents a detailed study of two techniques devoted to control voltage and power of each of the DC buses of the FB10 topology.

The first control technique presented in this chapter is dedicated to compensate asymmetries in the output current when the voltage levels of the two DC buses are not equal. If this kind of asymmetry is not compensated, DC current component could be injected to the grid, which might cause, among other problems, saturation on grid transformers. The second control technique presented in this chapter is devoted to regulate the power delivered by each DC bus. This controller is indispensable in those applications in which the power set-point for each DC source should be independently controlled.

5.1. Operation of the FB10 topology under DC bus voltage unbalance

PV panels are not constant DC sources; their DC voltage set-point varies according to the solar irradiation, temperature and the delivered power [5.4], [5.5]. As the FB10 power converter topology consists of two DC buses, which can operate under different set-points,

the modulation strategy should be able to work under such unbalanced DC voltage conditions to guarantee the injection of symmetrical and sinusoidal currents into the electrical grid. With this goal in mind, a modification on the SVM techniques presented in Chapter 4 is performed in order to compensate the effect of the DC voltage unbalance by varying the application time of the active and zero vectors.

The main idea supporting the proposed compensation technique consists on extending the application time of the active vector to compensate the differences between the two DC bus voltages. As an example, if the voltage of the DC bus A (V_{dcA}) is higher than the voltage of the DC bus B (V_{dcB}), the time for the active vectors applied from the DC bus B, i.e., the even vectors, should be increased. The opposite case occurs when V_{dcA} is lower than V_{dcB}. The expression to determine how long the application of a given vector should be increased is very simple and it is based on the unbalance ratio between the two DC buses of the FB10 power converter. This variation for the active vectors application is graphically depicted in Figure 5.1.

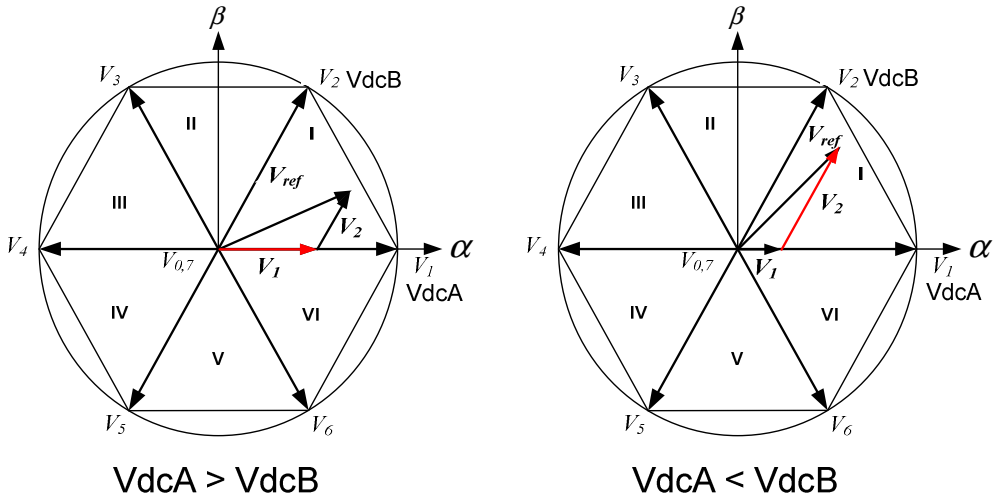

Figure 5.1. Active voltage modification under unbalance DC bus conditions in the FB10 three-phase PV converter.

Considering t_1 as the application time of the active vector from the DC bus A (odd vectors), t_2 as the application time of the active vector for the DC bus B, t_0 the application time for the zero vectors, then the equation to modify t_2 in order compensate the effect of the DC voltage unbalance in the modulation algorithm when $V_{dcA} > V_{dcB}$ can be written as:

$$t_2^{'} = \frac{t_2 \cdot V_{dcA}}{V_{dcB}}. \qquad (5.1)$$

Likewise, in case that $V_{dcA} < V_{dcB}$ the equation to modify t_1 can be written as:

$$t_1' = \frac{t_1 \cdot V_{dcB}}{V_{dcA}}. \tag{5.2}$$

In both cases, the prolongation in application time for the active vectors is taken from the reduction of the time for applying the zero vectors. Therefore, there is a DC unbalance compensation limit, which is reached when the zero vectors time is not enough to fit the required extra time application of the active vectors within a switching period. In such case, the compensation can be performed in two ways; by extending the switching period or by reducing both active vectors to a certain limit. In the first case the switching frequency will be reduced and in the second case the maximum output power will be reduced. In this case the second alternative was chosen. In order to calculate the limit of time to reduce both active vectors, a new variable is defined and it is called maximum active time t_{acm}, and is defined by,

$$t_{acm} = t_s - n \cdot t_{blank}, \tag{5.3}$$

where t_S represents the switching period, t_{blank} is the dead-time required to avoid a short circuit in a leg by the connection/disconnection of the DC bus, i.e., during the zero vector application and, n is the number of zero vectors applied in the switching pattern.

When the total active time for the active vectors, i.e., t_1+t_2' or t_1'+t_2 calculated from (5.1) and (5.2), exceeds the maximum active time t_{acm}, then the times for t_1 and t_2 can be readjusted by using,

$$t_1' = \frac{t_1 \cdot t_{acm}}{t_1 + t_2} \tag{5.4}$$

and

$$t_2' = \frac{t_2 \cdot t_{acm}}{t_1 + t_2}. \tag{5.5}$$

The value of t_{acm} depends on the modulation index that is used to modulate the converter. When the modulation index is low, the application of the zero vectors increases, and hence the time to compensate DC unbalance situations is longer than in the case of a high

modulation index, i.e., with lower modulation index it is possible to compensate higher DC voltage unbalancing.

In order to verify the correct operation of the proposed compensation technique some simulations and experiments have been conducted considering different voltage levels for the DC sources. Figure 5.2 shows the simulation results when V_{dcA} = 600V and V_{dcB} = 650V.

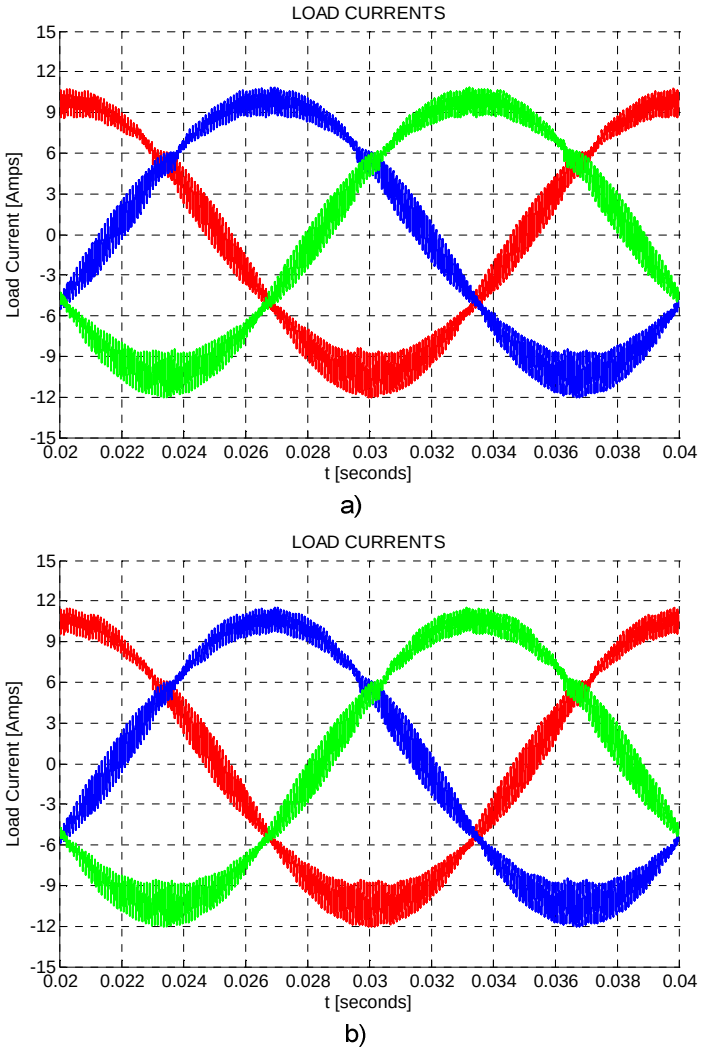

Figure 5.2. Simulation results when V_{dcA} = 600V and V_{dcB} = 650V; a) Without balancing technique and b) With balancing technique.

The load currents in Figure 5.2 a) correspond to the case in which the balancing technique is not applied. Even though the DC voltage unbalance is not very high (600 V / 650 V), it can be observed that the peak value of the load current is slightly lower in the positive half cycle compared to the negative one, i.e., the current injected into the grid is not symmetric as a consequence of the DC bus unbalance, existing a threatening DC offset that can rises serious problems in the AC grid. In order to attenuate the effect of the unbalanced DC voltages, the compensation technique exposed above is used to adjust the active vectors application time. The resulting current waveforms are shown in Figure 5.2 b), where can be observed a higher symmetry level than in the previous case, although there are still some differences between the positive and negative half-cycle due to the inherent asymmetry of the modulation technique used in this simulation (UZP-SVM).

Likewise, the simulation results for the case in which the V_{dcA} = 650V and V_{dcB} = 600V are shown in Figure 5.3.

As in the previous case, Figure 5.3 a) shows the output currents when no compensation is used and Figure 5.3 b) shows the output currents when the technique for compensating the effect of the DC unbalanced voltage is applied.

Considering that the modulation index used in the simulations presented above was around 90% and that the output voltage of the two PV panels connected to the DC buses will not differ too much from each other when they work with practical irradiation conditions [5.6], it can be stated that the compensation technique presented here is suitable for most of the practical PV applications.

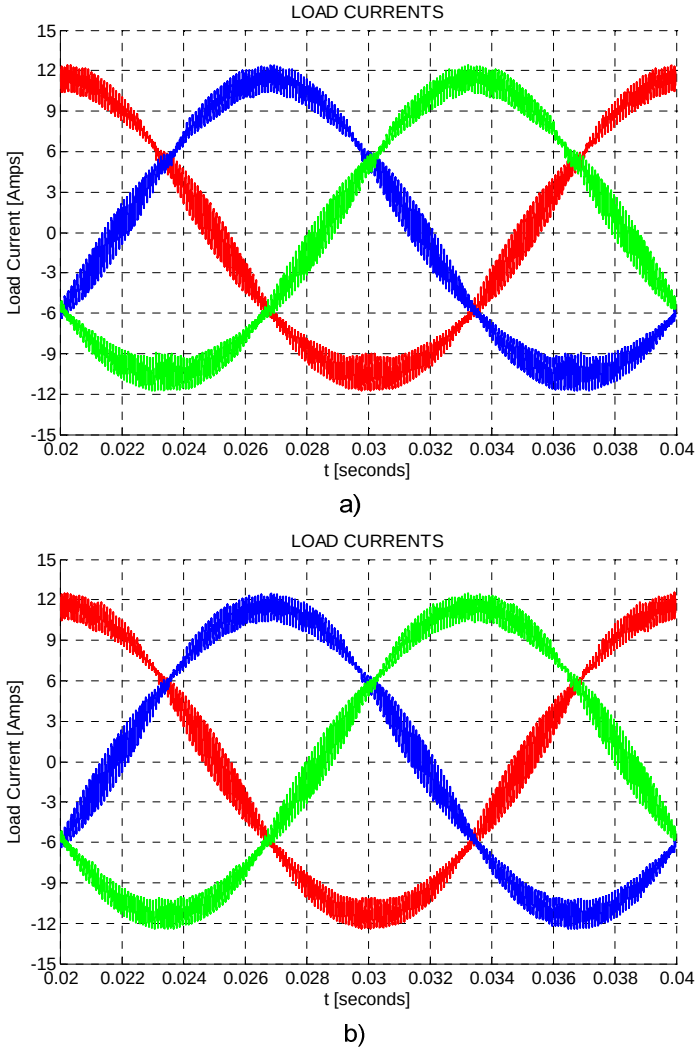

Figure 5.3. Simulation results when V_{dcA} = 650V and V_{dcB} = 600V; a) Without balancing technique and b) With balancing technique.

The simulations shown in Figure 5.2 and Figure 5.3 were also tested in the experimental setup. The setup was basically the same used for the experiments of Chapter 3 and Chapter 4 and the only difference is that the DC buses were intentionally unbalanced. Two DC voltage sources were used to control the DC unbalance level, instead of the isolation transformers and the rectifiers used in previous experiments. Figure 5.4 shows the resulting experimental currents when the DC voltage sources were hardly unbalanced (600 V / 540 V).

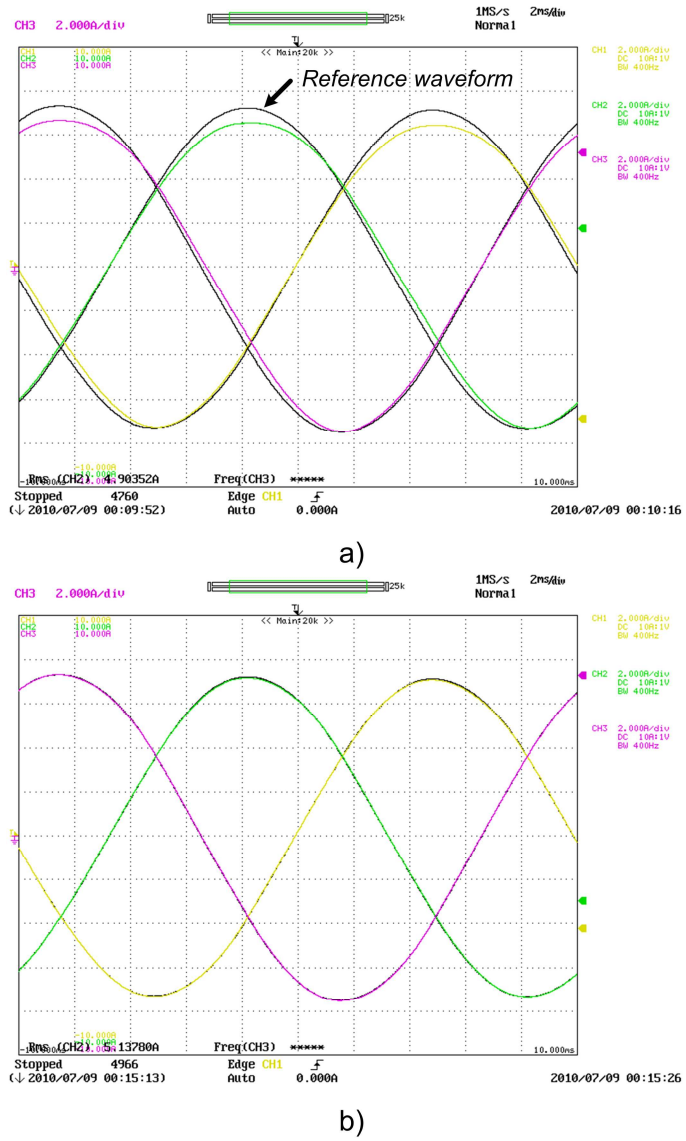

Figure 5.4. Experimental results when V_{dcA} = 540V and V_{dcB} = 600V; a) Without balancing technique and b) With balancing technique.

The black lines in the waveforms shown in Figure 5.4 a) indicate the reference currents for the converter. In case of a DC voltage unbalance with $V_{dcA} > V_{dcB}$ the positive peak in the output currents does not reach the reference values. Under such unbalanced situation DC current components are injected into the grid and the THD of the output currents increases. Figure 5.4 b) shows the output current waveforms when the technique for compensating the

effect of the DC voltage unbalance is applied. As it can be observed, the current waveforms perfectly track the sinusoidal references after using the compensation technique.

Figure 5.5 shows the experimental current waveforms for the experiment case of $V_{dcA} < V_{dcB}$.

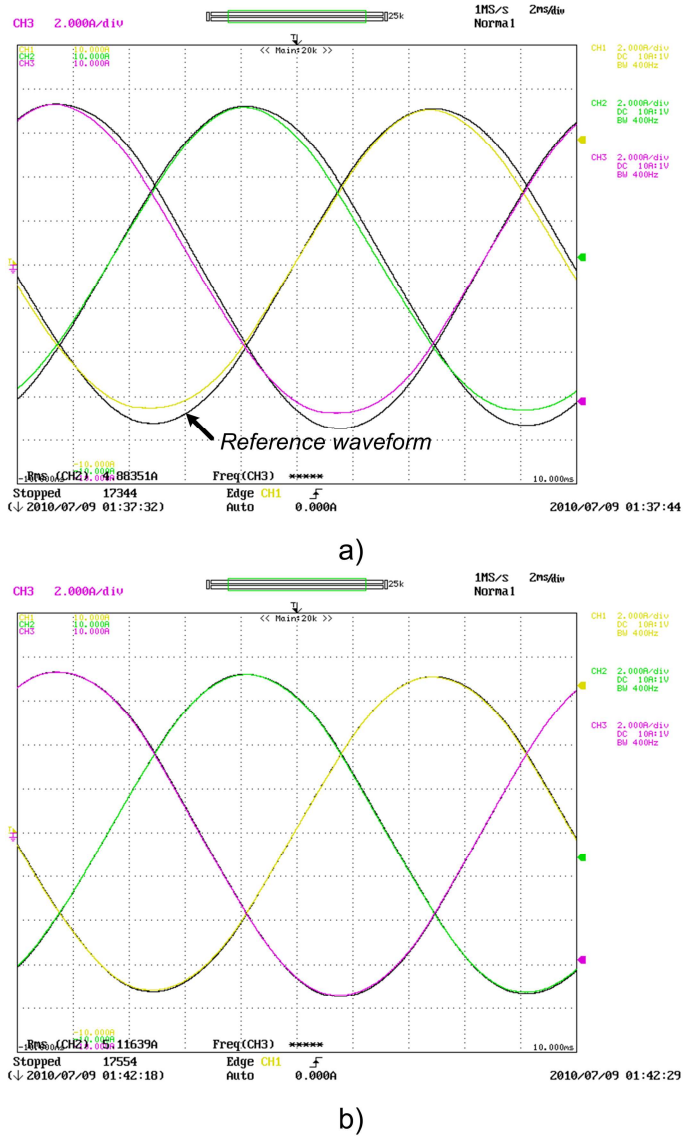

Figure 5.5. Experimental results when V_{dcA} = 600V and V_{dcB} = 540V; a) Without balancing technique and b) With balancing technique.

As Figure 5.5 a) shows, the output current presents the highest tracking error during the negative peaks when no compensation is used in this second case. However, Figure 5.5 b) shows how the output current waveforms perfectly track the reference signals when the voltage compensation strategy is applied. The experimental current waveforms shown in Figure 5.4 and Figure 5.5 do not present any ripple because a low pass filter was enabled in the scope to show clearly the distortion in the load currents when no compensation technique was applied under unbalanced DC bus conditions. Figure 5.6 shows the current waveforms when V_{dcA} = 600V and V_{dcB} = 540V and the low pass filter was disable in the scope.

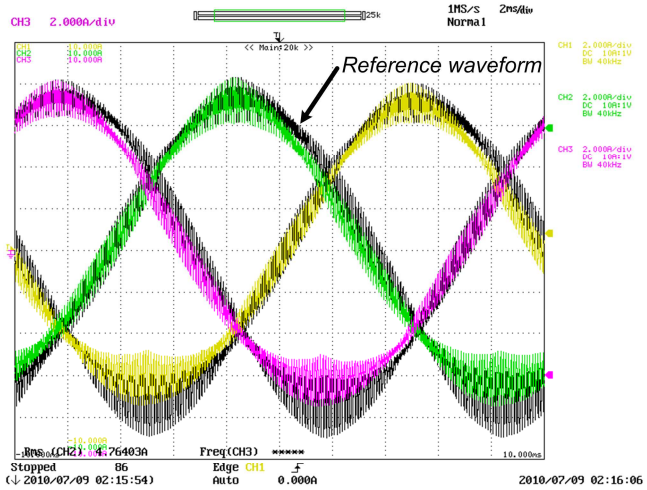

Figure 5.6. Experimental results to show the ripple in the load currents and the effect of the DC voltage compensation technique when $V_{dcA} > V_{dcB}$.

5.2. Power sharing between the two DC buses of the FB10 power converter

The maximum power that can be generated by a PV panel depends mainly on the solar irradiation and temperature [5.8], [5.9]. Therefore, the two sets of PV panels connected to the two DC buses of the FB10 power conversion topology can present different optimal set-points as the irradiation and temperature conditions can be different for each of them. These variations can be increased due to the effect of clouds, dust, etc., [5.7]. Therefore, the FB10 topology should be able to manage different power levels for each of its DC buses. In order to comply with this requirement, a control technique for regulating power sharing in the FB10 power converter is proposed in this section.

In the FB10 topology one of the buses is in charge of generating the odd vectors, for instance the DC bus A, while the other, the DC bus B, is in charge of generating the even ones. Therefore, when the synthesized vector is very close to the position of an odd generating vector (V_1, V_3 or V_5) the output current will be mainly supplied by the DC bus A. Likewise, the output current will be mainly supplied by DC bus B when the synthesized vector is close to an even vector (V_2, V_4 or V_6). When the relative phase-angle of the synthesized voltage vector is equal to 30º within a 60º sector the output current will be equally supplied by both DC buses. Therefore, it is possible to design a power balancing technique to regulate the output power sharing between the two DC buses by swapping the role of both DC power sources (PV panels) in a proper time within each 60º sector. The swapping of the two buses will cause a change on the voltage across the stray capacitances of each DC bus, which results in a small increase in the leakage ground current [5.10], [5.11]. Figure 5.7 graphically depicts this idea.

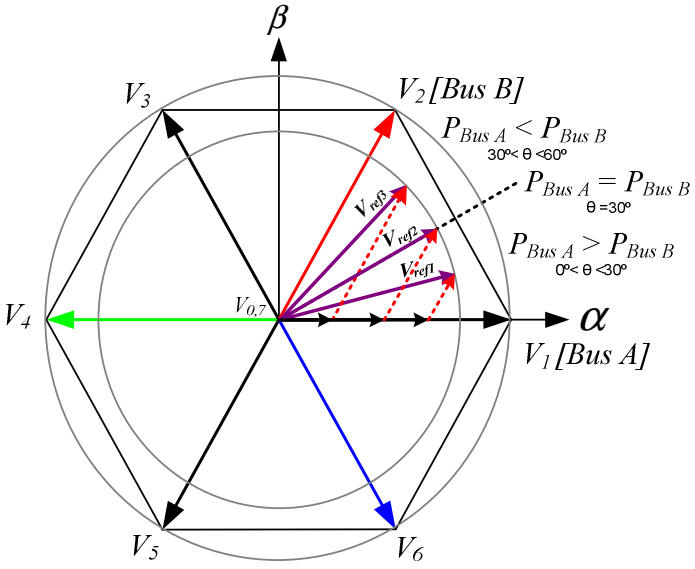

Figure 5.7. Power sharing under normal operation of FB10 converter.

Figure 5.7 represents three locations of the reference voltage vector within the Sector I. In case of V_{ref1}, with $\theta < 30º$, the application time for V_1 is higher than the one for V_2. In case of V_{ref2}, with $\theta = 30º$, the application time of V_1 is equal to the one for V_2. In case of V_{ref3}, with $\theta > 30º$, the application time for V_1 is lower than the one for V_2. In the FB10 power conversion topology the odd vectors can be supplied by the DC bus A and the even vectors by the DC bus B. Therefore, considering $V_{dcA} = V_{dcB}$, it seems logical to assume that the power delivered by the DC bus A will be higher than the one delivered by the DC bus B for $\theta < 30º$, equal for $\theta = 30º$ and lower for $\theta > 30º$.

To conduct a more detailed analysis of the currents flowing through both DC buses of the FB10 power converter, Figure 5.8 shows these currents when the voltage reference vector moves along the Sector I.

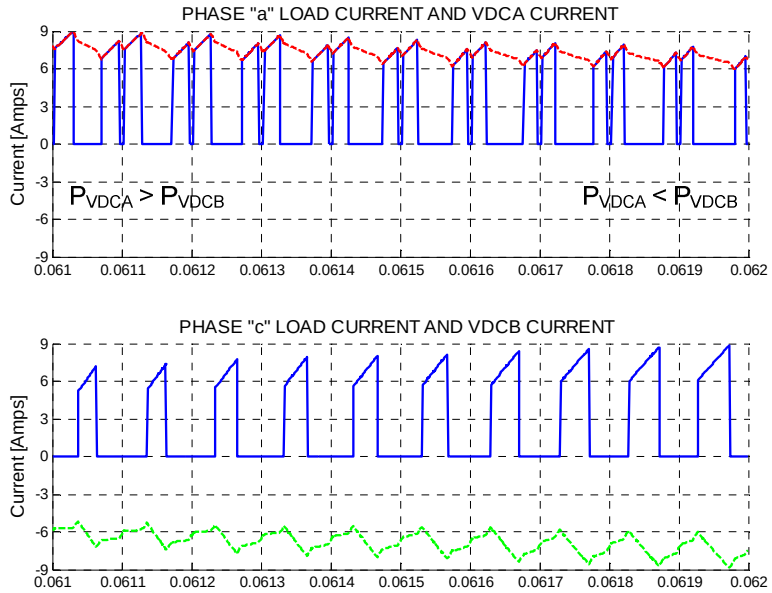

Figure 5.8. DC currents along the Sector I in a symmetrical power sharing situation.

As it can be observed in Figure 5.8, the currents in the DC bus A and B follow a symmetrical evolution along the Sector I. As the DC bus A is in charge of generating the voltage vector V_1, the current supplied by the DC bus A matches the current of the phase 'a' during the application of the odd active vectors in the Sector I. Likewise, the DC bus B, in charge of generating the voltage vector V_2, sinks the current of the phase 'c' during the application of the even active vectors in the Sector I. Therefore, assuming unitary power factor operation without loss of generality, the current flowing through the DC bus A will be higher than the one of the DC bus B for $\theta < 30º$. The opposite case occurs when $\theta > 30º$. This analysis of the evolution of the DC currents allows confirming that the power delivered by

the DC bus A will be higher than the one from the DC bus B for $0 < \theta < 30^o$ and lower when $30^o < \theta < 60^o$. The equilibrium point occurs for $\theta = 30^o$. Moreover, the symmetric evolution of the currents flowing through both DC buses along the Sector I implies that the two DC power sources deliver the same average power over the Sector I period. This analysis is also valid for other sectors along the grid period. In order to facilitate the analysis, it is possible to define a new reference angle $\theta' = \theta - 30^o$. With this phase rotation, the equilibrium point occurs at $\theta'=0$, and the power delivered by DC bus A will be higher than the one from DC bus B for $-30<\theta'<0$ and lower for $0<\theta'<30$.

As mentioned above, when the DC bus A generates the odd vectors and the DC bus B the even ones, both DC power sources will deliver the same average power over a sector period. However, this power sharing can be modified if the role of both DC power sources is swapped at a given position of the reference voltage vector within each sector. To explain this power sharing technique, α is defined as a power regulation angle. According to that, the role of the two DC buses of the FB10 topology within the Sector I can be assigned as follows:

$$\begin{array}{ll} -30^o \le \theta' \le \alpha & \text{DC bus A even vectors and DC bus B odd vectors} \\ 30^o - \alpha \le \theta' \le 30^o & \text{DC bus A even vectors and DC bus B odd vectors} \\ \text{other case} & \text{DC bus A odd vectors and DC bus B even vectors} \end{array} \quad (5.6)$$

According to (5.6), it is easy to note that the equilibrium point fulfills the condition $\theta'=0$ and the role modification is symmetric to this point. The regulation angle α is bounded to $-30<\alpha<30^o$. The power delivered by DC bus A will be higher than the one from DC bus B for $-30<\theta'<0$ because during the role modification DC bus A will provide the power to the even vectors in the zone in which they require more energy and, in the sequel it will provides the energy to the odd vectors and it will be lower for $0<\theta'<30$ because it will works in the opposite way.

In order to demonstrate the power compensation behavior some simulation and experimental results were carried out. Figures from Figure 5.9 to Figure 5.12 show the simulation results for $\alpha = 20^o$. Figures from Figure 5.13 to Figure 5.16 shows the simulation results for $\alpha = -20^o$. The experimental results for $\alpha = 20^o$ are depicted in Figures from Figure 5.17 to Figure 5.19, while the experimental results for $\alpha = -20^o$ are presented in Figures from Figure 5.20 to Figure 5.22. In the following each case is analyzed in detail.

The Figure 5.9 shows the simulation results for $\alpha = 20^o$, condition in which the power delivered by DC bus B will be higher than the one provided by DC bus A. From top to bottom, it shows the load currents in Figure 5.9 a), the voltages across the stray capacitances in Figure 5.9 b) and the leakage ground current in Figure 5.9 c). It should be noted that the voltages across the stray capacitances are changing each sextant and as a consequence some current spikes in the leakage ground current appear at the same time. This change is actually the transition for the power sharing from DC bus A to DC bus B and vice-versa.

In Figure 5.10 a) the phase to negative terminal of the DC bus A (z) voltages are shown. The CMV referred to this "z" point is depicted in Figure 5.10 b). As it can be seen, the CMV is jumping from 1/3 Vdc to 2/3 Vdc and going back each sextant, as expected.

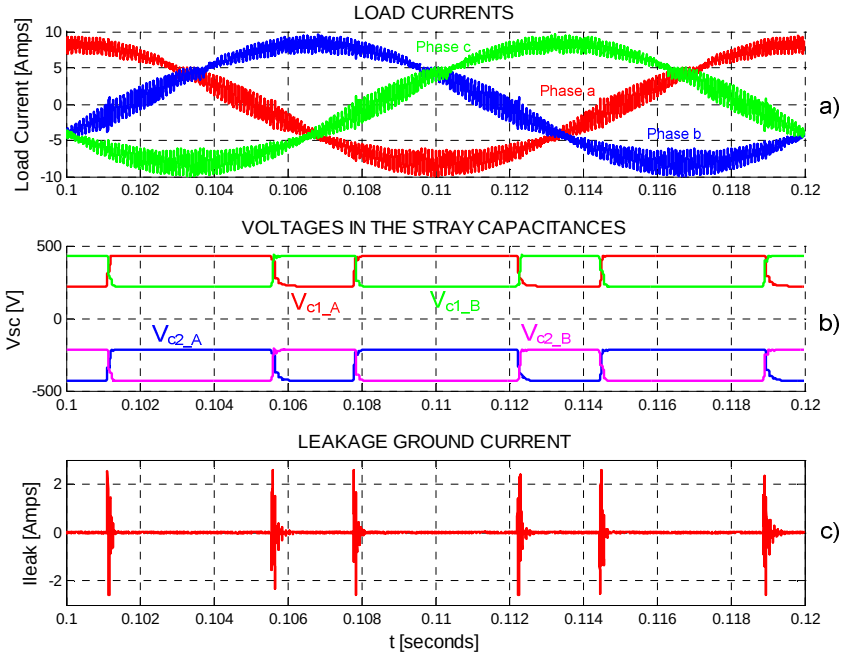

Figure 5.9. Simulation results for the power sharing technique with a regulation angle α = 20º.

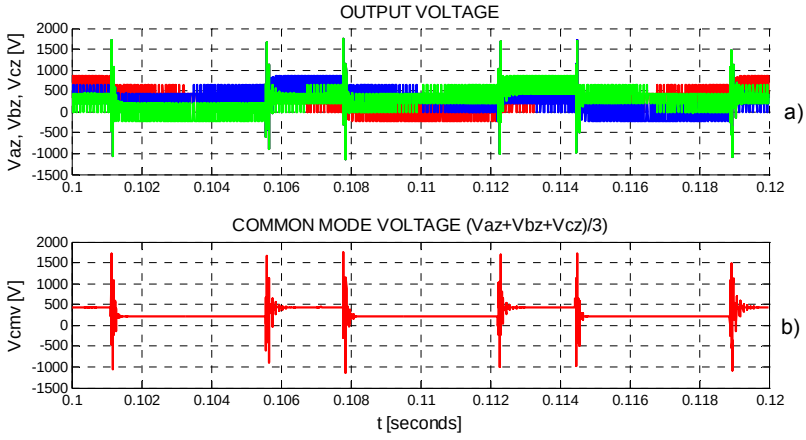

Figure 5.10. CMV in the case of power compensation technique using a regulation angle α = 20º.

The active times for both DC buses, namely t_{DCA_ON} and t_{DCB_ON}, respectively, are shown in Figure 5.11 a). The blue waveform corresponds to the active time for the DC bus B, t_{DCB_ON}. Observe that from t = 0.1s to t = 0.101s approximately which means $0<\theta'<20$, the DC bus have changed their roles (this analysis is also valid for the next sextants) t_{DCB_ON} has increased the active time and as a result the power provided by the DC bus B is higher than the other one as it is show in Figure 5.11 b). Finally, in Figure 5.11 c), the six sectors along the grid period are also shown.

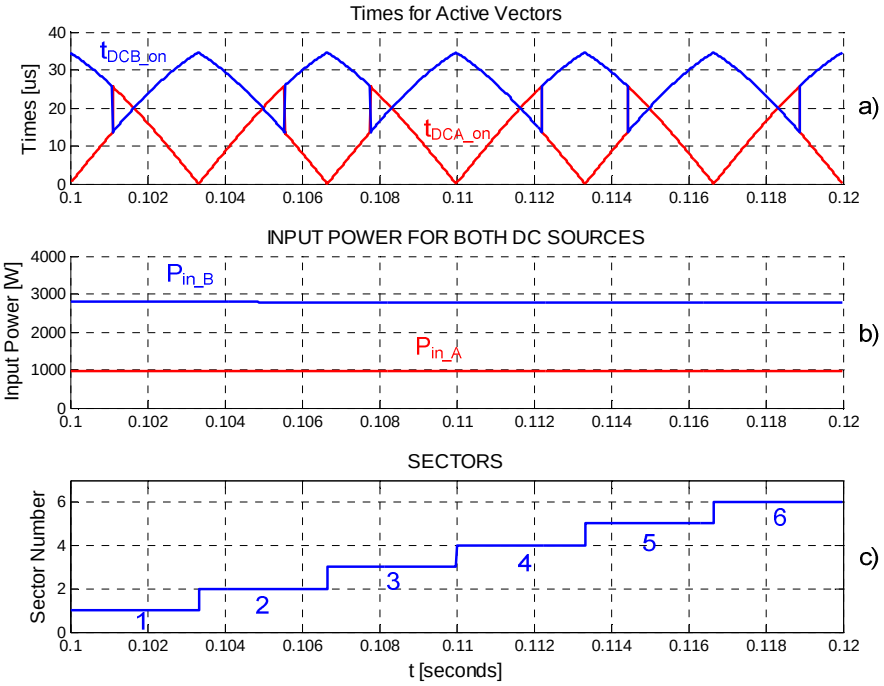

Figure 5.11. a) Active times, b) Power measured and c) Sectors, in the case of the power sharing technique using a regulation angle $\alpha = 20^{o}$.

The spectrum of leakage ground current generated using this technique can be appreciated in Figure 5.12.

The case in which the power delivered by DC bus A is higher than the one provided by DC bus B was also simulated using a regulation angle $\alpha = -20^{o}$. In Figure 5.13 a), the load currents waveforms are depicted. In Figure 5.13 b), the voltages across the stray capacitances are shown; these voltages are changing each sextant due to the change in the role of the DC sources. These changes (dv/dt in the stray capacitance) produce the leakage ground current shown in Figure 5.13 c).

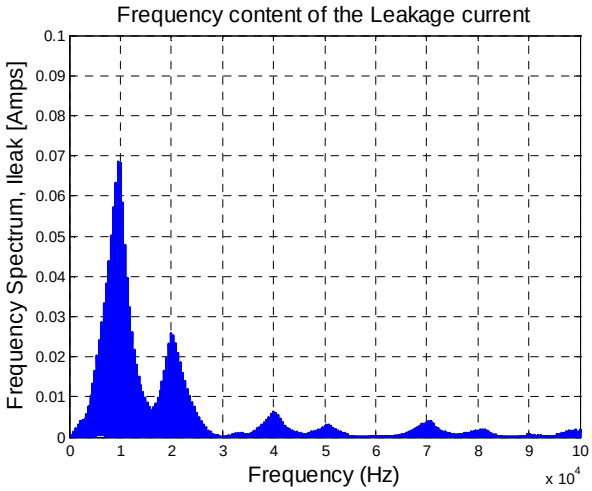

Figure 5.12. Frequency spectrum of the leakage ground current when the power sharing technique is applied using a regulation angle $\alpha = 20^{o}$.

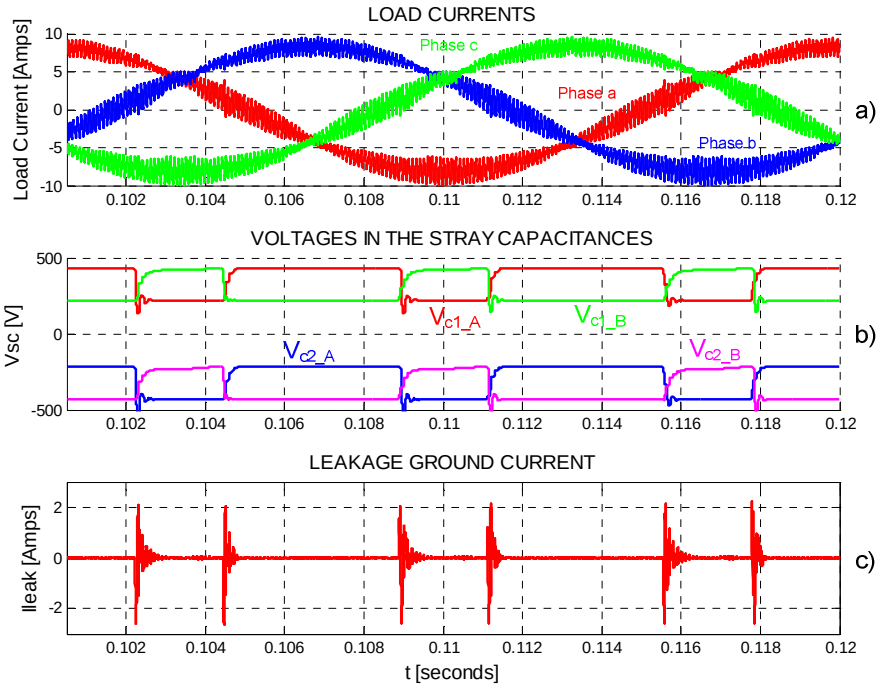

Figure 5.13. Simulation results for the power sharing technique for a regulation angle $\alpha = -20^{o}$.

The phase to negative terminal of the DC bus A voltages are shown in Figure 5.14 a) and the resulting CMV is jumping between 1/3 Vdc and 2/3 Vdc as can be observed in Figure 5.14 b).

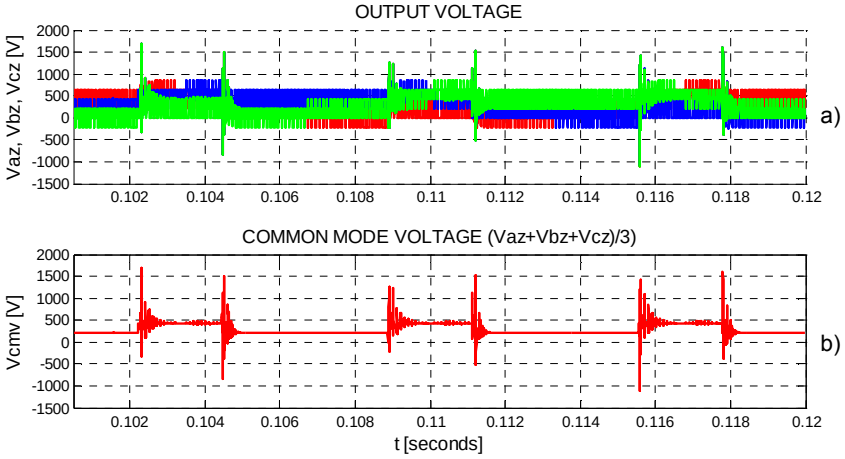

Figure 5.14. CMV in the case of power sharing technique applied when the regulation angle α = -20º.

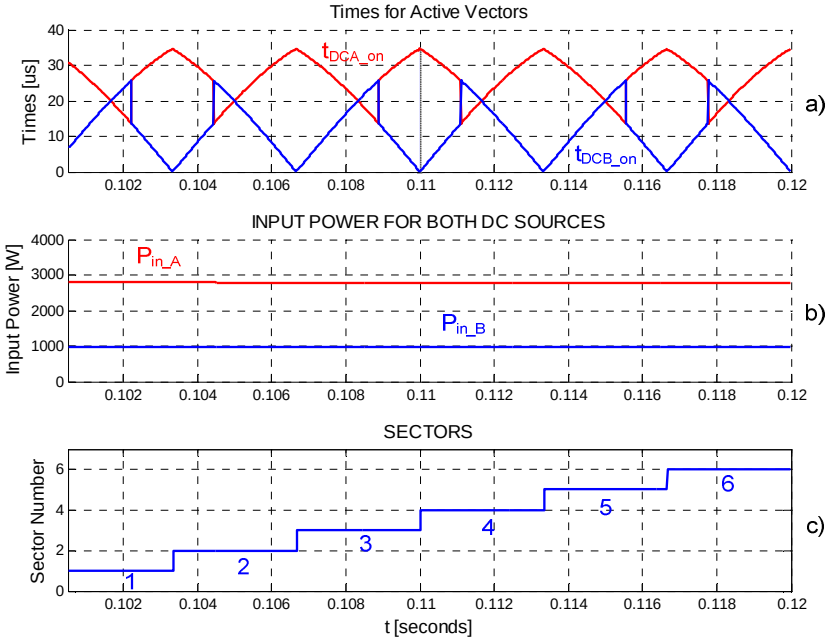

Figure 5.15. a) Active times, b) Power measured and c) Sectors, in the case of the power sharing technique applied using a regulation angle α = -20º.

In Figure 5.15 a) the active times in both DC sources are depicted. Note how from t = 0.1025s to t = 0.1045s approximately which means -20<θ'<20, the DC bus have change their roles (this analysis is also valid for the next sextants) T_{DCA_ON} has increase the active time and the power provided by the DC bus A is higher than the other one as it is shown in Figure 5.15 b). Finally the sectors along the grid period are shown in Figure 5.15 c).

The spectrum of the leakage ground current produced by the dv/dt of the CMV is depicted in Figure 5.16.

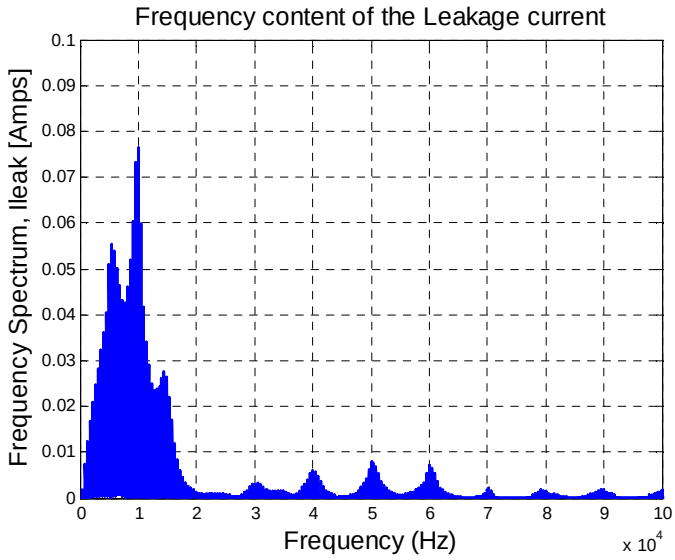

Figure 5.16. Frequency spectrum of the leakage ground current when the power sharing technique is applied using a regulation angle α = -20º.

In Figure 5.17 the experimental waveforms of the load currents, voltage across the stray capacitances and leakage ground current using a regulation angle α = 20º are shown. Figure 5.17 a) presents de load current. The voltages across the stray capacitances depicts in Figure 5.17 b) describe the effect of the role changes in the DC buses, it changes from 1/3 Vdc to 2/3 Vdc and vice-versa each sextant. The change in these voltages will generate spikes in the leakage ground current as it is shown in Figure 5.17 c).

The phase to negative terminal of the DC bus A voltages were also obtained; these voltages are depicted in Figure 5.18 a). The computed CMV is shown in Figure 5.18 b).

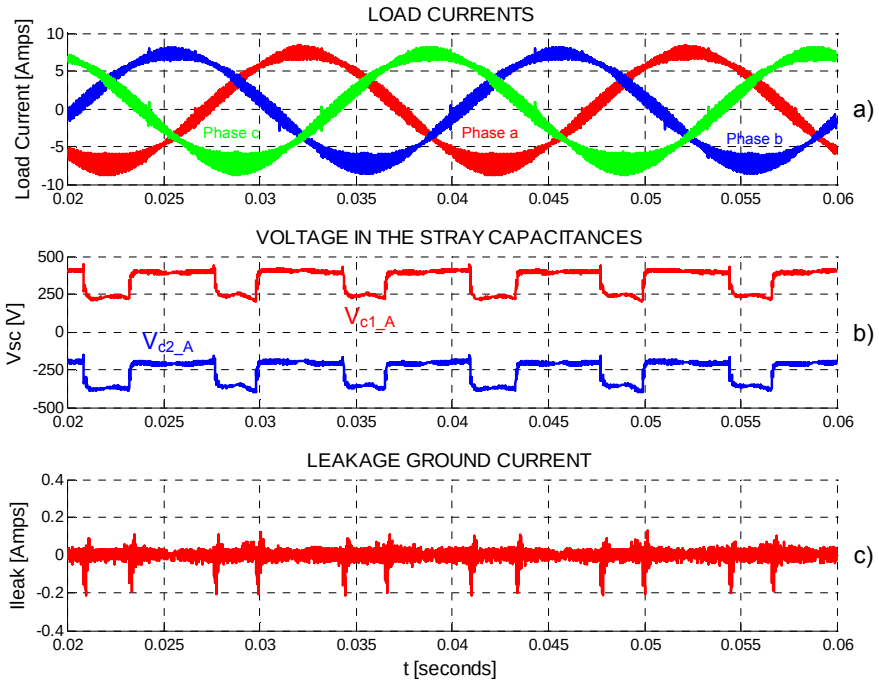

Figure 5.17. Experimental results for the power sharing strategy applied when a regulation angle α = 20º is applied.

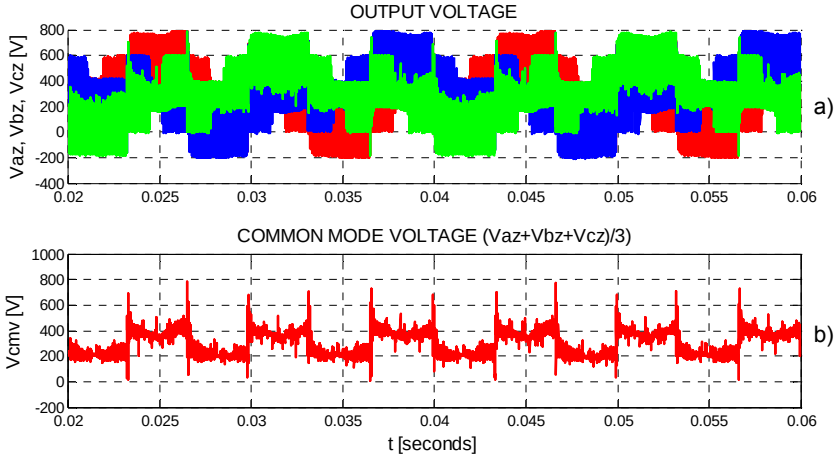

Figure 5.18. Experimental CMV in the case of power sharing technique applied with a regulation angle α = 20º.

Finally, in Figure 5.19 the experimental frequency spectrum of the leakage ground current is shown. As can be seen, the magnitude of the current components at each frequency is very low and as a consequence the converter fulfills the standard to be used in three-phase transformerless PV applications.

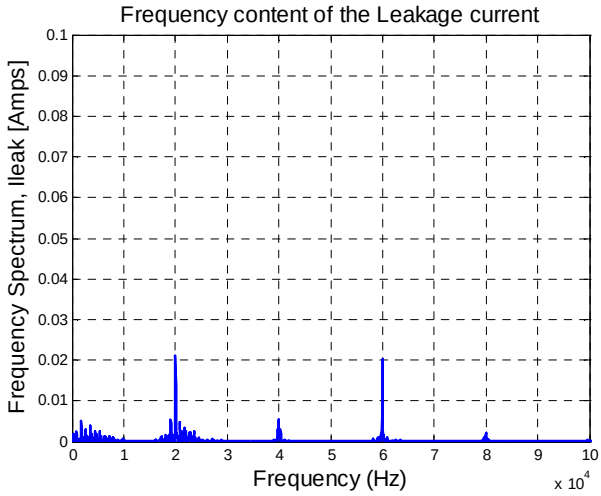

Figure 5.19. Experimental frequency spectrum of the leakage ground current in the case of Power sharing technique applied with a regulation angle $\alpha = 20^{o}$.

The mode in which it is possible to provide more power from the DC bus A than the one from the DC bus B was also tested in the experimental setup. The regulation angle was set at $\alpha = -20^{o}$. Figure 5.20 shows the load currents, voltage across the stray capacitances and leakage ground current. Note the jumps for the voltage across the stray capacitances in the Figure 5.20 b) because of the role changing of the DC buses. The jumps in the voltage magnitude across the stray capacitances match with the spikes in the leakage ground current as it appears in Figure 5.20 c).

In Figure 5.21 a) the phase voltage to negative terminal of the DC bus A voltages are shown. Based in these voltages, the CMV was computed and presented in Figure 5.21 b).

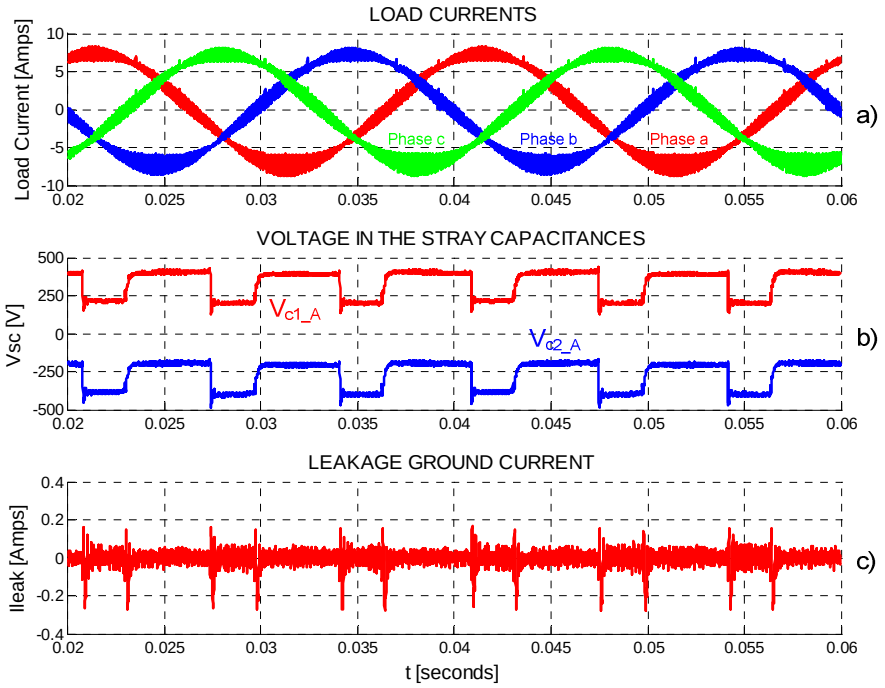

Figure 5.20. Experimental results for the power sharing strategy applied when a regulation angle α = -20º is applied.

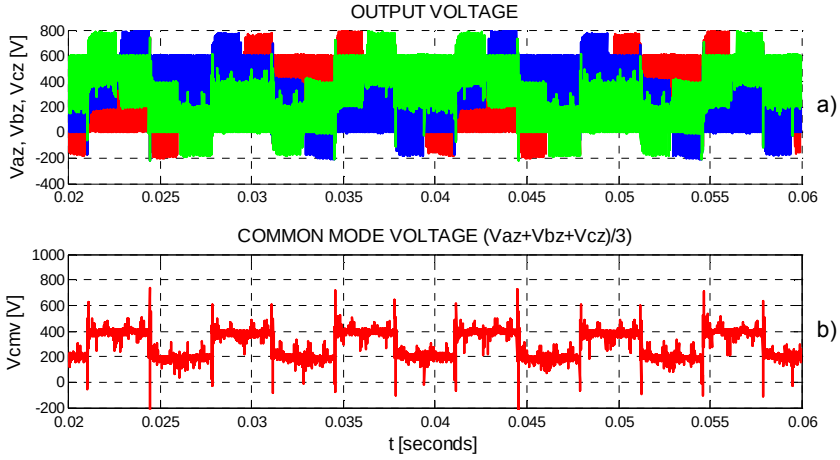

Figure 5.21. Experimental CMV in the case of power sharing technique applied with a regulation angle α = -20º.

Finally the experimental frequency spectrum of the output current is shown in Figure 5.22. The higher component has a *rms* value around 30 mA. This current value is not a safety problem for the operation of transformerless PV systems.

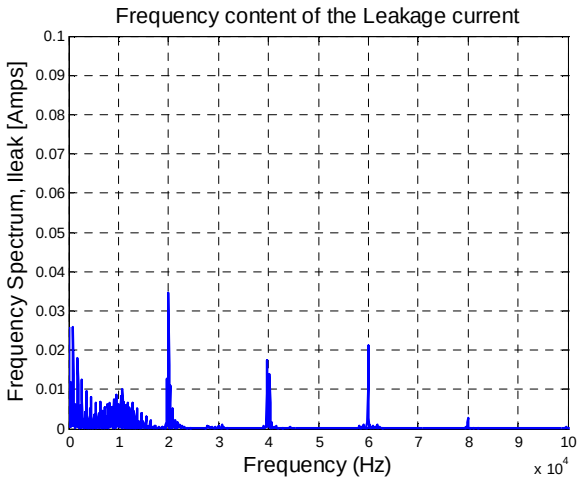

Figure 5.22. Experimental frequency spectrum of the leakage ground current in the case of Power sharing technique applied with a regulation angle $\alpha = -20^{o}$.

5.3. Conclusions

PV applications require power converters able to work with a nonlinear power supply. In a conventional two stages PV system [5.12], the first stage consists in a DC-DC converter that can control and boost the input voltage. On the other hand in a single stage system this function is performed by the inverter [5.13]. The voltage provide by the PV panel can has variations as a function of the irradiation (that can be affected by clouds). When two or more PV panels are connected at the input of a power converter like FB10, the voltage and the power delivered from each one can be different, therefore the power converter should be able to work under these conditions.

In this chapter an algorithm to compensate the variations of the output voltage in the PV panels was presented, the provided simulated and experimental results have certified the suitable operation of this algorithm. Additionally, an algorithm to manage the power provide by each PV panel was also implemented. Experimental and simulation results were also obtained concluding that the algorithm works properly and it can be adapted to extract different `power levels from the PV panels. The above results indicate that FB10 is suitable for transformerless PV applications.

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CHAPTER 6.

Conclusions and future works

The work presented in this thesis deals with the CMV problem in transformerless grid connected PV power converters. The CMV generated by transformerless PV power converters can produce high leakage ground currents that can affect negatively the overall operation of the system. The magnitude and frequency of the CMV depends on the pulse width modulation strategy and the power converter structure. In the particular case of transformerless PV systems, the CMV can reduce the lifetime of the PV panels because of the leakage currents and also pose human safety problems.

The PV systems require high efficiency in the energy conversion process because of the low efficiency of the PV panels. The power losses in the PV power converters depend on the switching frequency, modulation strategy and structure. In order to achieve a good performance of PV system, the power converters must be designed with the minor number of stages, minor number of semiconductors, soft switching (if is possible), minor number of passive elements (no transformers and inductors) and with an efficient control algorithm.

6.1. Summary

Currently, transformerless PV inverters widely provide some of the requirements mentioned above, like no transformer, few semiconductors and just a single stage. In the first chapter of this PhD dissertation, the study and evaluation of some interesting PV structures was presented, considering many different topology structures with transformer and transformerless, that are used by the PV industry or have been proposed as transformerless PV inverters, concluding that transformerless topologies are smaller in size and have higher efficiencies than inverters with high-frequency or low-frequency transformers. The main conclusion in the first chapter is that transformerless PV power converters are very attractive to be used in PV power generation facilities.

Chapter 2 conducted a deep evaluation of successful single-phase PV power converters like H5 and HERIC topology structures (based on the full-bridge single-phase inverter), concluding with the proposal of a new single-phase transformerless PV power converter topology called "HB-ZVR" (Half Bridge Zero-Voltage Stage Rectifier Topology) which is mainly based in the HERIC topology. The proposed topology uses a bidirectional switch located at the grid side which is a variant of that used in HERIC topology; in this case the bidirectional switch is formed by an IGBT and a diode rectifier. The bidirectional switch is mainly used to isolate the power converter from the grid during null states. The HB-ZVR topology is a very good alternative for transformerless PV power generation facilities due to its high efficiency and very low leakage ground current (constant CMV).

Chapter 3 dealt with the three-phase PV power conversion systems. In this chapter, the common mode model of the three-phase converter was analyzed and a new three-phase transformerless topology was proposed. The proposed topology is based on the conventional three-phase full-bridge inverter and in the single-phase H5 and Roberto González topologies exposed in chapter 1. Unlike the HERIC topology case, in this case the switch to isolate the power converter from the grid side is located on the DC side. Two independent DC sources were used to feed the power to the load. The common mode analysis of the proposed topology was also provided. The new topology was called FB10 (Full-Bridge 10), where number 10 comes from number of semiconductors used in its implementation. In this chapter the PWM strategy to control the semiconductors was also implemented. The modulation strategy was mainly based on the SVM, which has the flexibility to modify the vectors sequence. According with the simulation and experimental results presented in this chapter, it can be concluded that the proposed topology is also a good alternative in transformerless applications (even for big power PV plants), thanks to its high efficiency and no leakage current.

In Chapter 4, four different modulation strategies to control the FB10 topology were proposed, named: Unsymmetrical Zero Placement Space Vector Modulation (UZP-SVM), Symmetrical Zero Placement Space Vector Modulation (SZP-SVM), Combine Zero Placement Space Vector Modulation (CZP-SVM) and Combine Double Zero Placement Space Vector Modulation (CDZ-SVM). The four modulation strategies use one DC bus to feed the odd vectors and the other one to feed the even vectors, the main difference among all of them is the sequence in which the active and null vectors were applied. A deep analysis (by means of simulations and experiments) of power losses, power quality, current ripple magnitude and CMV was performed for each modulation strategy. All the simulations and experiments were done in open-loop. The major conclusion from such analysis is that all modulation strategies provides leakage ground current close to zero, thus complying with current PV regulations, which is very important for the objectives of this PhD dissertation.

Finally, in Chapter 5, two very important techniques to manage the DC bus in the proposed topology were also presented. The first one dealt with the unbalances in the DC bus, which is formed with two DC sources as was mentioned before. These two power sources can be implemented by means of two PV arrays. The PV panels operation depend on weather conditions, this means that the voltage and current delivered by each PV array may

vary over a day. Therefore the PV power converter must be able to manage these changes at the input DC voltage; otherwise DC current injection can appears at the AC side. The proposal to solve this problem was implemented using a simple strategy to compensate the unbalances on the DC side. The strategy was to reduce or enlarge the active time of the vectors according to the voltage differences at the input. The second strategy was designed to solve the unbalance situations in the power delivered by each DC bus. The solution implemented in this case, was to swap the DC sources as a function of the reference vector position, since the reference vector is formed at each time by the contribution of those two DC sources. Simulations and experiments showed how the unbalance conditions on the DC side can be manage by the FB10 inverter.

6.2. Main contributions

A short list of contributions can be summarised in the following points:

- Review of PV topologies

A comprehensive review of several single- and three-phase topologies with and without transformer was conducted. A general discussion of the topologies that are implemented using transformer was provided. Moreover, in the case of the transformerless topologies, a deeper analysis was conducted. In this last case, the PWM strategy was analyzed step by step to understand their switching sequence and their main advantages and drawbacks regarding CMV performance.

- Single-Phase HB-ZVR Topology

A new topology for single-phase PV transformerless applications is proposed. The topology uses a bidirectional switch at the AC side in order to short-circuiting the output of the inverter during the null states periods. The modulation strategy to control the switching states of the PV inverter is designed and is based on the HERIC PWM pattern. The PWM pattern and the power structure proposed permits to reduce the leakage ground current close to zero in PV system where there is not galvanic isolation.

- Three-Phase FB10 topology

A new three-phase PV transformerless topology called FB10 is also proposed. The topology consists in a full-bridge structure and two DC sources (which can be PV panels or PV arrays) coupled by means of two IGBTs each one. The main idea in this case is to disconnect the DC side from the AC side during null states in order to get constant CMV voltage. The PWM strategy (based on H5 operation) to control the power inverter is also proposed. The FB10 inverter reduces the leakage ground current to very low levels (close to zero), complying with the current PV regulations in some countries. Moreover the topology proposed gets a very good efficiency which is a very important characteristic in PV systems.

- Modulation strategies for FB10 topology

Four modulation strategies to manage the FB10 were also proposed. Due that FB10 is a new topology; different ways to switching the converter were investigated. The modulation strategies were obtained modifying in different ways the sequence of the active and null vectors applied to the power converter. The simulation and experimental results provide information about the efficiency and power quality in each case. Each modulation strategy was explored in depth.

- DC bus management for three-phase FB10 topology

As the PV panels are no constant DC sources, the DC-AC power converter must be capable to manage variations of voltage and current at its input. In order to overcome this unbalances at the input of FB10, two strategies to compensate the voltage and power variations were proposed. In the first case the voltage compensation strategy uses the active time of the vector components of the reference vector. The idea is to reduce or enlarge the magnitude of the components according with the conditions of the DC buses. On the other hand, the strategy to compensate the differences between the two DC buses consists in to swap the DC sources according with the position of the vector reference. In this way, it is possible to obtain different power levels from the DC sources. Even when this exchange between DC buses can produce some leakage ground current, it is not enough to overcome the limits established by the regulations.

6.3. Future work

There are several tasks to be developed following the ideas presented in this PhD. dissertation, being some of them listed in the following:

- ✓ DC current injection under unbalanced and balance conditions in the FB10 topology could be deeper investigated. DC current injection can be a very important problem when a transformerless inverter is connected to the grid. A DC component at the AC side can produce saturation in the network transformers, tripping of the protection systems, losses increase, etc. For these reasons it is very important to ensure no DC current injection.

- ✓ New modulation strategies to control FB10 inverter could be interesting to improve efficiency. Even when the modulation strategies proposed in this PhD thesis have very good performance regarding efficiency, some other alternatives can be explored. Switching techniques like zero voltage and zero current switching can be explored.

- ✓ The FB10 topology can be optimized by choosing better semiconductors, as SiC, for diodes and IGBT´s to improve the efficiency.

- ✓ FB10 topology should be test using PV panels under partial shading conditions in a real PV power plant. This will provide information about the behaviour of the strategies to compensate unbalances at the DC input.

- ✓ Multi-DC bus concept can be also explored for FB10 topology (by using some DC buses providing ODD active vectors and others providing EVEN active vectors).

- ✓ Other power strategies to control the power injected by each DC bus could be investigated. For instance, a power compensation strategy can be designed using three active vectors.

- ✓ Grid connection could be explored using different current control algorithms and modulations strategies for the FB10 topology. Different techniques to synchronize the power converter with the grid can be studied.